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Application note

Migrating from STM32WB1x/5x to STM32WB1x/5x MCUs microcontrollers

Introduction

For designers of STM32 microcontroller applications, the ability to replace one microcontroller smoothly with another from the same product family is an important asset. Migrating an application to a different microcontroller is often necessary when product requirements grow. This puts extra demand on memory size, or increases the number of I/Os. Cost reduction is another motivation to switch to smaller components and shrink the PCB area.

This document analyzes the key steps required for migration between STM32WB10/15/50/55 microcontrollers. These are: hardware, peripheral availability, firmware, security, and tools. For a full understanding of the information in this application note, the end user must be familiar with STM32WB10/15/50/55 microcontrollers (see Table 2).

Table 1. Applicable products

Type	Part numbers
Microcontrollers	STM32WB10CC, STM32WB15CC, STM32WB50CG, STM32WB55CC, STM32WB55CE, STM32WB55CG, STM32WB55RC, STM32WB55RE, STM32WB55RG, STM32WB55VC, STM32WB55VE, STM32WB55VG, STM32WB55VY

1 General information

This document applies to STM32WB10/15/50/55 microcontrollers, based on Arm® Cortex® cores.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

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Table 2. Reference documents and tools

Available at www.st.com.

Reference	Document ID	Title
R1	RM0434I	Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth®Low Energy and 802.15.4 radio solution
R2	DS11929	Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® 5 and 802.15.4 radio solution
R3	-	STM32CubeMX: video
R4	AN5185	ST firmware upgrade services for STM32WB Series
R5	AN5105	Getting started with touch sensing control on STM32 microcontrollers
R6	ES0394	STM32WB55xx/STM32WB35Cx device errata
R7	ES0492	STM32WB50CG/30CE device errata
R8	DS13047	Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® Low Energy or 802.15.4 radio solution
R9	RM0471	Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® or 802.15.4 radio solution
R10	DS13258	Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® 5.2 radio solution
R11	DS13259	Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® 5.2 radio solution
R12	ES0556	STM32WB10 device errata
R13	ES0557	STM32WB15 device errata

2 Hardware migration

This section presents a summary of the main hardware differences.

2.1 Package overview

The table below details the available packages for STM32WB10/15/50/55 microcontrollers.

Table 3. Package information

Package[1] [2]	Number of pins	STM32WB55	STM32WB15	STM32WB50	STM32WB10	Part numbers
UFQFPN48	48	X	X	X	X	STM32WB55CxU STM32WB15CCU STM32WB50CGU STM32WB10CCU
VFQFPN68	68	X	-	-	-	STM32WB55RxV
WLCSP100	100	X	-	-	-	STM32WB55VxY
UFBGA129	129	X	-	-	-	STM32WB55VxQ
UFQFPN48 with extended I/Os option	48	-	X	-	-	STM32WB15CCUxE
WLCSP49	49	-	X	-	-	STM32WB15CCY

1. *"x" = available, "-" = device is not produced with this package.*
2. *In UFQFPN48 for ST32WB5x there is excessive current on V_{DDA} or V_{DD} when V_{DD} level is different from V_{DDA} level. This limitation should be taken into account when migrating form STM32WB1x to STM32WB5x and vice versa or from package to another one- see R6 and R7*

2.2 RF performance

STM32WB50/55 microcontrollers embed a powerful and ultra-low power radio compliant with Bluetooth® Low Energy stack and with IEEE 802.15.4- 2011.

STM32WB10/15 microcontrollers embed a powerful and ultra-low power radio compliant with Bluetooth® Low Energy stack.

Table 4. Bluetooth low energy on-air data rate

Bluetooth low energy on-air data rate	STM32WB55	STM32WB15	STM32WB50	STM32WB10
2 Mbit/s	X	X	-	-
1 Mbit/s	X	X	X	X

Note: For more details regarding RF electrical characteristics refer to R9, R10 and R11.

2.3 Pinout differences

STM32WB10/15/50/55 microcontrollers have different packages, therefore migration requires a particular attention regarding GPIOs and their associated alternate functions. The pin-to-pin compatible devices are listed below (for other packages refer to R2, R8,R10,R11).

- STM32WB55 in UFQFPN48 package is pin-to-pin compatible with STM32WB15 in UFQFPN48 package.
- STM32WB50 in UFQFPN48 package is pin-to-pin compatible with STM32WB10 in UFQFPN48 package.

2.4 Clock tree

The clock tree for STM32WB55 and STM32WB15 is different. The LCD, 802.15.4, AHB3, PLLSAI1, SAI1,USB, HSI48 RC, are not available on STM32WB15xx but the LSI can be selected for bluetooth low energy wakeup. For more details refer to Figure 1 and Figure 3.

Figure 1. STM32WB55 clock tree

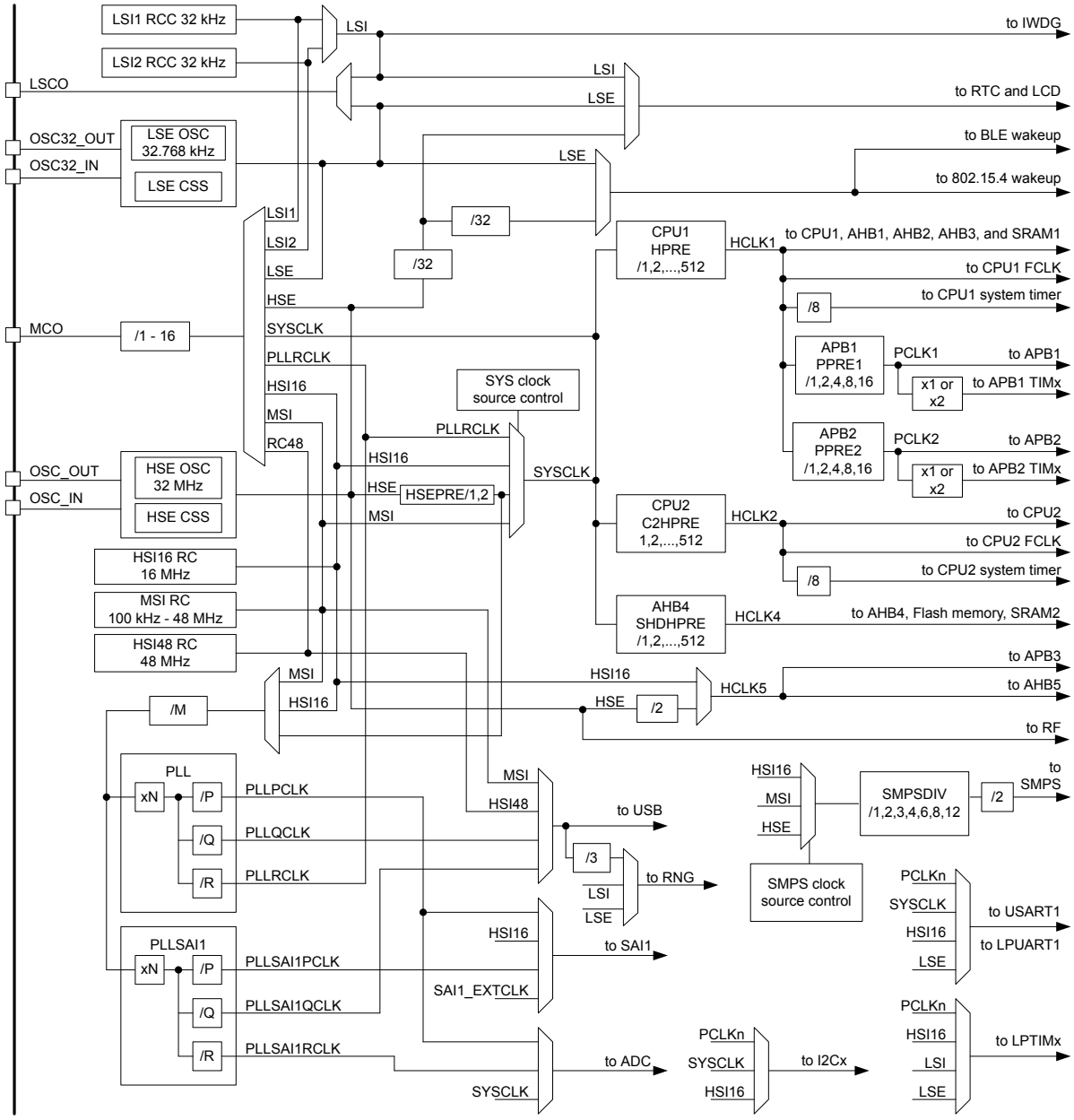
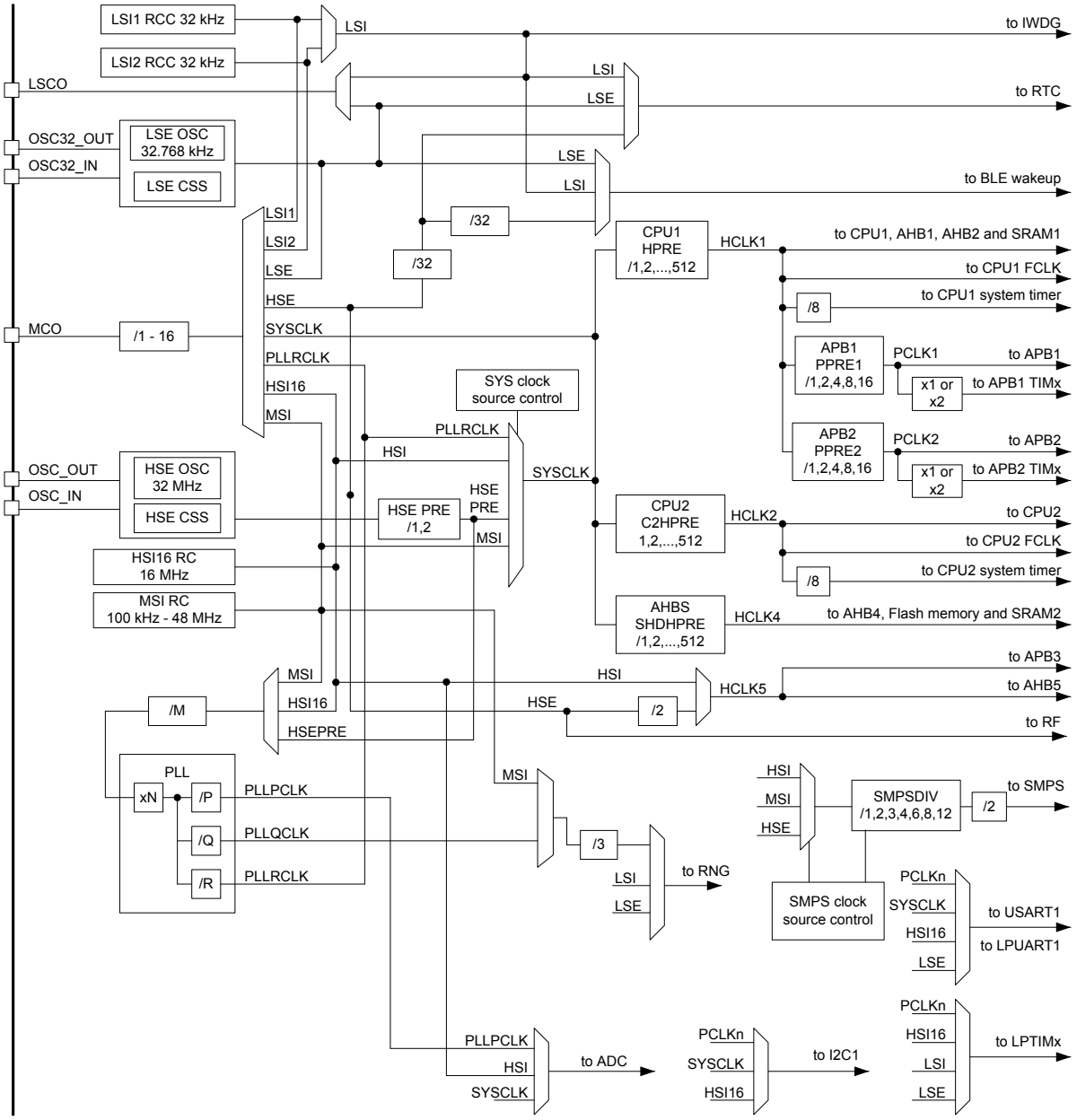


Figure 2. **STM32WB15 clock tree**



The clock tree for STM32WB10 and STM32WB50 is different. The 802.15.4, HSI48 RC is not available on STM32WB10xx but the LSI can be selected for bluetooth low energy wakeup. For more details refer to the figure below.

Figure 3. STM32WB50 clock tree

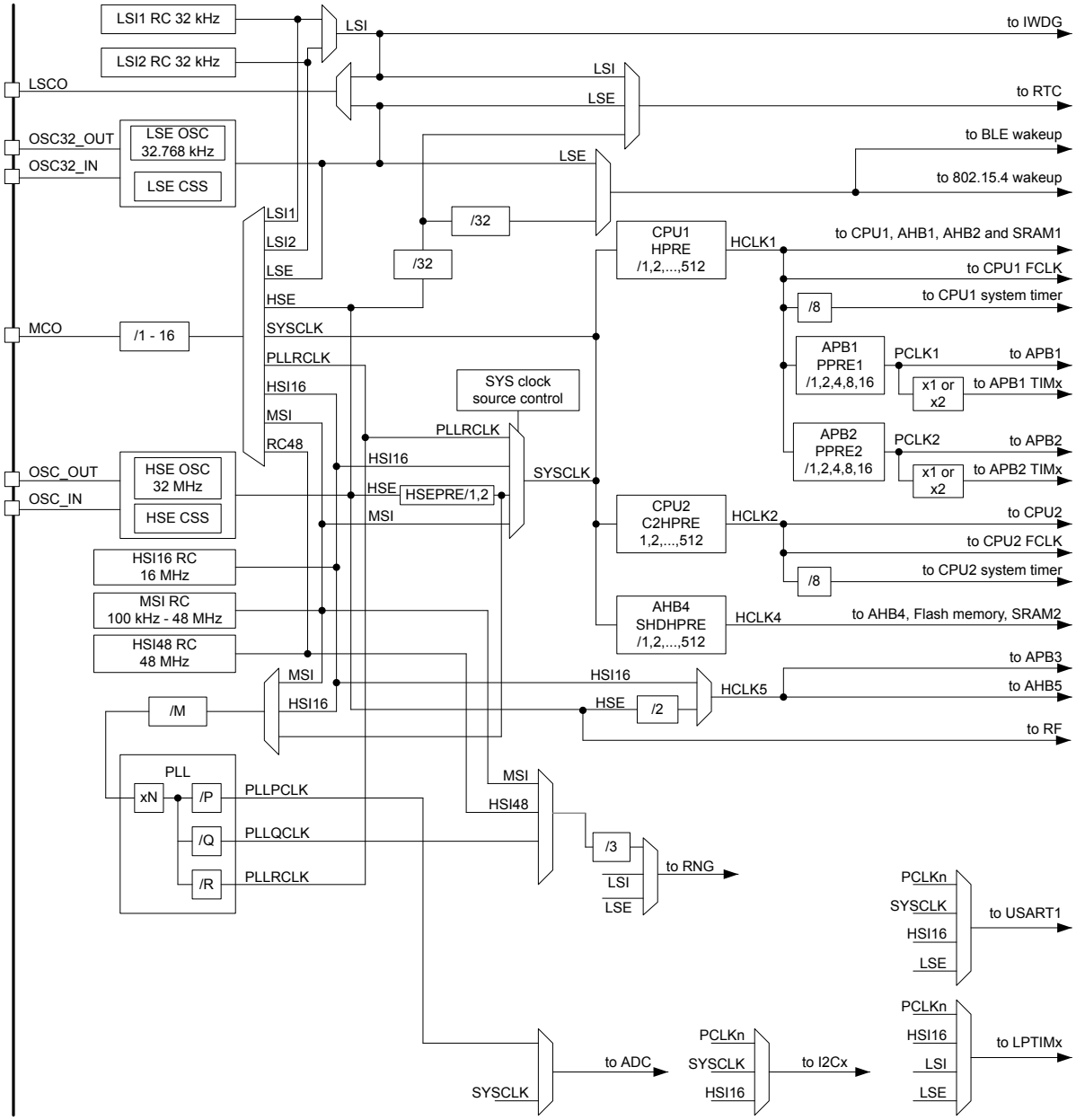
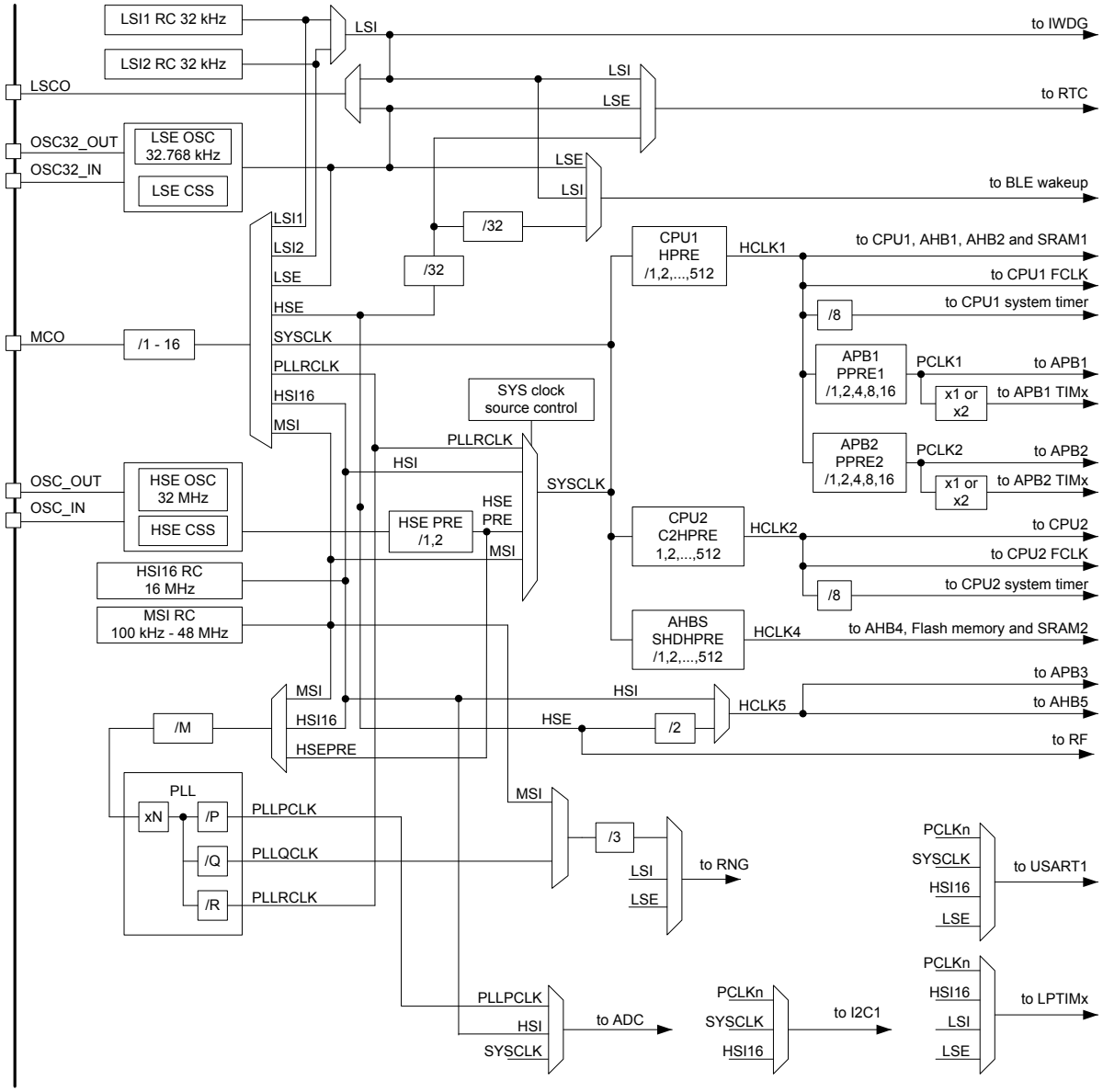


Figure 4. **STM32WB10 clock tree**



3 Peripheral migration

The table below summarizes the peripheral compatibility and features changes when migrating between STM32WB10/15/50/55 microcontrollers.

Table 5. Peripheral compatibility and features on STM32WB10/15/50/55

Peripheral / Features	STM32WB55				STM32WB15		STM32WB50	STM32WB10
	UFQFPN48	VFQFPN68	WLCSP100	UFBGA129	UFQFPN48[1]	WLSCP49	UFQFPN48	UFQFPN48
Bluetooth 5	Yes				Yes	Yes	Yes	Yes
IEEE 802.15.4	Yes				No	No	Yes	No
Concurrent mode	Yes				No	No	No	No
Dual core CPU (Cortex-M4 + Cortex-M0+)	Yes				Yes	Yes	Yes	Yes
Flash memory	Up to 1 Mbyte				320 Kbytes	320 Kbytes	1 Mbyte	320 Kbytes
SRAM	Up to 256 Kbytes				48 Kbytes	48 Kbytes	128 Kbytes	48 Kbytes
QUADSPI	1				0	0	0	0
DMA	2 (14 channels)	2 (14 channels)	2 (14 channels)	2 (14 channels)	1 (7 channels)	1 (7 channels)	1 (7 channels)	1 (7 channels)
16-bit advanced timer TIM1	1				1	1	1	1
32-bit general purpose timers TIM2	1				1	1	1	1
16-bit general purpose timers TIM16/TIM17	2				0	0	2	0
16-bit low-power timer LPTIM1/ LPTIM2	2				2	2	2	2
Watchdog timer	2				2	2	2	2
SysTick timer	1				1	1	1	1
SPI	1	2	2	2	1	1	1	1
I^2C (inter-integrated circuit)	2				1	1	1	1
USART (can be used as SPI)	1				1	1	1	1
LPUART	1				1	1	No	No
SAI (serial audio interface)	1 (dual channel)				No	No	No	No
USB FS	1				No	No	No	No
RTC	1				1	1	1	1
Tamper pins	1	3	3	3	1	1	1	1
Wakeup pins	2	5	5	5	2	2	2	2
LCD (COMxSEG)	Yes (4 × 13)	Yes (4 × 28)	Yes (8 × 40 or 4 × 44)	Yes (8 × 40 or 4 × 44)	No	No	No	No

Peripheral / Features	STM32WB55				STM32WB15		STM32WB50	STM32WB10
	UFQFPN48	VFQFPN68	WLCSP100	UFBGA129	UFQFPN48[1]	WLSCP49	UFQFPN48	UFQFPN48
GPIOs	30	49	72	72	30 (37 for extended I/Os option)	25	30	30
TSC (capacitive touch sensing)	No	6	18	18	3 (8 for extended I/Os option)	2	No	3
12-bit ADC	13 channels	19 channels	19 channels	19 channels	13 channels	13 channels	10 channels	13 channels
Internal Vref	Yes				Yes	Yes	Yes	Yes
Analog comparator (COMP)	2				1	1	No	No
Max CPU frequency	64 MHz				64 MHz	64 MHz	64 MHz	64 MHz
JTAG/SW-DP	1 / 1				1 / 1	1 / 1	1 / 1	1 / 1
ETM	Yes				No	No	No	No
PLL	2				1	1	1	1
Operating temperature range 1	-40 to +85 °C				-40 to +85 °C	-40 to +85 °C	-10 to +85 °C	-10 to +85 °C
Operating temperature range 2	-40 to +105 °C				-40 to +105 °C	-40 to +105 °C	No	No
Operating voltage	1.71 to 3.6 V				1.71 to 3.6 V	1.71 to 3.6 V	2.0 to 3.6 V	2.0 to 3.6 V
SMPS	Yes				Yes (no extended I/Os option)	Yes	No	No

1. *There are two configurations in UFQFPN48, with SMPS or with extended I/Os option.*

3.1 Hardware changes description

This section provides further details regarding the modified or suppressed features during the migration process between STM32WB10/15/50/55 microcontrollers.

3.1.1 Flash memory mapping

Different Flash memory sizes are available according to the package selected, for more information refer to the table below.The STM32WB5x page size is 4 Kbytes and 2 Kbytes for ST32WB1x devices.

Table 6. Flash memory sizes and their mapping

Device	Flash memory size (Kbytes)	Mapping addresses	Description
STM32WB55	256, 512, 1024	0x0800 0000 – 0x080F FFFF	The Flash memory start addresses are the same for all STM32WB10/15/50/55 microcontrollers.
STM32WB50	1024	0x0800 0000 – 0x080F FFFF	
STM32WB15	320	0x0800 0000 – 0x0804 FFFF	
STM32WB10	320	0x0800 0000 – 0x0804 FFFF	

3.1.2 SRAM mapping

As shown in the table below the SRAM1 density of STM32WB15 and STM32WB10 is reduced compared with, respectively, STM32WB55 and STM32WB50.

Table 7. SRAM sizes and their mapping

Device	SRAM(1)	Size (Kbytes)	Mapping addresses	STM32WB5x versus STM32WB3x
STM32WB55	SRAM1 SRAM2a SRAM2b	64/192(2) 32 32 Total: 128/256	0x2000 0000 - 0x2002 FFFF 0x2003 0000 - 0x2003 7FFF 0x2003 8000 - 0x2003 FFFF	• SRAM1 size can be reduced from 192 to 12 Kbytes and starts at the same address on STM32WB55 and STM32WB15. • SRAM2a has the same size and starts at the same address on STM32WB55 and STM32WB15. • SRAM2b size is reduced from 32 to 4 Kbytes. SRAM2b starts at the same address on STM32WB55 and STM32WB15.
STM32WB15	SRAM1 SRAM2a SRAM2b	12 32 4 Total: 48	0x2003 0000 - 0x2003 2FFF 0x2003 0000 - 0x2003 7FFF 0x2003 0000 - 0x2003 8FFF	
STM32WB50	SRAM1 SRAM2a SRAM2b	64 32 32 Total: 128	0x2000 0000 - 0x2000 FFFF 0x2003 0000 - 0x2003 7FFF 0x2003 8000 - 0x2003 FFFF	• SRAM1 size is reduced from 64 to 12 Kbytes and starts at the same address on STM32WB50 and .STM32WB15. • SRAM2a has the same size and starts at the same address on STM32WB50 and STM32WB10. • SRAM2b size is reduced from 32 to 4 Kbytes. SRAM2b and starts at the same address on STM32WB50 and STM32WB10.
STM32WB10	SRAM1 SRAM2a SRAM2b	12 32 4 Total: 48	0x2003 0000 - 0x2003 2FFF 0x2003 0000 - 0x2003 7FFF 0x2003 0000 - 0x2003 8FFF	

1. *SRAM2a is retained in Standby mode for all products. SRAM1 and SRAM2b are retained in standby mode for STM32WB15/10 products..*
2. *There are two possible configurations, according to the device part number.*

3.1.3 Peripheral migration compatibility

This section presents a complete view of the number of peripherals available when migrating between STM32WB10/15/50/55 microcontrollers. For more details regarding electrical characteristics refer to R9 R11 and R10.

Table 8. Peripheral compatibility analysis

Peripheral	STM32WB55				STM32WB15		STM32WB50	STM32WB10
	UFQFPN48	VFQFPN68	WLCSP100	UFBGA129	UFQFPN48	WLSCP49	UFQFPN48	UFQFPN48
QUADSPI(1)	1	1	1	1	0	0	0	0
DMA (7 channels)	2	2	2	2	1	1	1	1
SPI	1	2	2	2	1	1	1	1
I^2C (inter-integrated circuit)	2	2	2	2	1	1	1	1
SAI (serial audio interface) (2)	1	1	1	1	0	0	0	0
LPUART(3)	1	1	1	1	1	1	0	0
USB(4)	1	1	1	1	0	0	0	0
ADC(5)	1 × 13 channels	1 × 19 channels	1 × 19 channels	1 × 19 channels	1 × 13 channels	1 × 13 channels	1 × 13 channels	1 × 13 channels
COMP	2	2	2	2	0	0	0	0
GPIOs(6)	30	49	72	72	(37 for extended I/Os option)/30	25	30	30
TSC(7)	0	6	18	18	8 (3 for extended I/Os option)	2	0	3
LCD(8)	4 × 13	4 × 28	8 × 40 or 4 × 44	8 × 40 or 4 × 44	0	0	0	0
Tamper pins	1	3	3	3	1	1	1	1
JTAG/SWD	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1
ETM (embedded trace macrocell)	No	No	Yes	Yes	No	No	No	No
PLL (phase-locked loop)	2	2	2	2	1	1	1	1

1. *No QUADSPI on STM32WB15, STM32WB50 and STM32WB10 microcontrollers.*
2. *No SAI on STM32WB15, STM32WB50 and STM32WB10.*
3. *No LPUART on STM32WB50 and STM32WB10 microcontrollers.*
4. *No USB on STM32WB50 and STM32WB1x microcontrollers.*
5. *For the ADC sampling rate refer to Table 9.*
6. *STM32WB10/15/50/55 microcontrollers in UFQFPN48 package are pin-to-pin compatible.*
7. *Number of keys including the shield that can be driven with the TSC peripheral. For more information about TSC and connection of sensors refer to R5.*
8. *LCD is not available on STM32WB15, STM32WB50 and STM32WB10 microcontrollers.*

Table 9. **ADC sampling rate**

AD sampling rate (Mbit/s)						
Sampling rate resolution	STM32WB55		STM32WB15		STM32WB50	STM32WB10
	Fast channels	Slow channels	V_{DDA} > 2.0 V	V_{DDA} ≤ 2.0 V		
12 bits	4.26	3.36	2.50	2.18	2.13	2.50
10 bits	4.92	4.00	2.92	2.50	2.46	2.92
8 bits	5.81	4.57	3.50	2.92	2.91	3.50
6 bits	7.11	7.11	4.38	3.50	3.55	4.38

4 Software migration

This section gives an overview of the possible use-cases, and information on the available free memory space for Flash memory and SRAM when implementing the different scenarios.

The wireless stack and the application firmware can be upgraded over-the-air (OTA feature).

4.1 Memory density

Table 10. Flash memory and SRAM density

Footprint (Kbytes)	STM32WB55				STM32WB15	STM32WB50	STM32WB10
	Density 1	Density 2	Density 3	Density 4	Density 1		
Flash memory	256	512	640	1024	320	1024	320
SRAM1	64	192	192	192	12	64	12
SRAM2a	32	32	32	32	32	32	32
SRAM2b	32	32	32	32	4	32	4

4.2 Memory space availability

The following tables give the free memory space available after implementing each scenario (a dash indicates that the device is not supported). The values (expressed in Kbytes) are estimated and can change according to the scenario and the code used by Cortex-M0+.

Table 11. STM32WB55 free memory space by density, without OTA

STM32WB_Copro_Wireless_Binaries FW1.16.0	Density 1				Density 2				Density 3				Density 4			
	Flash (1)	SRAM1	SRAM2a	SRAM2b	Flash (1)	SRAM1	SRAM2a	SRAM2b	Flash (1)	SRAM1	SRAM2a	SRAM2b	Flash	SRAM1	SRAM2a	SRAM2b
stm32wb5x_BLE_Stack_full_extended_fw	71	64	2	10	327	192	2	10	455	192	2	10	791	192	2	10
stm32wb5x_BLE_Stack_full_fw	107	64	10	15	363	192	10	15	491	192	10	15	827	192	10	15
stm32wb5x_BLE_Stack_light_fw	135	64	18	13	391	192	18	13	519	192	18	13	855	192	18	13
stm32wb5x_BLE_HCILayer_extended_fw	155	64	9	25(2)	411	192	9	25(2)	539	192	9	25(2)	875	192	9	25(2)
stm32wb5x_BLE_HCILayer_fw	179	64	19	25(2)	435	192	19	25(2)	563	192	19	25(2)	899	192	19	25(2)
stm32wb5x_BLE_HCI_AdvScan_fw	221	64	23	25(2)	477	192	23	25(2)	605	192	23	25(2)	941	192	23	25(2)
stm32wb5x_BLE_LLD_fw	230	64	31	16	486	192	31	16	614	192	31	16	950	192	31	16
stm32wb5x_Thread_FTD_fw	-	-	-	-	71	144	4	0	199	144	4	0	535	144	4	0
stm32wb5x_Thread_MTD_fw	-	-	-	-	156	156	4	0	284	156	4	0	620	156	4	0
stm32wb5x_Thread_RCP_fw	176	64	4	0	432	192	4	0	560	192	4	0	896	192	4	0
stm32wb5x_Zigbee_FFD_fw	-	-	-	-	185	192	4	0	313	192	4	0	649	192	4	0
stm32wb5x_Zigbee_RFD_fw	-	-	-	-	244	192	4	0	372	192	4	0	708	192	4	0
stm32wb5x_BLE_Mac_fw	22	64	23	23(2)	278	192	23	23(2)	406	192	23	23(2)	742	192	23	23(2)
stm32wb5x_BLE_Thread_static_fw	-	-	-	-	-	-	-	-	39	144	4	0	375	144	4	0
stm32wb5x_BLE_Thread_dynamic_fw	-	-	-	-	-	-	-	-	31	144	4	0	367	144	4	0
stm32wb5x_BLE_Zigbee_FFD_static_fw	-	-	-	-	22	192	8	0	150	192	8	0	486	192	8	0
stm32wb5x_BLE_Zigbee_RFD_static_fw	-	-	-	-	80	192	8	0	208	192	8	0	544	192	8	0
stm32wb5x_BLE_Zigbee_FFD_dynamic_fw	-	-	-	-	15	192	8	0	143	192	8	0	479	192	8	0
stm32wb5x_BLE_Zigbee_RFD_dynamic_fw	-	-	-	-	75	192	8	0	203	192	8	0	539	192	8	0
stm32wb5x_Mac_802_15_4_fw	188	64	4	0	444	192	4	0	572	192	4	0	908	192	4	0
stm32wb5x_802_15_4_valid_cli	169	64	32	0	425	192	32	0	553	192	32	0	889	192	32	0

1. *When smaller than 1024 KB the FUS is an internally secured memory.*
2. *When FUS (48 KB Flash and 16 KB SRAM2b) is executed available SRAM2b is reduced by 16 KB.*

Table 12. STM32WB15/50/10 M4 free memory space without OTA

STM32WB_Copro_Wireless_Binaries FW1.16.0	STM32WB15 M4				STM32WB50				STM32WB10			
	Density 1				Density 1				Density 1			
	Flash	SRAM1	SRAM2a	SRAM2b	Flash	SRAM1	SRAM2a	SRAM2b	Flash	SRAM1	SRAM2a	SRAM2b
stm32wb5x_BLE_Stack_full_extended_fw	95	12	4	0	791	64	2	10	95	12	4	0
stm32wb5x_BLE_Stack_full_fw	133	12	10	0	827	64	10	15	133	12	10	0
stm32wb5x_BLE_Stack_light_fw	161	12	12	0	855	64	18	13	161	12	12	0
stm32wb5x_BLE_HCILayer_extended_fw	184	12	13	0	875	64	9	25(1)	184	12	13	0
stm32wb5x_BLE_HCILayer_fw	205	12	19	0	899	64	19	25(1)	205	12	18	0
stm32wb5x_BLE_HCI_AdvScan_fw	245	12	21(2)	0	941	64	23	25(1)	245	12	21(2)	0
stm32wb5x_BLE_LLD_fw	255	12	10	0	950	64	31	16	255	12	10	0
stm32wb5x_Thread_FTD_fw	-	-	-	-	535	16	4	0	-	-	-	-
stm32wb5x_Thread_MTD_fw	-	-	-	-	620	28	4	0	-	-	-	-
stm32wb5x_Thread_RCP_fw	-	-	-	-	896	64	4	0	-	-	-	-
stm32wb5x_Zigbee_FFD_fw	-	-	-	-	649	64	4	0	-	-	-	-
stm32wb5x_Zigbee_RFD_fw	-	-	-	-	708	64	4	0	-	-	-	-
stm32wb5x_Mac_802_15_4_fw	-	-	-	-	908	64	4	0	-	-	-	-
stm32wb5x_802_15_4_valid_cli	-	-	-	-	888	64	32	0	-	-	-	-

1. *When FUS (48 KB Flash and 16 KB SRAM2b) is executed available SRAM2b is reduced by 16 KB.*
2. *When FUS (40 KB Flash, 4 KB SRAM2b and 12 KB SRAM2a) is executed available SRAM2a is reduced to 20 KB.*

Table 13. **Cortex M0+ code size**

M0+ code STM32Cube_FW_WB_V1.16.0	STM32WB55				STM32WB50				STM32WB15				STM32WB10			
	Flash	SRAM1	SRAM2a	SRAM2b	Flash	SRAM1	SRAM2a	SRAM2b	Flash	SRAM1	SRAM2a	SRAM2b	Flash	SRAM1	SRAM2a	SRAM2b
stm32wb5x_BLE_Stack_full_extended_fw	185	0	30	22	185	0	30	22	185	0	28	4	185	0	28	4
stm32wb5x_BLE_Stack_full_fw	149	0	22	17	149	0	22	17	147	0	22	4	147	0	22	4
stm32wb5x_BLE_Stack_light_fw	121	0	14	19	121	0	14	19	119	0	20	4	119	0	20	4
stm32wb5x_BLE_HCILayer_extended_fw	101	0	23	7	101	0	23	7	96	0	19	4	96	0	19	4
stm32wb5x_BLE_HCILayer_fw	77	0	13	7	77	0	13	7	75	0	13	4	75	0	13	4
stm32wb5x_BLE_HCI_AdvScan_fw	35	0	9	7	35	0	9	7	35	0	11	4	35	0	11	4
stm32wb5x_BLE_LLD_fw	26	0	1	16	26	0	1	16	25	0	22	4	25	0	22	4
stm32wb5x_Thread_FTD_fw	441	48	28	32	441	48	28	32	-	-	-	-	-	-	-	-
stm32wb5x_Thread_MTD_fw	356	36	28	32	356	36	28	32	-	-	-	-	-	-	-	-
stm32wb5x_Thread_RCP_fw	80	0	28	32	80	0	28	32								
stm32wb5x_Zigbee_FFD_fw	327	0	28	32	327	0	28	32	-	-	-	-	-	-	-	-
stm32wb5x_Zigbee_RFD_fw	268	0	28	32	268	0	28	32	-	-	-	-	-	-	-	-
stm32wb5x_BLE_Mac_fw	234	0	9	9	234	0	9	9								
stm32wb5x_BLE_Thread_static_fw	601	32	28	32	-	-	-	-	-	-	-	-	-	-	-	-
stm32wb5x_BLE_Thread_dynamic_fw	609	32	28	32	-	-	-	-	-	-	-	-	-	-	-	-
stm32wb5x_BLE_Zigbee_FFD_static_fw	490	0	24	32	-	-	-	-	-	-	-	-	-	-	-	-
stm32wb5x_BLE_Zigbee_RFD_static_fw	432	0	24	32	-	-	-	-	-	-	-	-	-	-	-	-
stm32wb5x_BLE_Zigbee_FFD_dynamic_fw	497	0	24	32	-	-	-	-	-	-	-	-	-	-	-	-
stm32wb5x_BLE_Zigbee_RFD_dynamic_fw	437	0	24	32	-	-	-	-	-	-	-	-	-	-	-	-
stm32wb5x_Mac_802_15_4_fw	68	0	28	32	68	0	28	32	-	-	-	-	-	-	-	-
stm32wb5x_802_15_4_valid_cli	87	0	0	32	88	0	0	32	-	-	-	-	-	-	-	-

4.3 Application examples

The following table gives examples of footprints, depending upon the application. The values of memory size (expressed in Kbytes) are estimated and can change according to the scenario.

Example :	M0(1)				FUS			APPLI M4 (2)				TOTAL memory usage w/o OTA			
	Size SRAM Used							Size SRAM Used							
	Flash	SRAM1	SRAM2A	SRAM2B	FLASH	SRAM2B	SRAM2A	Flash	SRAM1	SRAM2A	SRAM2B	Flash	SRAM1	SRAM2A	SRAM2B
STM32WB5x Heart rate	149	0	22	17	48	16	0	19	6	3	0	216	6	25	17
STM32WB1x Heart rate	147	0	22	4	40	4	12	22	6	3	0	209	6	25	4

1. *M0 code from STM32Cube_FW_WB delivery FW1.16*
2. *Code compiled with EWARM version : IAR 9.30.1*

4.4 HAL (hardware abstraction layer)

The STM32 hardware abstraction layer is available, the prototype of the HAL is for all devices, only its implementation differs. The update of the HAL implementation of the HAL is facilitated through STM32CubeMX, refer to R3 for more information.

4.5 Wireless stack

The wireless stack is available for each device and the setup uses the same process for all devices. For more information refer to R3.

4.6 FUS (firmware upgrade service)

The firmware upgrade service is available for each device and the setup uses the same process for all devices. For more information refer to R4.

5 Security and identifier migration

The table below summarizes security and identifier compatibility and features changes when migrating between STM32WB10/15/50/55 microcontrollers.

Table 14. Security and identifier compatibility

Features	STM32WB55	STM32WB50 STM32WB1x
Secure firmware installation (SFI) for bluetooth low energy and 802.15.4 SW stack	Yes	Yes
Hardware encryption AES maximum 256-bit for the application, the bluetooth low energy and IEEE802.15.4 (1)	3	2
Customer key storage/key manager services	Yes	No
HW public key authority (PKA)	Yes	Yes
Cryptographic algorithms: RSA, Diffie-Helman, ECC over GF(p)	Yes	Yes
True random number generator (RNG)	Yes	Yes
Sector protection against R/W operation (PCROP)	Yes	Yes
CRC calculation unit	Yes	Yes
Die information: 96-bit unique identifier	Yes	Yes
IEEE 64-bit unique identifier. Possibility to derive 802.15.4 64-bit and Bluetooth Low Energy 48-bit.	Yes	Yes

1. *The BLE IP internal AES is used to encrypt/decrypt BLE packet (LL). In parallel, the BLE Host running on the M0+ may need to compute keys. In this case, it uses AES2 but it is possible to use a AES software available in the BLE Host Stack. This SW solution has been implemented in the STM32WB1x, but not in the case of STM32WB50. There is no HW AES available for M4 in the case of STM32WB50. The AES2 is available for M4 in the case of STM32WB1x and AES1 for STM32WB55.*

The part number codification defined in the engineering bytes area at 0x1FFF 77DC address is associated to the part number as shown in the table below.

Table 15. Part number codification

Part number	Address byte
STM32WB5x	0xXXXX XXXX
STM32WB15	0x0000 3531
STM32WB10	0x0000 3031

6 Tools

The tools listed below are for all STM32WB10/15/50/55 devices and are backward compatible.

- STM32CubeMX
- STM32CubeProgrammer
- STM32CubeMonitor-RF

STM32CubeMX is recommended for the migration between STM32WB10/15/50/55 microcontrollers.

Revision history

Table 16. **Document revision history**

Date	Revision	Changes
16-May-2022	1	Initial release
2-Aug-2022	2	Updated: • Table 11. STM32WB55 free memory space by density, without OTA • Table 13. Cortex M0+ code size • Section 4.3 Application examples
24-May-2023	3	Updated: • Section 4.2 Memory space availability • Section 4.3 Application examples • Section 5 Security and identifier migration

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