Page EEPROMs reset procedures

Introduction

Page EEPROMs have smart and robust reset procedures, which prevent data loss.

The purpose of this application note is to describe the different reset procedures for the STMicroelectronics Standard Serial Page EEPROMs.

This application note applies to the Page EEPROM products listed in the Applicable products table below.

Table 1. Applicable products

Series	Root Part Number
Standard Serial Page EEPROM	M95P32-I M95P32-E
	M95P16-I M95P16-E
	M95P08-I M95P08-E

1 Page EEPROM initial state

At power-up, the user can monitor the power-up flag bit, that is, the PUF bit in the safety register. This indicates if the power-up operation was completed successfully; "0" means successful, "1" indicates an error. For good page EEPROM usage, the user must also ensure that all safety register bits are set to "0" at power-up.

Once the device is fully accessible, the page EEPROM is in the initial state shown in Table 2.

Table 2. Page EEPROM initial state

Power mode	Chip select	Status register	Configuration register	Safety register	Volatile register
Standby	High (deselected)	SRWD, TB, BP2, BP1, and BP0 unchanged WEL = 0 WIP = 0	DRV1, DRV0, and LID unchanged	All bits to 0	All bits to 0 except BUFLD = 1

At power-up, the hardware protection mode, SRWD, and the protection bits: TB, BP2, BP1, BP0, are in the same state as the last-used page EEPROM. The output buffer strength (DRV1 and DRV0), the identification page lock (LID), and the data memory content are also unchanged.

2 Page EEPROM reset procedures

2.1 Page EEPROM reset operation

A reset operation in Page EEPROM devices consists in recovering the device in its initial state (see Table 2). The reset procedures available in Page EEPROM are:

- Power-down/up
- Software reset
- Deep power-down enter/release

When a reset operation is performed, an internal POR (power on reset) pulse is generated. The analog and logic circuits restart, and the Page EEPROM reads some internal configuration pages to reset the device to its initial state (see Table 2).

The reset operation is useful to reinitialize the different Page EEPROM registers: status, configuration, safety, and volatile registers. It can also reinstate an internal latch, or regenerate an incorrect analog voltage. These reset operations are very robust as they are independent of the Page EEPROM internal logic circuit. This means that these operations can be performed even if the device is stalled.

Hardware reset is not implemented in page EEPROM products. None of the page EEPROM pins are dedicated to the reset procedure.

2.2 Page EEPROM power-down/power-up

Page EEPROM products include a power on reset (POR) circuit to ensure the same starting conditions for each power-up.

Power-down

Before power-down, to avoid data corruption, the following actions are recommended:

1. Monitor the WIP bit from the status register (WIP = 0).
2. Deselect the Page EEPROM.

Note: For further information about data corruption during a power loss, see the application note: AN5747, Page EEPROM memory architecture.

During power-down, the voltage decreases from V_{CC} to below the power-on reset voltage (V_{POR}). When V_{CC} is below the V_{POR} voltage, the device is locked, and it is impossible to modify any logic or memory-cell states. The reset impulse is then delivered at power-up.

To ensure a successful reset at power-up, the user must respect the power-down time for reset t_{PWD} (10 µs) (see Figure 1).

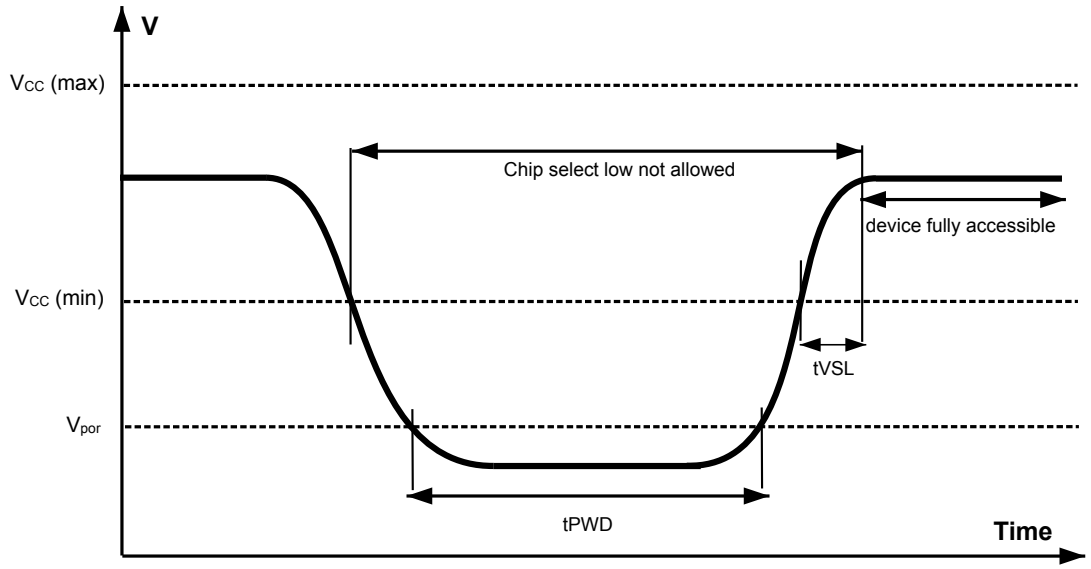
Power up

When the power supply is turned on, V_{CC} continuously rises from V_{SS} to V_{CC}. During this time, the chip select line is not allowed to float, but must follow the V_{CC} voltage. It is therefore recommended to connect the chip select line to V_{CC} via a suitable pull-up resistor (typically 100 kΩ).

When V_{CC} reaches V_{POR}, the page EEPROM is unlocked. A reset impulse is then generated and the device enters an initial state (see Table 2). This reset impulse ensures that the device always starts in a known state.

When V_{CC} reaches the minimum operating voltage (1.6 V), the device does not respond to any instruction (except status register read) during a delay of 30 µs (t_{VSL}). The read status register operation can be used to monitor the WIP (write in process) bit until the device is ready (WIP = 0).

Figure 1. Page EEPROM power-down/power-up



The power-up flag (PUF) bit in the safety register indicates whether the power-up operation was completed successfully: PUF = 0 (successful), PUF = 1 (error).

If the power-up operation fails, the device is in the following state:

- Status register bits at 1, except WEL and WIP bits at 0
- Configuration register bits at 1
- Safety register PUF bit at 1

A power-down followed by a power-up operation resets the device and places it in the same initial state (see Table 2) as the software reset and the deep power-down enter/release.

2.3 Page EEPROM software reset

The software reset procedure resets the device by triggering an internal POR. The device is then in the same initial state (see Table 2) as after power-up. To avoid accidental resets, two sequential operations must be done to perform the software reset procedure. The first sequential operation is the enable reset (RSTEN), which places the device in an enable reset state. The second sequential operation is the software reset (RESET).

Any operation other than RESET after the RSTEN command disables the enable reset state. Several enable reset operations can be sent before the software reset instruction. Once the RESET is performed, the device is reset after a delay according to Table 3. Any instruction during this period is discarded.

However, an operation (for example, a page program or a sector erase) might be running when the RESET instruction is triggered.

Therefore, the page EEPROM provides a smart software reset. This lets any ongoing modification operation such as, program, erase, write, to end before resetting the device. This is done by means of to the reset delay as shown in the table below:

Table 3. Reset delay

tRST1	tRST2	tRST3
Reset time when reset occurs with WIP = 0	Reset time when reset occurs in a modify operation, except chip erase	Reset time when reset occurs in chip erase execution
30 µs	12 ms	25 ms

Delay tRST1: WIP = 0

The WIP (write in progress) bit from the status register allows monitoring the memory state:

- WIP = 1: modification (erase, program, write) or power-up on-going
- WIP = 0: no modification in progress

If WIP = 0, then 30 µs (tRST1) is necessary to complete the full reset sequence and put the device in the initial state.

Delay tRST2: WIP = 1 and not chip erase in progress

The second longest modification operation is to write the status and the configuration registers, when two data bytes are sent. This instruction lasts a maximum of 8 ms. If WIP = 1, and no chip erase is in progress (see Table 2), the page EEPROM waits 12 ms to ensure that any modification operation has ended before resetting the device. This 12 ms covers the timing of any modification operations, such as page program, page write and erase instructions (except chip erase).

Delay tRST3: WIP = 1 and chip erase in progress

The longest modification operation in the Page EEPROM is the chip erase, which lasts between a typical value (specified in the product datasheet) and 25 ms. When a RESET is triggered, the Page EEPROM checks if a chip erase operation is running. The device waits for 25 ms (tRST3), to ensure that the chip erase operation has ended before the reset is executed.

These delays avoid a reset execution while a modification operation is in progress. The page EEPROM software reset therefore preserves the data integrity, preventing data loss.

Once the RESET operation is triggered, the page EEPROM can receive a new instruction after 30 µs, 12 ms or 25 ms. This depends on the different delays detailed previously (tRST1, tRST2 and tRST3).

The software reset operation resets the device to the same initial state as: a power-down followed by a power-up, or a deep-power down enter/release. (See Table 2.)

2.4 Page EEPROM deep power-down enter/release

The deep power-down enter (DPD) instruction allows the device to be in a very low consumption (1 µA) state. Thus, a limited number of commands is available. In the deep power-down state, only the deep power-down release (RDPD) and reset instructions (RSTEN and RESET) are recognized.

After the DPD operation is completed, Page EEPROM takes 10 µs maximum to be in the deep power mode state with low-power consumption.

When Page EEPROM is in a DPD state, if a deep power down release operation is sent then the device is reset, and ready to receive a new instruction (standby mode) 30 µs after the RDPD operation completion.

Deep power down enter/release resets the device and place it in the same initial state (see Table 2) as the power-down followed by a power-up and the software reset operation.

3 How to use reset procedures

A software reset is helpful when the user detects that an operation takes too long, or if the device stalls. The software reset procedure must be attempted before any other reset procedure.

If the software reset does not work, the user should attempt a deep power mode enter/release to reset the device. If this does not solve the issue, a power-down/up is the next procedure to attempt.

The reset impulse performed by the power-down/up procedure might help in the following cases: if the device stalls and does not process a software reset instruction, or during deep power mode enter/release (see Section 2.4).

The power-down/up procedure is the last reset procedure to attempt, as it might cause data corruption.

Revision history

Table 4. **Document revision history**

Date	Version	Changes
28-Feb-2023	1	Initial release.

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