

## Migrating from STM32WB10/30 to STM32WB15/35 microcontrollers

### Introduction

For designers of STM32 microcontroller applications, the ability to smoothly replace one microcontroller with another from the same product family is an important asset. Migrating an application to a different microcontroller is often a must when product requirements grow. This puts extra demand on memory size, or needs an increase of the number of I/Os. Cost reduction is another motivation to switch to smaller components, and shrink the PCB area.

This document analyzes the key steps required for migrating between STM32WB10/15/30/35 microcontrollers, namely hardware, peripheral availability, firmware, security, and tools. For a full understanding, the end user must be familiar with STM32WB series microcontrollers (see the documents in [Table 2](#)).

**Table 1. Applicable products**

| Type             | Part numbers                                                                 |
|------------------|------------------------------------------------------------------------------|
| Microcontrollers | STM32WB10CC, STM32WB15CC, STM32WB30CE, STM32WB35CC, STM32WB35CE, STM32WB35CZ |

## 1 General information

This document applies to STM32WB10/15/30/35 microcontrollers, based on Arm® Cortex® cores.

*Note:* Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.



**Table 2. Reference documents and tools**

| Reference | Document ID | Title                                                                                                                              |
|-----------|-------------|------------------------------------------------------------------------------------------------------------------------------------|
| R1        | RM0434      | Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® Low Energy and 802.15.4 radio solution <sup>(1)</sup> |
| R2        | DS11929     | Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® 5.2 and 802.15.4 radio solution <sup>(1)</sup>        |
| R3        | -           | STM32CubeMX: video <sup>(1)</sup>                                                                                                  |
| R4        | AN5185      | ST firmware upgrade services for STM32WB Series <sup>(1)</sup>                                                                     |
| R5        | AN5105      | Getting started with touch sensing control on STM32 microcontrollers <sup>(1)</sup>                                                |
| R6        | RM0473      | Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® 5.2 radio solution <sup>(1)</sup>                     |
| R7        | RM0478      | Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® 5.2 radio solution <sup>(1)</sup>                     |
| R8        | RM0471      | Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® Low Energy or 802.15.4 radio solution <sup>(1)</sup>  |
| R9        | DS13258     | Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® 5.2 radio solution <sup>(1)</sup>                     |
| R10       | DS13259     | Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® 5.2 radio solution <sup>(1)</sup>                     |
| R11       | DS13047     | Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® 5.2 or 802.15.4 radio solution <sup>(1)</sup>         |
| R12       | ES0394      | STM32WB55xx/STM32WB35Cx device errata <sup>(1)</sup>                                                                               |
| R13       | ES0492      | STM32WB50CG/30CE device errata <sup>(1)</sup>                                                                                      |
| R14       | ES0556      | STM32WB10CC device errata <sup>(1)</sup>                                                                                           |
| R15       | ES0557      | STM32WB15CC device errata <sup>(1)</sup>                                                                                           |

1. Available at [www.st.com](http://www.st.com).

## 2 Hardware migration

This section presents a summary of the main hardware differences.

### 2.1 Package overview

Table 3 details the available packages.

**Table 3. Package information**

| Package <sup>(1)</sup>            | Number of pins | STM32WB15 | STM32WB35 | STM32WB10 | STM32WB30 | Part numbers                                                 |
|-----------------------------------|----------------|-----------|-----------|-----------|-----------|--------------------------------------------------------------|
| UFQFPN48 <sup>(2)</sup>           | 48             | X         | X         | X         | X         | STM32WB15CCU<br>STM32WB35CxU<br>STM32WB10CCU<br>STM32WB30CEU |
| UFQFPN48 with extended IOs option | 48             | X         | -         | -         | -         | STM32WB15CCUxE                                               |
| WLCSP49                           | 49             | X         | -         | -         | -         | STM32WB15CCY                                                 |

1. "X" = available, "-" = device is not produced with this package.

2. On UFQFPN48 packages of STM32WB3x, there is excessive current on VDDA or VDD when V<sub>DD</sub> is different from V<sub>DDA</sub>. The limitation is detailed in [R12](#) and [R13](#).

### 2.2 RF performance

The STM32WB30/35 microcontrollers embed a powerful and ultra-low power radio compliant with Bluetooth® Low Energy stack and with IEEE 802.15.4-2011. The STM32WB10/15 microcontrollers embed a powerful and ultra-low power radio compliant with Bluetooth® Low Energy stack.

**Table 4. Bluetooth Low Energy on-air data rate**

| Bluetooth Low Energy on-air data rate | STM32WB15 | STM32WB35 | STM32WB10 | STM32WB30 |
|---------------------------------------|-----------|-----------|-----------|-----------|
| 2 Mbit/s                              | X         | X         | -         | -         |
| 1 Mbit/s                              | X         | X         | X         | X         |

**Note:** For more details regarding RF electrical characteristics refer to the datasheets.

### 2.3 Pinout differences

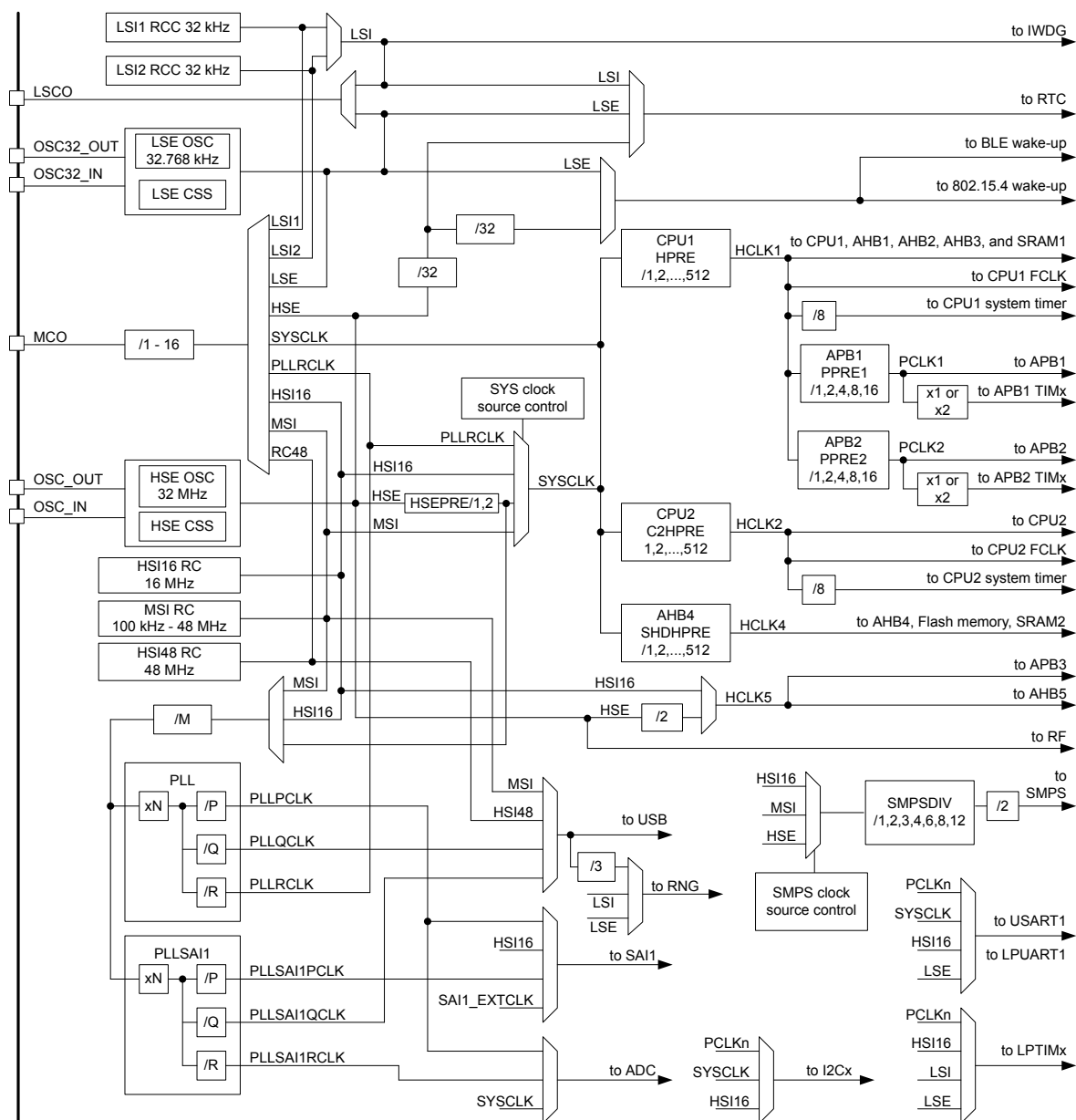
The STM32WB10/15/30/35 microcontrollers have different packages, therefore migration requires a particular attention regarding GPIOs and their associated alternate functions. The pin-to-pin compatible devices are listed below (for other packages refer to the datasheets).

- STM32WB35 in UFQFPN48 package is pin-to-pin compatible with STM32WB15 in UFQFPN48 package.
- STM32WB30 in UFQFPN48 package is pin-to-pin compatible with STM32WB10 in UFQFPN48 package.

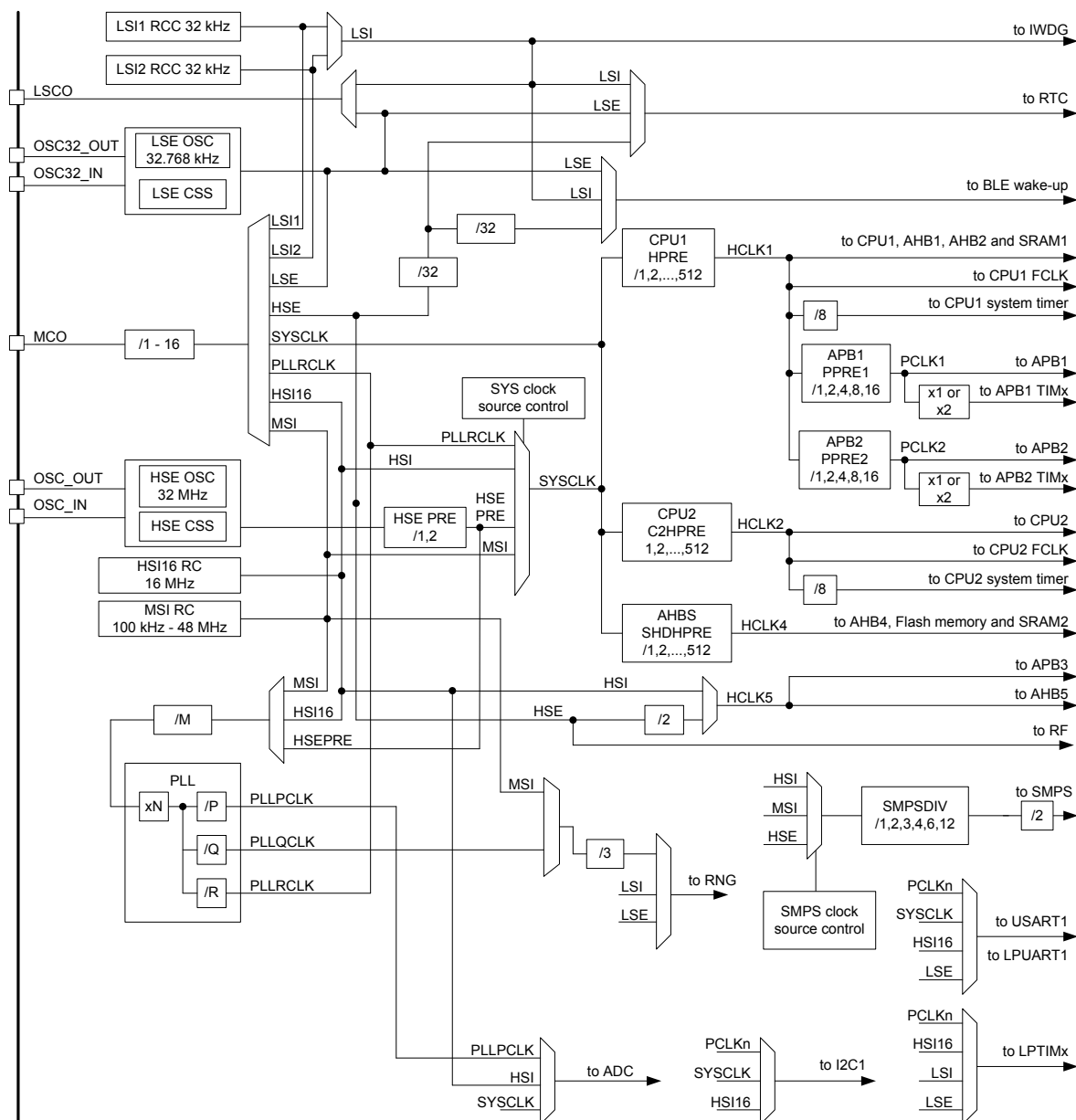
### 2.4 Clock tree

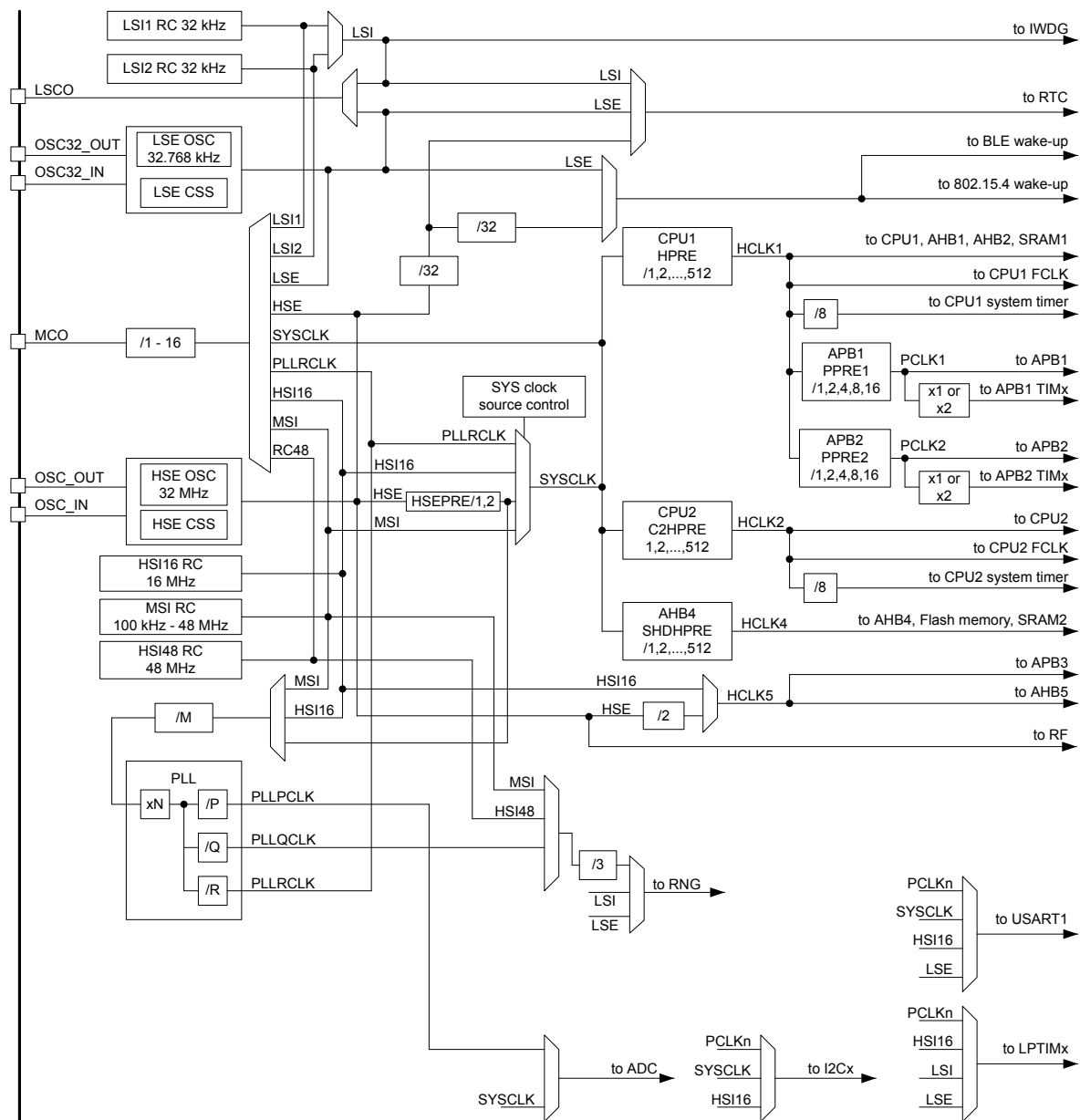
The STM32WB35 and STM32WB15 clock trees are shown, respectively, in [Figure 1](#) and [Figure 2](#). The 802.15.4, the AHB3, the PLLSAI1, the SAI1, the USB, and the HSI48 RC, are not available on STM32WB15, but the LSI can be selected for BLE wake-up.

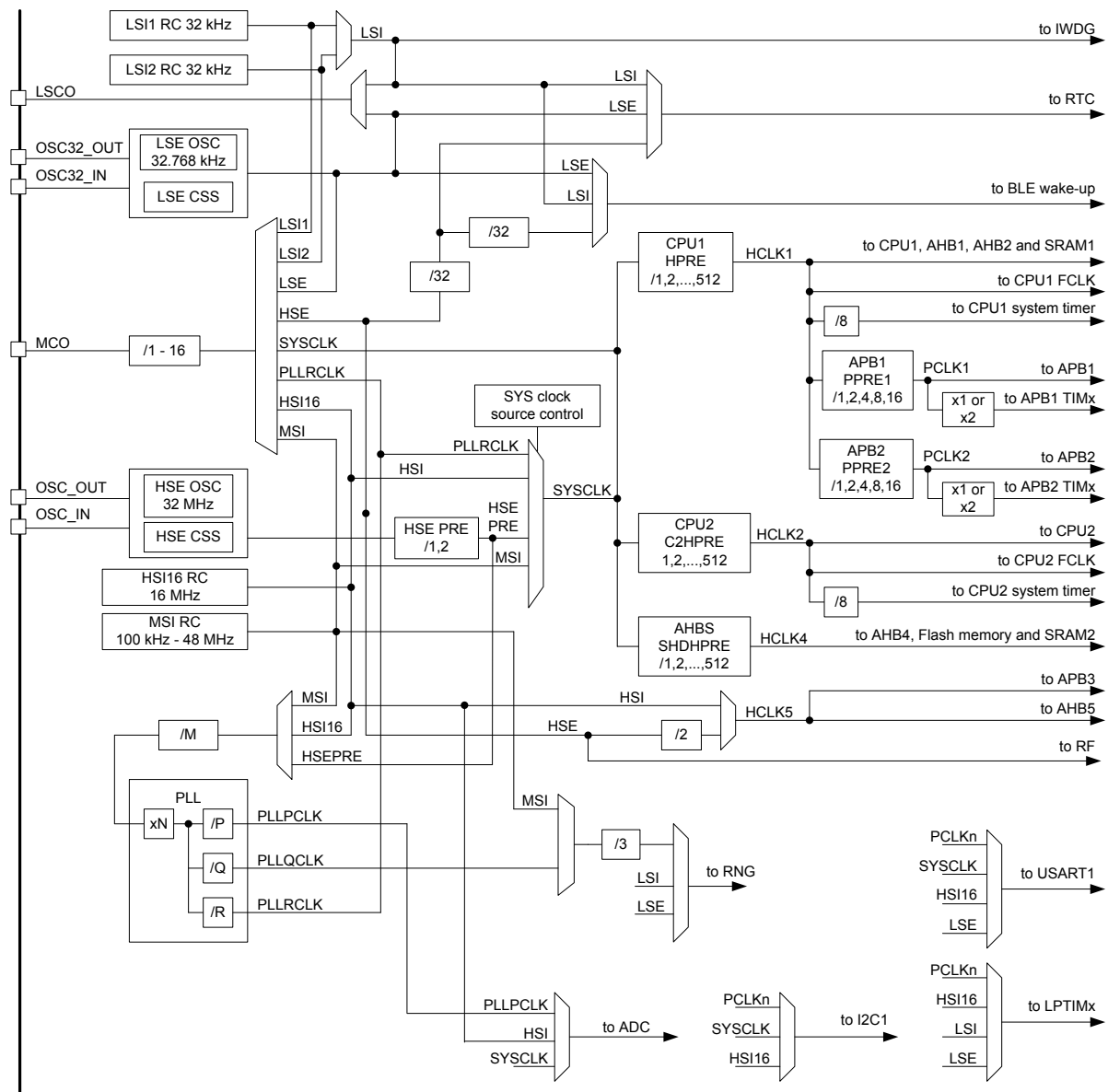
The STM32WB30 and STM32WB10 clock trees are shown, respectively, in [Figure 3](#) and [Figure 4](#). The 802.15.4 and the HSI48 RC are not available on STM32WB10, but the LSI can be selected for BLE wake-up.

**Figure 1. STM32WB35 clock tree**


### Figure 2. STM32WB15 clock tree



**Figure 3. STM32WB30 clock tree**


**Figure 4. STM32WB10 clock tree**


### 3 Peripheral migration

Table 5 summarizes the compatibility of peripherals, and the features changes.

**Table 5. Peripheral compatibility and features**

| Peripheral / Features                       | STM32WB15                        |         | STM32WB35        | STM32WB10      | STM32WB30 |
|---------------------------------------------|----------------------------------|---------|------------------|----------------|-----------|
|                                             | UFQFPN48 <sup>(1)</sup>          | WLCSP49 | UFQFPN48         | UFQFPN48       | UFQFPN48  |
| Bluetooth 5                                 | Yes                              |         |                  |                |           |
| IEEE 802.15.4                               | No                               |         | Yes              | No             | Yes       |
| Dual core CPU (Cortex-M4 and M0+)           | Yes                              |         |                  |                |           |
| Flash memory (Kbytes)                       | 320                              |         | Up to 512        | 320            | 512       |
| SRAM (Kbytes)                               | 48                               |         | 96               | 48             | 96        |
| QUADSPI                                     | 0                                |         | 1                | 0              |           |
| DMA                                         | 1 (7 channels)                   |         | 2 (14 channels)  | 1 (7 channels) |           |
| 16-bit advanced timer (TIM1)                | 1                                |         |                  |                |           |
| 32-bit general purpose timer (TIM2)         | 1                                |         |                  |                |           |
| 16-bit general purpose timers (TIM16/TIM17) | 0                                |         | 2                | 0              | 2         |
| 16-bit low-power timers (LPTIM1/LPTIM2)     | 2                                |         |                  |                |           |
| Watchdog timer                              | 2                                |         |                  |                |           |
| SysTick timer                               | 1                                |         |                  |                |           |
| SPI                                         | 1                                |         |                  |                |           |
| I <sup>2</sup> C (inter-integrated circuit) | 1                                |         | 2                | 1              | 2         |
| USART (can be used as SPI)                  | 1                                |         |                  |                |           |
| LPUART                                      | 1                                |         |                  | No             |           |
| SAI (serial audio interface)                | No                               |         | 1 (dual channel) | No             |           |
| USB FS                                      | No                               |         | 1                | No             |           |
| RTC                                         | 1                                |         |                  |                |           |
| Tamper pins                                 | 1                                |         |                  |                |           |
| Wake-up pins                                | 2                                |         |                  |                |           |
| GPIOs                                       | 30 (37 for extended IOs option)  | 25      | 30               |                |           |
| TSC (capacitive touch sensing)              | 3 (8 for extended IOs option)    | 2       | No               | 3              | No        |
| 12-bit ADC                                  | 13 channels                      |         |                  |                |           |
| Internal V <sub>REF</sub>                   | Yes                              |         |                  |                |           |
| Analog comparator (COMP)                    | 1                                |         | 2                | No             |           |
| Max CPU frequency                           | 64 MHz                           |         |                  |                |           |
| JTAG / SW-DP                                | 1 / 1                            |         |                  |                |           |
| PLL                                         | 1                                |         | 2                | 1              |           |
| Operating temperature range 1               | -40 to +85 °C                    |         |                  | -10 to +85 °C  |           |
| Operating temperature range 2               | -40 to +105 °C                   |         |                  | No             |           |
| Operating voltage                           | 1.71 to 3.6 V                    |         |                  | 2.0 to 3.6 V   |           |
| SMPS                                        | Yes (No for extended IOs option) | Yes     |                  | No             |           |

1. Two configurations available, with SMPS or with extended IOs.



## 3.1 Hardware migration

This section presents a summary of the main hardware differences.

### 3.1.1 Flash memory mapping

Different memory sizes are available according to the package selected, for more information refer to the table below. The page size is 4 Kbytes for STM32WB30/5 devices, 2 Kbytes for STM32WB10/5 devices.

**Table 6. Flash memory sizes and their mapping**

| Device    | Flash memory size (Kbytes) | Mapping addresses         | Description                                                                   |
|-----------|----------------------------|---------------------------|-------------------------------------------------------------------------------|
| STM32WB15 | 320                        | 0x0800 0000 – 0x0804 FFFF | The start addresses are the same for all STM32WB10/15/30/35 microcontrollers. |
| STM32WB10 | 320                        | 0x0800 0000 – 0x0804 FFFF |                                                                               |
| STM32WB35 | 256, 512                   | 0x0800 0000 – 0x0807 FFFF |                                                                               |
| STM32WB30 | 512                        | 0x0800 0000 – 0x0807 FFFF |                                                                               |

### 3.1.2 SRAM mapping

As shown in Table 7 the SRAM1 density of STM32WB15 and STM32WB10 is reduced when compared with, respectively, STM32WB35 and STM32WB30.

**Table 7. SRAM sizes and their mapping**

| Device    | SRAM <sup>(1)</sup> | Size (Kbytes) | Mapping addresses         | STM32WB1x versus STM32WB3x                                                                                                                                                                                                                                                            |
|-----------|---------------------|---------------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| STM32WB15 | SRAM1               | 12            | 0x2000 0000 - 0x2000 2FFF | <ul style="list-style-type: none"> <li>SRAM1 size is reduced from 32 to 12 Kbytes, and starts at the same address.</li> <li>SRAM2a has the same size, and starts at the same address.</li> </ul>                                                                                      |
|           | SRAM2a              | 32            | 0x2003 0000 - 0x2003 7FFF |                                                                                                                                                                                                                                                                                       |
|           | SRAM2b              | 4             | 0x2003 8000 - 0x2003 8FFF |                                                                                                                                                                                                                                                                                       |
|           |                     | Total: 48     |                           |                                                                                                                                                                                                                                                                                       |
| STM32WB35 | SRAM1               | 32            | 0x2000 0000 - 0x2000 7FFF | <ul style="list-style-type: none"> <li>SRAM1 size is reduced from 32 to 12 Kbytes, and starts at the same address.</li> <li>SRAM2a has the same size, and starts at the same address.</li> </ul>                                                                                      |
|           | SRAM2a              | 32            | 0x2003 0000 - 0x2003 7FFF |                                                                                                                                                                                                                                                                                       |
|           | SRAM2b              | 32            | 0x2003 8000 - 0x2003 FFFF |                                                                                                                                                                                                                                                                                       |
|           |                     | Total: 96     |                           |                                                                                                                                                                                                                                                                                       |
| STM32WB10 | SRAM1               | 12            | 0x2000 0000 - 0x2000 2FFF | <ul style="list-style-type: none"> <li>SRAM1 size is reduced from 32 to 12 Kbytes, and starts at the same address.</li> <li>SRAM2a has the same size, and starts at the same address.</li> </ul>                                                                                      |
|           | SRAM2a              | 32            | 0x2003 0000 - 0x2003 7FFF |                                                                                                                                                                                                                                                                                       |
|           | SRAM2b              | 4             | 0x2003 8000 - 0x2003 8FFF |                                                                                                                                                                                                                                                                                       |
|           |                     | Total: 48     |                           |                                                                                                                                                                                                                                                                                       |
| STM32WB30 | SRAM1               | 32            | 0x2000 0000 - 0x2000 7FFF | <ul style="list-style-type: none"> <li>SRAM1 size is reduced from 32 to 12 Kbytes, and starts at the same address.</li> <li>SRAM2a has the same size, and starts at the same address.</li> <li>SRAM2b size is reduced from 32 to 4 Kbytes, and starts at the same address.</li> </ul> |
|           | SRAM2a              | 32            | 0x2003 0000 - 0x2003 7FFF |                                                                                                                                                                                                                                                                                       |
|           | SRAM2b              | 32            | 0x2003 8000 - 0x2003 FFFF |                                                                                                                                                                                                                                                                                       |
|           |                     | Total: 96     |                           |                                                                                                                                                                                                                                                                                       |

1. SRAM2a is retained in Standby mode for all products. SRAM1 and SRAM2b are retained in Standby mode for STM32WB10/15 products.

### 3.1.3 Peripheral migration compatibility

This section presents a complete view of the number of available peripherals. For more details regarding electrical characteristics refer to the datasheets.

**Table 8. Peripheral compatibility analysis**

| Peripheral <sup>(1)</sup>                   | STM32WB15                        |         | STM32WB35       | STM32WB10      | STM32WB30 |
|---------------------------------------------|----------------------------------|---------|-----------------|----------------|-----------|
|                                             | UFQFPN48 <sup>(2)</sup>          | WLCSP49 | UFQFPN48        | UFQFPN48       | UFQFPN48  |
| QUADSPI                                     | NA                               |         | 1               | NA             |           |
| DMA                                         | 1 (7 channels)                   |         | 2 (14 channels) | 1 (7 channels) |           |
| SPI                                         | 1                                |         |                 |                |           |
| I <sup>2</sup> C (inter-integrated circuit) | 1                                |         |                 |                |           |
| SAI (serial audio interface)                | NA                               |         | 1               | NA             |           |
| LPUART                                      | 1                                |         |                 | NA             |           |
| USB                                         | NA                               |         | 1               | NA             |           |
| ADC <sup>(3)</sup>                          | 1 × 13 channels                  |         |                 |                |           |
| COMP                                        | NA                               |         | 2               | NA             |           |
| GPIOs <sup>(4)</sup>                        | 30 (37 for extended I/Os option) | 25      | 30              |                |           |
| TSC <sup>(5)</sup>                          | 3 (8 for extended I/Os option)   | 2       | 0               | 3              | 0         |
| Tamper pins                                 | 1                                |         |                 |                |           |
| JTAG / SWD                                  | 1 / 1                            |         |                 |                |           |
| PLL (phase-locked loop)                     | 1                                |         |                 |                |           |

1. NA: Not available.
2. Two configurations available, with SMPS or with extended IOs.
3. For the ADC sampling rate refer to [Table 9](#).
4. STM32WB10/15/30/35 microcontrollers in UFQFPN48 package are pin-to-pin compatible.
5. Number of keys including the shield that can be driven with the TSC peripheral. For more information about TSC and connection of sensors refer to [R5](#).

**Table 9. ADC sampling rate (Mbit/s)**

| Resolution | STM32WB35     |               | STM32WB15                |                          | STM32WB30 | STM32WB10 |
|------------|---------------|---------------|--------------------------|--------------------------|-----------|-----------|
|            | Fast channels | Slow channels | V <sub>DDA</sub> > 2.0 V | V <sub>DDA</sub> ≤ 2.0 V |           |           |
| 12 bits    | 4.26          | 3.36          | 2.50                     | 2.18                     | 2.13      | 2.50      |
| 10 bits    | 4.92          | 4.00          | 2.92                     | 2.50                     | 2.46      | 2.92      |
| 8 bits     | 5.81          | 4.57          | 3.50                     | 2.92                     | 2.91      | 3.50      |
| 6 bits     | 7.11          | 7.11          | 4.38                     | 3.50                     | 3.55      | 4.38      |

## 4 Software migration

This section gives an overview of the possible use cases, and information on the available free memory space for flash memory and SRAM when implementing the different scenarios.

The wireless stack and the application firmware can be upgraded over-the-air (OTA feature).

### 4.1 Memory density

**Table 10. Flash memory and SRAM densities**

| Footprint (Kbytes) | STM32WB15 | STM32WB35 |           | STM32WB10 | STM32WB30 |
|--------------------|-----------|-----------|-----------|-----------|-----------|
|                    | Density 1 | Density 1 | Density 2 |           |           |
| Flash memory       | 320       | 256       | 512       | 320       | 512       |
| SRAM1              | 12        | 32        |           | 12        | 32        |
| SRAM2a             | 32        |           |           |           |           |
| SRAM2b             | 4         | 32        |           | 4         | 32        |

## 4.2 Memory space availability

The following tables give the free memory space available after implementing each scenario (a dash indicates "Not supported"). The values (expressed in Kbytes) are estimated and can change according to the scenario and to the code used by Cortex-M0+.

**Table 11. STM32WB35 free memory space by density, without OTA**

| STM32WB_Copro_Wireless_Binaries<br>FW1.14.1 | Density 1            |       |        |                   | Density 2            |       |        |                   |
|---------------------------------------------|----------------------|-------|--------|-------------------|----------------------|-------|--------|-------------------|
|                                             | Flash <sup>(1)</sup> | SRAM1 | SRAM2a | SRAM2b            | Flash <sup>(1)</sup> | SRAM1 | SRAM2a | SRAM2b            |
| stm32wb5x_BLE_Stack_full_extended_fw        | 71                   | 32    | 2      | 10                | 327                  | 32    | 2      | 10                |
| stm32wb5x_BLE_Stack_full_fw                 | 107                  | 32    | 10     | 15                | 363                  | 32    | 10     | 15                |
| stm32wb5x_BLE_Stack_light_fw                | 135                  | 32    | 18     | 13                | 391                  | 32    | 18     | 13                |
| stm32wb5x_BLE_HCILayer_extended_fw          | 155                  | 32    | 9      | 25 <sup>(2)</sup> | 411                  | 32    | 9      | 25 <sup>(2)</sup> |
| stm32wb5x_BLE_HCILayer_fw                   | 179                  | 32    | 19     | 25 <sup>(2)</sup> | 435                  | 32    | 19     | 25 <sup>(2)</sup> |
| stm32wb5x_BLE_HCI_AdvScan_fw                | 221                  | 32    | 23     | 25 <sup>(2)</sup> | 477                  | 32    | 23     | 25 <sup>(2)</sup> |
| stm32wb5x_BLE_LLD_fw                        | 230                  | 32    | 31     | 16                | 486                  | 32    | 31     | 16                |
| stm32wb5x_Thread_FTD_fw                     | -                    | -     | -      | -                 | -                    | -     | -      | -                 |
| stm32wb5x_Thread_MTD_fw                     | -                    | -     | -      | -                 | -                    | -     | -      | -                 |
| stm32wb5x_Thread_RCP_fw                     | 176                  | 32    | 4      | 0                 | 432                  | 32    | 4      | 0                 |
| stm32wb5x_Zigbee_FFD_fw                     | -                    | -     | -      | -                 | 185                  | 32    | 4      | 0                 |
| stm32wb5x_Zigbee_RFD_fw                     | -                    | -     | -      | -                 | 244                  | 32    | 4      | 0                 |
| stm32wb5x_BLE_Mac_fw                        | 22                   | 32    | 23     | 23 <sup>(2)</sup> | 278                  | 32    | 23     | 23 <sup>(2)</sup> |
| stm32wb5x_BLE_Thread_static_fw              | -                    | -     | -      | -                 | -                    | -     | -      | -                 |
| stm32wb5x_BLE_Thread_dynamic_fw             | -                    | -     | -      | -                 | -                    | -     | -      | -                 |
| stm32wb5x_BLE_Zigbee_FFD_static_fw          | -                    | -     | -      | -                 | -                    | -     | -      | -                 |
| stm32wb5x_BLE_Zigbee_RFD_static_fw          | -                    | -     | -      | -                 | -                    | -     | -      | -                 |
| stm32wb5x_BLE_Zigbee_FFD_dynamic_fw         | -                    | -     | -      | -                 | -                    | -     | -      | -                 |
| stm32wb5x_BLE_Zigbee_RFD_dynamic_fw         | -                    | -     | -      | -                 | -                    | -     | -      | -                 |
| stm32wb5x_Mac_802_15_4_fw                   | 188                  | 32    | 4      | 0                 | 444                  | 32    | 4      | 0                 |
| stm32wb5x_802_15_4_valid_cli                | 169                  | 32    | 32     | 0                 | 425                  | 32    | 32     | 0                 |

1. The FUS is an internally secured memory.

2. When FUS (48 KB flash and 16 KB SRAM2b) is executed, available SRAM2b is reduced to 16 KB.

**Table 12. STM32WB15/30/10 free memory space, without OTA**

| STM32WB_Copro_Wireless_Binaries<br>FW1.14.1 | STM32WB15 |       |                   |        | STM32WB30            |       |        |                   | STM32WB10 |       |                   |        |
|---------------------------------------------|-----------|-------|-------------------|--------|----------------------|-------|--------|-------------------|-----------|-------|-------------------|--------|
|                                             | Flash     | SRAM1 | SRAM2a            | SRAM2b | Flash <sup>(1)</sup> | SRAM1 | SRAM2a | SRAM2b            | Flash     | SRAM1 | SRAM2a            | SRAM2b |
| stm32wb5x_BLE_Stack_full_extended_fw        | 95        | 12    | 4                 | 0      | 327                  | 32    | 2      | 10                | 135       | 12    | 4                 | 0      |
| stm32wb5x_BLE_Stack_full_fw                 | 133       | 12    | 10                | 0      | 363                  | 32    | 10     | 15                | 173       | 12    | 10                | 0      |
| stm32wb5x_BLE_Stack_light_fw                | 161       | 12    | 12                | 0      | 391                  | 32    | 18     | 13                | 201       | 12    | 12                | 0      |
| stm32wb5x_BLE_HCIDLayer_extended_fw         | 184       | 12    | 13                | 0      | 411                  | 32    | 9      | 25 <sup>(2)</sup> | 224       | 12    | 13                | 0      |
| stm32wb5x_BLE_HCIDLayer_fw                  | 205       | 12    | 19                | 0      | 435                  | 32    | 19     | 25 <sup>(2)</sup> | 245       | 12    | 18                | 0      |
| stm32wb5x_BLE_HCI_AdvScan_fw                | 245       | 12    | 21 <sup>(3)</sup> | 0      | 477                  | 32    | 23     | 25 <sup>(2)</sup> | 285       | 12    | 21 <sup>(3)</sup> | 0      |
| stm32wb5x_BLE_LLD_fw                        | 255       | 12    | 10                | 0      | 486                  | 32    | 31     | 16                | 295       | 12    | 10                | 0      |
| stm32wb5x_Thread_FTD_fw                     | -         | -     | -                 | -      | -                    | -     | -      | -                 | -         | -     | -                 | -      |
| stm32wb5x_Thread_MTD_fw                     | -         | -     | -                 | -      | -                    | -     | -      | -                 | -         | -     | -                 | -      |
| stm32wb5x_Thread_RCP_fw                     | -         | -     | -                 | -      | 432                  | 32    | 4      | 0                 | -         | -     | -                 | -      |
| stm32wb5x_Zigbee_FFD_fw                     | -         | -     | -                 | -      | 185                  | 32    | 4      | 0                 | -         | -     | -                 | -      |
| stm32wb5x_Zigbee_RFD_fw                     | -         | -     | -                 | -      | 244                  | 32    | 4      | 0                 | -         | -     | -                 | -      |
| stm32wb5x_BLE_Mac_fw                        | -         | -     | -                 | -      | 278                  | 32    | 23     | 23 <sup>(2)</sup> | -         | -     | -                 | -      |
| stm32wb5x_BLE_Thread_static_fw              | -         | -     | -                 | -      | -                    | -     | -      | -                 | -         | -     | -                 | -      |
| stm32wb5x_BLE_Thread_dynamic_fw             | -         | -     | -                 | -      | -                    | -     | -      | -                 | -         | -     | -                 | -      |
| stm32wb5x_BLE_Zigbee_FFD_static_fw          | -         | -     | -                 | -      | -                    | -     | -      | -                 | -         | -     | -                 | -      |
| stm32wb5x_BLE_Zigbee_RFD_static_fw          | -         | -     | -                 | -      | -                    | -     | -      | -                 | -         | -     | -                 | -      |
| stm32wb5x_BLE_Zigbee_FFD_dynamic_fw         | -         | -     | -                 | -      | -                    | -     | -      | -                 | -         | -     | -                 | -      |
| stm32wb5x_BLE_Zigbee_RFD_dynamic_fw         | -         | -     | -                 | -      | -                    | -     | -      | -                 | -         | -     | -                 | -      |
| stm32wb5x_Mac_802_15_4_fw                   | -         | -     | -                 | -      | 444                  | 32    | 4      | 0                 | -         | -     | -                 | -      |
| stm32wb5x_802_15_4_valid_cli                | -         | -     | -                 | -      | 424                  | 32    | 32     | 0                 | -         | -     | -                 | -      |

1. The FUS is an internally secured memory.
2. When FUS (48 KB flash and 16 KB SRAM2b) is executed, available SRAM2b is reduced to 16 KB.
3. When FUS (40 KB flash, 4 KB SRAM2b and 12 KB SRAM2a) is executed, available SRAM2a is reduced to 20 KB.

**Table 13. Cortex M0+ code size**

| M0 code STM32Cube_FW_WB_V1.14.1      | STM32WB15 |       |        |        | STM32WB35 |       |        |        | STM32WB10 |       |        |        | STM32WB30 |       |        |        |
|--------------------------------------|-----------|-------|--------|--------|-----------|-------|--------|--------|-----------|-------|--------|--------|-----------|-------|--------|--------|
|                                      | Flash     | SRAM1 | SRAM2a | SRAM2b | Flash     | SRAM1 | SRAM2a | SRAM2b | Flash     | SRAM1 | SRAM2a | SRAM2b | Flash     | SRAM1 | SRAM2a | SRAM2b |
| stm32wb5x_BLE_Stack_full_extended_fw | 185       | 0     | 28     | 4      | 185       | 0     | 30     | 22     | 185       | 0     | 28     | 4      | 185       | 0     | 30     | 22     |
| stm32wb5x_BLE_Stack_full_fw          | 147       | 0     | 22     | 4      | 149       | 0     | 22     | 17     | 147       | 0     | 22     | 4      | 149       | 0     | 22     | 17     |
| stm32wb5x_BLE_Stack_light_fw         | 119       | 0     | 20     | 4      | 121       | 0     | 14     | 19     | 119       | 0     | 20     | 4      | 121       | 0     | 14     | 19     |
| stm32wb5x_BLE_HCILayer_extended_fw   | 96        | 0     | 19     | 4      | 101       | 0     | 23     | 7      | 96        | 0     | 19     | 4      | 101       | 0     | 23     | 7      |
| stm32wb5x_BLE_HCILayer_fw            | 75        | 0     | 13     | 4      | 77        | 0     | 13     | 7      | 75        | 0     | 13     | 4      | 77        | 0     | 13     | 7      |
| stm32wb5x_BLE_HCI_AdvScan_fw         | 35        | 0     | 11     | 4      | 35        | 0     | 9      | 7      | 35        | 0     | 11     | 4      | 35        | 0     | 9      | 7      |
| stm32wb5x_BLE_LLD_fw                 | 25        | 0     | 22     | 4      | 26        | 0     | 1      | 16     | 25        | 0     | 22     | 4      | 26        | 0     | 1      | 16     |
| stm32wb5x_Thread_FTD_fw              | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      |
| stm32wb5x_Thread_MTD_fw              | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      |
| stm32wb5x_Thread_RCP_fw              | -         | -     | -      | -      | 80        | 0     | 28     | 32     | -         | -     | -      | -      | 80        | 0     | 28     | 32     |
| stm32wb5x_Zigbee_FFD_fw              | -         | -     | -      | -      | 327       | 0     | 28     | 32     | -         | -     | -      | -      | 327       | 0     | 28     | 32     |
| stm32wb5x_Zigbee_RFD_fw              | -         | -     | -      | -      | 268       | 0     | 28     | 32     | -         | -     | -      | -      | 268       | 0     | 28     | 32     |
| stm32wb5x_BLE_Mac_fw                 | -         | -     | -      | -      | 234       | 0     | 9      | 9      | -         | -     | -      | -      | 234       | 0     | 9      | 9      |
| stm32wb5x_BLE_Thread_static_fw       | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      |
| stm32wb5x_BLE_Thread_dynamic_fw      | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      |
| stm32wb5x_BLE_Zigbee_FFD_static_fw   | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      |
| stm32wb5x_BLE_Zigbee_RFD_static_fw   | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      |
| stm32wb5x_BLE_Zigbee_FFD_dynamic_fw  | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      |
| stm32wb5x_BLE_Zigbee_RFD_dynamic_fw  | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      | -         | -     | -      | -      |
| stm32wb5x_Mac_802_15_4_fw            | -         | -     | -      | -      | 68        | 0     | 28     | 32     | -         | -     | -      | -      | 68        | 0     | 28     | 32     |
| stm32wb5x_802_15_4_valid_cli         | -         | -     | -      | -      | 88        | 0     | 0      | 32     | -         | -     | -      | -      | 88        | 0     | 0      | 32     |

### 4.3 Application examples

Table 14 gives examples of footprints, depending upon the application. The values of memory size (expressed in Kbytes) are estimated and can change according to the scenario.

**Table 14. Used memory (Kbytes)**

| Example              | Cortex M0+ |       |        |        | FUS   |        |        | Cortex M4 (application)<br>(2) |       |        |        | Total used memory<br>(without OTA) |       |        |        |
|----------------------|------------|-------|--------|--------|-------|--------|--------|--------------------------------|-------|--------|--------|------------------------------------|-------|--------|--------|
|                      | Flash      | SRAM1 | SRAM2a | SRAM2b | Flash | SRAM2b | SRAM2a | Flash                          | SRAM1 | SRAM2a | SRAM2b | Flash                              | SRAM1 | SRAM2a | SRAM2b |
| STM32WB3x heart rate | 149        | 0     | 22     | 17     | 48    | 16     | 0      | 19                             | 6     | 3      | 0      | 216                                | 6     | 25     | 17     |
| STM32WB1x heart rate | 147        | 0     | 22     | 4      | 40    | 4      | 12     | 22                             | 6     | 3      | 0      | 209                                | 6     | 25     | 4      |

1. Code from STM32Cube\_FW\_WB\_V1.16 delivery.
2. Code compiled with EWARM version IAR™ 9.30.1.

#### 4.4 HAL (hardware abstraction layer)

The STM32 hardware abstraction layer is available, the prototype of the HAL is for all devices, only its implementation differs. The update of the HAL implementation of the HAL is facilitated through STM32CubeMX, refer to [R3](#) for more information.

#### 4.5 Wireless stack

The wireless stack is available for each device and the setup uses the same process for all devices. For more information refer to [R3](#).

#### 4.6 FUS (firmware upgrade service)

The firmware upgrade service is available for each device and the setup uses the same process for all devices. For more information refer to [R4](#).

## 5 Security and identifier migration

The table below summarizes security and identifier compatibility and features changes when migrating between STM32WB10/15/30/35 microcontrollers.

**Table 15. Security and identifier compatibility**

| Features                                                                                                              | STM32WB35 | STM32WB10<br>STM32WB15<br>STM32WB30 |
|-----------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------|
| Secure firmware installation (SFI) for Bluetooth Low Energy and 802.15.4 SW stack                                     | Yes       |                                     |
| Hardware encryption AES maximum 256-bit for the application, the Bluetooth Low Energy and IEEE802.15.4 <sup>(1)</sup> | 3         | 2                                   |
| Customer key storage/key manager services                                                                             | Yes       | No                                  |
| HW public key authority (PKA)                                                                                         | Yes       |                                     |
| Cryptographic algorithms: RSA, Diffie-Helman, ECC over GF(p)                                                          | Yes       |                                     |
| True random number generator (RNG)                                                                                    | Yes       |                                     |
| Sector protection against R/W operation (PCROP)                                                                       | Yes       |                                     |
| CRC calculation unit                                                                                                  | Yes       |                                     |
| Die information: 96-bit unique identifier                                                                             | Yes       |                                     |
| IEEE 64-bit unique identifier. Possibility to derive 802.15.4 64-bit and Bluetooth Low Energy 48-bit.                 | Yes       |                                     |

1. The internal AES is used to encrypt/decrypt Bluetooth Low Energy packets (LL). In parallel, the host running on Cortex M0+ may need to compute keys. In this case, it uses AES2, but it is possible to use an AES software available in the Bluetooth Low Energy host stack. This solution has been implemented on STM32WB1x devices, but not on STM32WB30 (where there is no AES available for Cortex M4). AES2/AES1 are available for Cortex M4, respectively, on STM32WB1x/STM32WB35.

The part number codification defined in the engineering bytes area at 0x1FFF 77DC address is associated to the part number as given in the table below.

**Table 16. Part number codification**

| Part number | Address byte |
|-------------|--------------|
| STM32WB10   | 0x0000 3031  |
| STM32WB15   | 0x0000 3531  |
| STM32WB30   | 0x0000 3033  |
| STM32WB35   | 0x0000 3533  |



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## 6 Tools

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The tools listed below are for all STM32WB10/15/30/35 devices and are backward compatible.

- STM32CubeMX
- STM32CubeProgrammer
- STM32CubeMonitor-RF

STM32CubeMX is recommended for the migration between STM32WB10/15/30/35 microcontrollers.

## Revision history

**Table 17. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                    |
|-------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12-May-2022 | 1        | Initial release.                                                                                                                                                                                                                                                                                                           |
| 02-Aug-2022 | 2        | Updated Table 11. STM32WB35 free memory space by density, without OTA, Table 12. STM32WB15/30/10 free memory space, without OTA, Table 13. Cortex M0+ code size, and footnote <sup>(1)</sup> of Table 14. Used memory (Kbytes).                                                                                            |
| 02-May-2023 | 3        | Updated document title and Section Introduction.<br>Added footnote to Table 3. Package information .<br>Updated Table 11. STM32WB35 free memory space by density, without OTA, Table 12. STM32WB15/30/10 free memory space, without OTA, Table 13. Cortex M0+ code size, Table 14. Used memory (Kbytes) and its footnotes. |

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