Application note

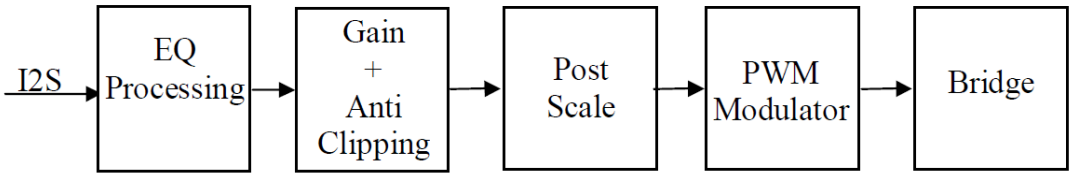
# Configurable output power rate using STA339BW

## Introduction

The aim of this application note is to illustrate a standard methodology describing how STA339BW features can be used in TV applications to control and guarantee the maximum output power level when different supply voltage SMPS can be selected.

# 1 Overview

The continuous cost reduction in the TV market requires simplifications and compromise in the application. In particular, the SMPS circuit must be reused as much as possible among different models. To allow this compromise, the amplifier must have the capability to control its maximum output power whatever the supply voltage. This means that 10 W models can be implemented with a 12 V power supply as far as an 18 V power supply. The STA339BW provides an anticlipping and a scaling factor feature suitable to allow this kind of control. The data flow is:




Using the Anti Clipping block, the output power is controlled with a limited amount of distortion giving a more "musical" sound, then with the post scale feature, the output power can be fine tuned to obtain the desired results.

# 2 Implementation

## 2.1 Specification

Digital amplifiers in TV products must follow these specifications:

- When the input level is -12 dBFs, the output signal must be undistorted and the output power must be X watts.
- When the input level is 0 dBFs, the output signal must be limited (eventually a minimum distortion is allowed) to (X * 1.5) watts.

## 2.2 Procedure

Once the $V_{cc}$ supply value is selected, three thresholds must be defined:

- P1: undistorted maximum power
- P10: 10% distortion maximum power
- P20: 20% distortion maximum power

P1 is the maximum undistorted power that can be delivered once $V_{cc}$ and Rload are fixed.

Equation 1

$$P1 = \frac{(Vcc \cdot 0.94)^2}{2 \cdot (Rload + 2 \cdot Rdson)^2} \cdot Rload$$

Note that the term Rdson should take in account also the parasitic series resistance of the output filter to get precise results.

P10 is defined as the maximum power delivered with 10% THD, and it is computed as 1.28*P1.

P20 is defined as the maximum power delivered with 20% THD, and it is computed as 1.58*P1.

Note that the 0.94 constant in the above formula depends on DDX ternary modulation, for binary modulation, the formula is similar but 0.88 must be used instead of 0.94.

Three different cases are analyzed here:

1. The desired amplifier max power when 0 dBFs input is less or equal to P1.
2. The desired amplifier max power when 0 dBFs input is greater than P1 but less or equal to P10.
3. The desired amplifier max power when 0 dBFs input is greater than P10 but less or equal to P20.

If the desired output power is greater than P20, it is not recommended (only for audio quality reasons) to use the selected $V_{cc}$ value, but a greater $V_{cc}$ value should be used.

# 3 Max power undistorted settings

## 3.1 Gain selection (AC0)

For gain selection we should respect two constraints, P(0 dBFs) and P(-12 dBFs), both undistorted, and P(-12 dBFs) * 1.5 = P(0 dBFs). To do that, gain must be selected to +10 dB; in this way the -12 dB input is boosted to -2 dB and there is an extra 2 dB margin to reach 0 dB output power (that is, around 1.5 times more power).

## 3.2 Anticlipping selection (AC0)

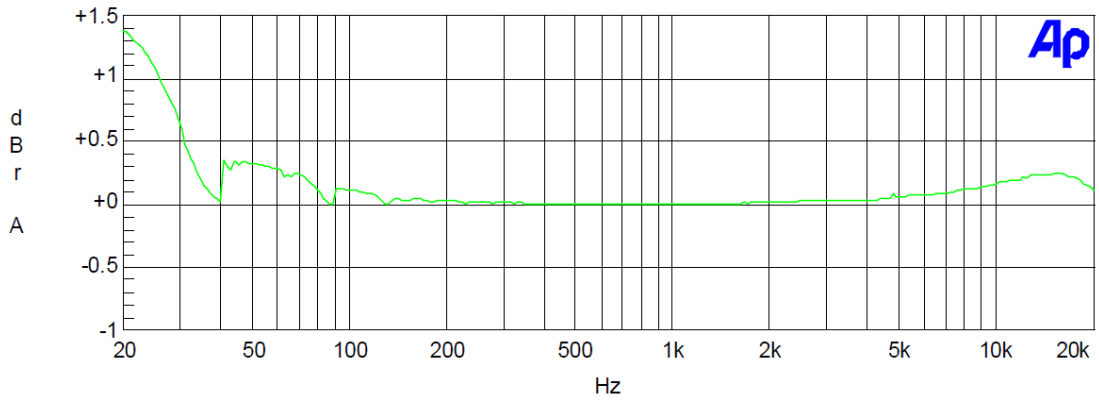
To limit the distortion due to the +10 dB gain selected above, the anticlipping/DRC feature of the STA339BW should be used.

The best settings for the max power undistorted case is:

- AC mode (reg. 0x03 bit 5 = '0')
- Gain +10 dB (reg. 0x08 = 0x4C)
- Select limiter 1 for both left and right channels (reg. 0x0E bit 5 and 4 = "01"; reg. 0x0F bit 5 and 4 = "01")
- A/R rates (reg. 0x12 = 0x2F)
  - Attack rate 2.2560
  - Release rate 0.0104
- A/R thresholds (reg. 0x13 =0x66)
  - Attack threshold 0 dB
  - Release threshold 0 dB
- Disable zero crossing (reg. 0x04 bit 6 = "0")

In Figure 1 the output level versus input frequency (0 dBFs sinus) is shown. It can be seen that the response is not completely flat. The high frequency 'ripple' is due to the output filter selection (choosing different R/L values results in a much flatter response), while the low frequencies 'ripple' is due to the DRC/AC settings. The response can be flattened at low frequencies decreasing the release rate, but as the release rate is lowered some hysteresis effects can arise. In Figure 2 the input level vs. output level graph is depicted. It is clear that starting from 10 dBFs input, the output is limited to 0 dB. Lowering the release rate (to -2 dB, for example) and keeping all the other settings unchanged results in the graph in Figure 3. Here the hysteresis is clearly visible. Rising or lowering the input level results in different output levels in the hysteresis window. The window amplitude is directly proportional to the release threshold setting. If some hysteresis can be tolerated by the application, the recommendation is to lower the release threshold as much as possible with respect to the above configuration (but not lower than -7 dB).

**Figure 1. Output level vs. input frequency (0 dBFs sinus).**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Green | Solid | 1 | Anlr.Level A | Left | |

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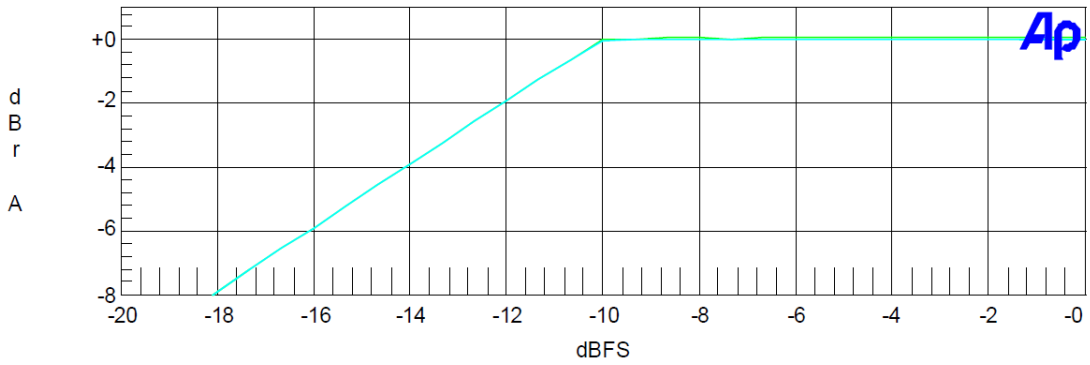
Figure 2. **AC0 Input level vs. output level.**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Green | Solid | 1 | Anlr.Level A | Left | |
| 2 | 1 | Cyan | Solid | 1 | Anlr.Level A | Left | |

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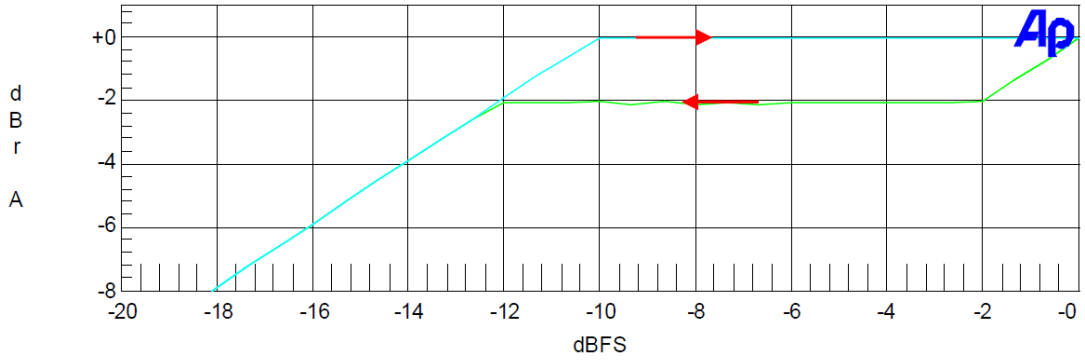
Figure 3. **Input level vs. output level (-2 dB release threshold), cyan curve is when the input level rises up, green curve is when the input level drops down.**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Green | Solid | 1 | Anlr.Level A | Left | |
| 2 | 1 | Cyan | Solid | 1 | Anlr.Level A | Left | |

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## 3.3 Post scale selection

The purpose of the post scale is to tune the output level to the desired power.

The max undistorted output power can be computed using Equation 1. This power level corresponds to the 0 dB output level described in the previous sections.

Using the post scale attenuation, it is possible to decrease the max power level to any value.

If Pmax is the maximum desired output level, the post scale attenuation should be set to:

$$A = round\left(\left(\sqrt{\frac{P\max}{P1}}\right)\cdot(2^{23}-1)\right)$$

# 4 Max power 10% THD

## 4.1 Gain selection (AC1)

For gain selection we should respect three constraints, -12 dBFs input undistorted, P(- 12 dBFs) * 1.5 = P (0 dBFs), and max power-out equal to P10. To do that, the gain must be selected to +11 dB.

## 4.2 Anticlipping selection (AC1)

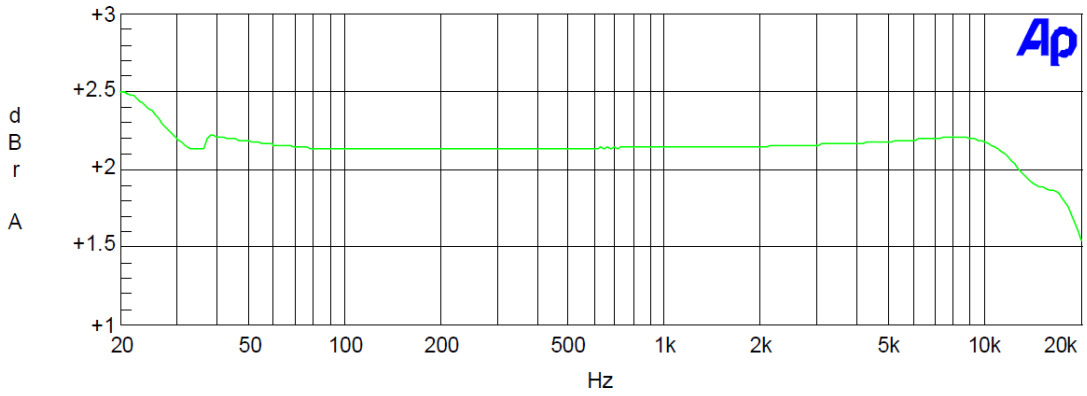
To limit the distortion due to the +11 dB gain selected above, the anticlipping/DRC feature of the STA339BW should be used.

The best settings for the max power 10% THD case is:

- AC mode (reg. 0x03 bit5 = '0')
- Gain +11 dB (reg. 0x08 = 0x4A)
- Select limiter 1 for both left and right channels (reg. 0x0E bit 5 and 4 = "01"; reg. 0x0F bit 5 and 4 = "01")
- A/R rates (reg. 0x12 = 0x2F)
  - Attack rate 2.2560
  - Release rate 0.0104
- A/R thresholds (reg. 0x13 =0x7F)
  - Attack threshold 2 dB
  - Release threshold 0 dB
- Disable zero crossing (reg. 0x04 bit 6 = '0')

In Figure 4 the output level versus input frequency (0 dBFs sinus) is shown. It can be seen that the response is not completely flat. The high frequency 'ripple' is due to the output filter selection and to the saturation of the PWM cycles, while the low frequencies 'ripple' is due to DRC/AC settings. In this case the response is flatter with respect to the AC0 settings, the response can be anyway flattened at low frequencies decreasing the release rate, but as the release rate is lowered some hysteresis effects can arise as for AC0 settings. In Figure 5 the input level vs. output level graph is depicted. It is clear that starting from -11 dBFs input the output start to be limited. Some hysteresis is present because it is impossible to completely avoid it when the attack threshold is greater than 0 dB, but in this case the relationship with the release threshold is no longer direct due to PWM saturation effects.

**Figure 4. Output level vs. input frequency (0 dBFs sinus).**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Green | Solid | 1 | Anlr.Level A | Left | |

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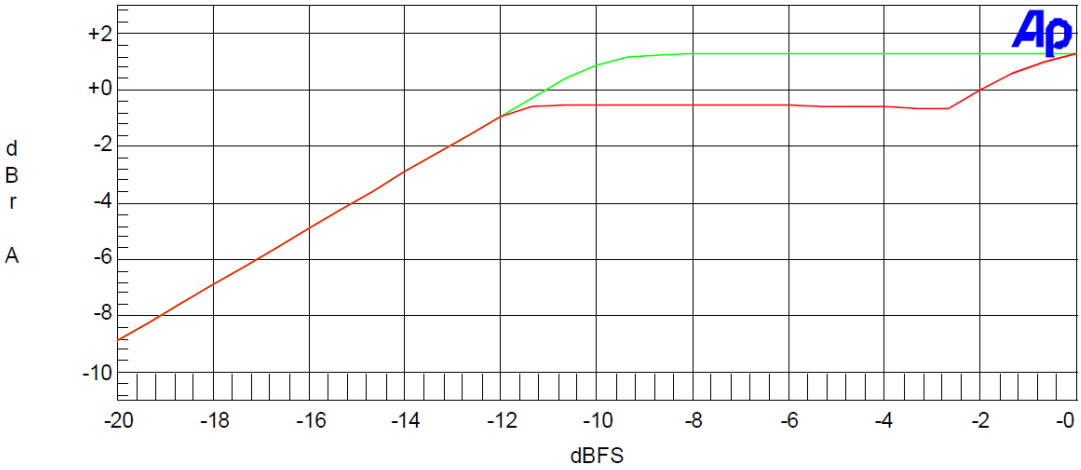
Figure 5. **Input level vs. output level.**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Green | Solid | 1 | Anlr.Level A | Left | |
| 2 | 1 | Red | Solid | 1 | Anlr.Level A | Left | |

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## 4.3 Post scale selection

The purpose of the post scale also in this case is to tune the output power level to the desired power.

Using the post scale attenuation it is possible to decrease the max power level to any value.

If Pmax is the maximum desired output level, the post scale attenuation should be set to:

$$A = round\left(\left(\sqrt{\frac{P\max}{P10 \cdot 1.05}}\right) \cdot (2^{23} - 1)\right)$$

The 1.05 corrective factor is inserted because the AC1 settings limit to 1.29 dB instead of exactly 1 dB as needed to get exactly P10.

Note that when the amplifier is working in saturation mode, the above formula should be tuned by hand to precisely tune the output power.

# 5 Max power 20% THD

## 5.1 Gain selection (AC2)

For gain selection we should respect three constraints, -12 dBFs input undistorted, P(- 12 dBFs) * 1.60 = P(0 dBFs), and max power-out equal to P20.

To do that, the gain must be selected to +12 dB, in this way the -12 dB input reaches the P1 level at the output, while 0 dBFs input reaches P20.

## 5.2 Anticlipping selection (AC2)

To limit the distortion due to the +12 dB gain selected above, the anticlipping/DRC feature of the STA339BW should be used.

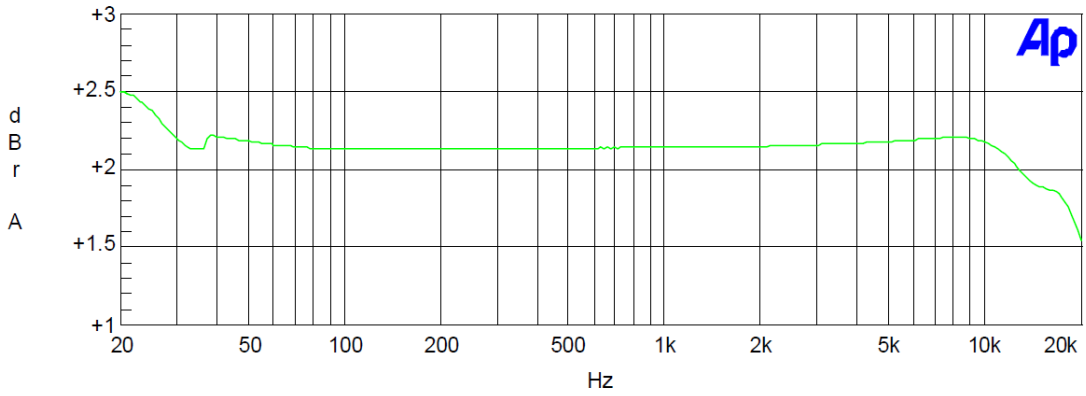
The best settings for the max power 20% THD case is:

- DRC mode (reg. 0x03 bit5 = '1')
- Gain +12 dB (reg. 0x08 = 0x48)
- Select limiter 1 for both left and right channels (reg. 0x0E bit 5 and 4 = "01"; reg. 0x0F bit 5 and 4 = "01")
- A/R rates (reg. 0x12 = 0x2F)
  - Attack rate 2.2560
  - Release rate 0.0104
- A/R thresholds (reg. 0x13 = 0xEE)
  - Attack threshold -7 dB
  - Release threshold -9 dB
- Disable zero crossing (reg. 0x04 bit 6 = '0')

Please note that to use DRC mode as anticlipping, the gain and volumes should not be changed from the above settings.

In Figure 6 the output level versus input frequency (0 dBFs sinus) is shown. It can be seen that the response is not completely flat. The high frequency 'ripple' is due to the output filter selection and to the saturation of the PWM cycles, while the low frequencies 'ripple' is due to DRC/AC settings. In this case the response is flatter with respect to the AC0 settings, the response can be anyway flattened at low frequencies decreasing the release rate, but as the release rate is lowered some hysteresis effects can arise as for AC0 settings. In Figure 7 the input level vs. output level graph is depicted. It is clear that starting from - 12 dBFs input, the output starts to be limited. Some small hysteresis is present, but in this case the relationship with the release threshold is no longer direct due to PWM saturation effects.

**Figure 6. Output level vs. input frequency (0 dBFs sinus).**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Green | Solid | 1 | Anlr.Level A | Left | |

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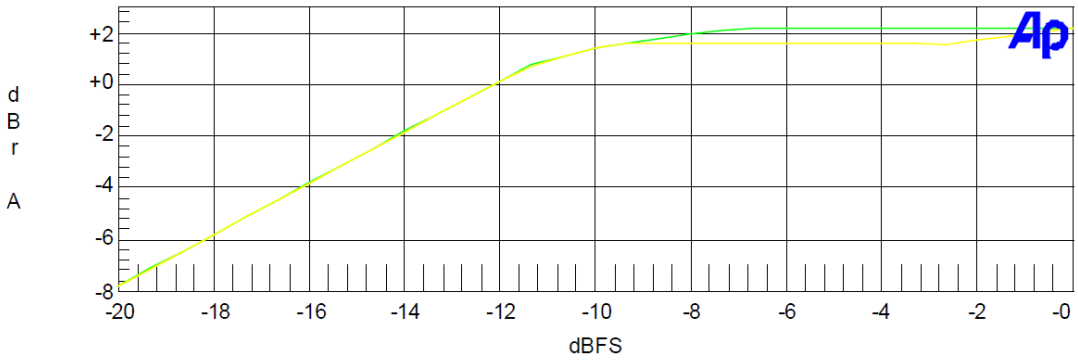
Figure 7. **Input level vs. output level.**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Green | Solid | 1 | Anlr.Level A | Left | |
| 2 | 1 | Yellow | Solid | 1 | Anlr.Level A | Left | |

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## 5.3 Post scale selection

The purpose of the post scale also in this case is to tune the output power level to the desired level.

Using the post scale attenuation it is possible to decrease the max power level to any value.

If Pmax is the maximum desired output level, the post scale attenuation should be set to:

$$A = round\left(\left(\sqrt{\frac{P\max}{P20}}\right)\cdot(2^{23}-1)\right)$$

Note that when the amplifier is working in saturation mode, the above formula should be tuned by hand to precisely tune the output power.

# 6 Example

All the following examples consider:

- Rdson = 0.2 mohm
- Parasitic resistance of the output filter = 0.18 ohm

Note that when using AC1 and AC2, a manual tuning of the post scale factor should be mandatory for a better power level control.

## 6.1 $V_{cc}$ = 9 V @ 8 ohm

If the desired power level when 0 dBFs input Pmax is < = 3.73W

- Set +10 dB gain
- Use AC0 settings for DRC/limiter
- Set post scale to

$$A = round\left(\left(\sqrt{\frac{P\max}{3.73}}\right)\cdot(2^{23}-1)\right)$$

If the desired power level when 0 dBFs input Pmax is > 3.73 W and < = 4.77 W

- Set +11 dB gain
- Use AC1 settings for DRC/limiter
- Set post scale to

$$A = round\left(\left(\sqrt{\frac{P\max}{4.77}}\right)\cdot(2^{23}-1)\right)$$

If the desired power level when 0 dBFs input Pmax is > 4.77W and < = 5.89 W

- Set +12 dB gain
- Use AC2 settings for DRC/limiter
- Set post scale to

$$A = round\left(\left(\sqrt{\frac{P\max}{5.89}}\right)\cdot(2^{23}-1)\right)$$

Max power greater than 5.89 W with 9 V supply has a distortion that is too high.

## 6.2 $V_{cc}$ = 12 V @ 8 ohm

If the desired power level when 0 dBFs input Pmax is < = 6.63 W

- Set +10 dB gain
- Use AC0 settings for DRC/limiter
- Set post scale to

$$A = round\left(\left(\sqrt{\frac{P\max}{6.63}}\right)\cdot(2^{23}-1)\right)$$

If the desired power level when 0 dBFs input Pmax is > 6.63 W and < = 8.49 W

- Set +11 dB gain
- Use AC1 settings for DRC/limiter
- Set post scale to

$$A = round\left(\left(\sqrt{\frac{P\max}{9.7}}\right)\cdot(2^{23}-1)\right)$$

If the desired power level when 0 dBFs input Pmax is > 8.49 W and < =10.47 W

- Set +12 dB gain
- Use AC2 settings for DRC/limiter
- Set post scale to

$$A = round\left(\left(\sqrt{\frac{P\max}{11.85}}\right)\cdot(2^{23}-1)\right)$$

Max power greater than 10.47 W with 12 V supply has a distortion that is too high.

## 6.3 $V_{cc}$ = 14 V @ 8 ohm

If the desired power level when 0 dBFs input Pmax is < = 8.92 W

- Set +10 dB gain
- Use AC0 settigns for DRC/limiter
- Set post scale to

$$A = round\left(\left(\sqrt{\frac{P\max}{8.92}}\right)\cdot(2^{23}-1)\right)$$

If the desired power level when 0 dBFs input Pmax is > 8.92 W and < = 11.42 W

- Set +11 dB gain
- Use AC1 settings for DRC/limiter
- Set post scale to

$$A = round\left(\left(\sqrt{\frac{P\max}{11.42}}\right)\cdot(2^{23}-1)\right)$$

If the desired power level when 0 dBFs input Pmax is > 11.42 W and < = 14.09 W

- Set +12 dB gain
- Use AC2 settings for DRC/limiter
- Set post scale to

$$A = round\left(\left(\sqrt{\frac{P\max}{14.09}}\right)\cdot(2^{23}-1)\right)$$

Max power greater than 14.09 W with 14 V supply has a distortion that is too high.

## 6.4 $V_{cc}$ = 18 V @ 8 ohm

If the desired power level when 0 dBFs input Pmax is < = 14.73 W

- Set +10 dB gain
- Use AC0 settings for DRC/limiter
- Set post scale to

$$A = round\left(\left(\sqrt{\frac{P\max}{14.73}}\right)\cdot(2^{23}-1)\right)$$

If the desired power level when 0 dBFs input Pmax is > 14.73 W and < = 18.85 W

- Set +11 dB gain
- Use AC1 settings for DRC/limiter
- Set post scale to

$$A = round\left(\left(\sqrt{\frac{P\max}{18.85}}\right)\cdot(2^{23}-1)\right)$$

If the desired power level when 0 dBFs input Pmax is > 18.85 W and < = 23.27 W

- Set +12 dB gain
- Use AC2 settings for DRC/limiter
- Set post scale to

$$A = round\left(\left(\sqrt{\frac{P\max}{23.27}}\right)\cdot(2^{23}-1)\right)$$

Max power greater than 23.27 W with 18 V supply has a distortion that is too high.

# Revision history

Table 1. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 22-Jun-2022 | 1 | Initial release. |

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