# High voltage Hot Swap, Soft Start and Oring

## Introduction

STPM801 is a controller which operates in conjunction with external back-to-back connected N-channel power MOSFETs, realizing a connection between the input voltage supply line, and the output supply line. The main advantage of integrating STPM801 in the application is the availability of a voltage supply, on OUT, protected against high voltage transients and all the disturbances that are typically present on the supply lines. The product can be used either for 12 V or 24 V supply rails.

STPM801 acts as a pre-driver of two N-channel transistors, respectively, the Hot Swap and the Oring MOSFETs. The first is used as a normal power switch. The Oring MOSFET is mainly used as ideal diode, but it also helps blocking the current conduction in case of reverse battery detection (OUT > VB).

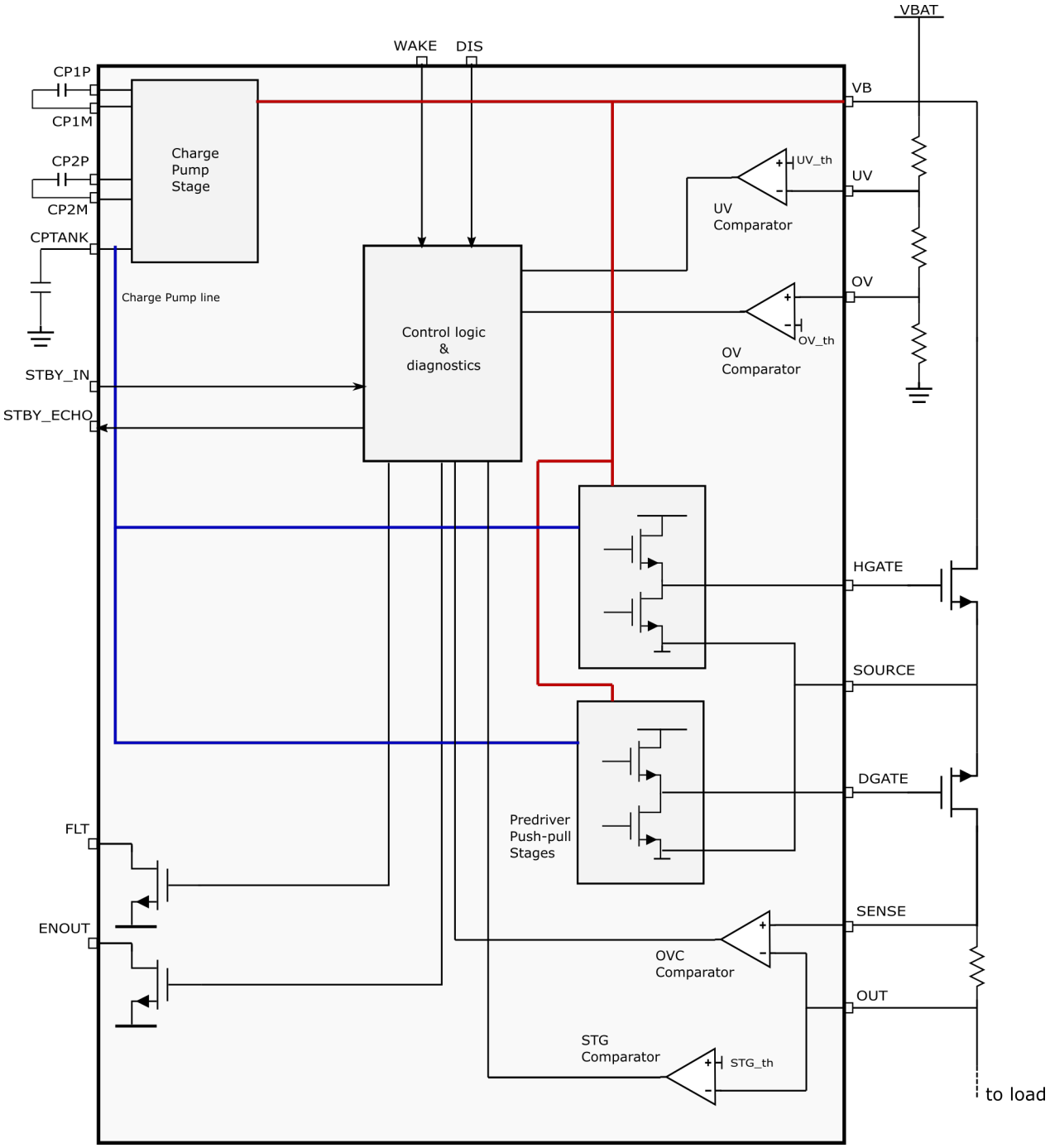
STPM801 can detect faulty conditions. In case of faults that can compromise the integrity of external components or the device itself, STPM801 reacts with a transition to the Safe State, switching OFF the pre-drivers.

A Stand-By mode is also available, with the device operating at reduced functionality, but allowing a reduction on power dissipation.

# 1 Block diagram and pin description

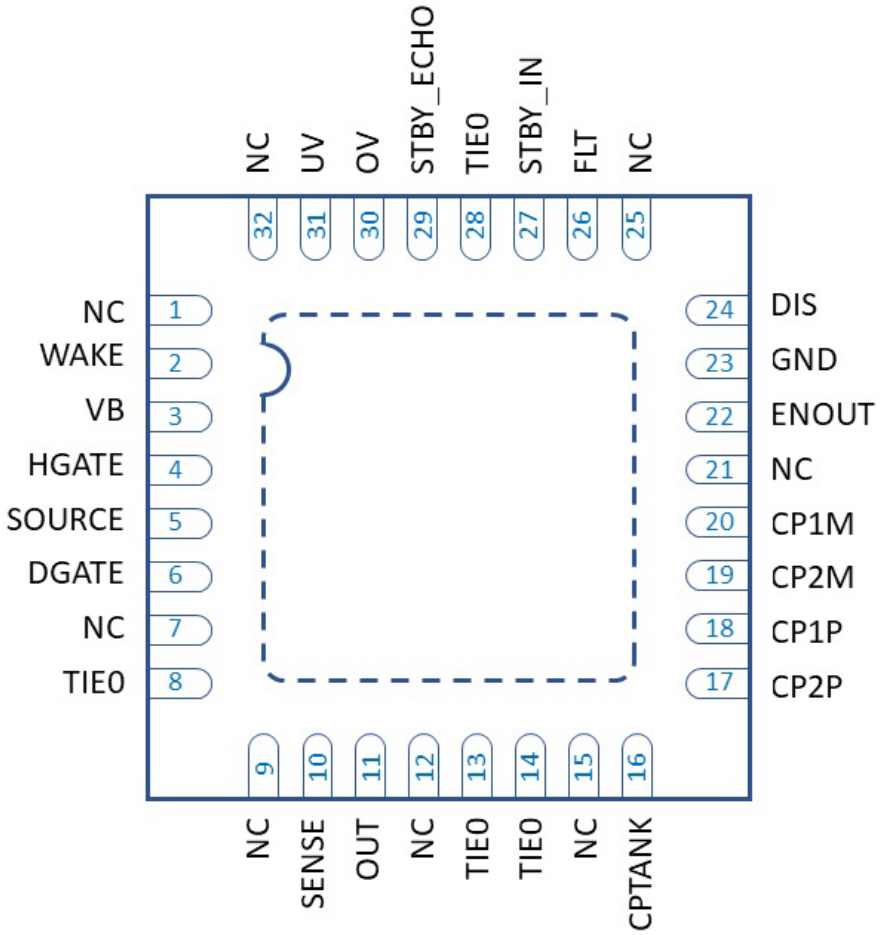
## 1.1 Block diagram

Figure 1. **Simplified Block diagram**



## 1.2 Pin description

Figure 2. **VFQFN32 package pin out (top view)**




*Note: Exposed pad not electrically connected to the internal substrate.*

*STPM801 VFQFN32 package is equipped with corner pins, which are electrically floating; it is in any case recommended to solder them towards GND in order to guarantee mechanical robustness.*

**Table 1. Pin functions and description**

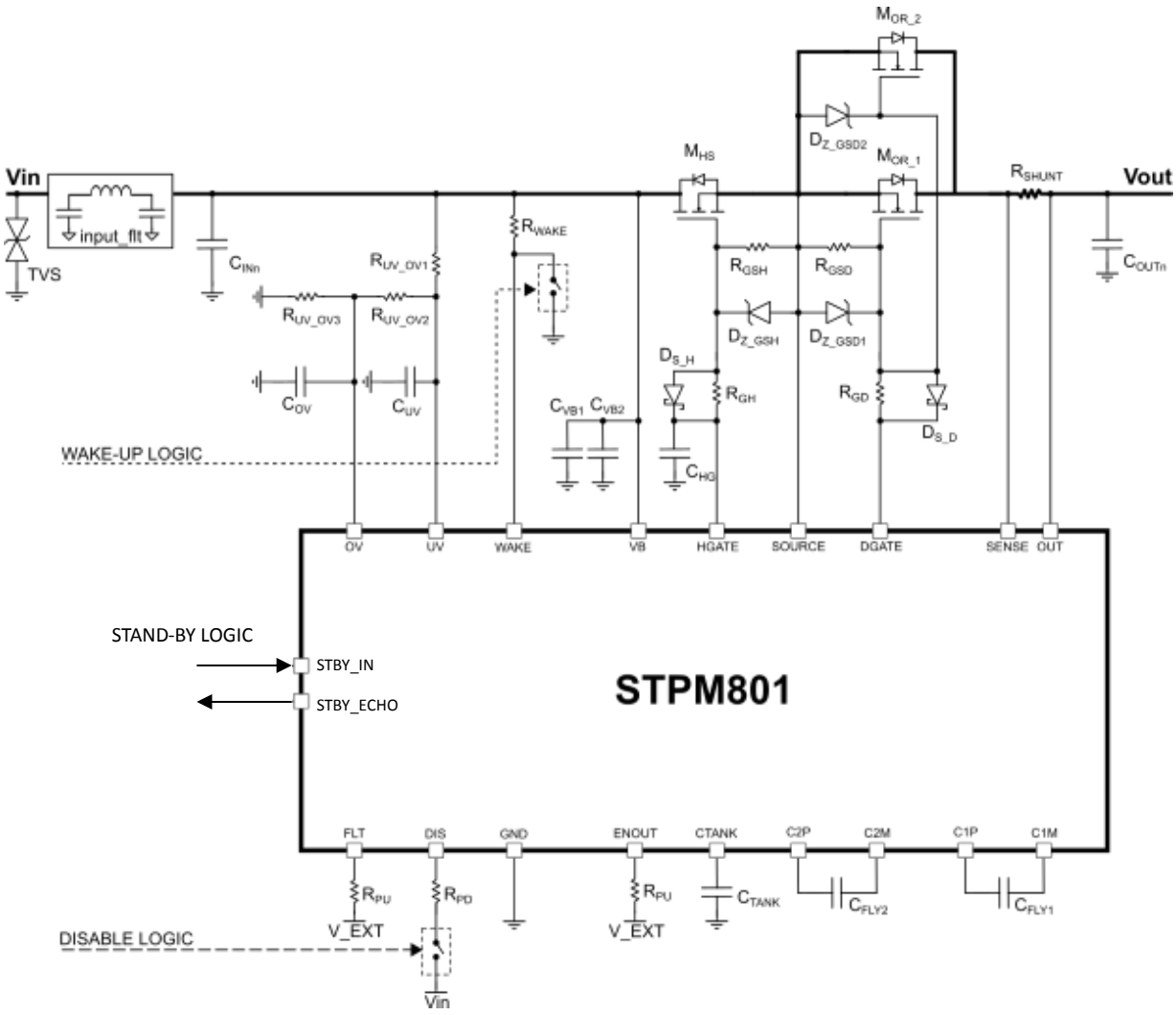
| No. | Name | Type | Description |
|---|---|---|---|
| 1 | NC | - | Connect directly to GND |
| 2 | WAKE | I | Shutdown control |
| 3 | VB | SUPPLY | Input voltage |
| 4 | HGATE | I/O | Gate drive output of Hot Swap MOS |
| 5 | SOURCE | I/O | Common Source Input and Gate Drive Return |
| 6 | DGATE | I/O | Diode controller gate drive output enabling Oring function |
| 7 | NC | - | Connect directly to GND |
| 8 | TIE0 | - | Connect directly to GND |
| 9 | NC | - | Connect directly to GND |
| 10 | SENSE | I | External resistor current sense |
| 11 | OUT | I | External MOS drain voltage sense |
| 12 | NC | - | Connect directly to GND |
| 13 | TIE0 | - | Connect directly to GND |
| 14 | TIE0 | - | Connect directly to GND |
| 15 | NC | - | Connect directly to GND |
| 16 | CPTANK | O | Charge pump output. Connect a capacitor to ground. Typical value 220 nF. |
| 17 | CP2P | I/O | Charge pump pin for capacitor 2, positive side |
| 18 | CP1P | I/O | Charge pump pin for capacitor 1, positive side |
| 19 | CP2M | I/O | Charge pump pin for capacitor 2, negative side |
| 20 | CP1M | I/O | Charge pump pin for capacitor 1, negative side |
| 21 | NC | - | Connect directly to GND |
| 22 | ENOUT | O | Output enable when external MOS are fully on. Internal Pulldown works as Open Drain Output and External resistor pulls up the output. Typical 4.7 kW for 5 V IO line. |
| 23 | GND | Ground | Ground |
| 24 | DIS | I | Disable |
| 25 | NC | - | Connect directly to GND |
| 26 | FLT | O | FLT output signal when a fault is present. Internal Pulldown works as Open Drain Output and External resistor pulls up the output. Typical 4.7 kW for 5 V IO line. |
| 27 | STBY_IN | I | Connect directly to GND if Stand-By mode is not used or drive it according to Stand-By chapter |
| 28 | TIE0 | - | Connect directly to GND |
| 29 | STBY_ECHO | O | Connect directly to GND if Stand-By mode is not used or read it according to Stand-By chapter |
| 30 | OV | I | Input overvoltage protection. Overvoltage comparator Input. |
| 31 | UV | I | Input undervoltage protection. Undervoltage comparator Input. |
| 32 | NC | - | Connect directly to GND |

**Legenda**: I = Input, O = Output, P = Power Supply, G = Ground, I/O = Input/Output

# 2 Applications overview

Figure 3 shows the typical application schematic for STPM801. In the next chapters a detailed explanation about the choice criteria for the external components is presented.

**Figure 3. Typical application schematic**

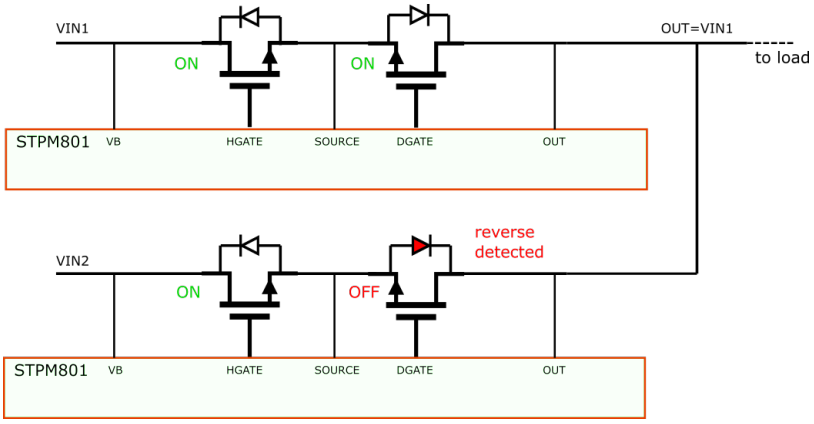



The most interesting way to use STPM801, is, however, when two supply lines are present. In this case two parts of STPM801 are required. This could be the case, for example, when it is important to guarantee the continuity of the supply, and an auxiliary supply line is therefore introduced, allowing to replace the main line when it is out of order (undervoltage issue or any other malfunction).

Figure 4 shows the principle of operation of a double supply line. The resulting voltage on the output line is the OR between the two input lines. The higher voltage propagates from VIN to VOUT; the lower is blocked since a reverse condition is detected on that line (being VOUT > VIN), and Oring driver is switched OFF. The intrinsic diode of the Oring is reverse biased and blocks the current back feeding from VOUT to VIN.

**Figure 4. OR condition between two supply lines**

VIN1 > VIN2



# 3 STPM801 functions

## 3.1 Main function

STPM801 takes, as input, a voltage supply line that is also its supply voltage (VB) and makes it available on OUT. The electrical connection between VB and OUT is realized through two pre-drivers:

- The Hot Swap: it is a usual power switch, driven with the highest possible value of Vgs, in order to have the lowest Rds_on;
- The Oring: it is used as ideal diode. Its driving voltage Vgs is regulated for having typically 30 mV of voltage drop across drain-to-source. In case of reverse condition (OUT > VB), it is switched OFF by internal diagnostic and, through its intrinsic diode, it prevents the current back-feeding toward battery (see also Figure 4).

In case of fault detection, STPM801 reacts realizing the transition to the Safe State, meaning that:

- The pre-drivers are turned off, and the electrical connection between VB and OUT is interrupted.
- FLT and ENOUT outputs are driven low, in order to communicate to external MCU that a faulty condition is present.

## 3.2 Diagnostics

In Table 2, all the faulty conditions are listed, with the associated filter times, the consequent state of the pre-drivers, and the re-engagement procedures.

The Short-to-GND fault is the only case when the reaction is FLT output asserted low only, without switching-OFF the pre-drivers. However, as explained in the product datasheet, if the Short-to-GND is also associated with an Overcurrent condition, the pre-drivers are switched OFF, with dedicated thresholds and filter times.

**Table 2. Fault table**

| Event | Filter time | HGATE | DGATE | FLT | Latched | Action for coming back to operating | Scenario |
|---|---|---|---|---|---|---|---|
| OV | 10 µs | Low | Low | Active | Not | OV disappear and no other faults present | Input overvoltage starting from device ON condition |
| UV | 100 µs | Low | Low | Active | Not | UV disappear | Input undervoltage starting from device ON condition |
| HOTSWAP VDS detection | 1 ms | Low | Low | Active | Yes | Toggling WAKE | After softstart finish, M1 is open |
| ORING VDS detection | 1 ms | Low | Low | Active | Yes | Toggling WAKE | M2 VDS short |
| Overcurrent | 1/100 µs | Low | Low | Active | Latched after 32 retries | Toggling WAKE | Output overcurrent |
| STG | 10us | No effect | No effect | Active | Not | N.A. | Output short to a lower fixed voltage level |
| VB < VOUT | 10 µs | High (VDS masked) | Low (VDS masked) | Not Active | Not | Reverse battery condition VB < VOUT disappear | Reverse current VBAT < Vout |
| CP_UV | 10 µs | Low | Low | Active | Not | If CP_UV disappears | UV on charge pump - VGS on MOSFETs cannot be guaranteed |
| OT | 10 µs | Low | Low | Active | Not | If OT disappears | Over-temperature detected |
| DIS | 3 µs Max | Low | Low | Active | Not | If DIS is not active | DIS pin is not asserted |

| Event | Filter time | HGATE | DGATE | FLT | Latched | Action for coming back to operating | Scenario |
|---|---|---|---|---|---|---|---|
| SAFETY_FAULT | 100 µs fault detection | Low | Low | Active | Yes | Toggling WAKE | Selftest fail or Clock monitor error or OTP CRC fail |

Recommendations:

- UV and OV input pins must not be left open, otherwise it is possible to observe instabilities on the output (oscillating signals on FLT and OUT).
- The resistors of the voltage divider connected to UV, OV pins have to be chosen considering the proper voltage levels to be used as thresholds for the under-voltage or over-voltage conditions. These values are, of course, different if a 12 V system or 5 V system is used.
- If the user is not interested in using OV or UV detection, OV must be tied to GND, and UV must be connected to 5 V line.

# 4 External components

## 4.1 Voltage divider on UV/OV pins

The set of $R_{UV\_OV1}$, $R_{UV\_OV2}$, $R_{UV\_OV3}$ values must be chosen in the range of kW, to minimize the static power dissipation. On the other hand, it is recommended that the current through them is higher than the leakage current values of UV and OV pin. As a rule, we can assume as acceptable a current 100 times higher than the leakage through UV and OV pin (which is in the order of a few µA).

Equations below must be considered to correctly size these resistors. VB_OV and VB_UV are, respectively, the over-voltage and the under-voltage limits allowed for the battery. These values depend mainly on the system in use (12 V or 24 V). OV_th and UV_th are the comparators detection thresholds (1.2 V for the over-voltage comparator, 1 V for the under-voltage comparator).

$$\frac{VB_{OV}}{R_{uvov1} + R_{uvov2} + R_{uvov3}} > \frac{OV_{th}}{R_{uvov3}} \quad (1)$$

$$\frac{VB_{UV}}{R_{uvov1} + R_{uvov2} + R_{uvov3}} < \frac{UV_{th}}{R_{uvov2} + R_{uvov3}} \quad (2)$$

$$\frac{VB}{(R_{uvov1} + R_{uvov2} + R_{uvov3})} > I_{leakage} \quad (3)$$

## 4.2 Charge pump capacitors

STPM801 has a charge pump to drive properly both the pre-drivers. It assures a proper operation of the device also in crank scenario with minimum battery voltage (4 V).

External capacitors must be connected to the device (see Figure 1 and Figure 3). For a proper operation fly capacitors shall be 100 nF, and tank output capacitor 220 nF, with a tolerance of 20%.

## 4.3 External MOSFETs

### 4.3.1 Hot Swap

The external MOSFET realizing the Hot Swap function, must be chosen considering these main parameters:

- Maximum continuous drain current $I_D$. This value shall exceed the maximum continuous load current of the application.
- Maximum drain to source voltage $V_{DS}$. It shall be high enough to withstand the highest differential voltage in the application.
- Maximum gate to source voltage $V_{GS}$. It shall be higher than the maximum $V_{GS}$ that STPM801 can drive for HGATE. Anyway, Zener diodes between Gate and Source can be added, to clamp $V_{GS}$ to safe levels (see also dedicated Section 4.6 Diodes connected to external MOSFETs).
- Drain to source On resistance $R_{ds\_ON}$. It is recommended a value as low as possible, to reduce the MOSFET conduction losses.

In case of high current loads the user can also put in parallel *n* MOSFETs in order to increase by a factor *n* the total available current. On the other hand, a slowing on the transient timings for turning on or off the Hot Swap stage shall be considered, since the total load capacitor to be charged, or discharged, is also increased.

The total input capacitance of MOSFETs connected to HGATE $C_{iss}$ is a key parameter for the evaluation of transient timings, and in particular during the soft-start (see Section 4.4 Soft Start capacitor).

### 4.3.2 Oring

Some requirements in the previous paragraph, about Hot Swap, can be extended also for Oring (maximum $I_D$, maximum $V_{DS}$ and $V_{GS}$). In particular, the conditions when $V_{DS}$ across Oring FETs could be particularly high are in reverse condition (when STPM801 diagnostics switches them off), or after any battery line switch OFF, with OUT remaining long time charged due to the slow transient discharge of output capacitors.

Anyway, there are some important differences, considering that Oring FETs are not used as traditional switches but as ideal diodes. For this reason:

- VGS driving voltage between DGATE and SOURCE is not the highest possible value but it is regulated in order to have typically 30 mV across drain and source;
- Consequently $R_{ds\_ON}$ is not as low as in the case of Hot Swap;
- The power dissipation also increases. Just as an example, with a load current of 10A, the power dissipation is 30 mV*10 A = 300 mW. Considering that the overcurrent limit is typically higher than 10 A, we conclude that a single Oring FETs can dissipate more than 1 W with currents below the OVC threshold.

Just for limiting the power dissipation, the connection of at least two Oring FETs in parallel is strongly recommended (as shown in Figure 3). User can choose the proper number depending on the kind of application and the expected levels of load currents.

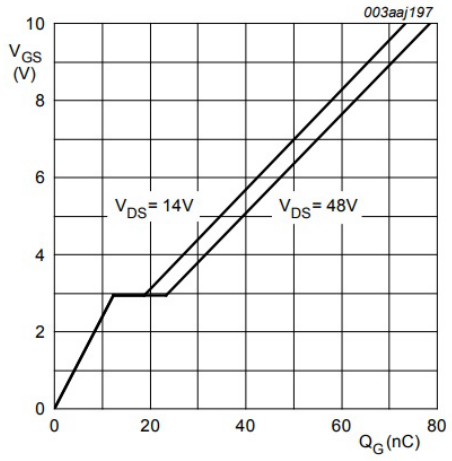
The Oring MOSFET is also expected to be very fast during the transients of switching ON and OFF. This is for example the case of recovery from reverse condition, or a switching OFF as reaction to a fault.

For this reason, a key parameter is the $Q_g$ (total gate charge) which is recommended to be as low as possible.

As example, an estimation of the turn ON timing, considering the MOSFET whose gate-charge characteristic is reported in Figure 5, is presented.

According also to product datasheet, with $Q_g$ = 40 nC, Vgs = 5 V, Vds = 48 V and $I_D$ = 25 A. For the case of Oring, where Vgs is not too high, a lower value of the gate charge can be considered (for example 30 nC, corresponding to Vgs = 3,7 V); with these values the MOSFET is, in any cases, turned on, and there is still a good margin, considering that Vds is for sure lower than 48 V.

**Figure 5. Gate-charge characteristics of a MOSFETs**




Assuming the worst case of pull-up current of 45 mA (at hot temperature, minimum battery voltage), the estimated timing (for 2 Oring in parallel) is:

$$t = \frac{2*Q_g}{Oring\_IDGATE(UP)\_VBmin} = \frac{(2*30)nC}{45\ mA} = 1{,}33\ \mu s \quad (4)$$

This example shows that a proper choice of Oring MOSFETs is done using devices reaching the full-on condition with $Q_g$ in the order of 40-50 nC; transient timings of about 1 µs can be obtained.

## 4.4 Soft Start capacitor

During the power-up of many applications it is important to limit the inrush current. For this reason, STPM801 is equipped with a Soft Start turning on. The principle of operation is the charge of a capacitor with a constant current value $I_{HG}$ coming from the charge pump (typical value 37 µA). Considering the total input capacitor $C_{iss}$ of the external MOSFET and another capacitor $C_{HG}$, added on HGATE, the Soft Start timing can be estimated by the equation below.

$$Timing\ soft\ start = \frac{C_{iss} + C_{HG}}{I_{HG}} \quad (5)$$

User can, in this way, program the soft-start timing by a proper choice of the external capacitor $C_{HG}$.

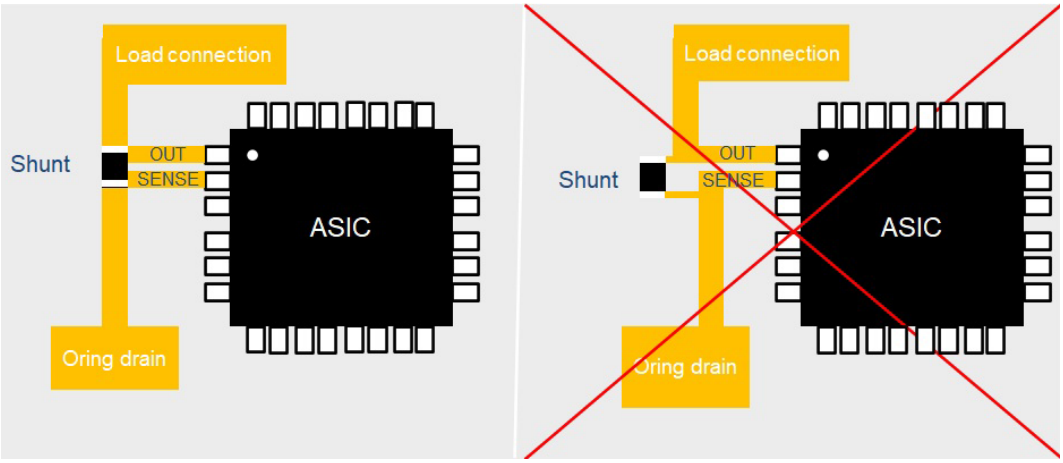
## 4.5 Sensing resistor

Overcurrent diagnostic is done by a shunt resistance, connected between SENSE and OUT. The overcurrent comparator inside STPM801 senses the voltage drop across this shunt resistor. Considering that the overcurrent threshold is typically 50 mV, the shunt resistor shall be sized considering the typical values of load current in the application (for example with 1 mΩ of shunt resistor the overcurrent fault is triggered with 50 A).

The connections between shunt resistance and the two pins of the device must be similar and as short as possible. The upper limit of these two connections is 100 µΩ (only PCB metal).

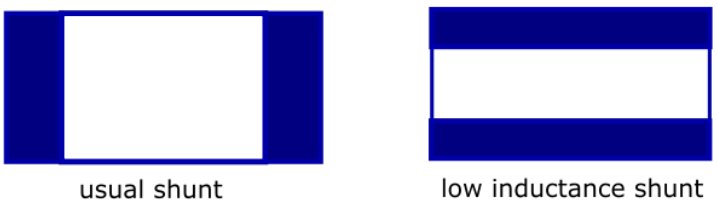
Figure 6 shows examples of good and bad connections of shunt resistor to the device.

**Figure 6. Rules for shunt connections**




Another suggestion is the utilization of low inductance shunts, as shown in Figure 7. In these shunts the contribution from parasitic inductances is lower because the distance between the contacts is reduced with respect to a normally used shunt.

**Figure 7. Usual and low inductance shunt**



## 4.6 Diodes connected to external MOSFETs

As shown in Figure 3 some helpful external diodes are connected to both FETs of Hot Swap and Oring.

### 4.6.1 Zener diodes

Zener diodes are connected between HGATE (or DGATE) and SOURCE pins, allowing to realize a clamp on the VGS voltage for both FETSs.

Even if STPM801 is designed with an internal pull-up structure, able to clamp the VGS voltage at specified values, the external Zener diodes help to protect the FETs in case of fast transients. Their connection is strongly recommended since the internal structure cannot guarantee a fast reaction.

### 4.6.2 Schottky diodes

As shown in Figure 3 two Schottky diodes are connected in parallel to gate resistors on both external FETs. When the external gates are driven on these diodes they are reverse biased; they enter in conduction during the transient of FETs switching off.

The connection of these diodes is not mandatory but it is recommended because they help to speed up the gate discharge transient, taking advantage of their reduced forward voltage (in the order of 200 - 300 mV).

## 4.7 Pull-up resistors for digital outputs

Both digital outputs (FLT and ENOUT) are realized as open drain. In case of anomalous conditions (fault detection, full ON condition not reached) these outputs are driven low, otherwise they are in high impedance.

Pull-up resistor shall be connected between FLT (or ENOUT) and a 5 V external supply line, for forcing high voltage level in case of no-faults.

Recommended values for these pull-up resistors are in the order of kΩ.

# Revision history

Table 3. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 14-Jun-2022 | 1 | Initial release. |
| 14-Mar-2023 | 2 | Confidentiality level changed from ST Restricted to ST Public. |

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