
Using VD55G0 with an STM32 MCU

Introduction

When using VD55G0 with an STM32 MCU, a MIPID02 and specific sensor firmware patch (23.7) must be used.

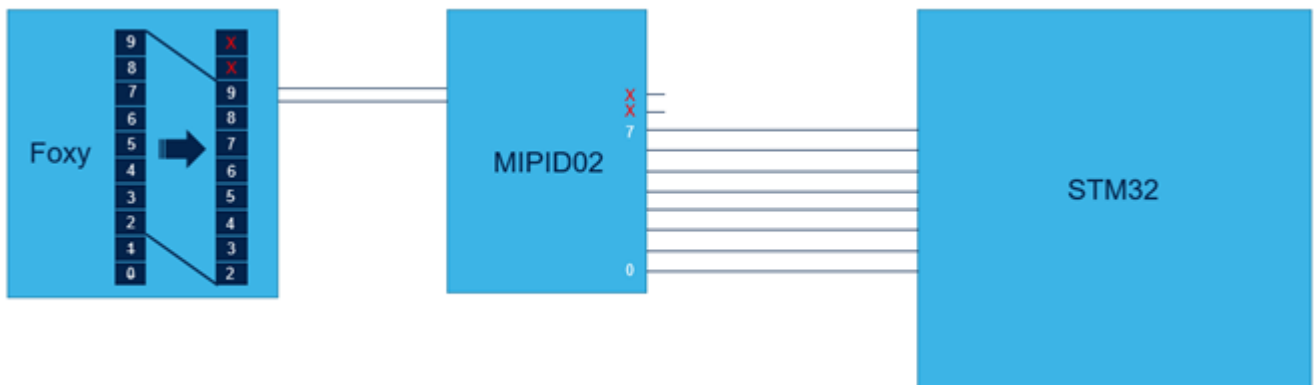
1 Firmware patch impacts

STM32 DCMI max frequency (pixel clock on a parallel interface) is 80 MHz. This means the CSI data speed must be lower than $8 \times 80 \text{ MHz} = 640 \text{ MHz}$. VD55G0 minimum data rate is 750 Mbps.

To reduce the pixel clock on a parallel bus after a MIPID02 deserialization, the firmware patch 23.7 configures the sensor to output 8-bit pixels on RAW10 format.

Default 10-bit data is digitally divided by 4, then clipped to 255 value.

Figure 1. title



With MIPID02 waiting for 10 bits, the frequency on parallel links is $750/10 = 75 \text{ MHz}$.

Note: Status lines are coded on 8-bits and are not available for STM32 with this system. It is too fast if decoded or scrambled if decoded as RAW10.

Other settings are automatically applied with the patch 23.7:

- CLK_PLL_MIPI register
 - Address: 0x224
 - Bits: (31:0)
 - Default value: 750000000
- LINE_LENGTH register
 - Address: 0x300
 - Bits: (15:0)
 - Default value: 1800
- DARKCAL_PEDESTAL register
 - Address: 0x416
 - Bits: (7:0)
 - Default value: 16

2 Exposure mode

The default values are as follows:

- `FOXY_sensorUi.SENSOR_SETTINGS.CLK_PLL_MIPI.bits.VALUE = 750000000;`
- `FOXY_sensorUi.STREAM_STATICS.LINE_LENGTH.reg= 1800;`
- `FOXY_sensorUi.STREAM_STATICS.OIF_CSI_BITRATE.bits.BIT_RATE = 750;`
- `FOXY_sensorUi.STREAM_DYNAMICS.DARKCAL_PEDESTAL.reg=0x10;`

Correcting computation of noiseGenMask with dgainInteger divider

DARKCAL

- `clipperLimit = 255, // Clip to 8 bit by default`
- `clipperThreshold = 255, // Clip to 8 bit by default`

Dividing dgain by 4

To update stats computation, multiply it by 4 so as to compensate dividing Dgain by 4.

Revision history

Table 1. Document revision history

Date	Version	Changes
14-Jun-2022	1	Initial release

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