EVLVIPGAN50FL: 15 V/50 W isolated flyback with VIPERGAN50

Introduction

This document describes the EVLVIPGAN50FL, a 15 V/50 W SMPS in wide input voltage range (90 V_{AC} – 265 V_{AC}), set in isolated quasi-resonant (QR) flyback topology with secondary side regulation (SSR) and with the following characteristics:

- 4-point average active mode efficiency at full load: > 90% (compliant with European CoC ver. 5)
- Input power consumption in no load condition: < 85 mW (@ 230 V_{AC})
- Compliant with IEC55022 Class B conducted EMI, even with reduced EMI filter
- RoHS compliant

The evaluation board has been developed using VIPERGAN50, a new advanced offline switcher by STMicroelectronics, having the following features:

- 650 V PowerGaN with embedded senseFET (Si) and HV startup;
- QR operation with dynamic blanking time and adjustable valley synchronization delay functions, to maximize efficiency at any input line and load condition;
- Valley-lock to ensure constant valley-skipping;
- Input voltage feedforward compensation for mains-independent OPP intervention;
- Adaptive burst mode for advanced power management in light load conditions;
- Frequency jittering for EMI suppression.

Enhanced system reliability is ensured by the built-in soft-start function and by the following set of protections:

- Input OVP (settable);
- Brown-in and brown-out (settable);
- Output OVP (settable);
- Output overload;
- OCP LEB;
- Embedded thermal shutdown.

Figure 1. **EVLVIPGAN50FL evaluation board top**

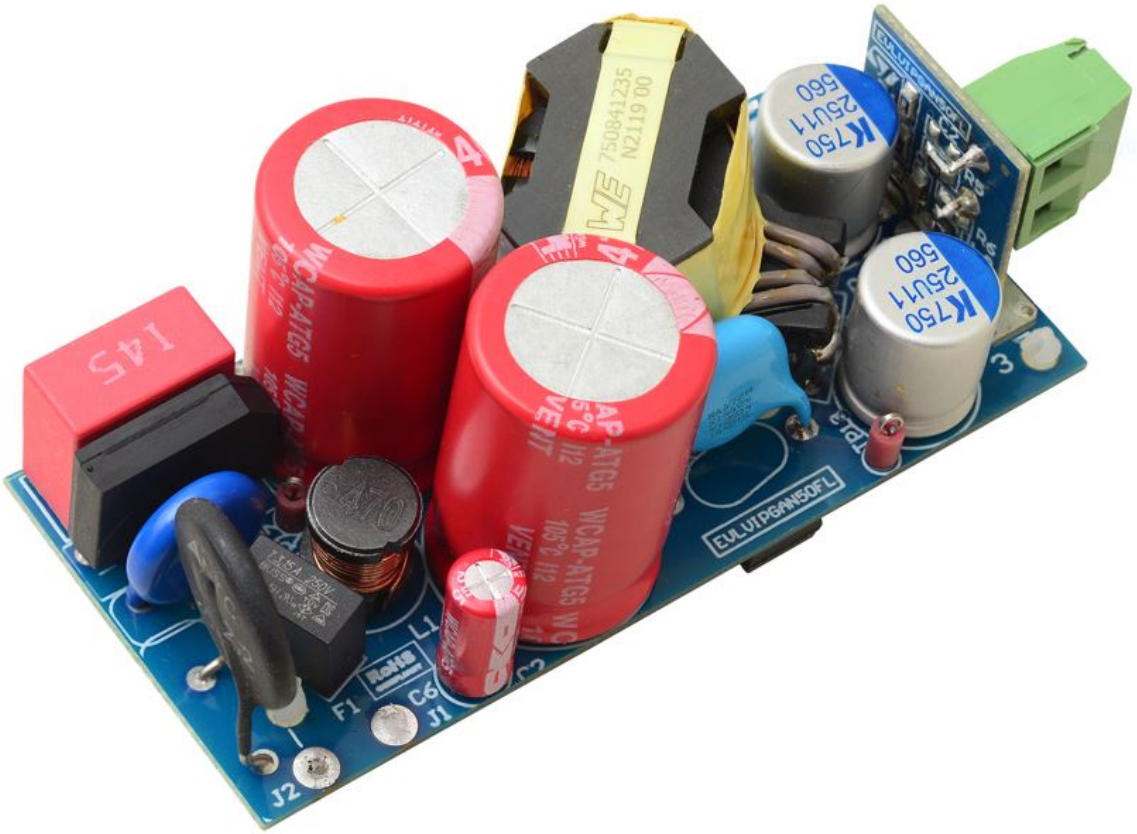
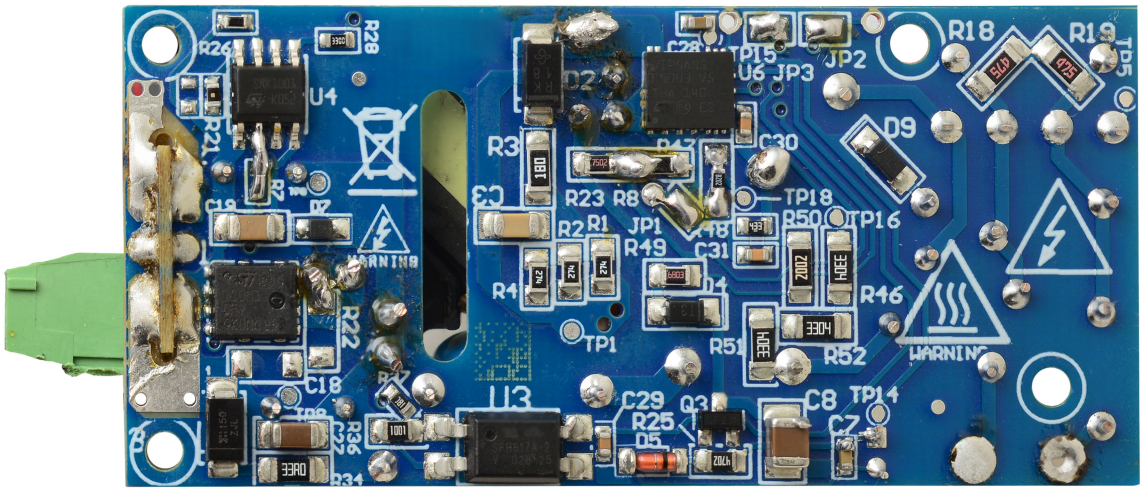


Figure 2. **EVLVIPGAN50FL evaluation board bottom**



1 Adapter features

The electrical specifications of the evaluation board are listed in Table 1.

Table 1. EVLVIPGAN50FL electrical specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	[90 V_{AC} - 265 V_{AC}]
Output voltage	V_{OUT}	15 V_{DC}
Max output current	I_{OUT}	3.33 A
Max output power	P_{OUT}	50 W
Precision of output regulation	Δ_{VOUT}	±5%
High frequency output voltage ripple	Δ_{VOUT}	50 mV
Max. ambient operating temperature	T_{AMB}	60 °C
Input OVP	V_{IN_OVP}	400 V_{DC}
Output OVP	V_{OUT_OVP}	19 V_{DC}
Brown-in	V_{IN_ON}	120 V_{DC}

2 Schematic and bill of materials

Figure 3. **EVLVIPGAN50FL schematic (mainboard)**

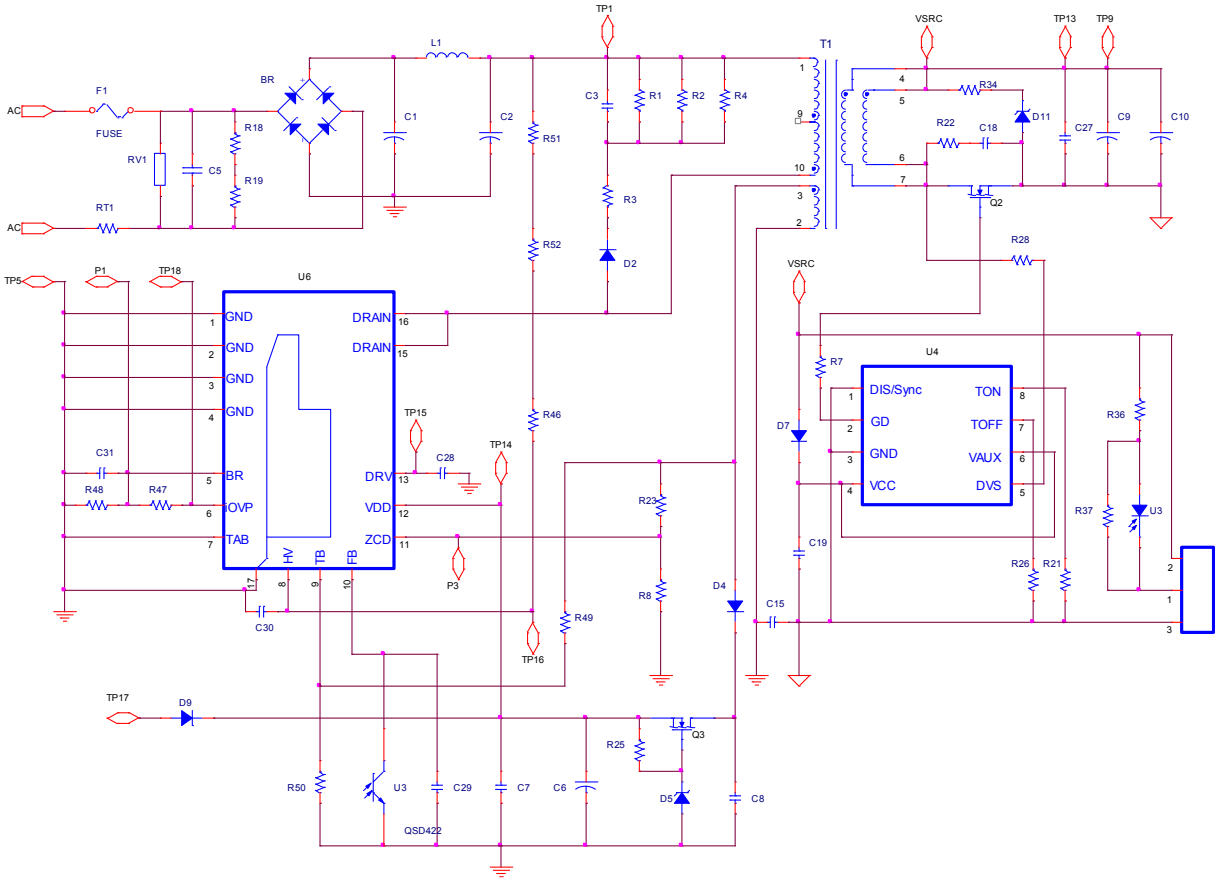


Figure 4. **EVLVIPGAN50FL schematic (daughterboard)**

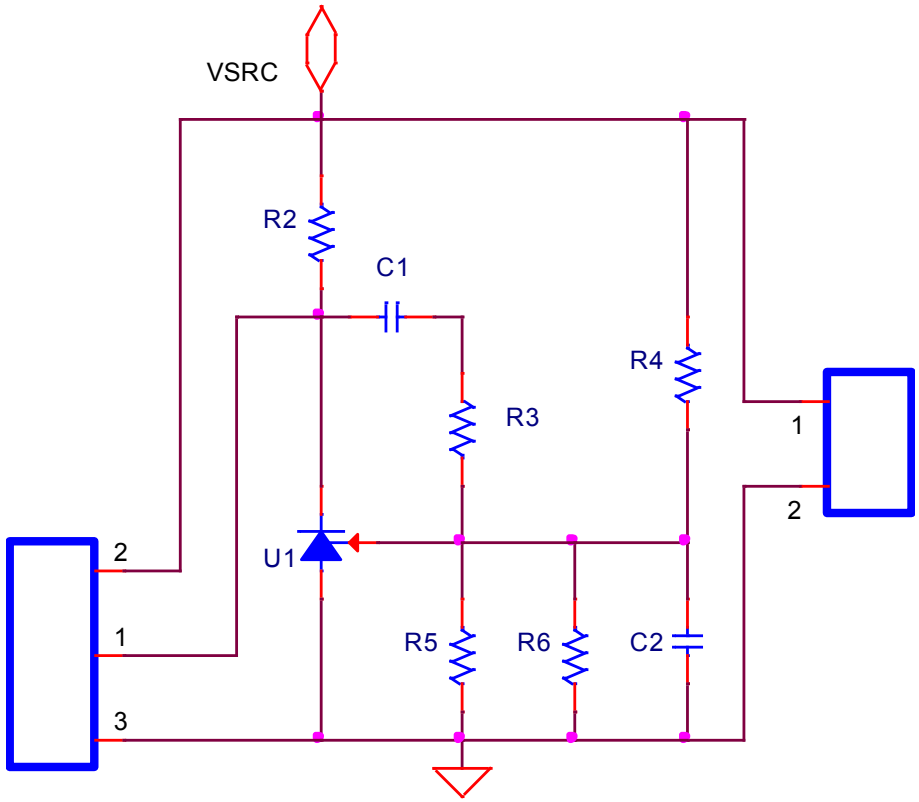


Table 2. **EVLVIPGAN50FL mainboard - Bill of materials**

Ref.	Description	Part number	Package	Supplier
C1, C2	Aluminum electrolytic 47uF 400V - 105°C 20%	860021380015	D=16, H=25, LS=7.5	Würth Electronics
C3	Multilayer ceramic X7R 470pF 1kV 10%	885342208017	1206	Würth Electronics
C5	EMI suppression MKP 0.1uF 305Vac X2 20%	890334023023CS	L=13, H=12, T=6; P=10	Würth Electronics
C6	Aluminum electrolytic 22uF 50V - 105°C 20%	860020672011	D=5, H=11, LS=2	Würth Electronics
C7	Multilayer ceramic X7R 0.1uF 50V 10%	885012206095	0603	Würth Electronics
C8	Multilayer ceramic X7R 4.7uF 100V 10%	12101C475K4T2A	1210	AVX
C9, C10	Ultra-low ESR Al. electrolytic cap, 560uF 25V - 105°C 20%	A750MS567M1EBAE015	D=10, H=12, LS=5	Kemet
C15	X1 Y1 ceramic 4.7nF 250Vrms - 85°C 20%	DE1E3RA472MA4BN01F	D=9, T=5, LS=10	Murata
C18	n.c.		1206	
C19	Multilayer ceramic X7R 4u7 25V 10%	885012208068	1206	Murata
C20	n.c.		0603	
C27	Multilayer ceramic X7R 10uF 25V 10%	885012208069	1206	Würth Electronics

Ref.	Description	Part number	Package	Supplier
C28	Multilayer ceramic X7R 1uF 25V 10%	885012206076	0603	Würth Electronics
C29	Multilayer ceramic X7R 6.8nF 50V 10%	885012206088	0603	Würth Electronics
C30	Multilayer ceramic X7R 220pF 50V 10%	885382206001	0603	Würth Electronics
C31	Multilayer ceramic X7R 1nF 50V 10%	885012206083	0603	Würth Electronics
R1, R2, R4	Anti-surge thick film chip 270k 0.5W 5%	ERJ-P06J274V	0805	Panasonic
R3	Anti-surge thick film chip 18R 0.5W 5%	ERJP08J180V	1206	Panasonic
R7	Thick film chip 0R 0.25W 0%	CRCW06030000Z0EAHP	0603	Vishay
R8	Thick film chip, 5.1k, 0.125W, 1%	ERJP6WF5101V	0805	Panasonic
R18, R19	Thick film chip, 4.7M, 0.250W, 5%	ERJ-U08J475V	1206	Panasonic
R21	Thick film chip 68k 0.0625W 5%	ERJ-PA3J683V	0603	Panasonic
R22	n.c.		1206	
R23	Thick film chip 75k 0.125W 1%	ERJU06F7502V	0805	Panasonic
R25	Thick film chip 47k 0.125W 1%	CRG0805F47K	0805	TE Connectivity
R26	Thick film chip 51k 0.1W 1%	ERJ3EKF5102V	0603	Panasonic
R28	Thick film chip 330R 0.1W 1%	CRCW0603330RFKEA	0603	Vishay
R34	Thick film chip 33R 0.250W 1%	CRG1206F33R	1206	TE Connectivity
R36	Thick film chip 1k 0.0625W 1%	ERJ6ENF1001V	0805	Panasonic
R37	Thick film chip 15k 0.25W 1%	CRGP0603F15K	0603	TE Connectivity
R46, R51, R52	Thick film chip 3M3 0.250W 1%	RC1206FR-073M3L	1206	Yageo
R47	Thick film chip 82k 0.25W 1%	CRCW060382K0FKEAHP	0603	Vishay
R48	Thick film chip 43k 0.1W 1%	CRCW060343K0FKEA	0603	Vishay
R49	Thick film chip 680k 0.250W 1%	ERJU06F6803V	0805	Panasonic
R50	Thick film chip 20k 0.250W 1%	CR1206-FX-2002ELF	1206	Bourns
RT1	NTC 2.2R 7A 20%	B57237S0229M000	Ø15 x 7 x p.7.5mm	Epcos
F1	Time-delay fuses 3.15A - 300Vac	SS-5H-3-15A-BK	L=4.3, H=7.85, LS=5.08	Copper Bussmann
RV1	SIOV metal oxide varistors 275Vac 25A	B72210S0271K101	L=12, H=14.5, LS=7.5	Epcos
L1	Fixed inductor 47uH 2.0A 10%	7447720470	D=7.8 H=9.5, LS=5	Würth Electronics
T1	Flyback transformer	750841235 rev. 00	RM8	Würth Electronics

Ref.	Description	Part number	Package	Supplier
D1	Bridge rectifier KBP306G 3A - 600V	KBP306G	L=14.8, H=10.6, LS=3.6	Diodes
D2	Fast switching rectifier RS1K 1A - 800V	RS1K-E3/61T	SMA	Vishay
D4	Switching diode BAV21W 0.250W	BAV21W-E3-08	SOD-123	Vishay
D5	Zener diode BZV55-C18 18V - 500mW 5%	BZV55-C18,115	SOD80C	Nexperia
D7	Schottky diode BAT43WS 0.200W	BAT43WS-7-F	SOD-323	Multicomp pro
D9	Small signal Schottky diodes BAT41ZFILM	BAT41ZFILM	SOD-123	STMicroelectronics
D11	Zener diode SMAZ24 24V - 1W 5%	SMAZ24-13-F	SMA	Diodes
Q2	Power MOSFET STL110N10F7 0.006ohm - 100V	STL110N10F7	PQFN 5x6mm	STMicroelectronics
Q3	Power MOSFET BSS169 12ohm - 100V	BSS169H6327XTSA1	SOT23	Infineon
U3	Optocoupler SFH617A-2	SFH617A-2X017	SMD-4	Vishay
U4	Synchronous retification controller SRK1001	SRK1001TR	SO-8	STMicroelectronics
U6	VIPERGAN50	VIPERGAN50	VFQFPN 5x6x1	STMicroelectronics

Table 3. EVLVIPGAN50FL daughterboard - Bill of materials

Ref.	Description	Part number	Package	Supplier
R2	Thick film chip 15k 0.125W 1%	CRG0805F15K	0805	TE Connectivity
R3	Thick film chip 0R 0.125W 0%	RC0805FR-070RL	0805	Yageo
R4	Thick film chip 270k 0.125W 1%	ERJ-6ENF2703V	0805	Panasonic
R5	Thick film chip 33k 0.125W 1%	CRG0805F33K	0805	TE Connectivity
R6	Thick film chip 110k 0.125W 1%	ERJPA3F1103V	0805	Panasonic
C1	Multilayer ceramic X7R 8.2nF 50V 5%	VJ0805Y822JXAAC	0805	Vishay
C2	N.C.		0805	
U1	1.24V programmable shunt voltage reference	TS3431AILT	SOT23-3L	STMicroelectronics

3 Circuit description

The EVLVIPGAN50FL is composed of a main board and a daughterboard, whose schematics are shown in Figure 2 and Figure 3 respectively.

The main board contains, on the primary side, a diode bridge for double wave rectification, an input pi filter for EMI, a flyback transformer, the VIPERGAN50 and all the related components needed for polarization and features setting, described in detail later; on the secondary side, the output capacitors and the output rectifier, realized by a power MOSFET driven by a synchronous rectifier for efficiency optimization.

The resistor R_{HV} = R51 + R52 + R46 from rectified mains to HV pin is used to activate the internal high-voltage current source, which charges the capacitor connected between VDD and GND at startup. As V_{DD} reaches V_{DD-ON} (15 V typ.), the high-voltage current source is turned off and the VIPERGAN50 starts switching. To minimize the residual consumption from the mains, the R_{HV} value is selected in the range of several tens of Mohms. In case of V_{DD} reduction below V_{DD-OFF}, (for instance, during a fault managed in auto-restart) the switching activity is immediately stopped and the high-voltage current source is activated again until VDD capacitor is charged back to V_{DD-ON}.

When the high-voltage current source is turned off, HV is internally connected to iOVP; this allows to use R_{HV} also as high-side resistor of a voltage divider sensing the rectified mains to set input overvoltage protection (low-side resistor is R47 + R48 between iOVP and GND) and brown-out protection (low-side resistor is R48 between BR and GND), as described later.

QR operation is realized through the ZCD pin, connected to the transformer auxiliary winding used also to supply the IC, through the voltage divider made up by R23 and R8. When the transformer completes the energy transfer to the output, the auxiliary winding voltage decreases, and as ZCD voltage falls below 60 mV, the GaN is enabled to switch, after some delay. The optimum value of this delay is the one for which turn-on occurs exactly at the valley of the resonance following the demagnetization, which minimizes the switching losses. It can be found experimentally, and easily set through the selection of R49 and R50, which form a voltage divider between auxiliary winding and TB.

An optocoupler brings the voltage reference error signal to the primary side, where it adjusts the FB pin voltage level (and thus the DRAIN peak current) to the value required by the control loop for output voltage regulation.

Voltage reference, voltage divider for the output voltage setting, compensation network and output connectors are contained in the daughterboard, which is soldered orthogonally to the main board.

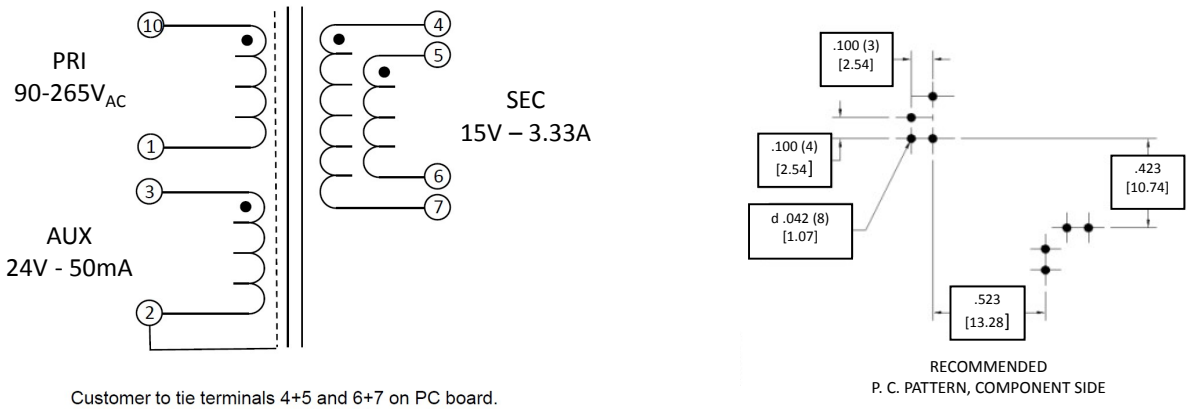
4 Transformer

The transformers' electric and mechanical characteristics are shown in the table and figures below.

Table 4. Transformer characteristics

Parameter	Value	Test conditions
Manufacturer	Wurth	
Part number	750841235 rev00	
Primary inductance (pins 10 - 1)	0.35mH ±10%	10kHz, 100mV, Ls
Leakage inductance	4.5uH typ, 7uH max.	tie(2+3+4+5+6+7),100kHz, 100mV, Ls
Primary to sec turn ratio	10:1	(10-1):(4-7), tie(4+5, 6+7)
Primary to aux turn ratio	5:1	(10-1):(3-2)
Reflected voltage	160V	
Saturation current	2.3A max.	20% roll-off from initial
Operating current	2.1A max.	
DC-DC resistance 10-1	0.35 ohms max.	20ºC
DC-DC resistance 4-7	0.01 ohms max.	tie (4+5, 6+7), @20ºC
DC-DC resistance 3-2	0.26 ohms max.	20ºC

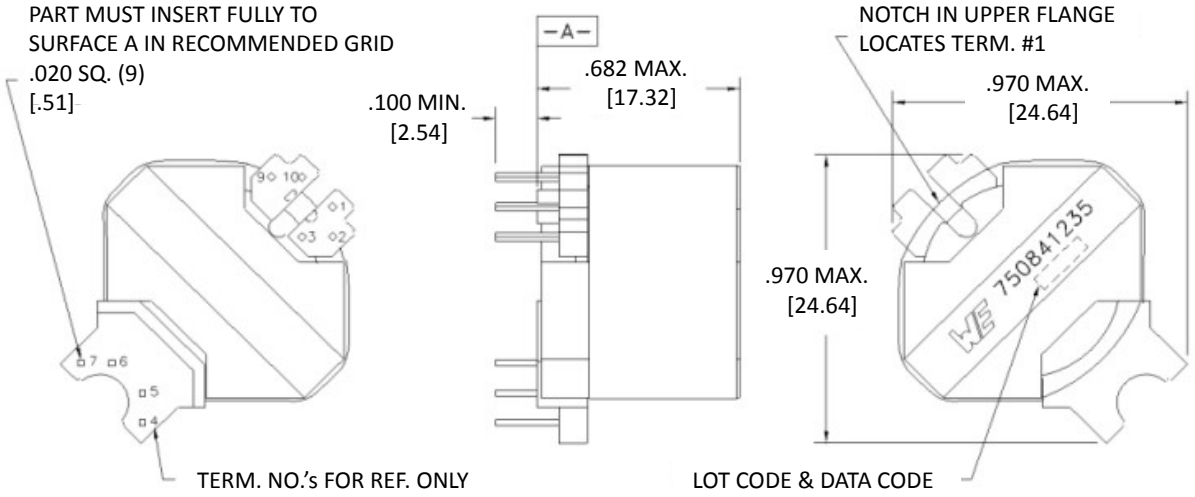
Figure 5. Transformer: electrical schematic (on the left); pin diagram bottom view (on the right)



Customer to tie terminals 4+5 and 6+7 on PC board.

Application of the transformer allows for the leadwires between terminals 4&5 and 6&7 to solder bridge.

Figure 6. Transformer size



5 Testing the board

5.1 Efficiency

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75%, and 100% of maximum load, at nominal input voltages (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}).

External power supplies (the power supplies which are contained in a separate housing from the end-use devices that they are powering) need to comply with the Code of Conduct, version 5 "Active mode efficiency" criterion, which states that an SMPS with power throughput of 50 W should have an active mode efficiency higher than 89.00%.

Another standard to be applied is the DOE (Department of energy) recommendation, whose active mode efficiency requirement for the same power throughput is 87.80%.

As shown in Table 5, the SMPS is compliant with both standards.

Table 5. Active mode efficiency

Regulation requirements @ P_{OUTnom} = 50W		EVLVIPGAN50FL performance
CoC5 req.	DOE req.	
89.00%	87.80%	90.44% (@ V_{IN} = 115V_{AC})
		90.03% (@V_{IN} = 230V_{AC})

5.2 Light-load performances

Figure 7. No load consumption vs. V_{IN}

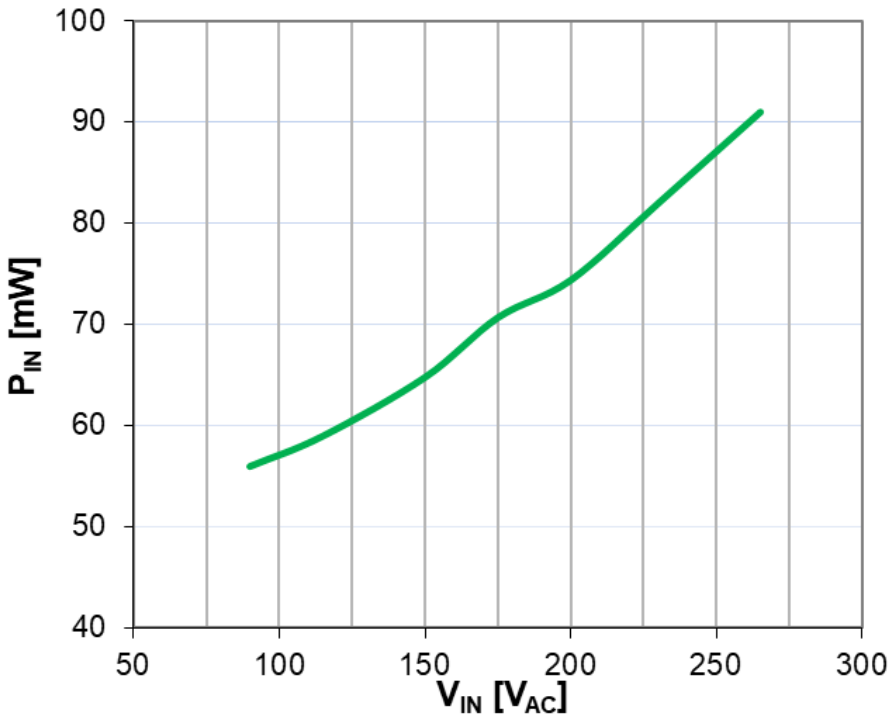
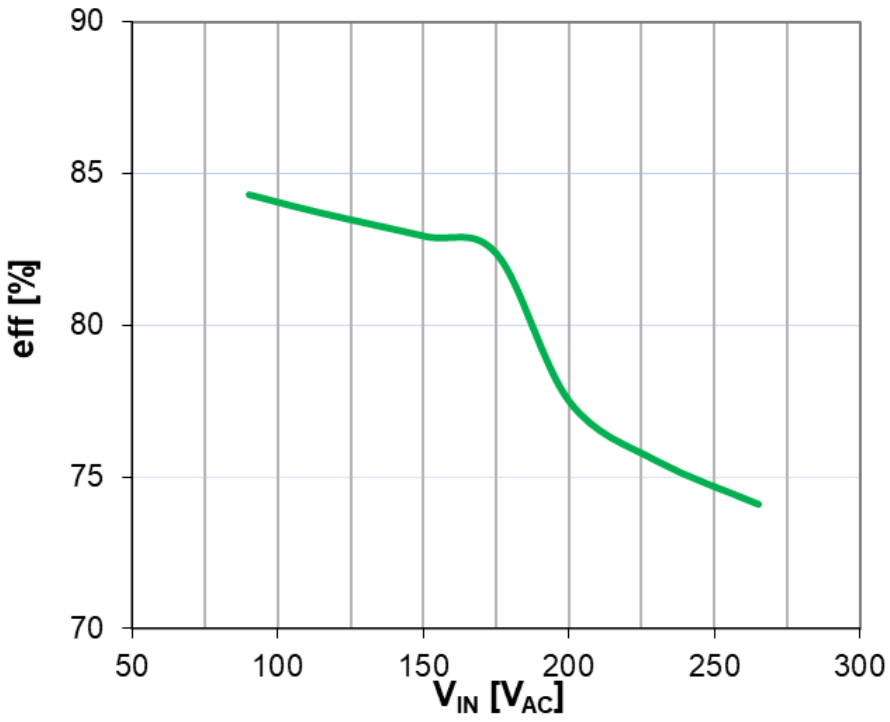


Figure 8. **Efficiency @ 10% output load vs. V_{IN}**



5.3 Typical waveforms

Drain voltage waveforms in full load condition for the two nominal input voltages are reported in Figure 9 and Figure 10, and for minimum and maximum input voltage in Figure 11 and Figure 12 respectively.

Figure 9. **115 V_{AC} full load V_{DRAIN} & I_{DRAIN}**

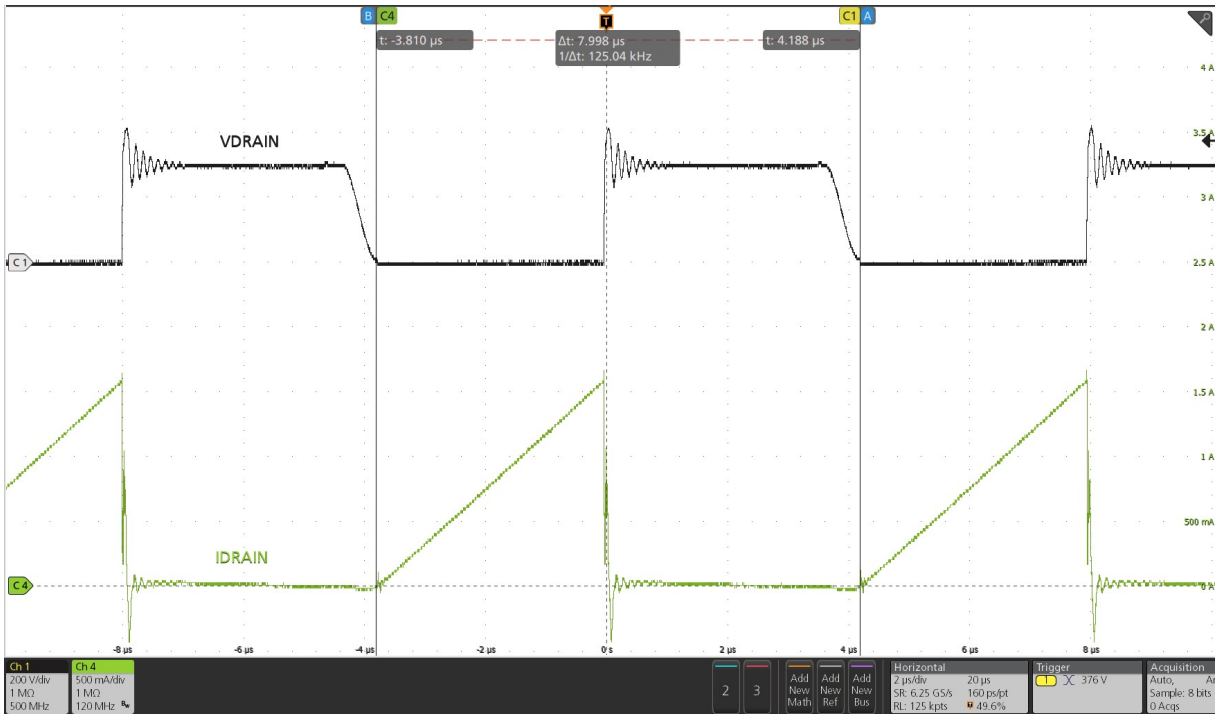


Figure 10. 230 V_{AC} full load V_{DRAIN} & I_{DRAIN}

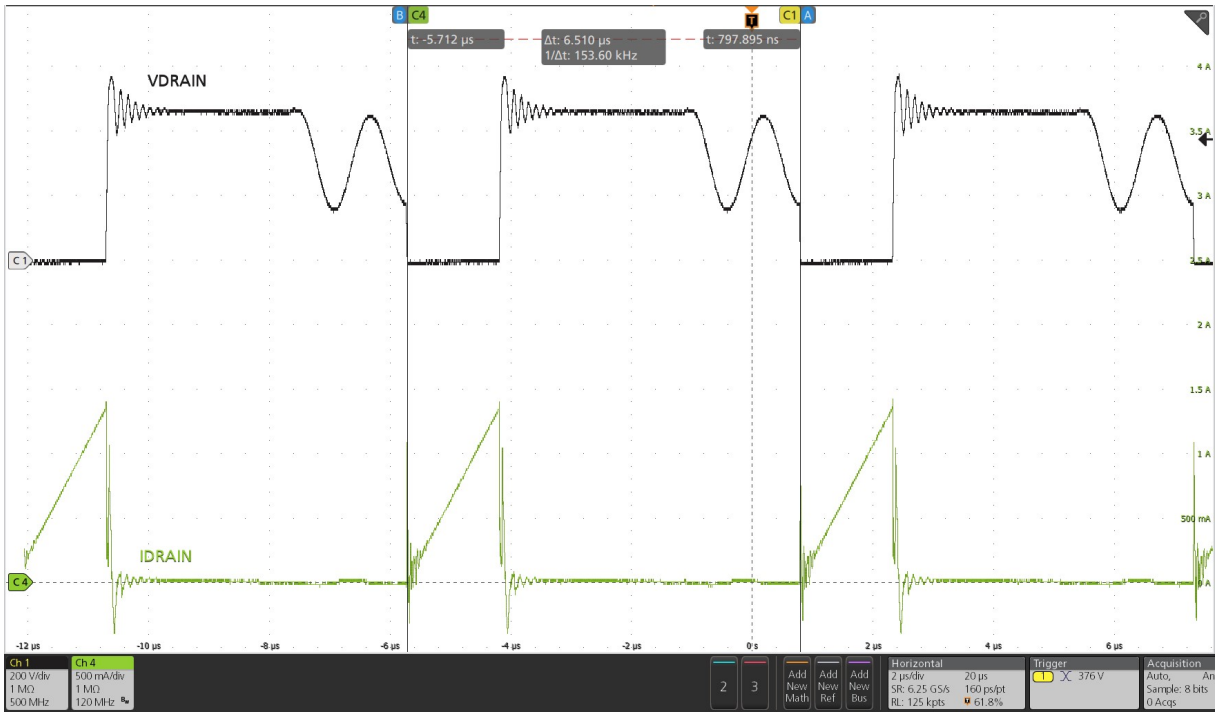


Figure 11. 100 V_{AC} full load V_{DRAIN} & I_{DRAIN}

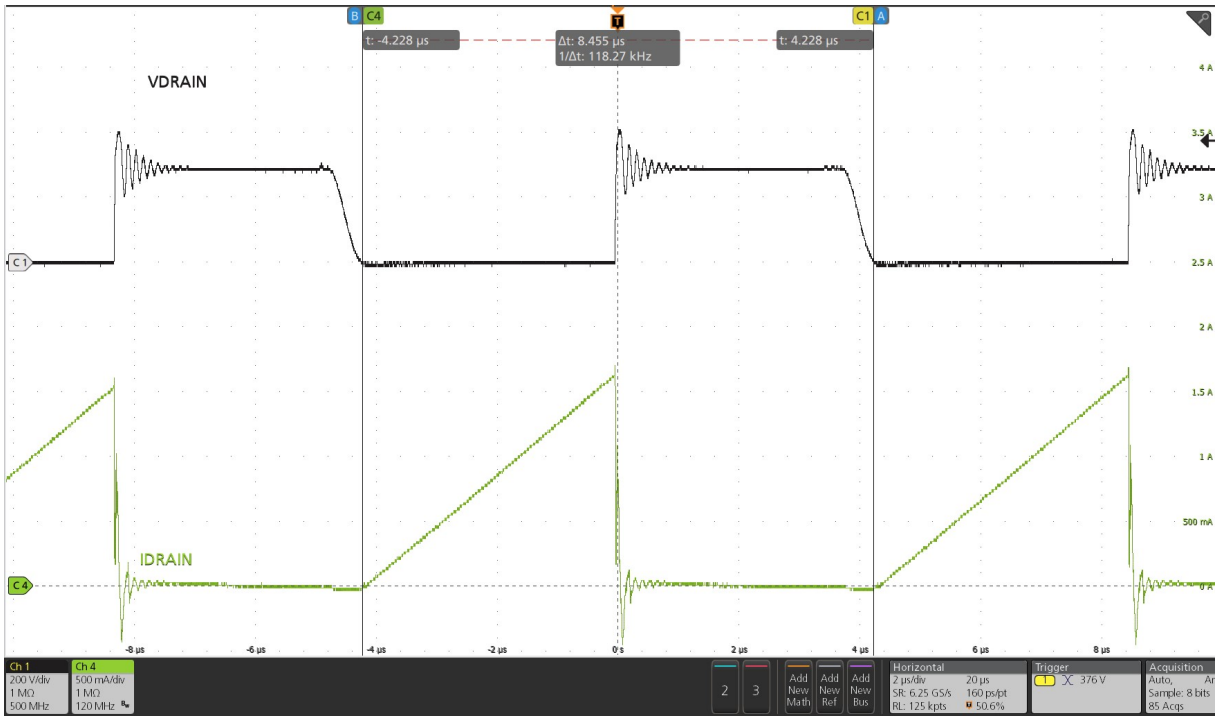
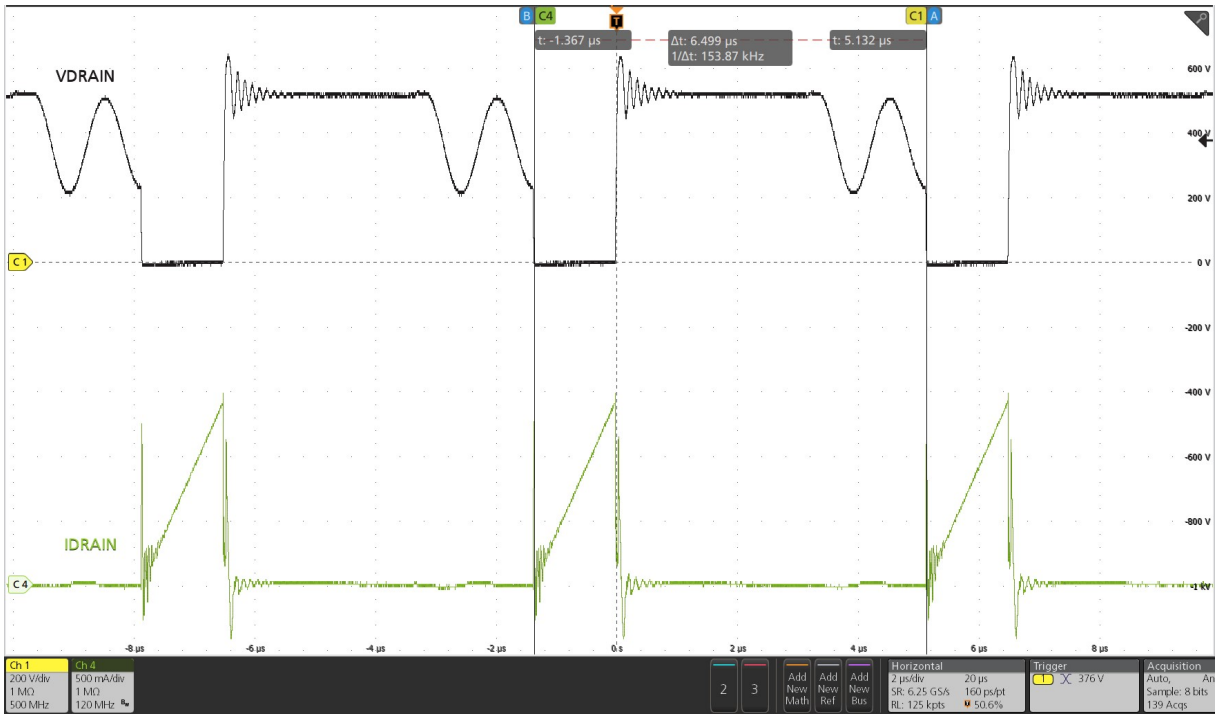


Figure 12. 265 V_{AC} full load V_{DRAIN} & I_{DRAIN}



6 ICs features

6.1 Dynamic blanking time and turn-on delay (TB)

Dynamic Blanking Time

To prevent the tendency of the system to excessively increase the frequency at light load and high input voltage, a blanking time function is implemented.

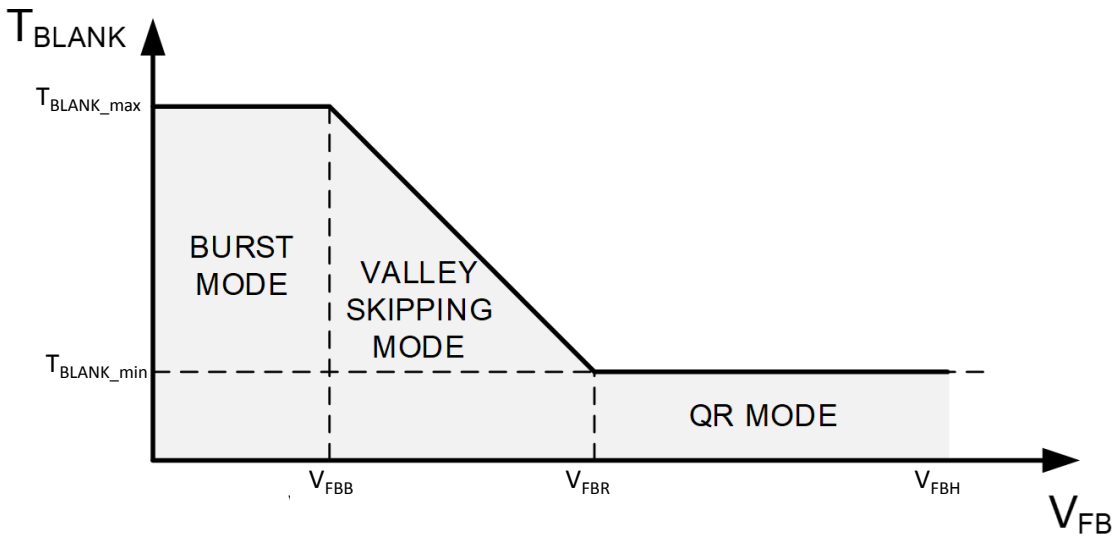
If the demagnetization completes - hence a negative-going edge appears on the ZCD pin - after a time exceeding T_{BLANK} from the previous turn-on, the GaN is turned on again, with some delay to ensure minimum voltage at turn-on (“QR mode”).

If the negative-going edge appears before T_{BLANK}, it is ignored, and only the first negative-going edge after T_{BLANK} turns on the GaN (“valley-skipping mode”).

When TB is connected to GND, the T_{BLANK} value only depends on V_{FB}, as shown in Figure 13. This is referred to as “static blanking time”: the switching frequency is progressively reduced with output load, resulting in lower frequency-related losses.

V_{FBB}, V_{FBR}, T_{BLANK_max}, and T_{BLANK_min} (0.7 V, 1.15 V, 16 us and 4.16 us typ., respectively) are reported in the datasheet.

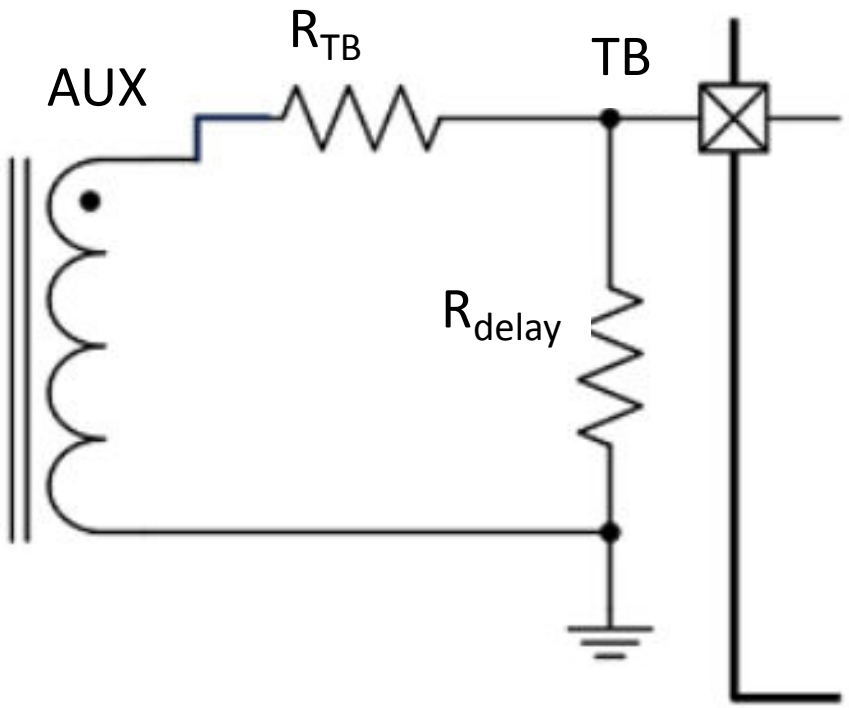
Figure 13. Blanking time vs. V_{FB} @ TB = GND (static blanking time)



But in QR systems, the switching frequency dramatically increases also with the input voltage and is one of the major limitations when designing high efficiency converters. To solve this issue, the VIPERGAN50 is equipped with a "dynamic blanking time" function.

Connecting TB to the auxiliary winding through a voltage divider, as shown in Figure 14, a current proportional to the input voltage is sourced during on-time from the pin through the high-side resistor R_{TB}.

Figure 14. **TB pin connection for dynamic blanking time and turn-on delay setting**



This current is internally sampled and used to increase the blanking time during the next off-time, according to the following formula:

$$T_{BLANK\_dyn(VIN)} = T_{BLANK\_min} + K_{BLANK} \cdot \frac{N_{AUX}}{N_{PRI}} \cdot \frac{V_{IN}}{R_{TB}} \quad (1)$$

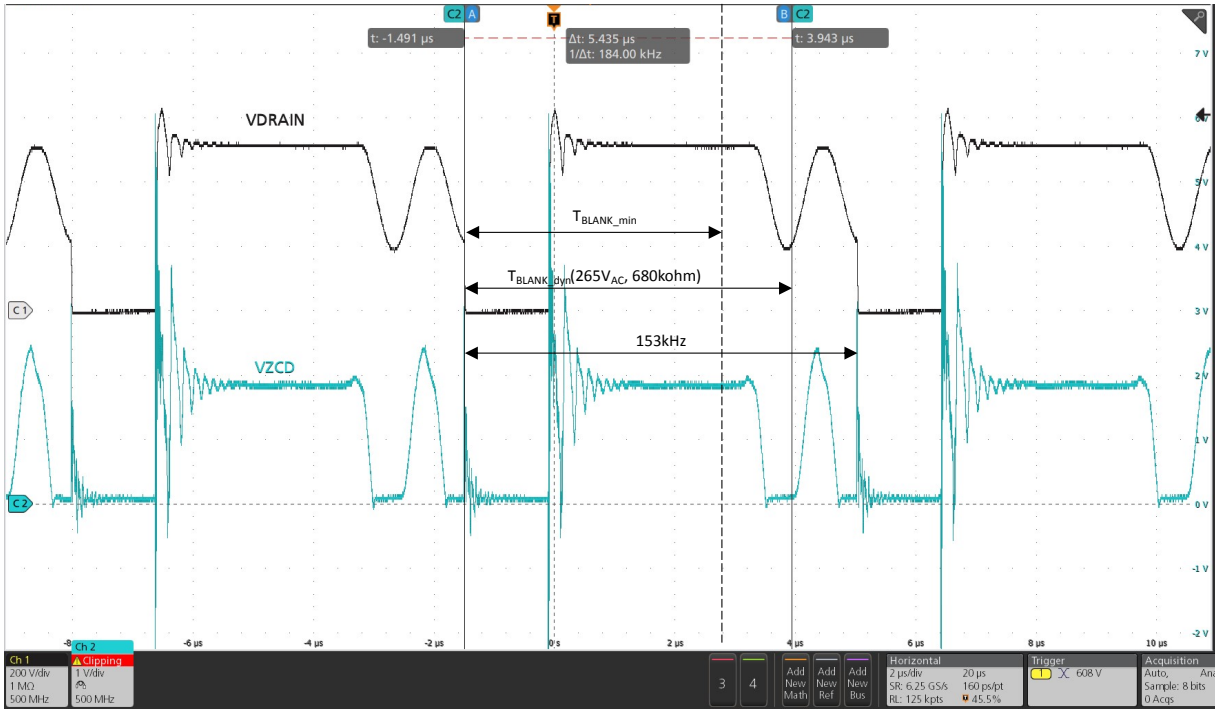
where K_{BLANK} is the blanking time gain, whose value is reported in the datasheet (10.91 usec/mA, typ.), and N_{AUX}/N_{PRI} is the auxiliary-to-primary turn ratio of the transformer.

In case of static blanking time, at heavy or full load condition ($V_{FB} > V_{FBR}$), the VIPERGAN50 would be enabled to turn on after T_{BLANK_min}, according to Figure 13. With reference to full load operation of EVLVIPGAN50FL at 265 V_{AC}, shown in Figure 15, this would mean first valley turn-on, or $f_{SW} = 1/(1/T_{BLANK\_min} + 1/T_{delay}) \sim 200$ kHz.

But in this evaluation board R_{TB} = R49 = 680 kohm has been set, which at 265 V_{AC}, according to 1, results in about 5.4 usec dynamic blanking time, enough to skip the first valley, thus reducing the switching frequency to 150 kHz.

At low line, where the contribution of the switching losses to the total power waste becomes less significant, the second addendum of 1 is negligible, so the blanking time value remains quite close to $T_{BLANKmin}$, and the converter is allowed to switch at higher frequencies.

Figure 15. Dynamic blanking time at 265 V_{AC}, full load, R_{TB} = 680 kohm



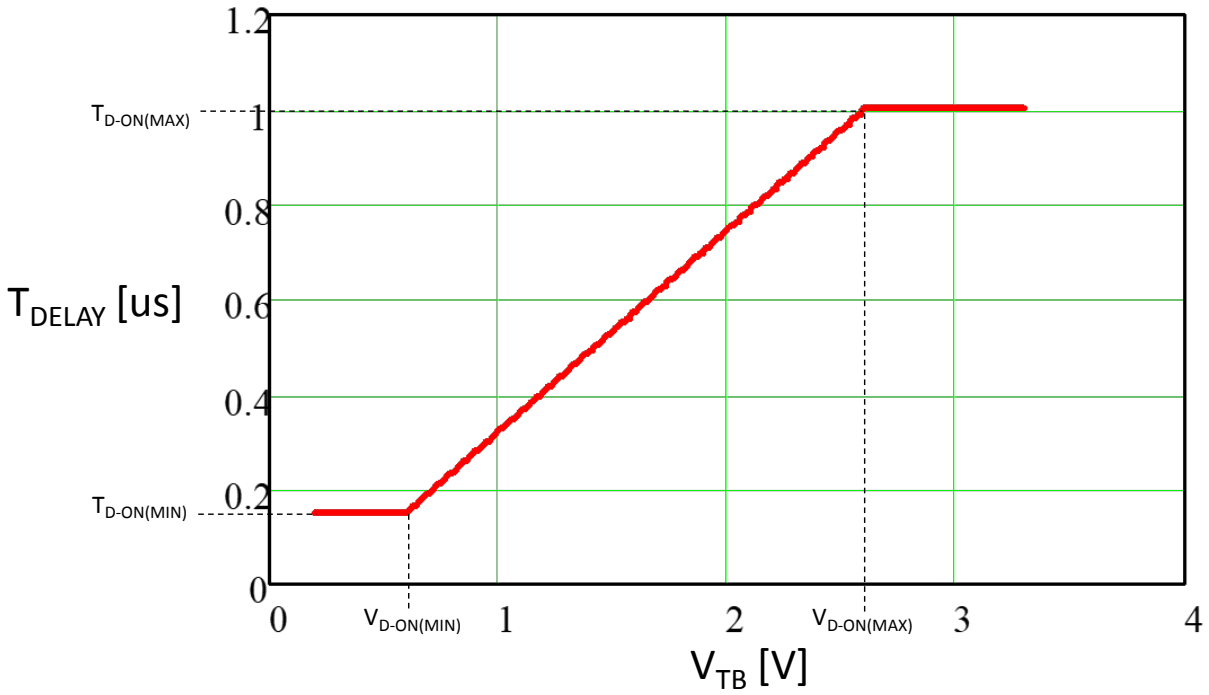
Turn-on delay

The time needed to reach V_{DRAIN} valley after the transformers' demagnetization can change a lot between one design and another, thus VIPERGAN50 integrates a special function to exactly synchronize the turn-on time at the valley of the resonance, minimizing the turn-on losses.

If TB is connected to GND, or V_{TB} < 0.6 V, the turn-on delay is set to default, $T_{D-ON(MIN)}$ (150 nsec typ.).

If TB is connected to a voltage divider, its value depends on the V_{TB} measured during the precedent turn-off, ranging from $T_{D-ON(MIN)}$ (at V_{TB} = 0.6 V) to $T_{D\text{-}ON(MAX)}$ = 1 usec, typ. (at V_{TB} = 2.6 V), as reported in the graph here below.

Figure 16. **Blanking time vs. V_{FB} @ TB = GND**



The needed additional turn-on delay can be found experimentally as follows:

- TB is connected to GND, a valley switching condition is selected and the default turn-on delay is measured as the time interval between the last V_{ZCD} crossing of V_{ZCD_th} = 60 mV with negative slope and the VIPERGAN50 turn-on (177 nsec in the present case, Figure 17).
- If turn-on occurs far from the valley, the period of the DRAIN voltage ringing after magnetization, T_{VDRAIN}, is measured, so to find out the additional turn-on delay, $T_{D\_ON(ADD)}$, necessary to complete the period (about 180 nsec in the present case, Figure 18).
- The V_{TB} value corresponding to T_{DELAY} (V_{TB}) = $T_{D\_ON(MIN)}$ + $T_{D\_ON(ADD)}$ is found from Figure 16 (about 0.97 V in the present case).

Figure 17. **TB = GND, measure of the default turn-on delay**

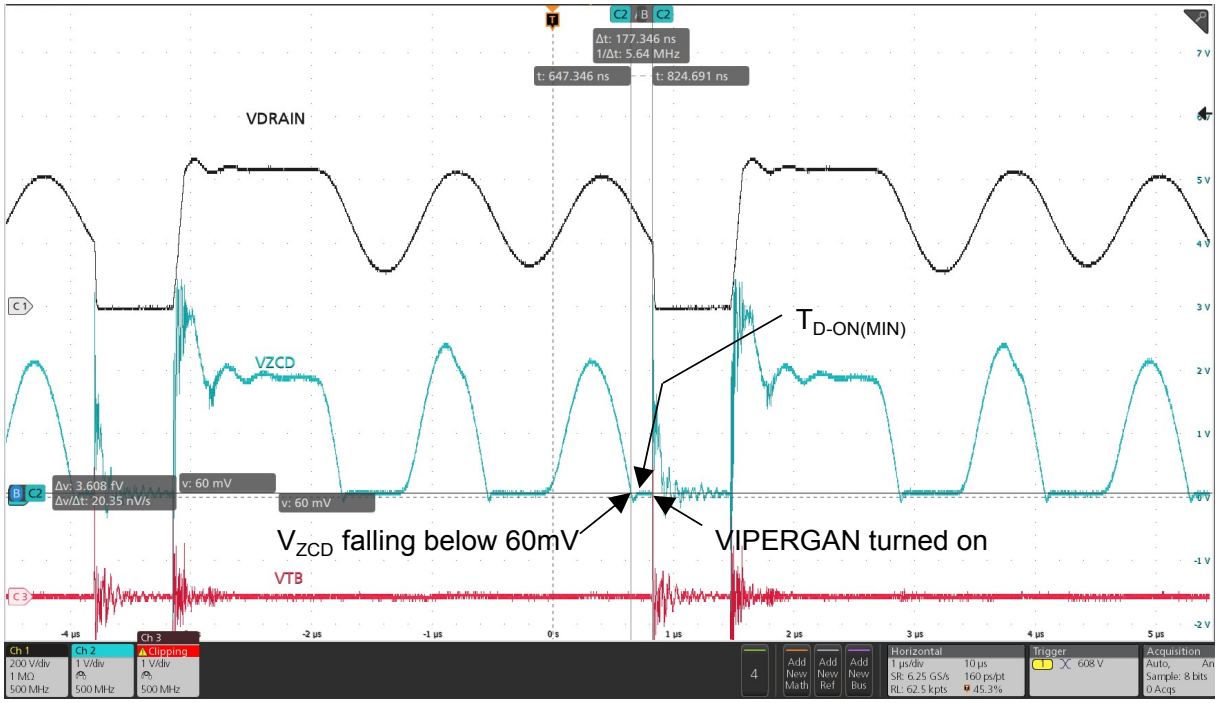
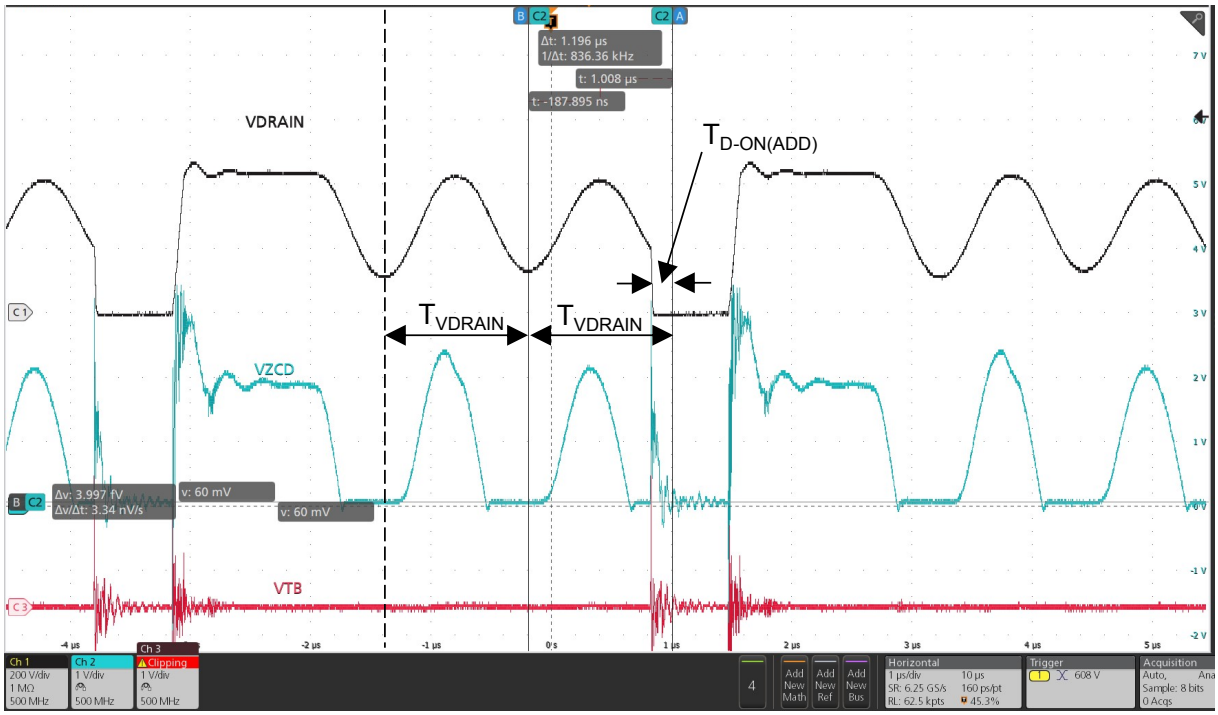


Figure 18. **TB = GND, measure of the additional turn-on delay**



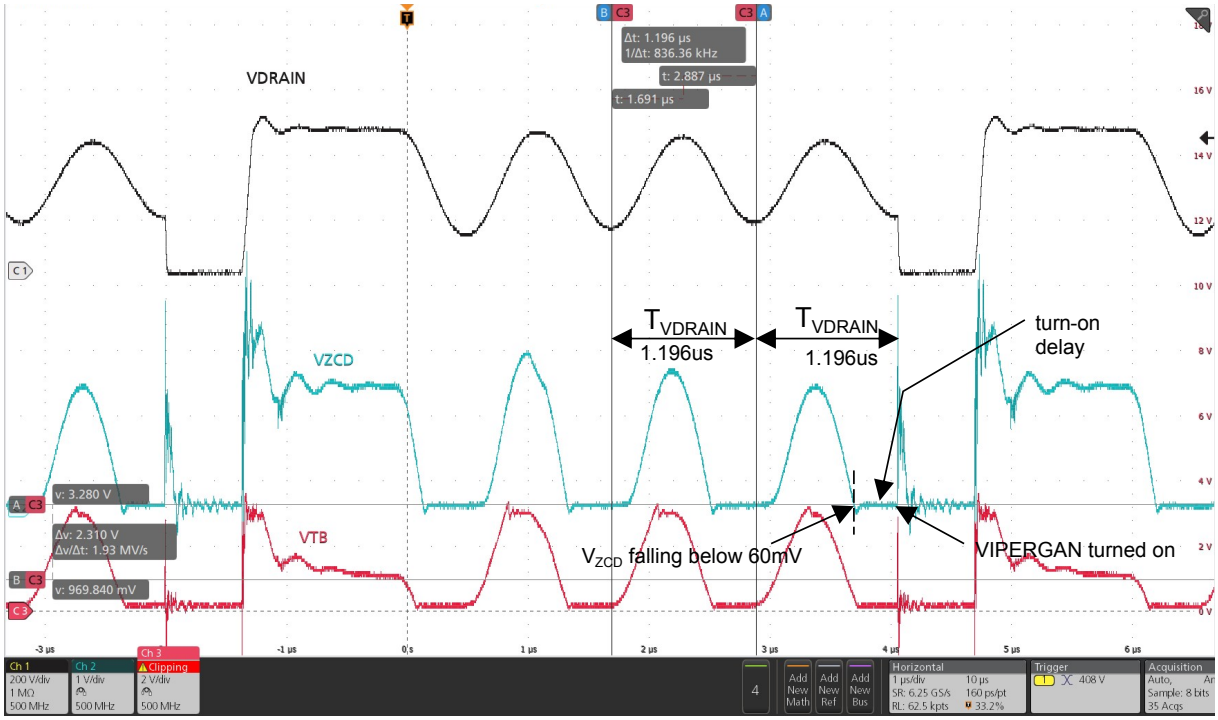
The obtained V_{TB} value, inserted in equation 2, allows to calculate the value of the low-side resistor R_{delay} = R50 to get the needed turn-on delay (the high-side resistor R_{TB} = R49 has been previously set for dynamic blanking time selection):

$$R_{delay} = \frac{R_{TB}}{\frac{N_{AUX}}{N_{SEC}} \cdot \frac{V_{OUT}}{V_{TB}} - 1} \quad (2)$$

Equation 2 gives 22 kohm for R_{delay}.

Figure 19 shows that V_{TB} = 0.97 V, and turn-on occurs right on the valley of the DRAIN voltage ringing after demagnetization.

Figure 19. Valley switching with R_{delay} = 22 kohm, V_{TB} = 0.97 V



6.2 Line voltage feedforward

In QR operation, the switching frequency increases with the input voltage, and since the overcurrent setpoint is fixed, the deliverable output power can change a lot from minimum to maximum input voltage, reaching a difference of more than twice in case of wide-range mains applications.

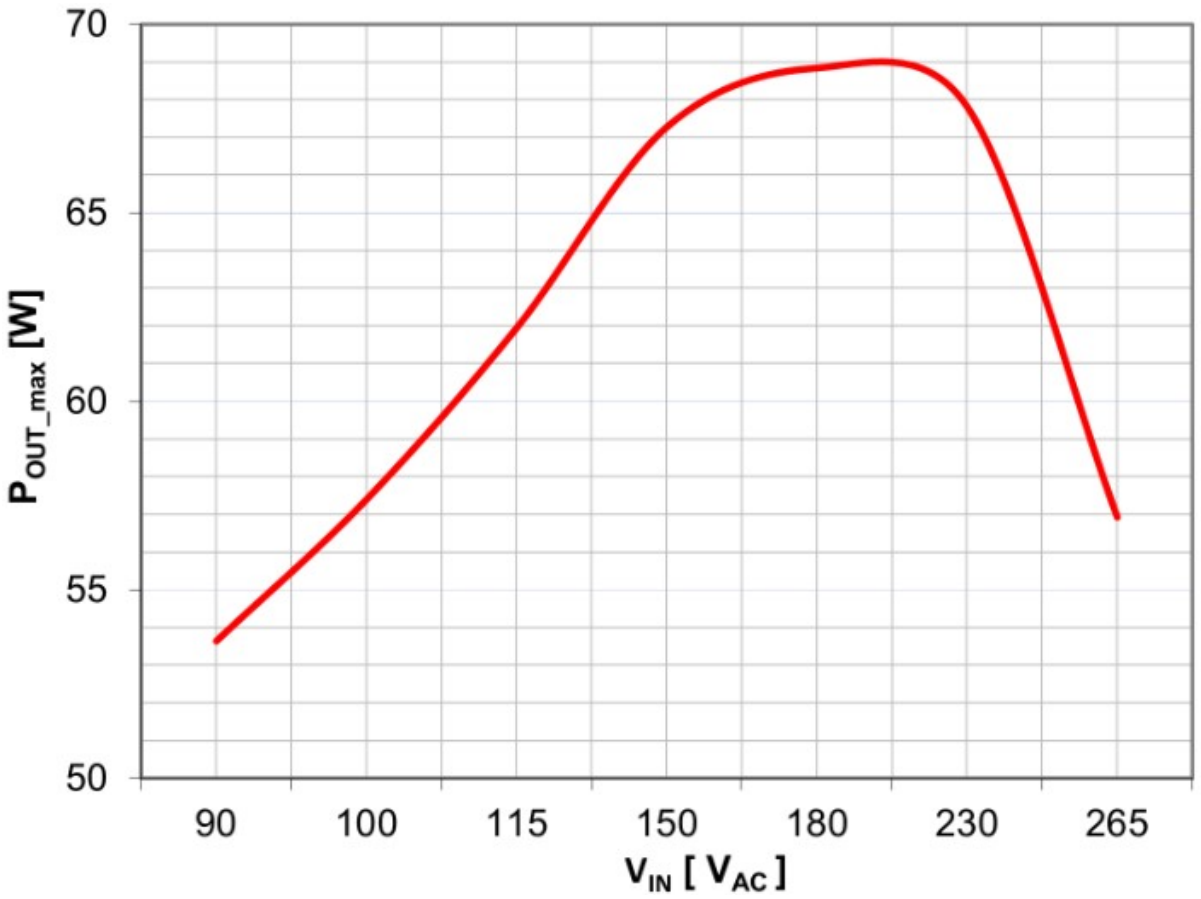
To solve this issue, the current sourced from the ZCD pin through the R23 resistor during GaN's on-time, given by the following formula:

$$I_{FF} = \frac{N_{AUX}}{N_{PRI}} \cdot \frac{V_{IN}}{R23} \quad (3)$$

It is internally mirrored and used to provide a reduction of the overcurrent setpoint, proportional to the input voltage. The optimum R23 value is that for which the maximum deliverable output power is the same at the extremes of the input voltage range.

After bench tests, the value of 75 kohm has been found, resulting in the power throughput shown in the figure below.

Figure 20. **Max. deliverable output power vs. V_{IN} with feedforward compensation**



6.3 Step load response

The undershoot/overshoot of the output voltage following a step load from 0.1 A (burst mode) to 3.3 A (max. load) or vice versa is within 3% of the nominal value.

Figure 21. **0.1 A to 3.3 A step load response @ 90 V_{AC}**

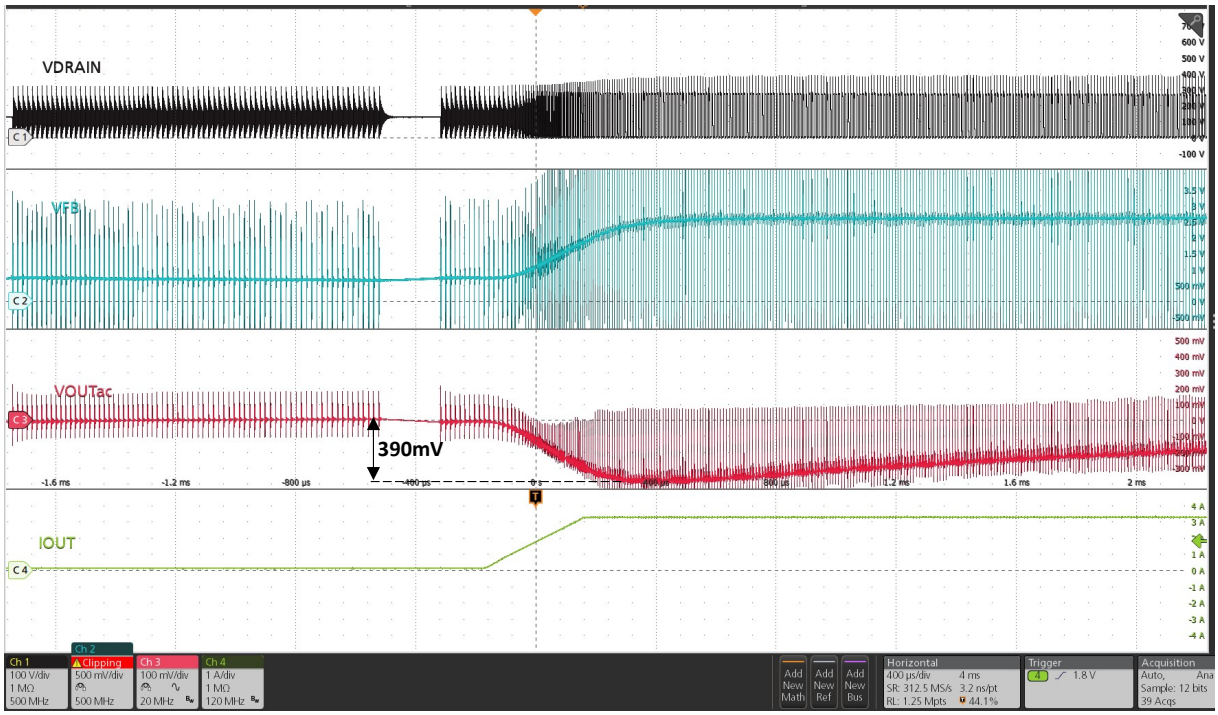
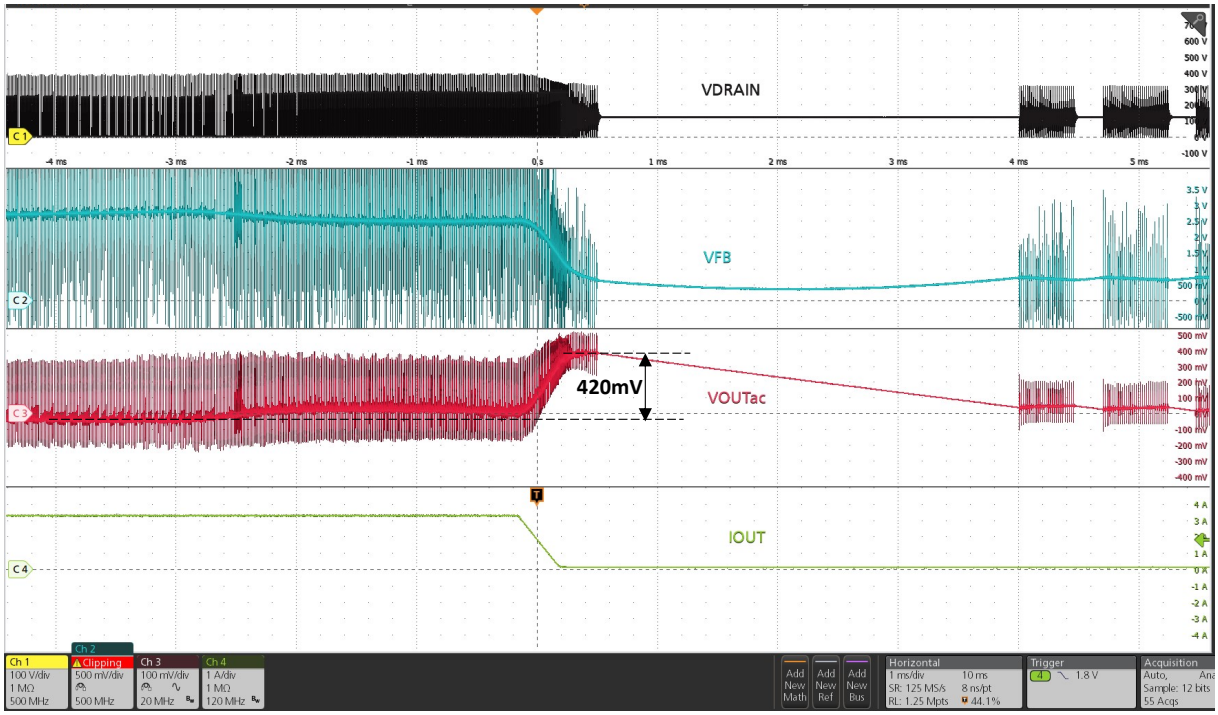


Figure 22. **3.3. A to 0.1 A step load response @ 90 V_{AC}**



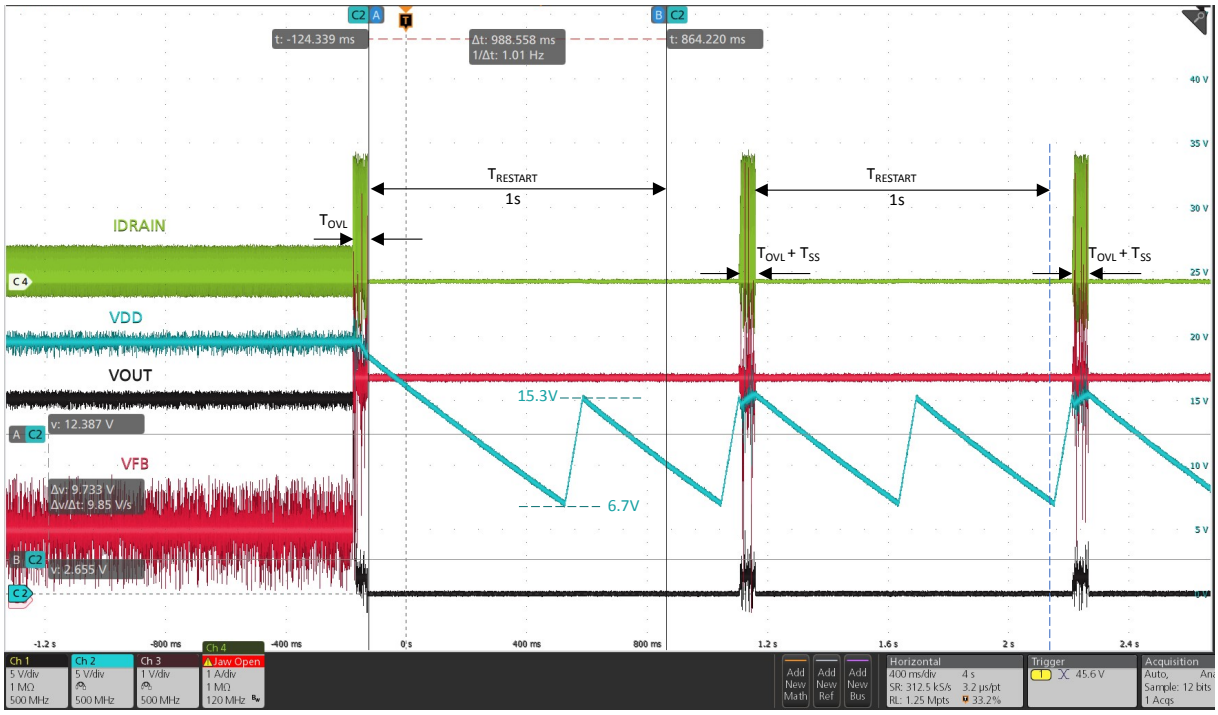
6.4 Overload protection

To manage an overload or a short-circuit condition, an internal up-down counter is incremented or decremented with an internal clock, depending on whether V_{FB} is, respectively, higher or lower than the upper saturation limit V_{FBH}.

In case of permanent overload/short-circuit event, the protection is tripped after a delay time equal to T_{OVL} (50 ms typical value), the IC is shut down and maintained off for a time equal to $T_{RESTART}$ (1 sec typical value). During overload condition, V_{DD} is maintained between the V_{DD-ON} and $V_{DD-RESTART}$ thresholds (15 V and 7 V typ. values, respectively) by the periodical activation of the internal HV current source.

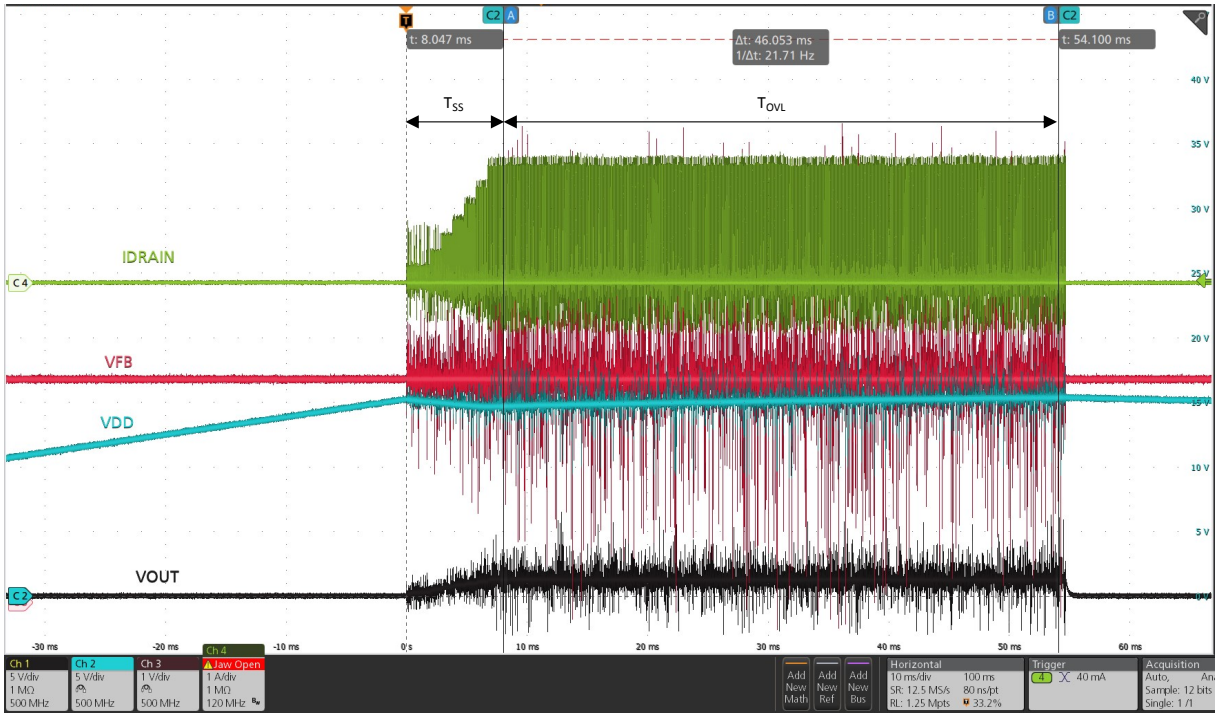
After $T_{RESTART}$, the device has to wait for the first V_{DD-ON} crossing, then restarts. If the fault is still present, the protection occurs indefinitely in the same way, as shown in Figure 23. This ensures low repetition rate restart attempts, so that the converter works safely with extremely low power throughput and avoids the IC overheating in case of repeated overload events.

Figure 23. Output short-circuit applied



At any restart attempt, soft-start is invoked (see Figure 24).

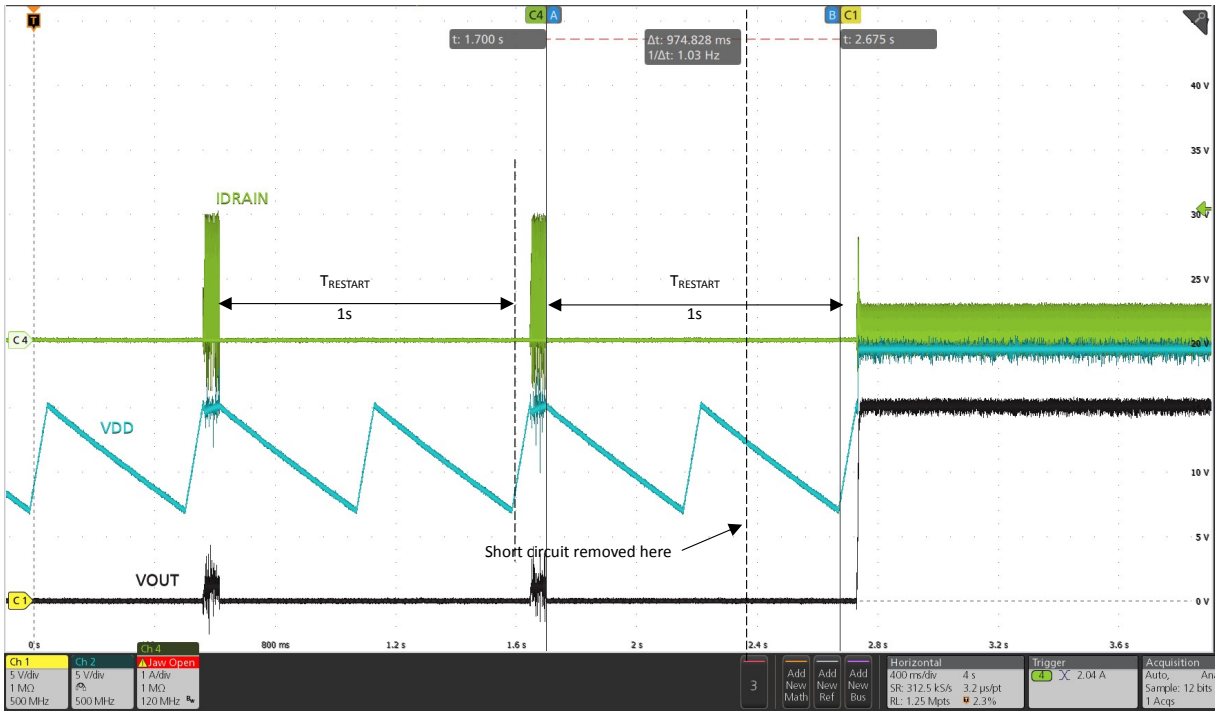
Figure 24. **Output short-circuit steady-state, restart attempts with soft-start**



After the fault removal, the IC resumes working normally (Figure 25). If the fault is removed during T_{SS} or T_{OVL}, that is, before the protection tripping, the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short-circuit is removed during $T_{RESTART}$, the IC has to wait until $T_{RESTART}$ has elapsed, and V_{DD} has recharged to V_{DD-ON} before resume switching.

Figure 25. **Output short-circuit removed and IC restart**



6.5 Input overvoltage protection

To avoid that the GaN's breakdown voltage could be exceeded following an overvoltage on the main line, an input overvoltage protection is realized, connecting the rectified input voltage mains to iOVP and GND through a voltage divider.

The input overvoltage level is set considering that:

- after startup, an internal switch connects iOVP to HV, which senses the rectified input voltage mains;
- when V_{iOVP} exceeds the internal threshold V_{iOVP_th} (5 V typ.) for more than T_{iOVP} (250 µs typ.), the switching activity is inhibited, and is resumed when V_{iOVP} falls below V_{iOVP_th}. The delay time T_{iOVP} is intended to filter out possible disturbances that may be coupled during operation and is implemented through an up/down counter. During protection, V_{DD} is recycled between $V_{DD\text{-}RESTART}$ and $V_{DD\text{-}ON}$ by the periodical activation of the internal HV current source.

In this evaluation board, the input OVP level is set to 400 V_{DC}, roughly corresponding to 285 V_{AC}. Triggering, steady-state and restart after fault removal are shown in the following figures, where V_{IN_DC} (V_{TP1} with reference to Figure 3) is the DC voltage appearing at the input of the converter after the pi filter rectification.

Figure 26. V_{IN} = 265 V_{AC} to 285 V_{AC}, input OVP triggered

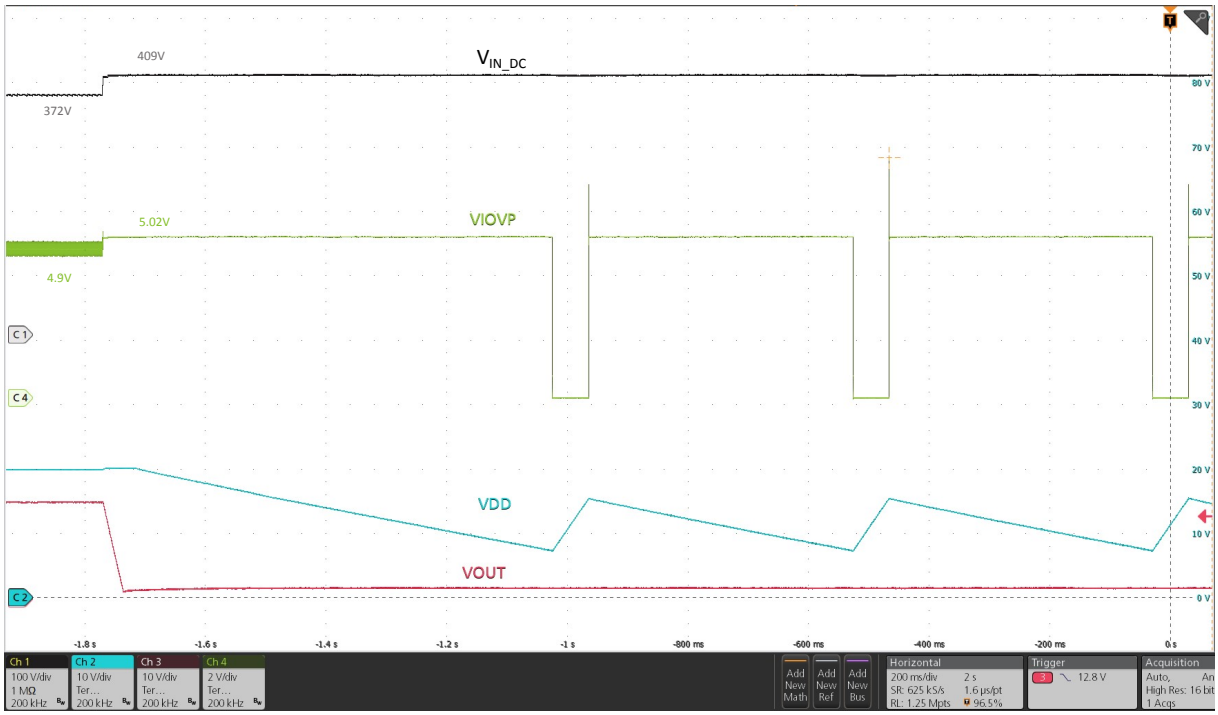


Figure 27. V_{IN} = 265 V_{AC} to 285 V_{AC}, input OVP triggered, T_{iOVP}

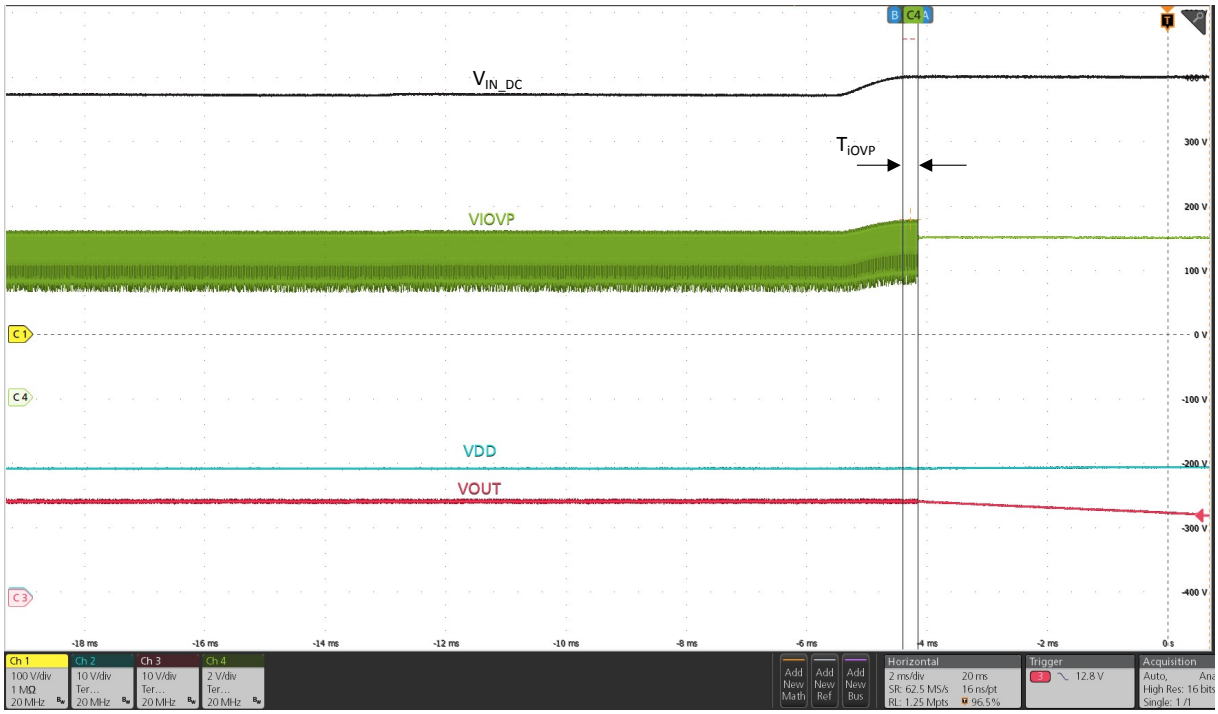


Figure 28. V_{IN} = 285 V_{AC}, input OVP steady-state

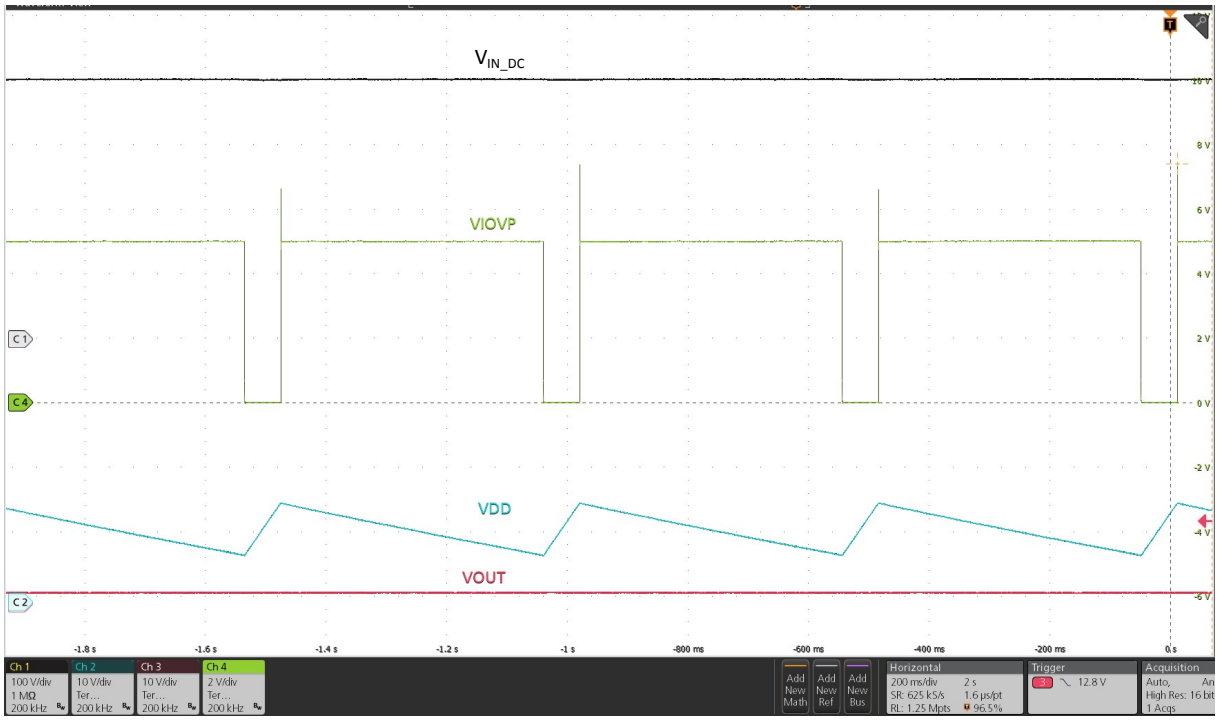
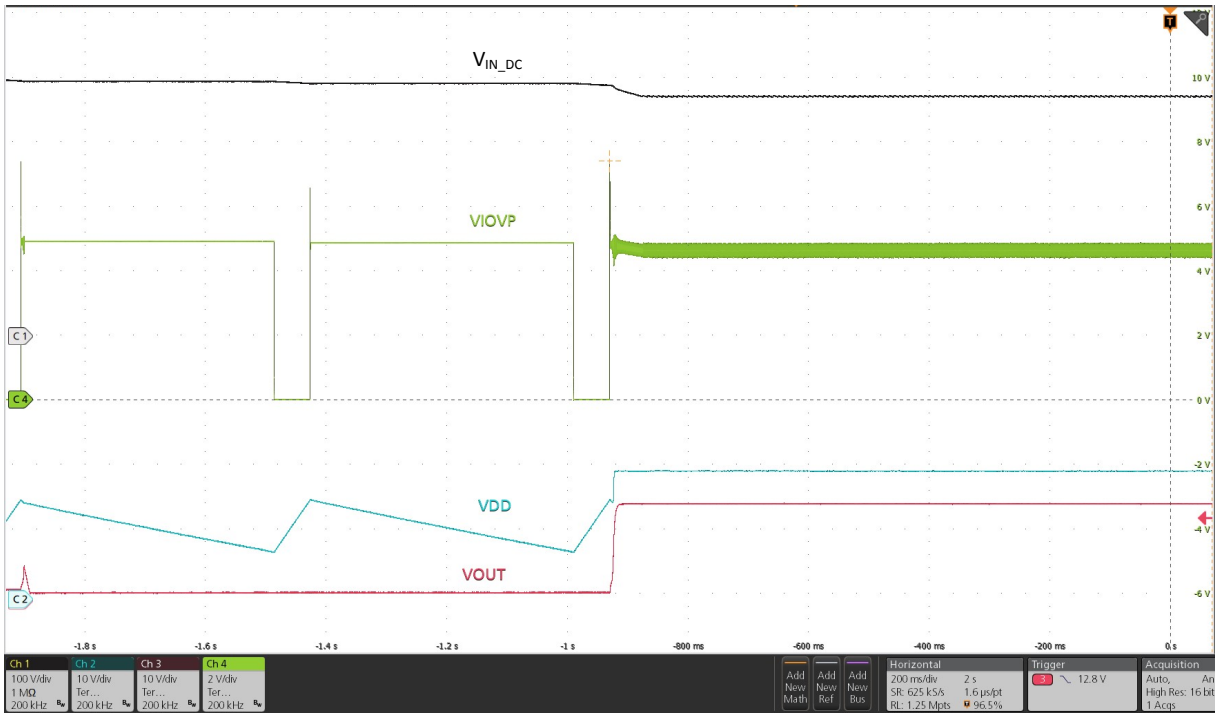
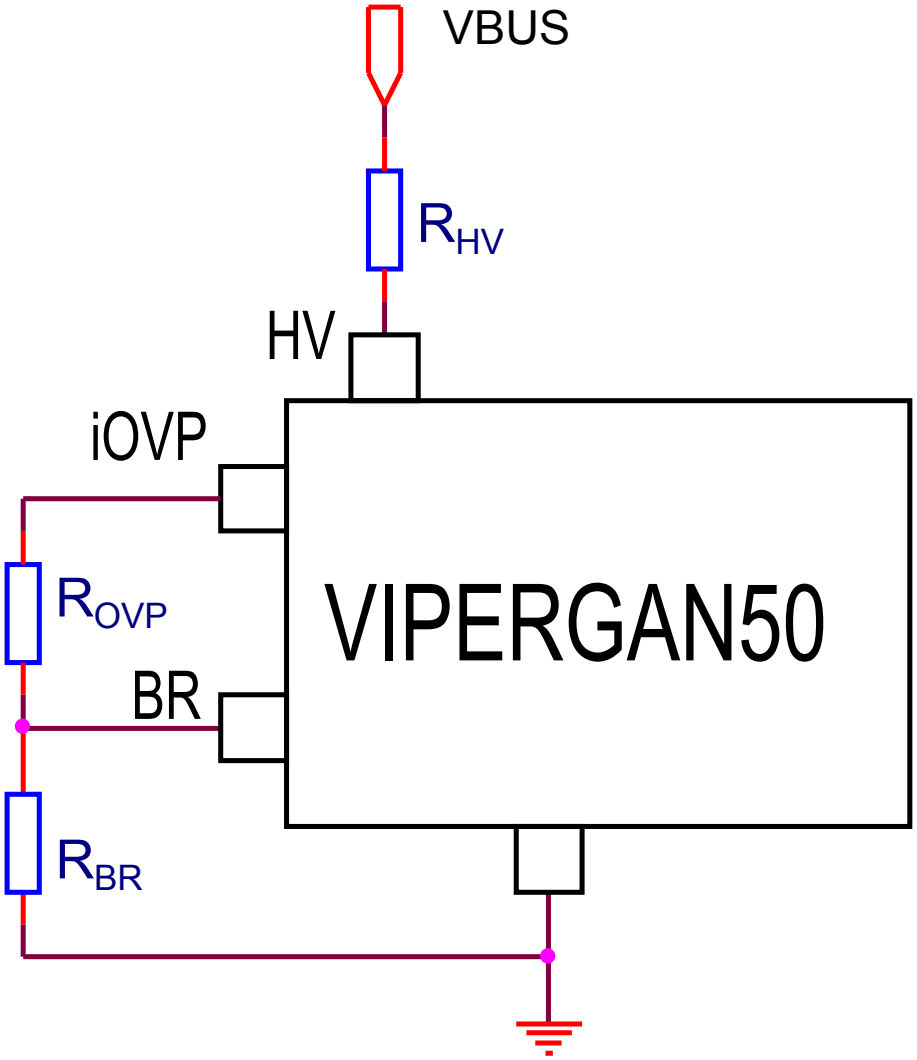


Figure 29. V_{IN} = 285 V_{AC} to 265 V_{AC}, input OVP removed and normal operation restored



To get minimal component count, the high-side resistor of the HV/iOVP voltage divider, R_{HV}, is also used for brown-in/brown-out protection setting, with the connection shown in the figure below.

Figure 30. **Input OVP, brown-in and brown-out setting**



The formulas to calculate R_{OVP} and R_{BR} taking both protections into account are given in equations 4 and 5. To disable input overvoltage protection, iOVP should be connected to GND.

6.6 Brown-out and brown-in

The minimum input voltage from which the converter starts operating (brown-in) and the minimum input voltage below which the converter stops operating (brown-out) are set through the voltage divider, which senses the rectified input voltage mains to BR.

In fact, if V_{BR} stays below the internal V_{BR-OUT} threshold (0.4 V typ.) for more than T_{BR-OUT} (30 ms, typ.), the VIPERGAN50 stops switching. If V_{BR} stays above the internal V_{BR-IN} threshold (0.5V typ.) for more than T_{BR-IN} (250 us, typ.), the VIPERGAN50 resumes switching.

The delay times are implemented through up/down counters, to reject temporary disturbances across the line. T_{BR-OUT} is also intended to avoid false protection triggering due to the input capacitor voltage ripple and to guarantee operations also in the case of some hold-up due to a missing cycle of the input line.

The resistors values are selected according to the equations below:

$$R_{OVP} = R_{HV} \cdot \left(\frac{V_{iOVP\_th}}{V_{IN\_OVP}} - \frac{V_{BR-IN}}{V_{IN\_ON}} \right) \quad (4)$$

$$R_{BR} = R_{HV} \cdot \frac{V_{BR-IN}}{V_{IN\_ON} - V_{BR-IN}} \quad (5)$$

where V_{IN_ON} and V_{IN_OVP} are the DC input voltages triggering brown-in and input overvoltage protection, respectively. The DC input voltage triggering brown-out, V_{IN_OFF}, is directly linked to V_{IN_ON} according to 6:

$$V_{IN\_OFF} = V_{IN\_ON} \cdot \frac{V_{BR-OUT}}{V_{BR-IN}} \quad (6)$$

The resistor R_{HV}, used to start up the converter and also as part of the iOVP and BR voltage divider, is arbitrary selected, with the recommendation to be few tens MΩ at least to minimize the residual consumptions from the input mains.

In this evaluation board, for voltage withstanding reasons, R_{HV} is realized through a series of three resistors (R46, R51, and R52), 3.3 Mohm each, resulting in a total of 9.9 Mohms.

Brown-in and input overvoltage specs inserted in 4 result in R_{OVP} = 82.5 Kohm (R47 of the BOM); input overvoltage spec inserted in 5 results in R_{BR} = 41.3 kohm (R48 of the BOM). From 6, $V_{IN\text{-}OFF}$ is calculated as 96 V_{DC}.

The commercial values R47 = 82 kohm and R48 = 43 kohm are selected, and the check on the bench, shown in the following figures, gives: V_{IN_ON} = 116 V_{DC}, V_{IN_OFF} = 93 V_{DC} and V_{IN_OVP} = 401 V_{DC}, quite in line with expectations.

Figure 31. V_{IN} = 127 V_{DC} to 92 V_{DC}, brown-out triggered and IC stop

Figure 32. V_{IN} = 127 V_{DC} to 92 V_{DC}, brown-out triggered and IC stop, T_{BR_OUT} detail

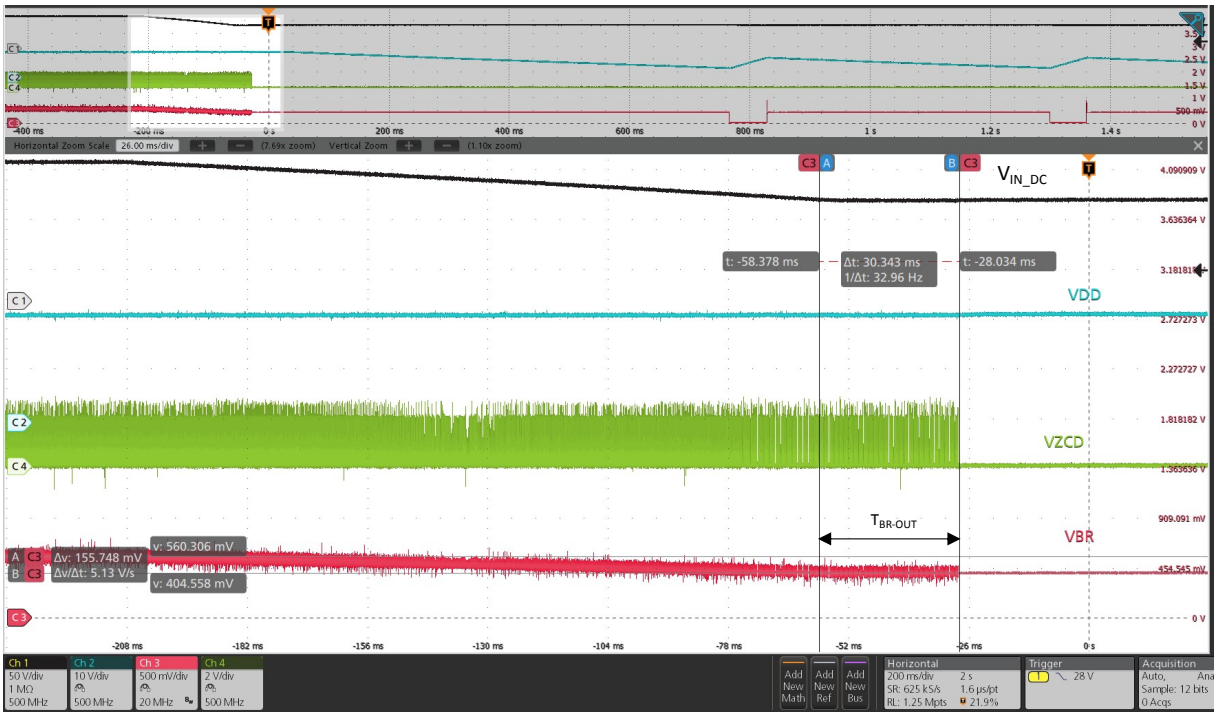


Figure 33. V_{IN} = 91 V_{DC} to 116 V_{DC}, brown-in triggered and IC restart

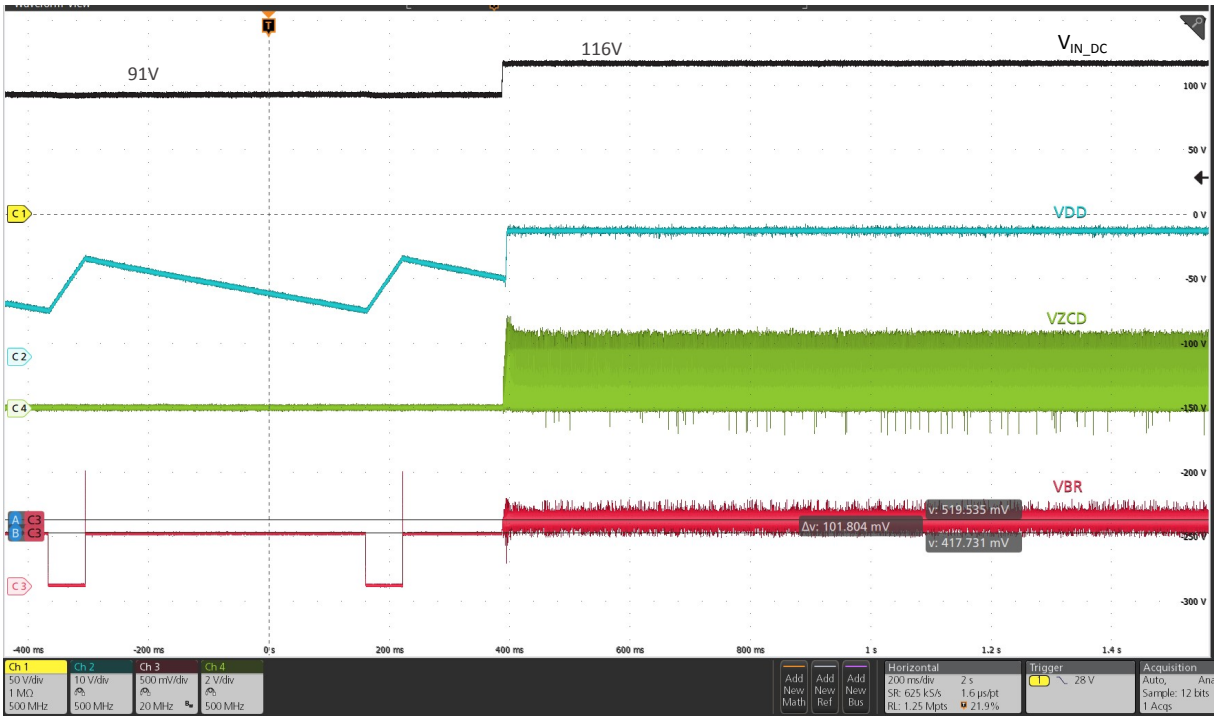
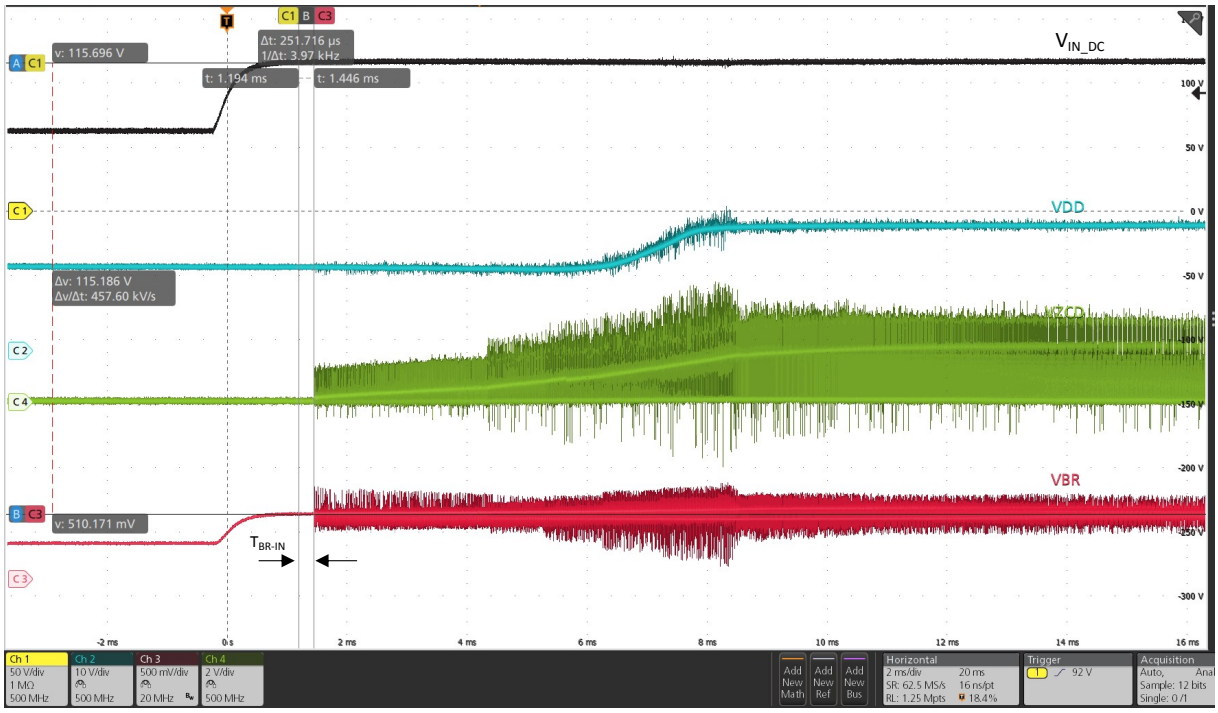


Figure 34. V_{IN} = 91 V_{DC} to 116 V_{DC}, brown-in triggered and IC restart, T_{BR-IN} detail



A 4.7 nF filter capacitor placed between BR and GND is necessary to avoid misbehavior of the brown-out logic when a high-voltage start-up unit is activated.

The power consumption of the input overvoltage/brown-in/brown-out network can be calculated as:

$$Pin_{(iOVP,BR\_IN/BR\_OUT)} = \frac{V_{IN}^2}{(R_{HV} + R_{OVP} + R_{BR})} \quad (7)$$

which results in about 10 mW consumption at 230 V_{AC} (~325 V_{DC}).

To disable brown-in/brown-out protection, BR should be connected to GND.

6.7 Output overvoltage protection

The voltage on the ZCD pin is monitored at the end of the transformer's demagnetization, when the auxiliary winding accurately tracks the converter output voltage, and compared with an internal reference. If the sampled voltage exceeds the internal OVP reference V_{OVP} (2.5 V typ.), an overvoltage condition is assumed, the switching is inhibited for $T_{RESTART}$ and V_{DD} is recycled between $V_{DD-RESTART}$, and V_{DD-ON} by the periodical activation of the HV current source.

The value of the low-side resistor of the ZCD voltage divider, R8, needed to activate the OVP protection at a certain output voltage level, V_{OUT_OVP}, can be found from the following formula:

$$R8 = \frac{V_{OVP}}{\frac{N_{AUX}}{N_{SEC}} \cdot (V_{OUT\_OVP} + V_{DSEC}) - V_{OVP}} \cdot \mathrm{R23} \quad (8)$$

where R23 is the high-side resistor of the ZCD voltage divider, already selected following feedforward considerations; V_{DSEC} is the forward voltage of the secondary rectifier.

In this evaluation board, V_{OUT} = 15 V, R23 = 75 kohm, and V_{OUT_OVP} has been set to 19 V, which gives a result of R8 = 5.2 kohm. The commercial value of 5.1 kohm has been selected, resulting in V_{OUT_OVP} = 19.5 V.

This is confirmed by the bench tests shown in the following figures, where the output overvoltage has been produced by shorting the low-side resistor of the output voltage divider, R5//R6, to the secondary ground.

After $T_{RESTART}$, switching is enabled at the first V_{DD} recharge to V_{DD-ON} and, since overvoltage is still present, the protection is invoked again in the same way; resulting in a low-frequency intermittent operation. If the short is removed, the IC resumes normal operation.

Figure 35. **OVP steady-state, $T_{RESTART}$**

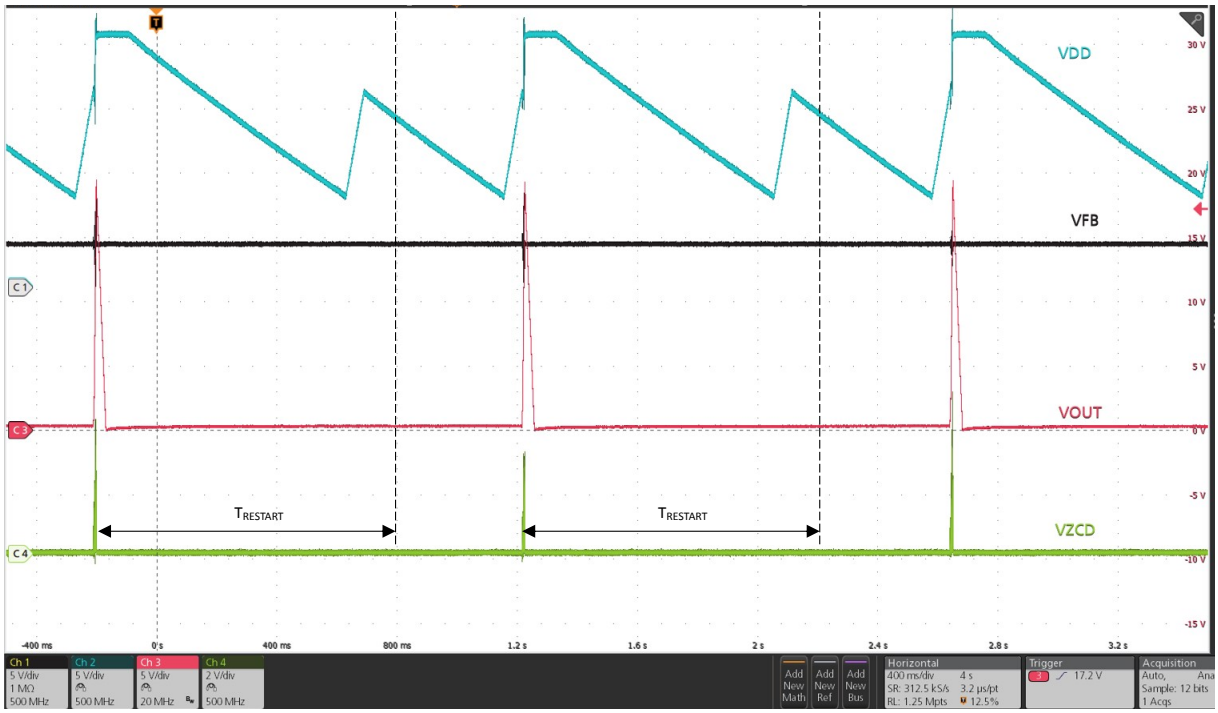
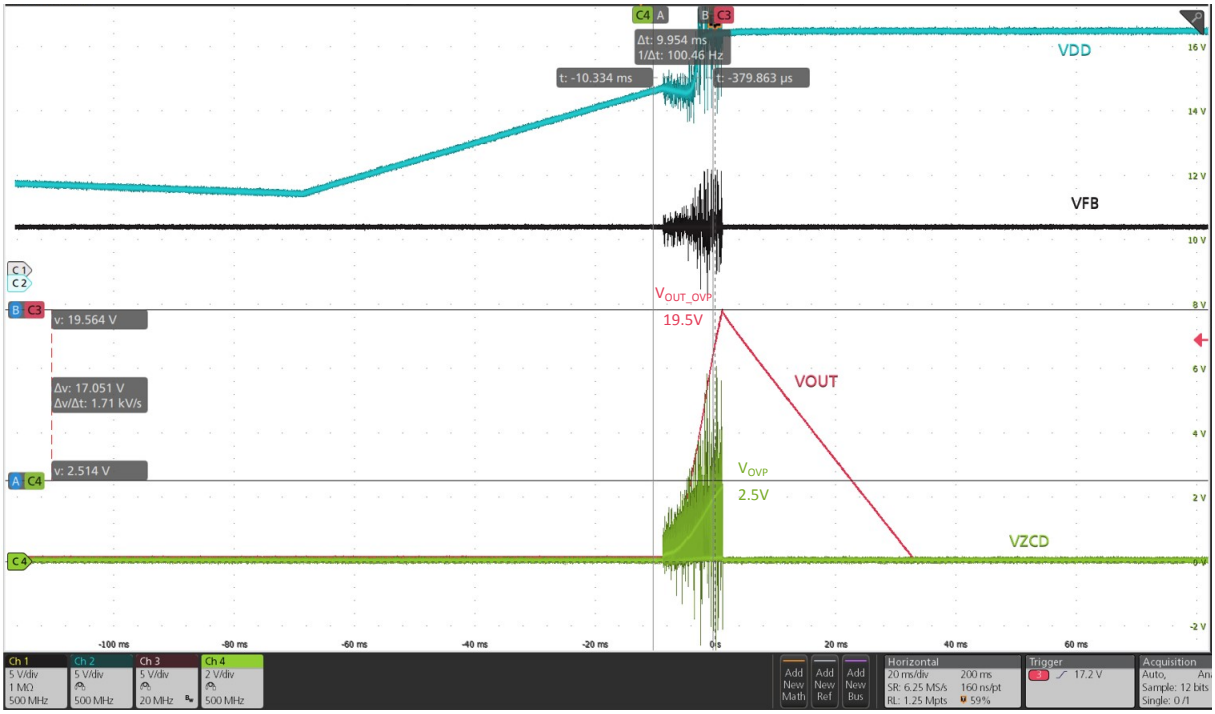
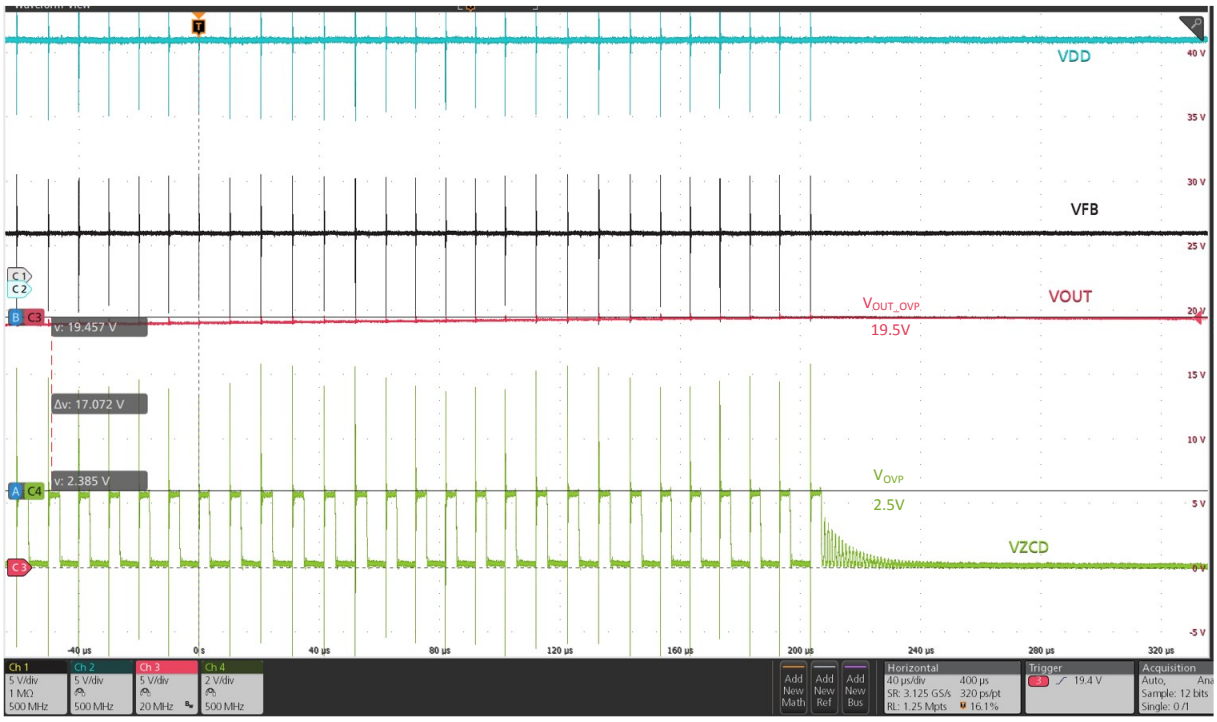


Figure 36. **OVP steady-state, V_{OUT_OVP}**



To reduce sensitivity to external noise and avoid false triggerings, the protection is activated if the OVP comparator is triggered for four consecutive oscillator cycles. A counter, which is reset every time the OVP comparator is not triggered in one oscillator cycle, is provided for this purpose.

Figure 37. **OVP steady-state, V_{ZCD}**



6.8 OCP LEB

When the secondary rectifier fails short, the transformer's inductance reduces to leakage inductance, and the current could reach dangerously high values in very short times. To avoid components damaging, if I_{DRAIN} exceeds I_{DLIM} within T_{ONmin} for two consecutive switching cycles, OCP LEB stops the switching of the IC for $T_{SD-REST}$ (2 sec, typ.). During fault condition, V_{DD} is maintained between V_{DD-ON} and $V_{DD-RESTART}$ by the periodical activation of the internal HV current source. At the end of $T_{SD-REST}$, the device has to wait for the first V_{DD-ON} crossing, then restarts. If the fault is still present, the protection occurs indefinitely in the same way, otherwise the IC resumes normal operation.

To test this protection, the secondary rectifier has been shorted, and an input voltage of 100 V_{AC} has been applied.

Figure 38. **OCP LEB @ 100 V_{AC}, T_{SD_REST}**

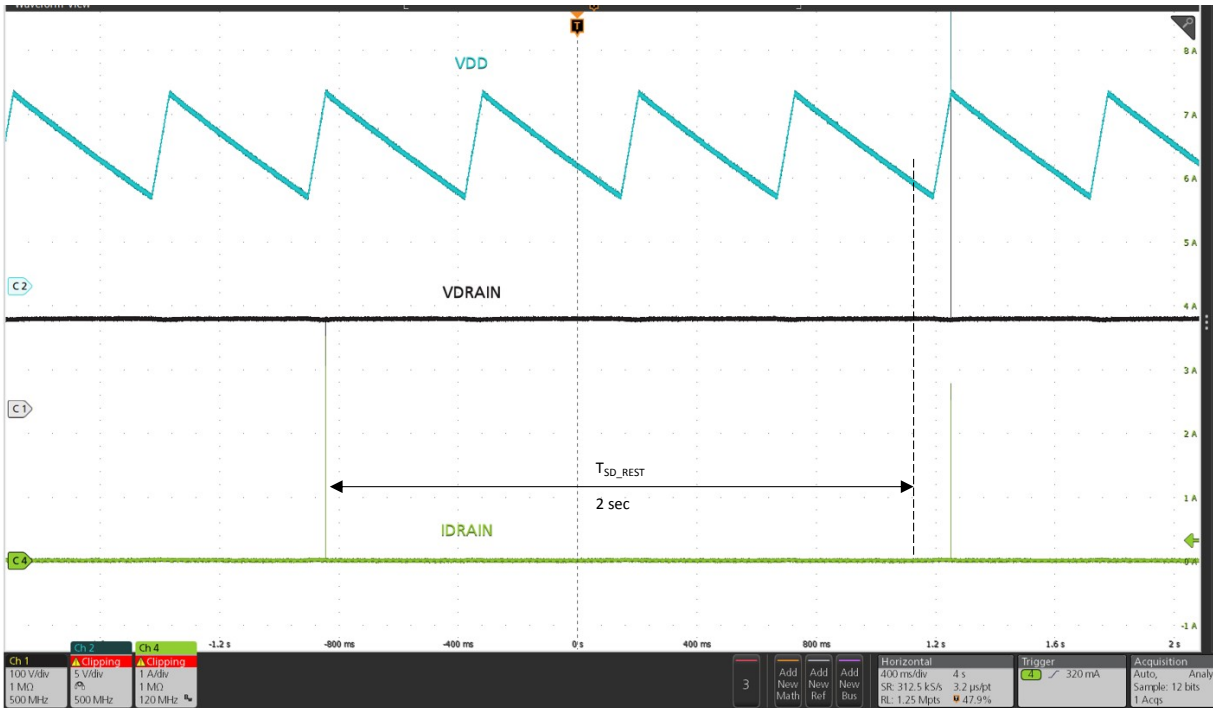


Figure 39. **OCP LEB @ 100 V_{AC}, 2 switching cycles for protection triggering**

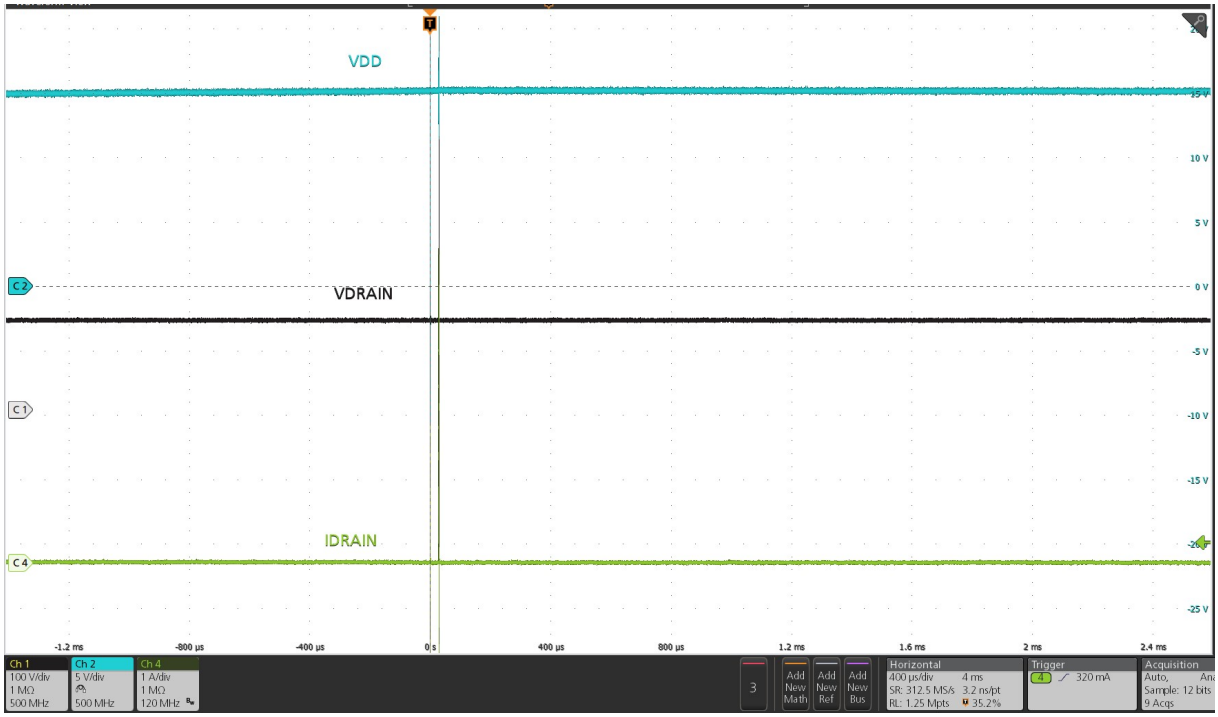


Figure 40. **OCP LEB @ 100 V_{AC}, 2 switching cycles for protection triggering**

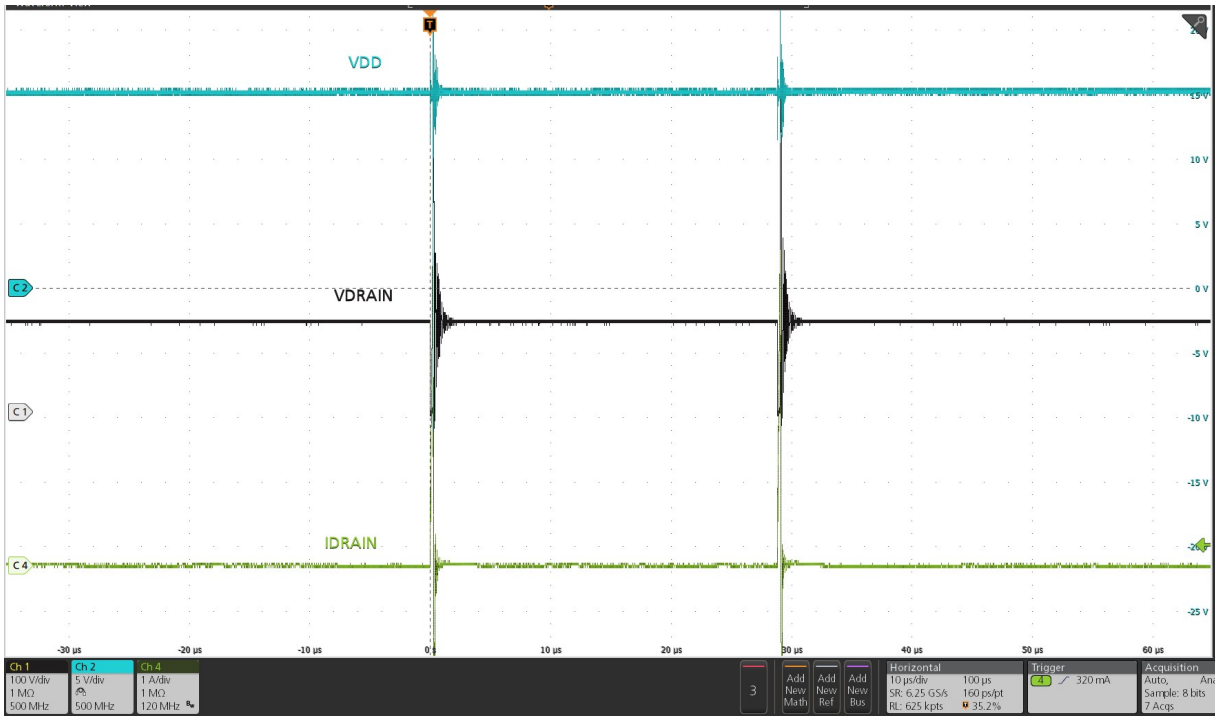
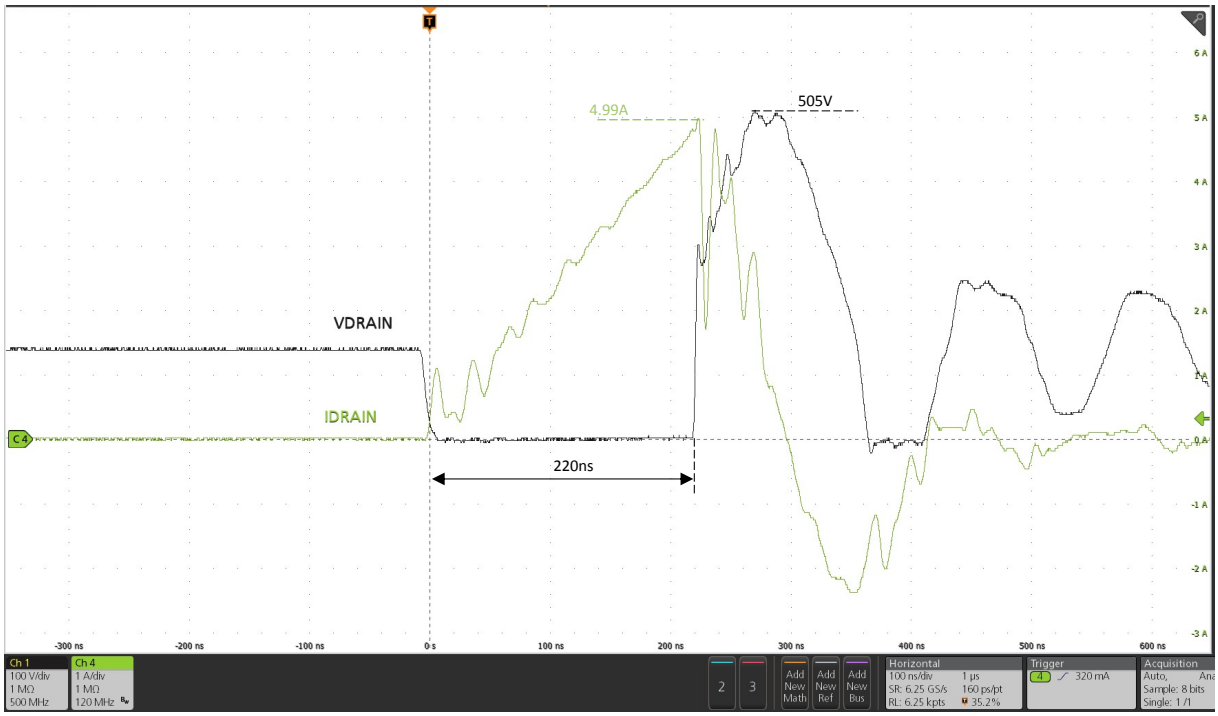


Figure 41. **OCP LEB @ 100 V_{AC}**



6.9 Overtemperature protection

When the controller temperature exceeds the shutdown threshold, T_{SD} (140 °C typ.) the device is shut down and maintained off for $T_{SD\text{-}REST}$ (2 sec. typ.) to prevent any dangerous overheating of the system.

During the fault, V_{DD} is continuously recycled between V_{DD-ON} and $V_{DD-RESTART}$ by the HV current source periodical activation to keep the controller alive (see OTP timing diagram in Figure 42), and the IC consumption is reduced to $I_{DD-FAULT}$ to further minimize the HV start-up losses.

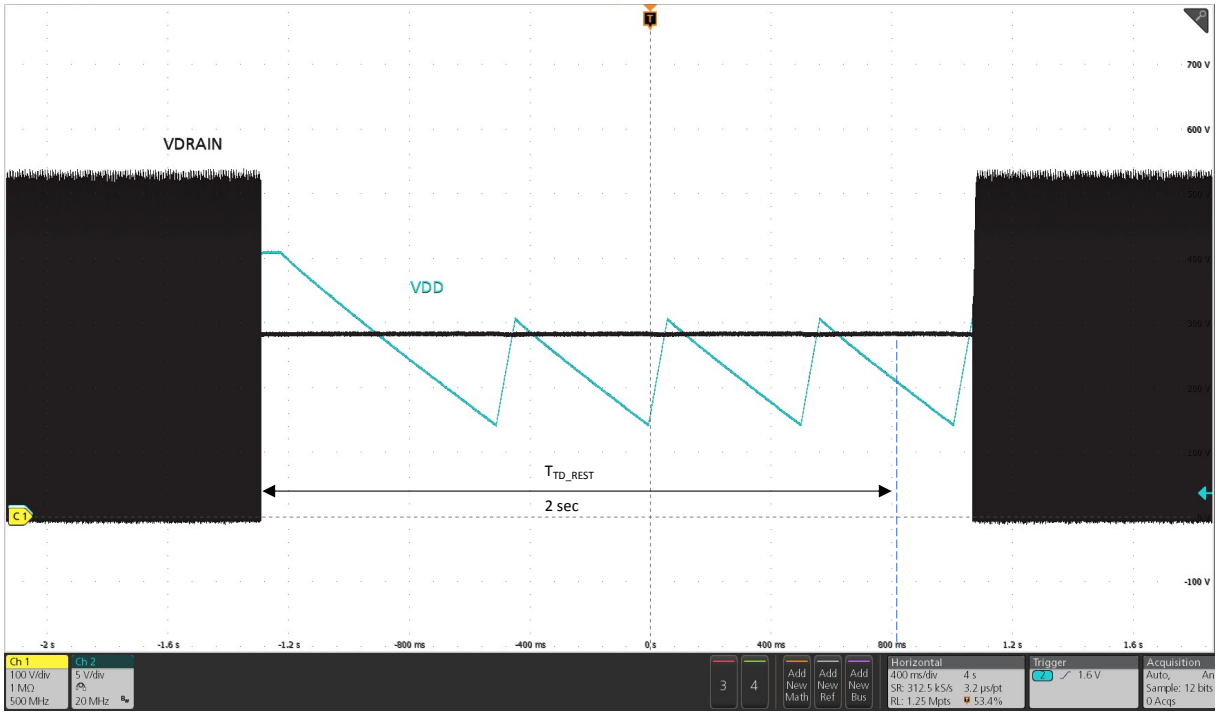
After $T_{SD-REST}$, the IC has to wait for the next V_{DD} recharge to V_{DD-ON}, then restarts. If a controller temperature higher than T_{SD} is measured, the protection occurs again in the same way, otherwise the IC resumes normal operation.

It is worth noting that, since the thermal sensor is embedded into the controller chip, the PowerGAN chip may have higher temperature.

The function has been tested soldering a 1 nF/630 V capacitor between DRAIN and GND in order to increase switching losses and junction temperature.

Protection has been tripped after a few minutes of operation at 180 V_{AC}/ 3.3 A.

Figure 42. Thermal shutdown protection and restart



6.10 Thermal measurements

A thermal analysis of the board at T_{AMB} = 30 °C has been performed at 90 V_{AC}, 115 V_{AC}, 230 V_{AC}, 265 V_{AC} mains input, full load condition using an IR image sensor. The results are shown in the following figures, where points 1, 2 and 3 indicate respectively: VIPERGAN50; snubber/transformer; output rectifier Q2.

HT is the highest temperature measured on the board in that operative condition.

Figure 43. Thermal measurement @ 90 V_{AC}, full load

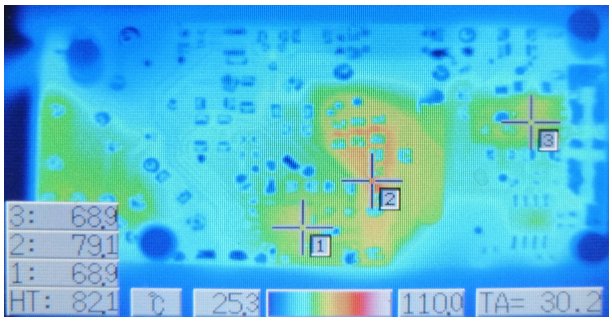


Figure 44. Thermal measurement @ 115 V_{AC}, full load

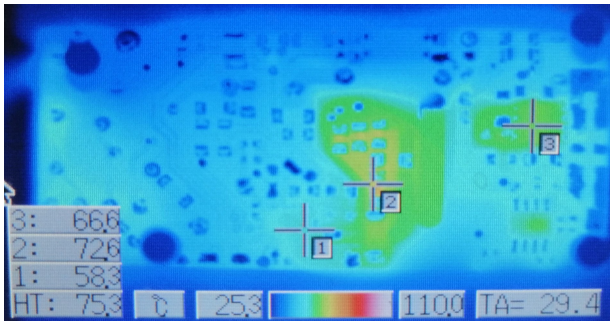


Figure 45. Thermal measurement @ 230 V_{AC}, full load

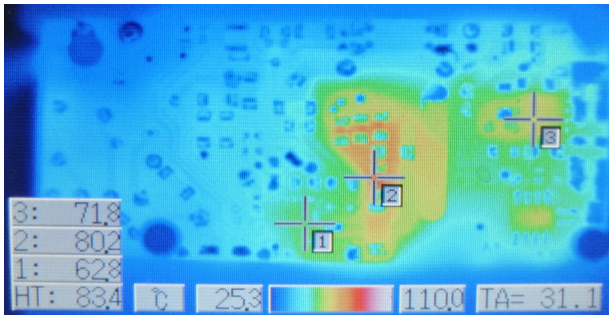
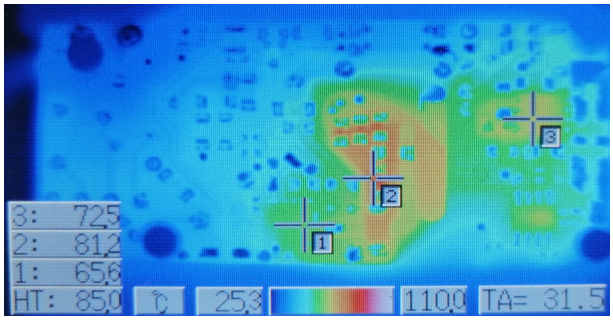


Figure 46. Thermal measurement @ 265 V_{AC}, full load



6.11 EMI measurements

A pre-compliance test to EN55022 (Class B) European normative with average detector has been performed using an EMC analyzer and an LISN. Results are reported in the figures below.

Figure 47. **Average measurements @ 115 V_{AC}, full load, T_{AMB} = 25 °C**

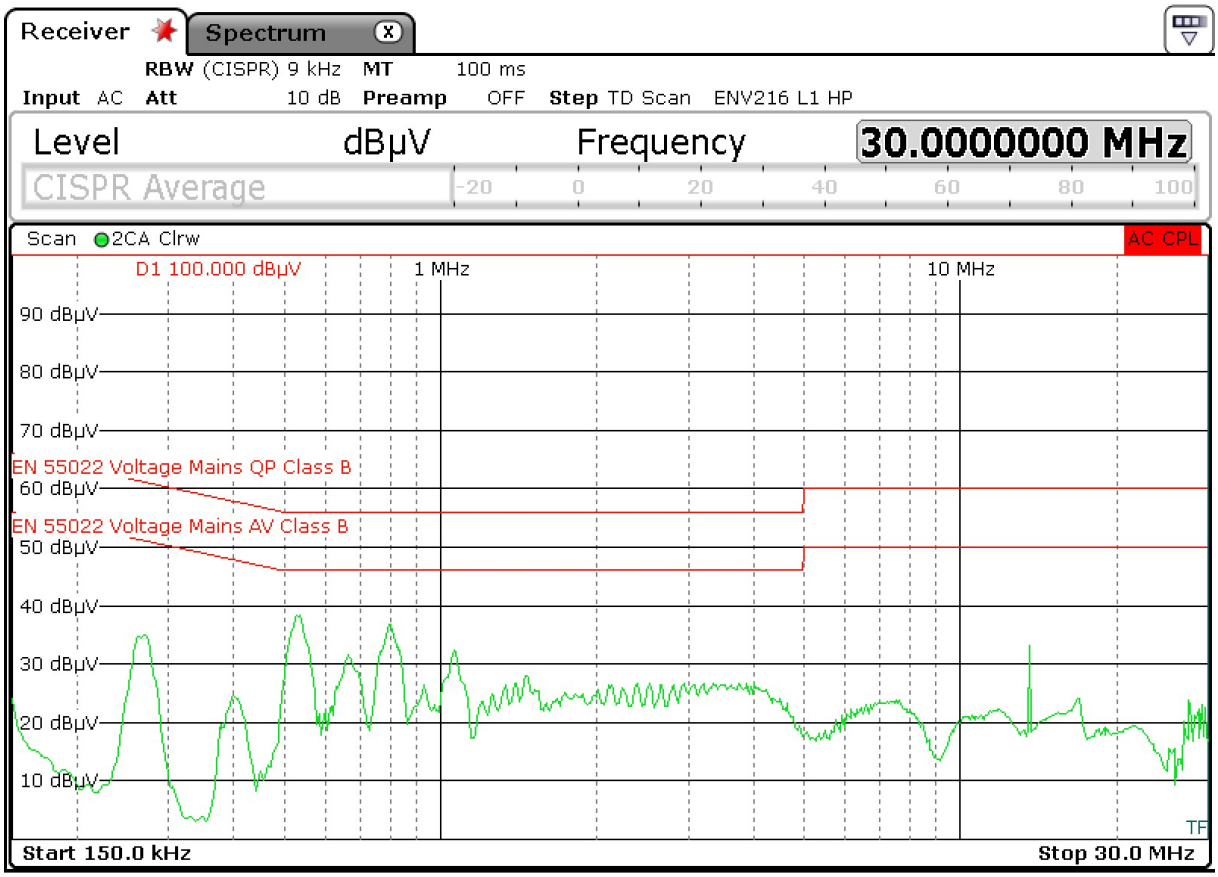
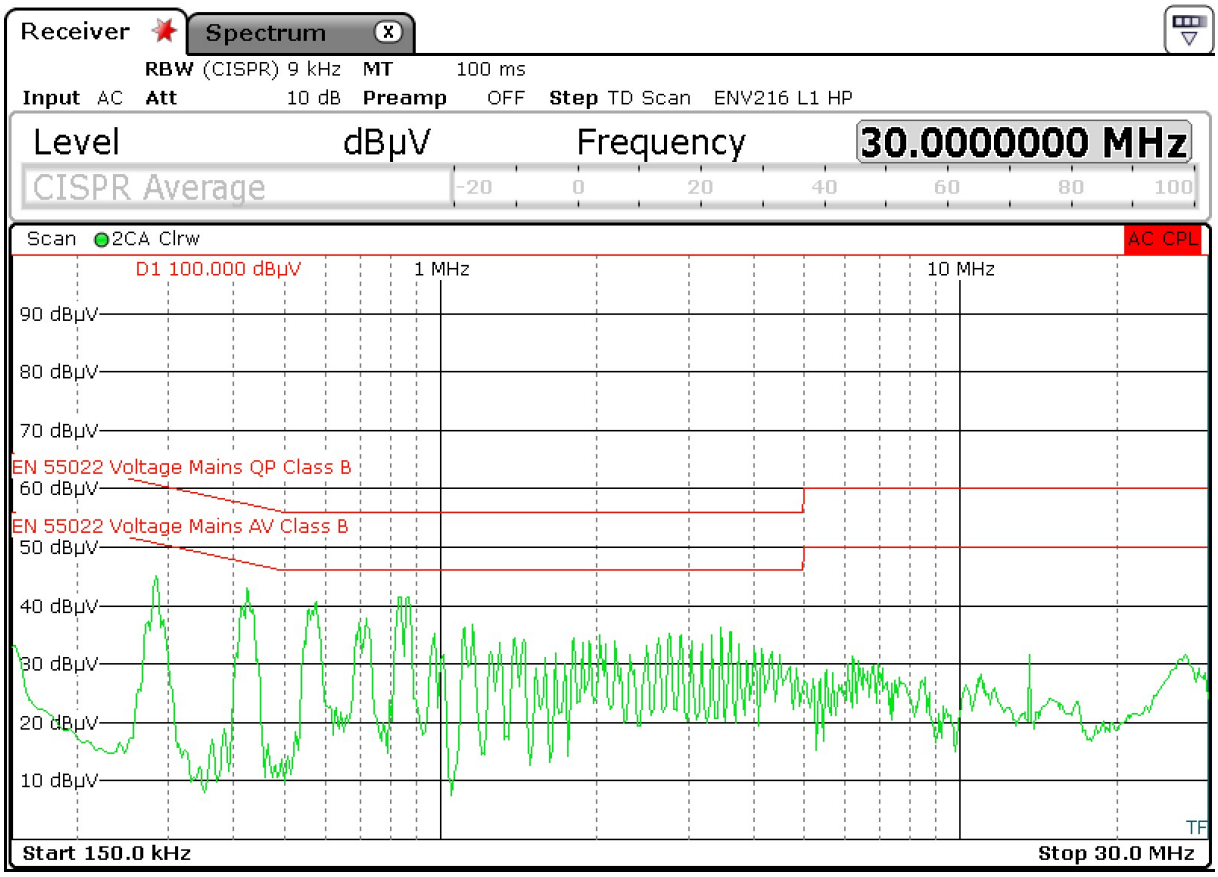


Figure 48. **Average measurements @ 230 V_{AC}, full load, T_{AMB} = 25 °C**



7 Board layout

Figure 49. **Mainboard layout**

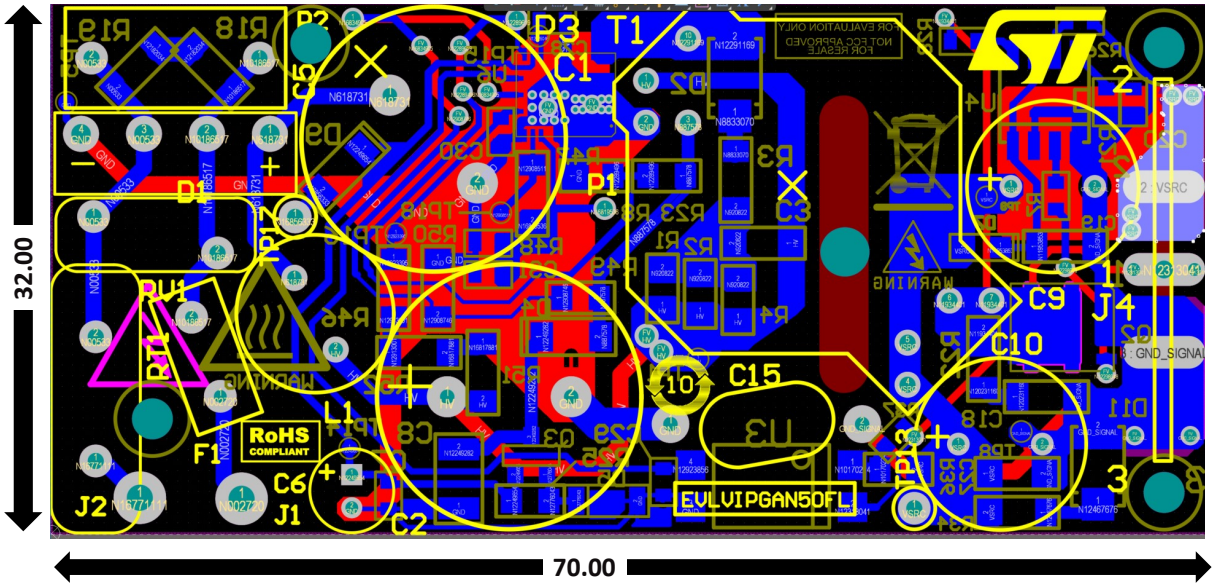


Figure 50. **Mainboard layout: top overlay, bottom overlay & bottom layer**

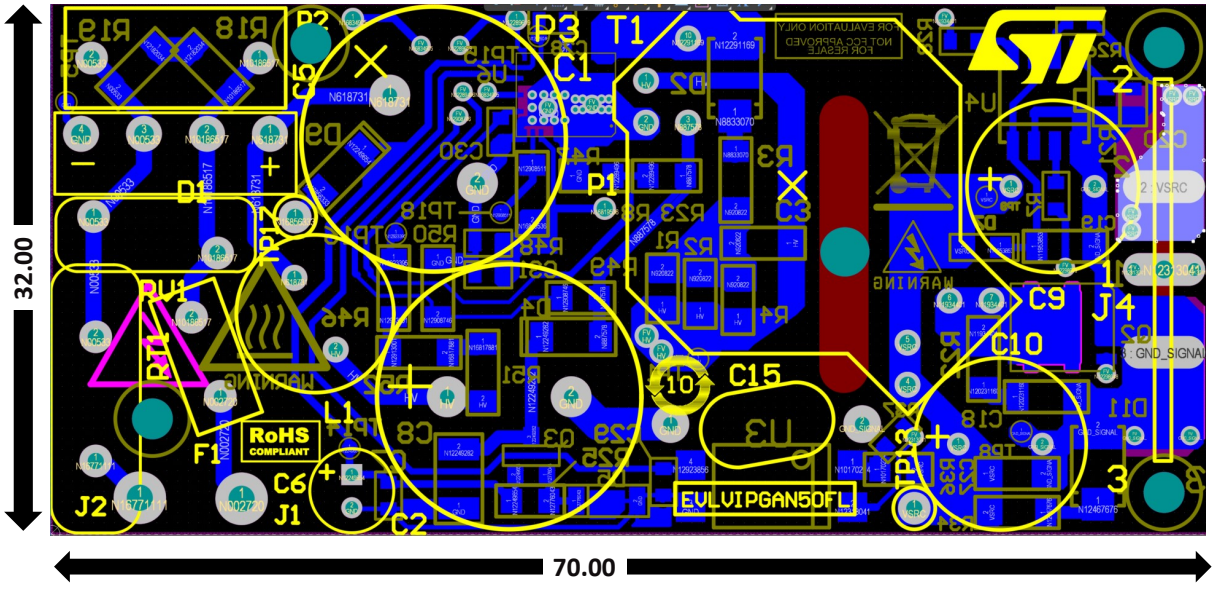


Figure 51. **Mainboard layout: top overlay, bottom overlay & top layer**

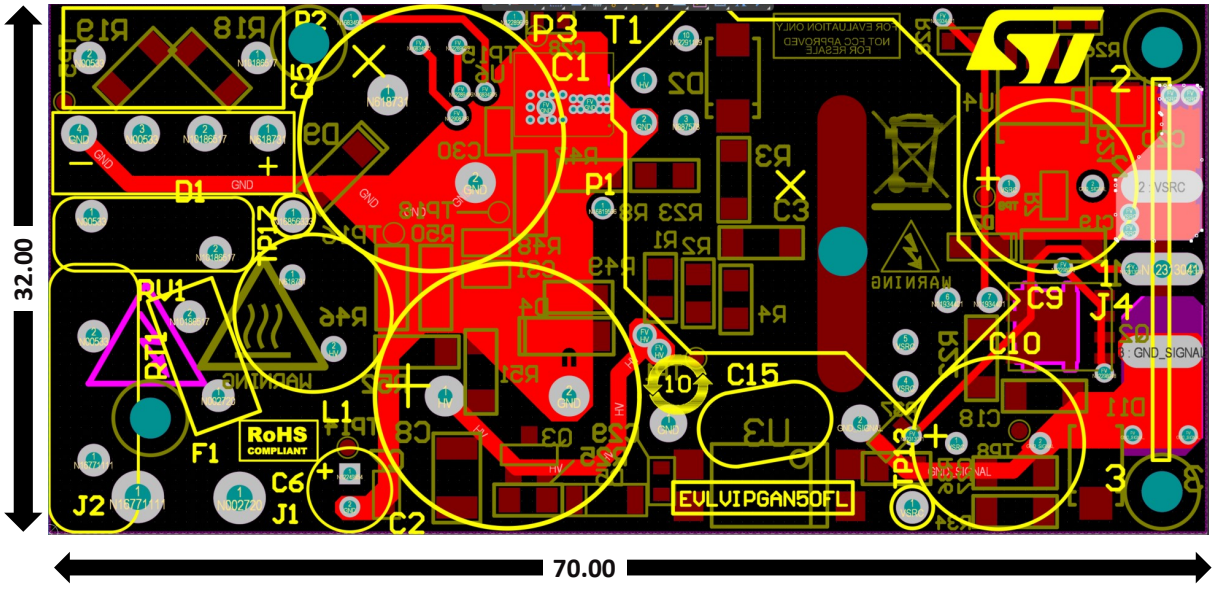


Figure 52. **Mainboard layout: bottom overlay & bottom solder**

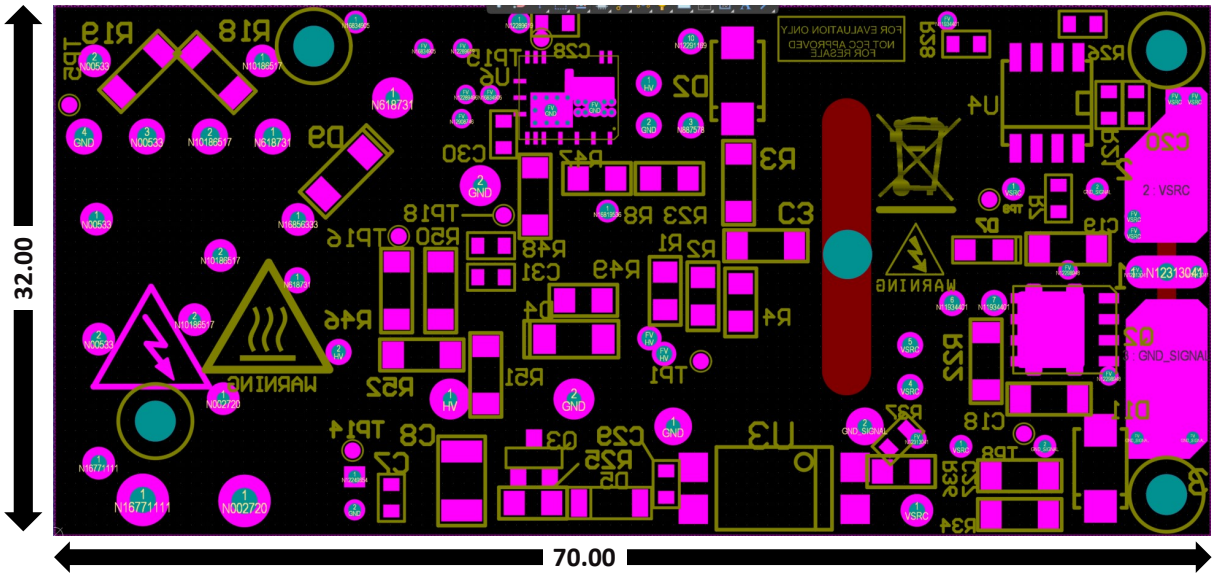
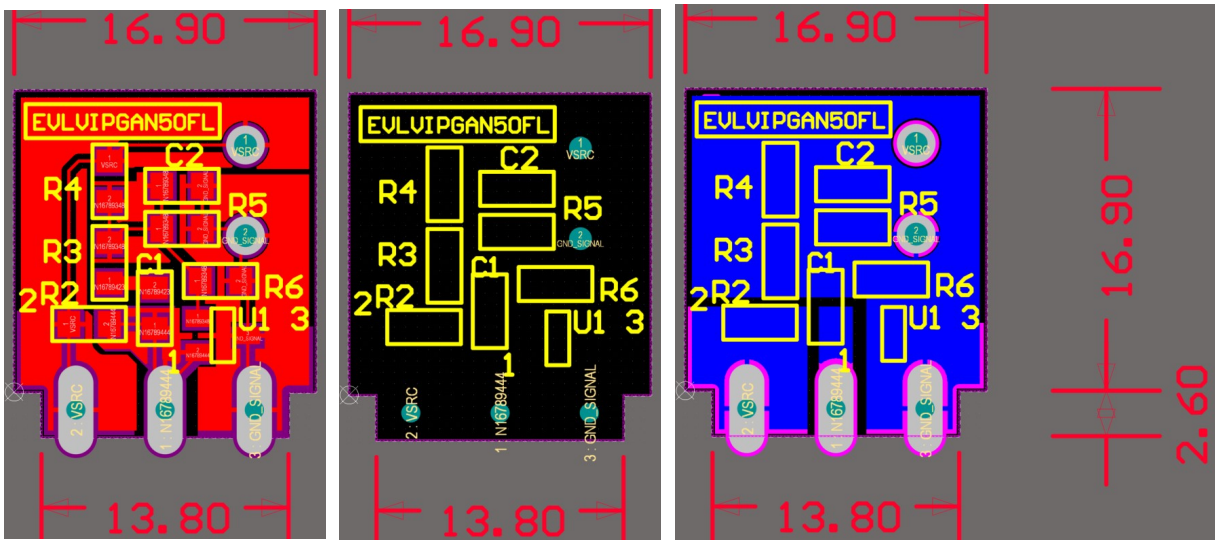


Figure 53. **Daughterboard layout: top layer, top overlay & bottom layer**



8 Conclusions

In this document the EVLVIPGAN50FL, a single-output 15 V/50 W evaluation board in flyback isolated topology, has been described and characterized, demonstrating that VIPERGAN50 allows designing an SMPS converter compliant with the most stringent energy regulations, in particular with average efficiency higher than 90% both at 115 V_{AC} and at 230 V_{AC} nominal input voltages.

9 10 References

VIPERGAN50 Datasheet (see www.st.com)

Appendix A

A.1 DCM flyback converter transfer function

In control theory terminology, the set PWM modulator + Power stage is usually referred to as “the plant”, and in the following, its transfer function (control-to-output) is indicated as $G_{vc}(s)$. In DCM, $G_{vc}(s)$ can be described by the approximate expression:

$$G_{vc}(s) \approx H_O \cdot \frac{1+\frac{s}{\omega_Z}}{1+\frac{s}{\omega_P}} \quad \text{(A1)}$$

Gain, poles and zero are defined below:

$$H_O = \frac{1}{H_{FB}} \cdot \sqrt{\frac{L_P \cdot f_{QR} \cdot R_O}{2}} \quad \text{(A2)}$$

$$\omega_Z = \frac{1}{R_C \cdot C_O} \quad \text{(A3)}$$

$$\omega_P = \frac{2}{R_O \cdot C_O} \quad \text{(A4)}$$

where:

H_{FB} = current sense gain (from VIPERGAN50 datasheet on www.st.com);

L_P = primary inductance of the flyback transformer;

f_{QR} = converter switching frequency (depends on the given input/output condition);

$R_0 = V_{OUT}/I_{OUT}$ = nominal output resistance;

C_0 = capacitance of the output capacitor;

R_C = ESR of the output capacitor.

A.2 Compensator design

A.2.1 Compensator transfer function

To compensate the DCM flyback a type-2 compensator is used, whose transfer function has the following expression:

$$G_C(s) = G_{C0} \cdot \frac{1+\frac{s}{\omega_{zc}}}{s \cdot \left(1+\frac{s}{\omega_{pc}}\right)} \quad \text{(A5)}$$

It provides the integrator effect to ensure the high DC gain to minimize the static error, and a pole-zero pair, to boost the phase according to the phase margin target.

The synthesis of the compensator is done using a manual pole-zero placement technique, in which the zero is placed in the vicinity of the power stage dominant pole to cancel its effect and the pole position is adjusted to achieve the required phase margin.

The below step-by-step procedure can be followed to design the compensator:

1. Select the phase margin Φ_m and crossover frequency f_C
2. Evaluate the gain and phase of the plant at crossover frequency:

$$G_{vc(f_C)} = |G_{vc}(2 \cdot \pi \cdot f_C)| \quad \text{(A6)}$$

$$\Phi_{vc(f_C)} = arg[G_{vc}(2 \cdot \pi \cdot f_C)] \quad \text{(A7)}$$

3. The compensated open-loop gain must attain the unit gain at f_C, with the required phase margin, so the compensator must be designed in order to have the following gain and phase at f_C:

$$G_{c(f_C)} = |G_c(2 \cdot \pi \cdot f_C)| = \frac{1}{G_{vc(f_C)}} \quad \text{(A8)}$$

$$\Phi_{c(f_C)} = arg[G_c(2 \cdot \pi \cdot f_C)] = 90 - 180 + \Phi_m - \Phi_{vc(f_C)} \quad \text{(A9)}$$

4. Cancel the pole of the plant, $f_P = \omega_P/(2\cdot\pi)$ by placing the zero of the compensator f_{zc}, in the neighborhood ($\alpha = 1$ to 5):

$$f_{zc} = \frac{\omega_{zc}}{2\cdot\pi} = \alpha \cdot f_P \tag{A10}$$

5. Place the pole of the compensator to boost the phase and to get the desired phase margin.

$$f_{pc} = \frac{f_C}{tan\left[tan^{-1}\left(\frac{f_C}{f_{zc}}\right) - \Phi_c(f_C)\right]} \tag{A11}$$

6. Calculate the gain G_{co}:

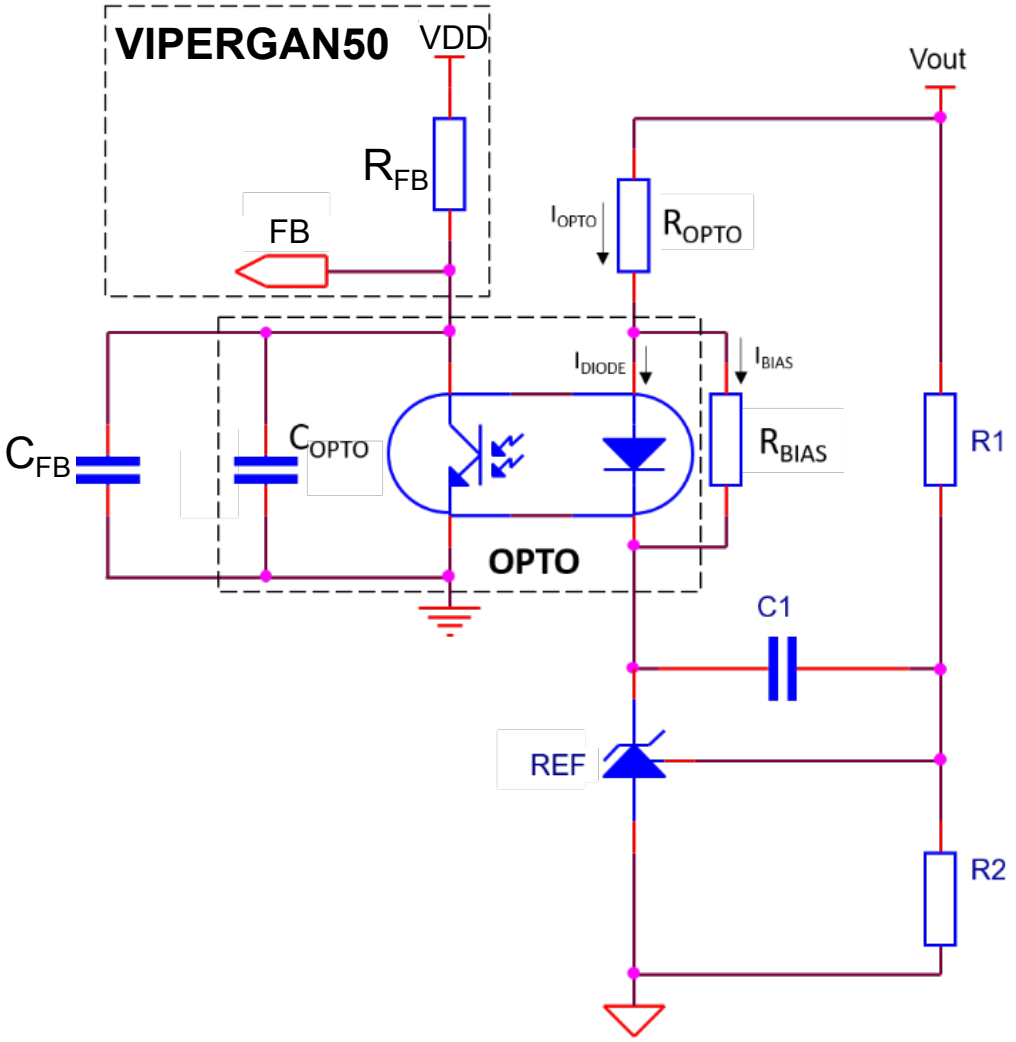
$$G_{co} = G_{c(f_C)} \cdot \frac{\omega_C \cdot \sqrt{1+\left(\frac{f_C}{f_{pc}}\right)^2}}{\sqrt{1+\left(\frac{f_C}{f_{zc}}\right)^2}} \tag{A12}$$

The synthesis of $G_C(s)$ is completed.

A.2.2 Compensator network implementation

In Figure 54 below the complete schematic arrangement for the type 2 error amplifier in secondary side regulation (SSR) is shown. The resistors R1 and R2 are used to define the output voltage setpoint. The resistor R_{OPTO} is used to bias the optocoupler, while the resistor R_{BIAS} is used to provide the minimum biasing current to the reference voltage, REF. The capacitors C1 and C_{COMP} are used for the compensation, even if the other components also play a role on the overall compensator transfer function.

Figure 54. **Secondary feedback implementation using secondary reference voltage and optocoupler**



With reference to the implementation of Figure 54, the transfer function of the compensator, presented in A5 can be detailed as below:

$$G_C(s) = \frac{CTR \cdot R_{FB}}{R_{OPTO} \cdot R1 \cdot C1} \cdot \frac{1 + s \cdot R1 \cdot C1}{s \cdot [1 + s \cdot R_{FB} \cdot (C_{FB} + C_{OPTO})]} \quad \text{(A13)}$$

In this equation, C_{OPTO} is the intrinsic capacitor of the optotransistor. Since this capacitor introduces a pole in the controller transfer function, limiting the frequency response, its value must be extracted through dedicated test bench on the selected optocoupler, as close as possible to the real operative conditions.

R_{FB} is the internal dynamic resistance of FB whose typical value, reported in VIPERGAN50 datasheet (see www.st.com), is 15 kohm.

Here below, the manual pole-zero placement procedure described in Section Appendix A.2.1 is applied to select each component of the compensator of Figure 54.

A.2.3 Compensator network calculation

First, the value of the resistor R_{BIAS} is calculated. The purpose of this resistor is to provide the minimum required bias current to the reference REF, to ensure correct operations. Considering that the forward voltage of the optodiode, V_F, is almost constant (typically ≈ 1 V), the value of R_{BIAS} is simply given by:

$$R_{BIAS} \leq \frac{V_F}{I_{BIAS}} \quad \text{(A14)}$$

where I_{BIAS} is the minimum cathode current for regulation of the reference (500 µA for TS3431).

Then, R1 value is selected: high enough to minimize the residual losses across the output, but low enough to ensure that the input current of the reference pin of REF is negligible compared with the current across R1. As a general rule, $I_{R1} \geq 50 \cdot I_{REF}$ can be set.

The resistor R2 is selected to define the output voltage set-point:

$$R2 = R1 \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}} \quad \text{(A15)}$$

where V_{REF} is the REF reference voltage (1.24 V for TS3431).

The value of the capacitor C1 is chosen in order to cancel the pole of the plant, according to A10:

$$C1 = \frac{1}{2 \cdot \pi \cdot R1 \cdot f_{zc}} \quad \text{(A16)}$$

The next step is the calculation of the resistor R_{OPTO}, whose value is carefully selected to ensure the minimum current through the optodiode to properly drive the FB pin with the current I_{FB}, ensuring the full dynamic of the pin.

If I_{OPTO} is the current flowing through R_{OPTO}, with reference to Figure 54, the current through the optodiode, I_{DIODE}, is given by:

$$I_{DIODE} = I_{OPTO} - I_{BIAS} = \frac{V_{OUT} - V_F - V_{REF}}{R_{OPTO}} - \frac{V_F}{R_{BIAS}} \quad \text{(A17)}$$

To ensure proper operation of the FB pin, the following condition must be verified:

$$I_{DIODE} \cdot CTR \geq I_{FB} \quad \text{(A18)}$$

Combining A17 and A18, the maximum value of R_{OPTO} can be immediately derived:

$$R_{OPTO} \leq \frac{V_{OUT} - V_F - V_{REF}}{\frac{I_{FB}}{CTR} + \frac{V_F}{R_{BIAS}}} \quad \text{(A19)}$$

The value of I_{FB} is the maximum source current provided by the pin (usually during burst mode condition) and is provided by the controller datasheet, whereas the value of CTR is achieved by characterization.

The final value of R_{OPTO} is selected to fulfill the compensator gain requirement:

$$R_{OPTO} = \frac{CTR \cdot R_{FB}}{R1 \cdot C1 \cdot G_{co}} \quad \text{(A20)}$$

provided that A19 is satisfied.

Finally, the value of C_{FB} is calculated from the compensator pole placing A11:

$$C_{FB} = \frac{1}{2 \cdot \pi \cdot f_{pc} \cdot R_{COMP\_DYN}} - C_{OPTO} \quad \text{(A21)}$$

In the table below, theoretical and commercial values, and the correspondence of each part with the evaluation board schematic components, are reported.

Table 6. Synthesis of the compensator

Part Figure 54	Part Figure 3 and Figure 4	Ref. equation	Theoretical value	Commercial value
R_{BIAS}	R37 Figure 4	$\leq \frac{V_F}{I_{BIAS}}$	15.4kΩ	15kΩ
R1	R4 Figure 5	$\frac{V_{OUT} - V_{REF}}{50 \cdot I_{REF}}$	306kΩ	270kΩ
R2	R5//R6 Figure 5	$R1 \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}}$	25kΩ	33kΩ//110kΩ
C1	C1 Figure 5	$\frac{1}{2 \cdot \pi \cdot R1 \cdot f_{Zc}}$	9.3nF	8.2nF

Part Figure 54	Part Figure 3 and Figure 4	Ref. equation	Theoretical value	Commercial value
R_{OPTO}	R36 Figure 5	$(CTR \cdot R_{FB})/(R1 \cdot C1 \cdot G_{CO})$	1.63kΩ	1.6kΩ
C_{FB}	C29 Figure 5	$\frac{1}{2 \cdot \pi \cdot f_{pc} \cdot R_{FB}} - C_{OPTO}$	1.08nF	1nF

The resulting crossover frequency f_C and phase margin Φ_m are:

f_C ~ 1.6 kHz

Φ_m ~ 76°

Revision history

Table 7. **Document revision history**

Date	Version	Changes
07-Nov-2022	1	Initial release.
19-Jun-2024	2	Updated Figure 3 and Figure 4.

Contents

List of tables

List of figures