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AN5858

Application note

The below-ground phenomenon in power applications

Introduction

One of the most critical issues affecting gate drivers in the past is the below-ground (or negative transient) phenomenon. It is the negative spike voltage on the half-bridge output that often occurs in power applications, especially when space or mechanical constraints do not allow an optimized PCB layout. The below-ground spike can lead to unwanted phenomena such as overcharging of the bootstrap capacitor and incorrect operation of the output stage when devices with insufficient ruggedness are used.

Recent technology and design solutions adopted by ST can overcome or mitigate the below-ground effects on final applications.

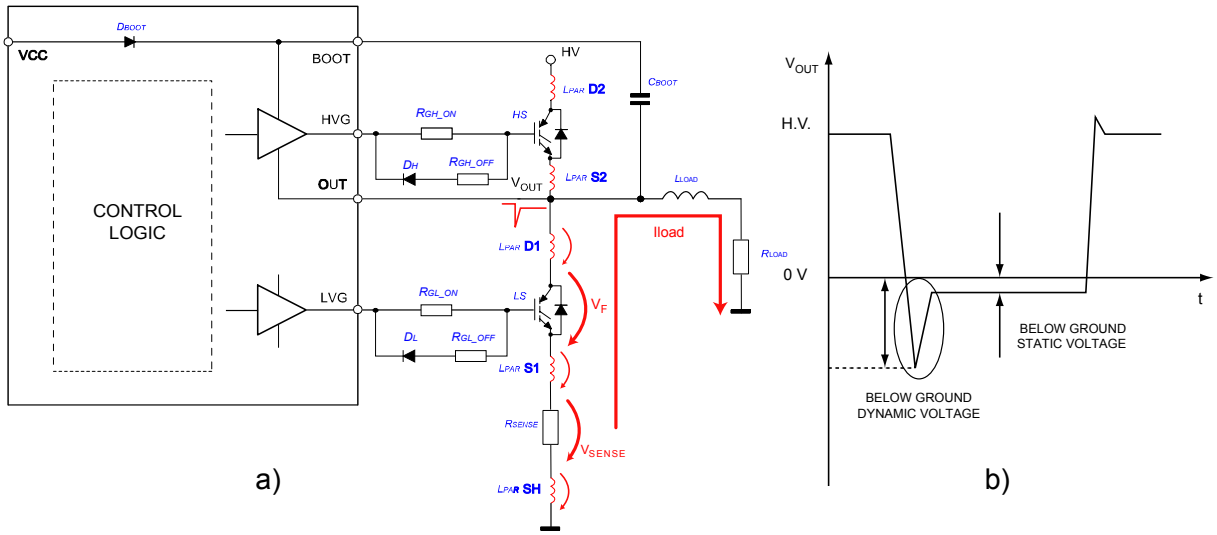
1 Below-ground phenomenon

In half-bridge topologies, especially when driving highly inductive loads, the output of the power half-bridge can experience a negative voltage, with an initial dynamic spike followed by a static component (Figure 1 b). This phenomenon occurs when the bridge makes a hard switching transition towards the low voltage level and the load current is outgoing (from the bridge to the load). When the high-side switch turns off, the inductive component of the load tries to keep the output current constant. The output voltage drops and, when it reaches the 'ground' value, the current starts flowing through the low-side freewheeling diode, which gets forward biased.

The main contributors to dynamic below-ground voltage are the spikes due to the high dI/dt experienced by the PCB parasitic inductances in series with the free-wheeling diode located along the low-side current path of the half-bridge. Other contributors are the forward peak voltage of the low-side freewheeling diode (V_{FP}), which passes from a high voltage reverse condition to a forward condition in a short time, and that of the parasitic inductance of the shunt (or sense) resistors.

The static below-ground is mainly due to the voltage drop on the sense resistor (if present) and the forward voltage of the free-wheeling diode.

Figure 1. Below-ground phenomenon



The following equation describes the below-ground:

$$V_{OUT} = -[(R_{SENSE} + R_{TRACE}) * I_{LOAD} + V_F] - \left(V_{FP} + L_p * \frac{dI_{LOAD}}{dt}\right) \quad (1)$$

Where:

- R_{SENSE} = sense resistance value
- R_{TRACE} = PCB trace resistance of the current path
- I_{LOAD} = load current
- V_F = forward voltage drop of the power switch body diode
- V_{FP} = forward peak voltage of the power switch body diode
- L_p = L_{PAR} (SH + S1 + D1) = parasitic inductance of PCB trace and transistor die bonding along current path.

The first term of Eq. (1) is the static part of the below-ground:

$$(R_{SENSE} + R_{TRACE}) * I_{LOAD} + V_F \quad (2)$$

The second term of Eq. (1) describes the dynamic component:

$$V_{FP} + L_p * \frac{dI_{LOAD}}{dt} \quad (3)$$

1.1 Below-ground static voltage

The below-ground static voltage is essentially due to the current recirculating through the sense resistor and the body diode of the power switch, as represented by Eq. (2). It is usually of small entity (up to a few volts) and does not represent a concern for most of the circuits based on MOSFETs or IGBTs.

For GaN based designs static below-ground might lead to an overcharge of the bootstrap capacitor due to these factors:

- owing to small gate charge, bootstrap capacitance is typically small
- static below-ground is big in GaN due to reverse conduction.

Therefore in GaN designs the below-ground static voltage can lead to exceed the gate source maximum rating (for instance a typical GaN can have a gate drive voltage of 5 to 6.5 V with a maximum rating of +7 V and +10 V transient).

Figure 2. Typical bootstrap capacitor charging mechanism

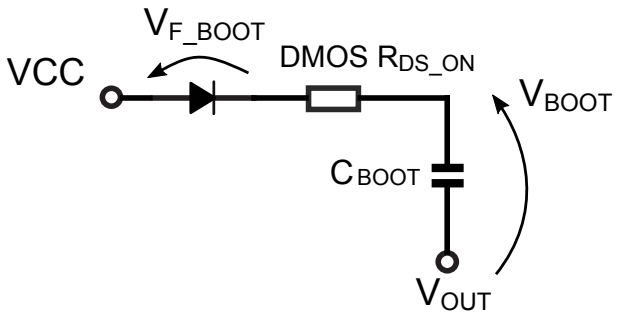


Figure 2 illustrates how the bootstrap capacitor voltage can exceed the V_{CC} value due to static below-ground when V_{OUT} falls below-ground for enough time, according to the equation below:

$$V_{BOOT} \cong V_{CC} - V_{OUT} = V_{CC} + (R_{SENSE} + R_{TRACE})^{*}I_{LOAD} + V_F \quad (4)$$

where the drop on the bootstrap diode is neglected.

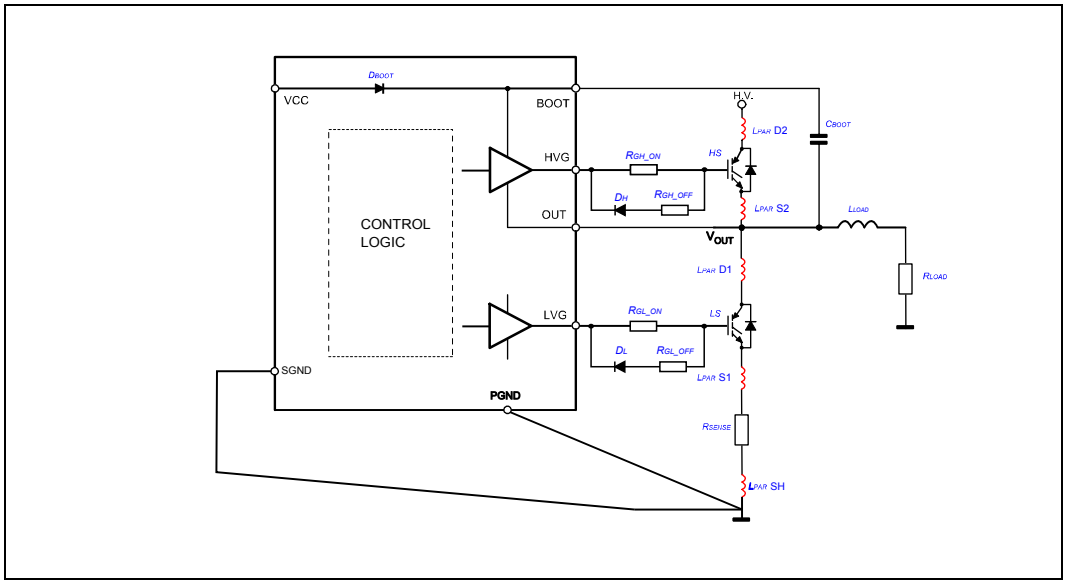
Therefore, to keep V_{BOOT} within its absolute maximum rating, we must choose an appropriately low value for R_{SENSE} and minimize trace resistance by designing large and short tracks for the load current.

Another option to maintain a safe value for the bootstrap capacitor voltage is to insert a Zener diode in parallel with the capacitor.

1.2 Below-ground dynamic voltage

The dynamic component of the below-ground is an undershoot spike caused by the parasitic inductances in the tracks between the OUT node and ground, indicated in the following figure as ParD1 and ParS1, respectively.

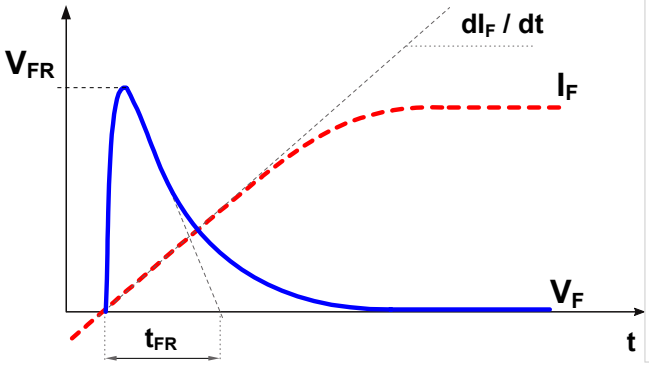
Figure 3. Parasitic inductances in PCB traces

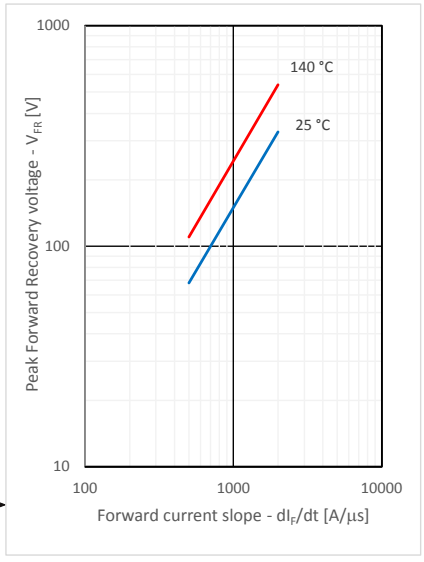


As defined by Eq. (3), the undershoot depends on three major contributors:

- The forward peak voltage of the diode, that depends on the dI/dt current and on the diode technology. The higher the dI/dt, the higher the peak forward voltage across the diode.

Figure 4. Peak forward recovery voltage of diode vs dI/dt





- The parasitic inductance of the traces along the current path, which is related to trace length and width
- The rate of change of the current flowing in the low side body diode when the high side switch turns off. This in turn depends on how fast the high side turn-off is, which is inversely proportional to the off-resistance value.

1.3 Below-ground when current enters the half bridge

There is another condition in which the output of the half bridge can experience a below-ground situation. It occurs when the low side switch turns on (hard switching) while the load current is circulating into the high side body diode.

In this situation, the diode recovery current is added to the load current and both terms contribute to the current flowing in the switch. When the recovery process is about to end, the current contribution from the high-side diode tends to decrease and a voltage drop builds up on parasitic inductances of PCB traces, generating a below-ground on the output (an example is shown in Figure 5 where a parasitic inductance of 190 nH has been inserted on the low side collector). Also in this case, the amount of below-ground depends on both the parasitic inductance entity and the recovery current decrease rate.

In any case, the entity of the negative transient when current enters the half bridge is always smaller than that of the outgoing current described above.

Figure 5. Below-ground measurement with current entering half bridge

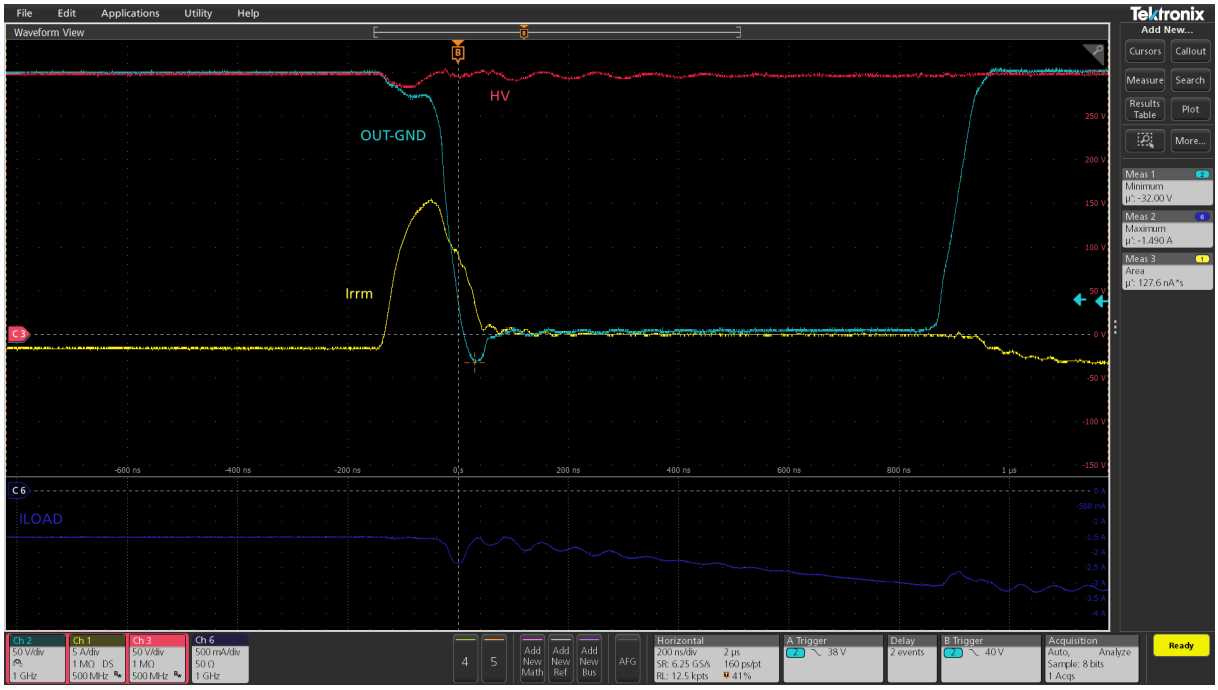
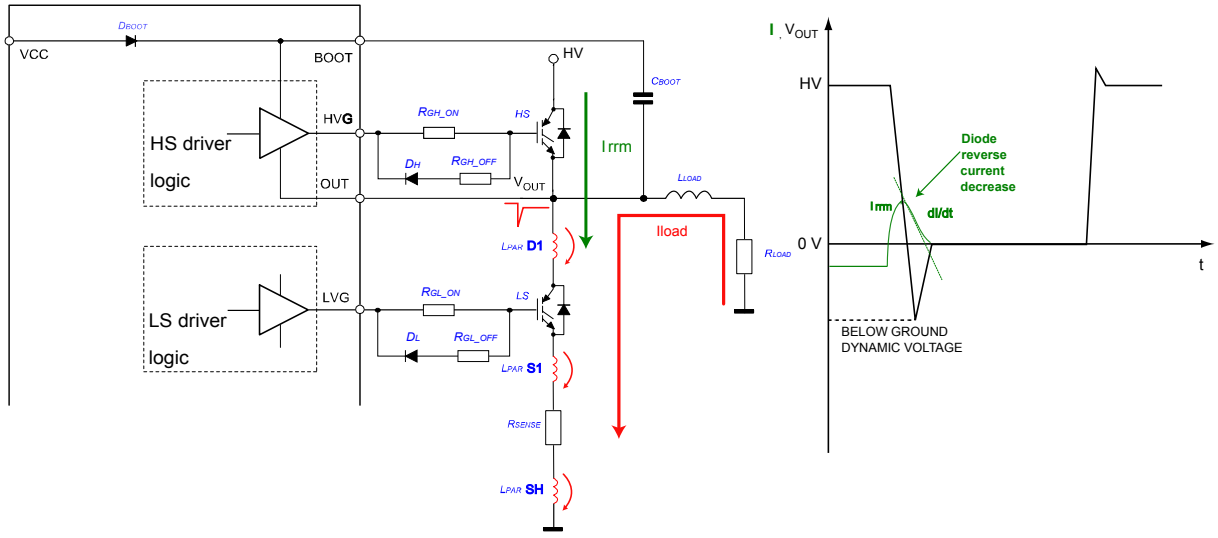


Figure 6 shows the dynamic drop that builds up in parasitic inductances as the diode current decreases.

Figure 6. Below-ground phenomenon when current enters half-bridge



2 How to measure below-ground

To correctly measure the below-ground, it is important to place the probe ground as close as possible to the ground pin of the device and the tip as close as possible to the output pin of the device. The ground loop area of the probe must be reduced so to minimize noise due to coupled magnetic fields and inductance.

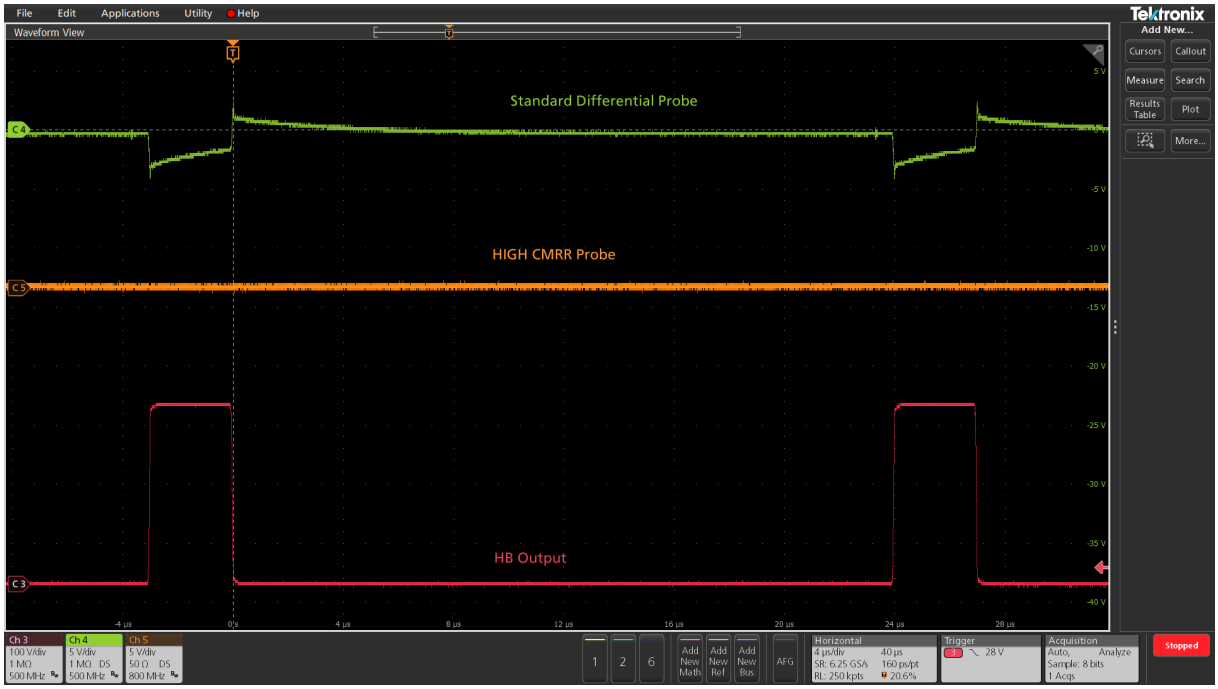
Figure 7. Below-ground measurement techniques

To perform measurements as accurately as possible, first make sure that probes are calibrated to the front end of your oscilloscope and then ensure the horizontal scale and resolution of the oscilloscope are set appropriately.

If you have to measure high-side Gate-Source voltage or the voltage across bootstrap capacitor, consider the use of high impedance probes to avoid discharge of bootstrap capacitor.

In case of differential measurements involving high-side nodes, such as the Gate-Source voltage of a MOSFET, pay attention to use high CMRR differential probes. Not following this indication can lead to artifacts as visible in Figure 8.

Figure 8. Different behavior of differential probes with short-circuited tips set on the half bridge output

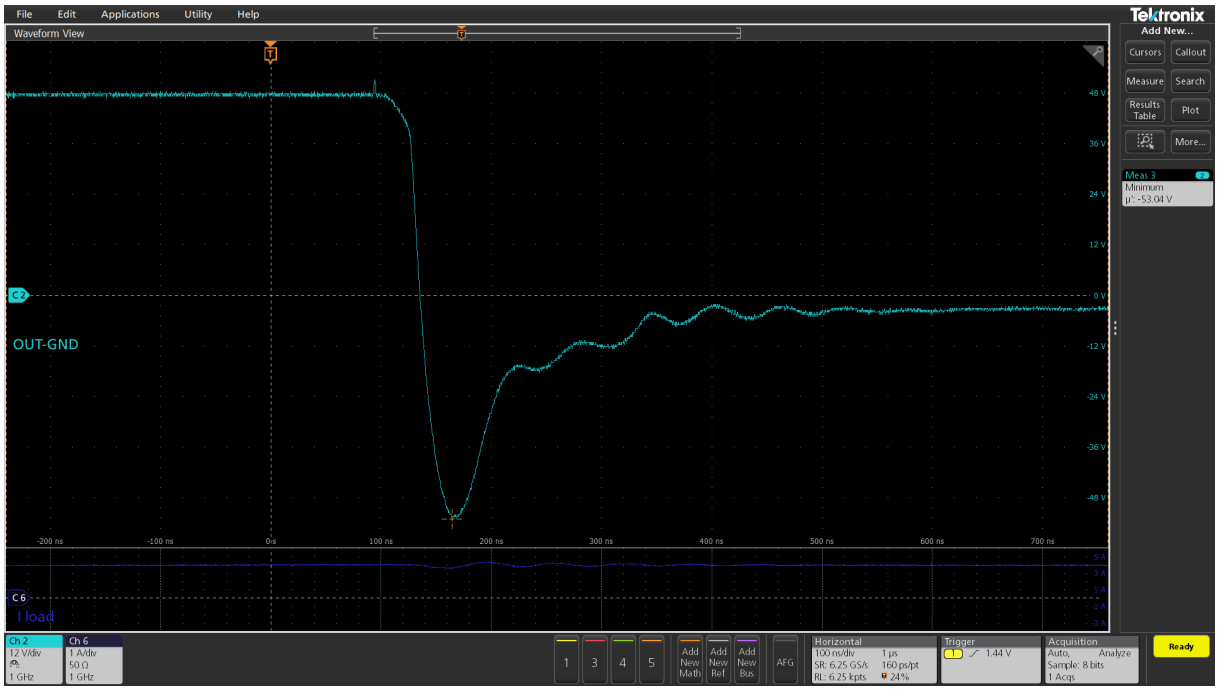


The horizontal scale should be set to include the waveforms of interest; the half-bridge output and boot node in case of below-ground, and, if needed, additional signals that can be observed in case of below-ground side-effects are expected (such as the driver high-side output node).

The resolution of the acquisition for below-ground events should be at least 1 ns/point to avoid under sampling and lose the real minimum value of the below-ground. The resolution should generally be the maximum available according to the horizontal scale set.

The vertical scale should be set to include the whole output (or boot) signal inside the screen to avoid saturation of the front-end logic of the oscilloscope, as shown in the following Figure 9.

Figure 9. Example of below-ground measurement with proper vertical scale and resolution



Choosing a probe with adequate bandwidth is also crucial for making below-ground measurements.

The universally accepted formula for bandwidth is bandwidth times the rise time (or fall time) equals 0.35 when evaluating a rising edge from 10% to 90% or a falling edge from 90% to 10%.

$$BW{*}T_R = 0.35 \quad (5)$$

The output signal slope in case of below-ground depends on many factors such as the load current and the rail-to-rail voltage swing, but as a rule of thumb, a probe with a minimum bandwidth of 20 MHz should be used. Comparing Figure 10 acquired with a 1-GHz bandwidth probe and Figure 11 with probe bandwidth limited to 20 MHz, the latter underestimates the negative transient, resulting in a 6% smaller measurement of the below-ground value.

Figure 10. Below-ground measurement with high bandwidth probe (1 GHz)

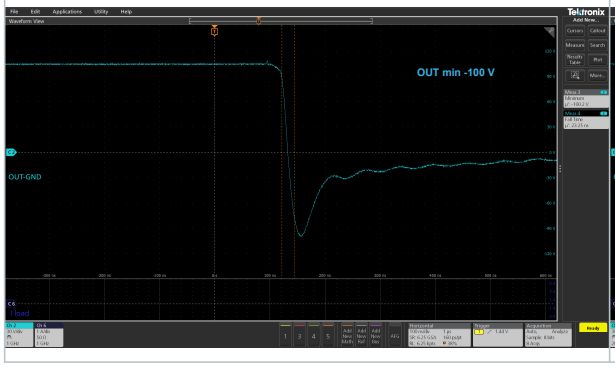
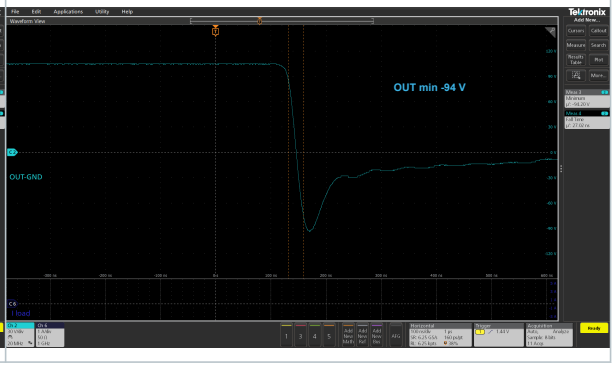


Figure 11. Below-ground measurement with a limited bandwidth probe (20 MHz)

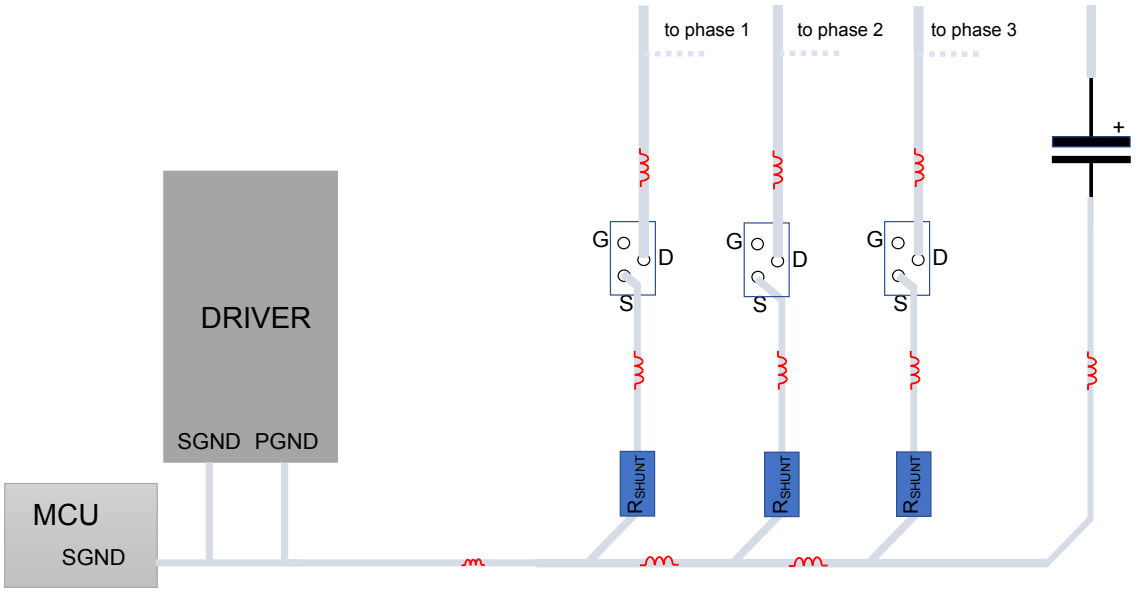


3 Below-ground mitigation

3.1 Layout

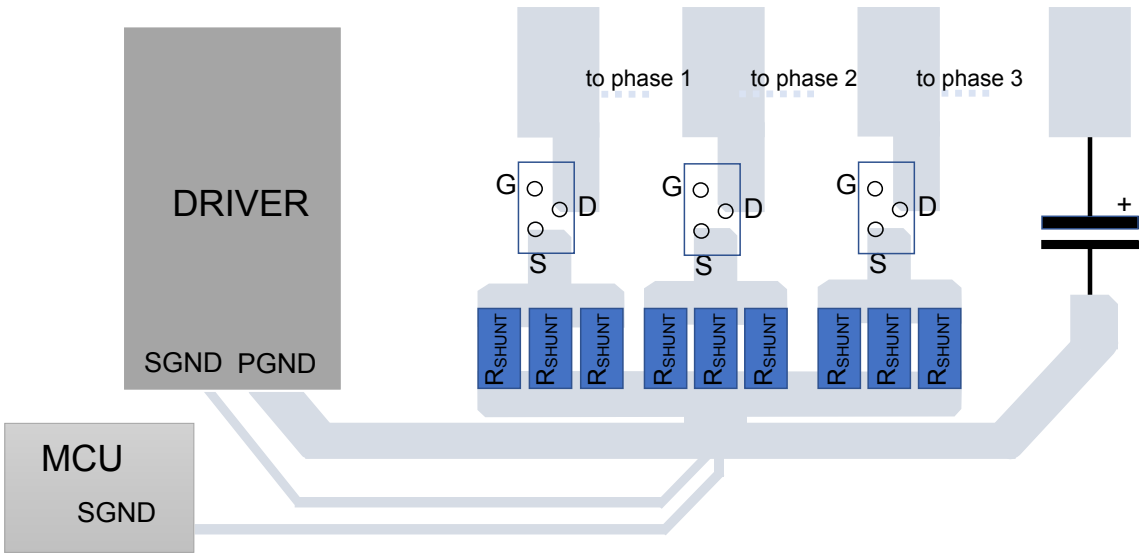
An optimized layout is very important to reduce the value of the parasitic elements that contribute to the below-ground spike. In Figure 12 for instance, the trace connecting the low-side source to the shunt is very narrow and long and will likely introduce a considerable parasitic inductance. The same applies for traces connecting drains to their respective phases and other traces bringing a considerable amount of current, like the connection to the bulk capacitor and to the driver power ground.

Figure 12. Non-optimized layout example



In Figure 13, the same traces have been designed to shorten the path between the source and the shunt. In addition, many shunts in parallel have been used instead of one. The overall parasitic inductance of this solution is much less than in Figure 12.

Figure 13. Optimized layout example

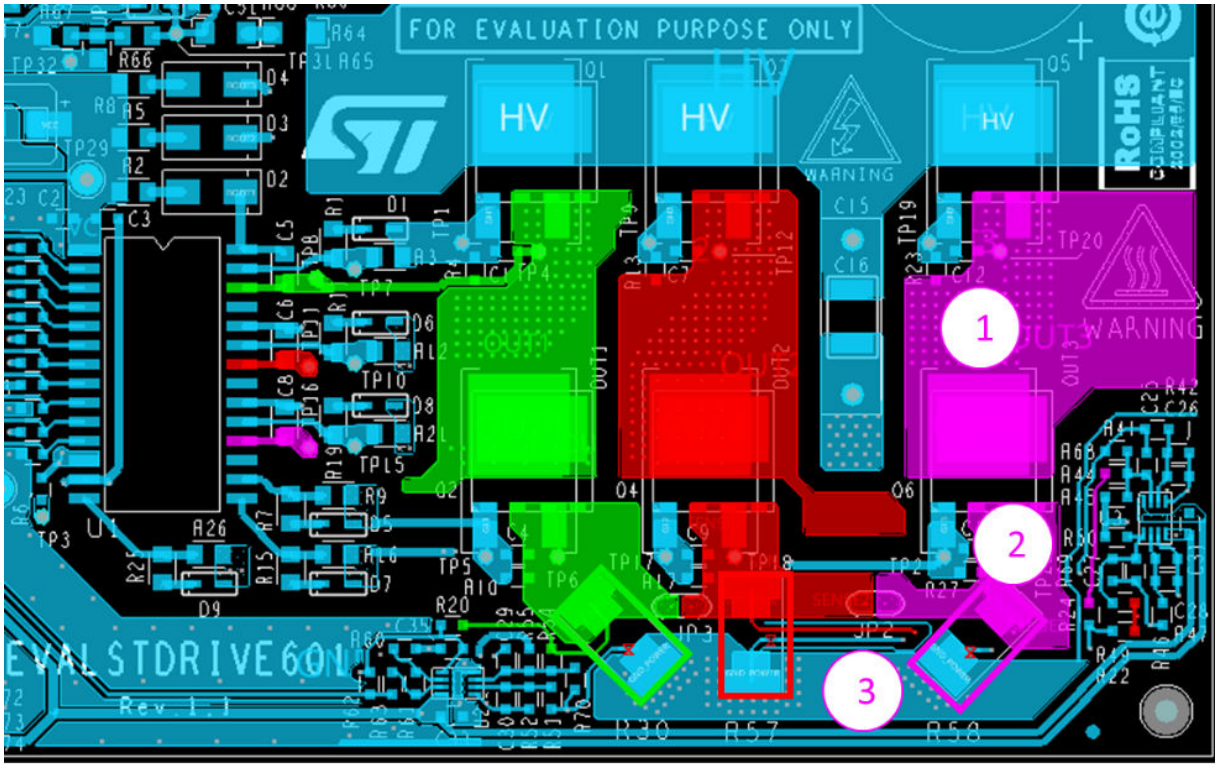


3.1.1 Layout examples

The following figures show some optimized layout examples regarding below-ground.
The following traces are all as short and wide as possible:

1. between low-side MOSFET (IGBT) drain (collector) and output node
2. between low-side MOSFET (IGBT) source (emitter) and shunt resistor
3. between shunt resistor and ground

Figure 14. **EVALSTDRIVE601 layout example**



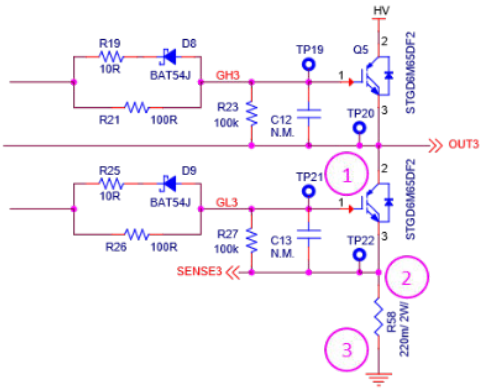


Figure 15. **EVAL6498 layout example**

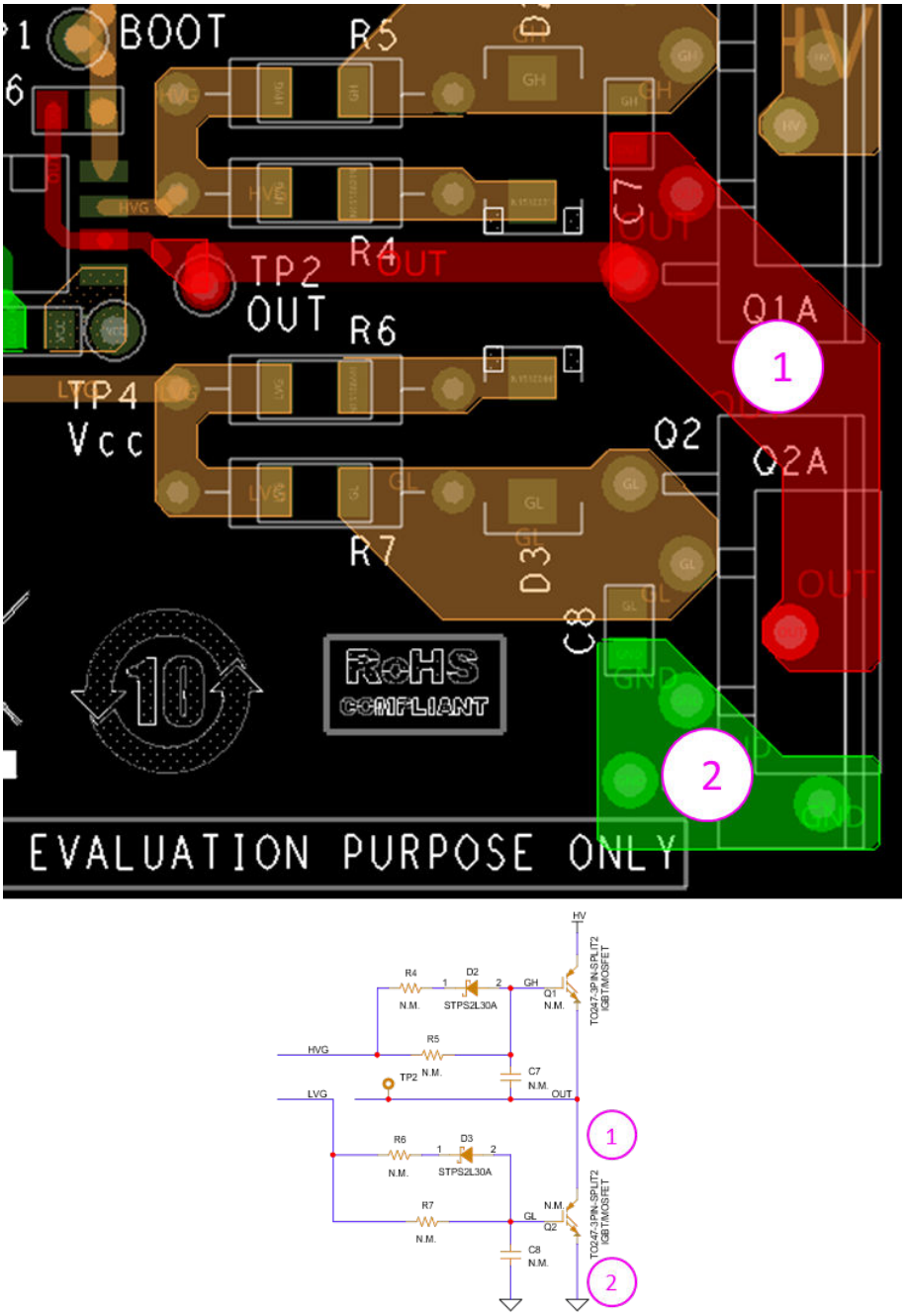
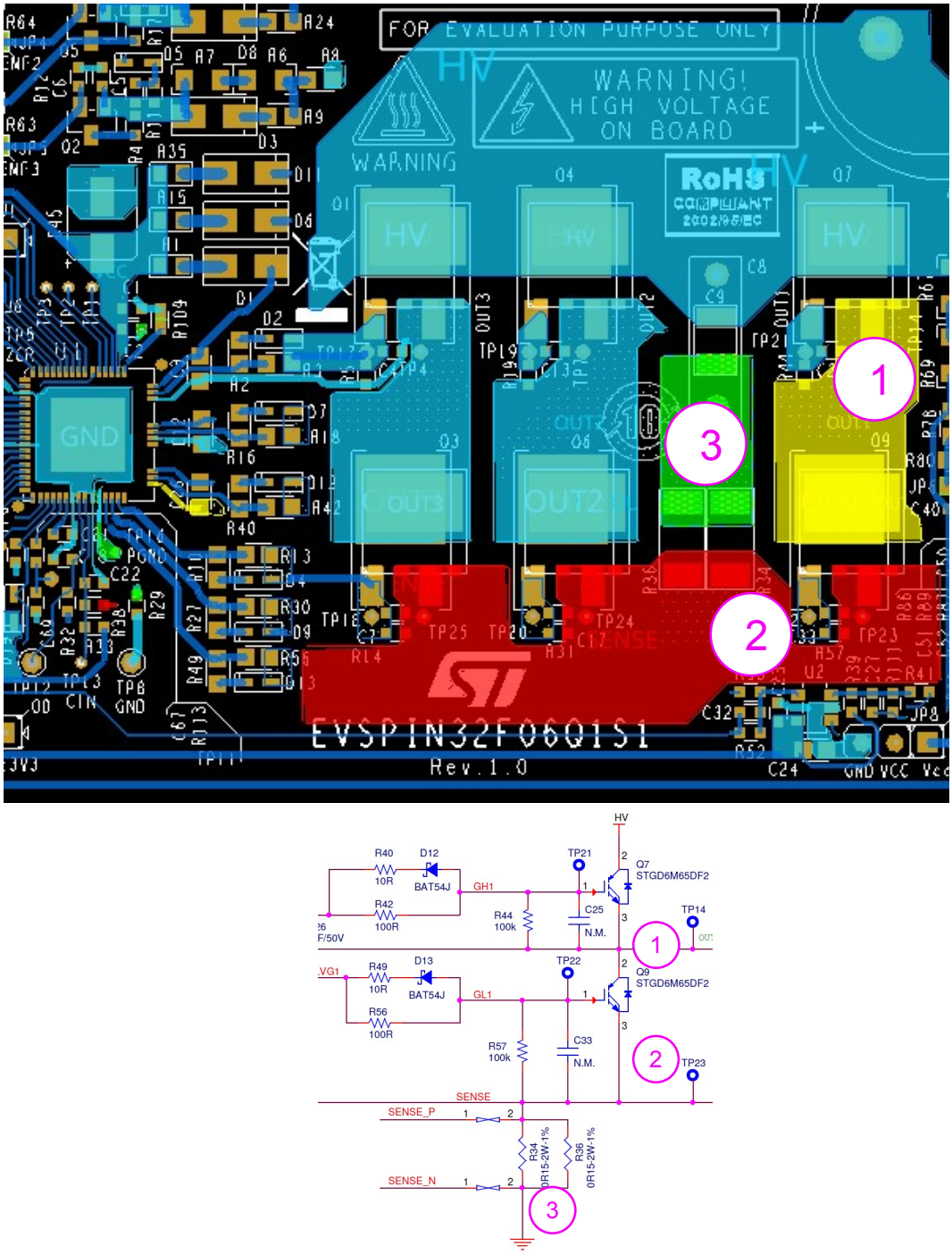


Figure 16. **EVSPIN32F06Q1S1 layout example**



In Figure 16 there is an example of three phase driving solution with single shunt. In similar cases, to keep balanced connections between MOSFET and shunt, it is better to place the shunt near the central MOSFET instead of a lateral position, far from the center.

3.2 Circuit improvements

In high-power or noisy applications, the effect of the below-ground can be limited by:

1. adding a small resistor (R_{OUT} = 5-20 Ω) in series with the OUT pin
2. adding a diode between the OUT pin and GND (the OUT-series resistor is mandatory when this diode is added)
3. an external bootstrap diode.

Workarounds at points 2 and 3 are no more needed for new drivers with enhanced ruggedness.

Figure 17. Resistor added on OUT to mitigate below-ground

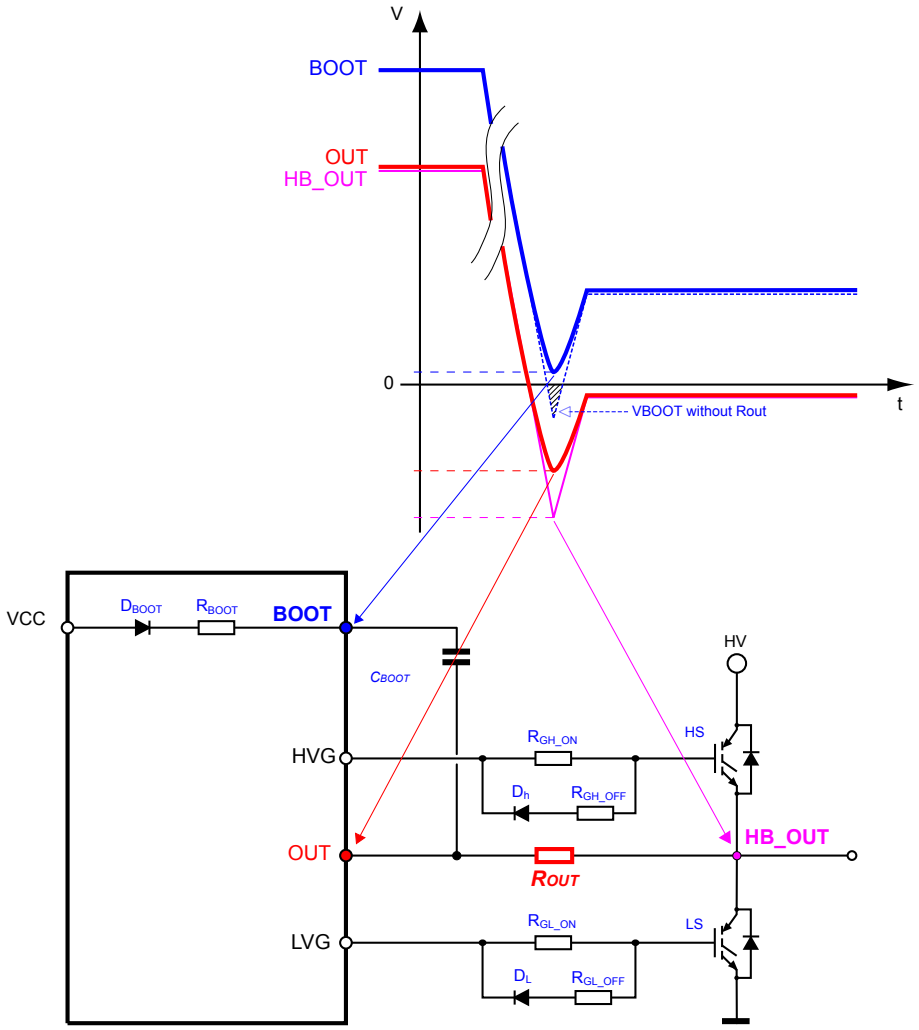
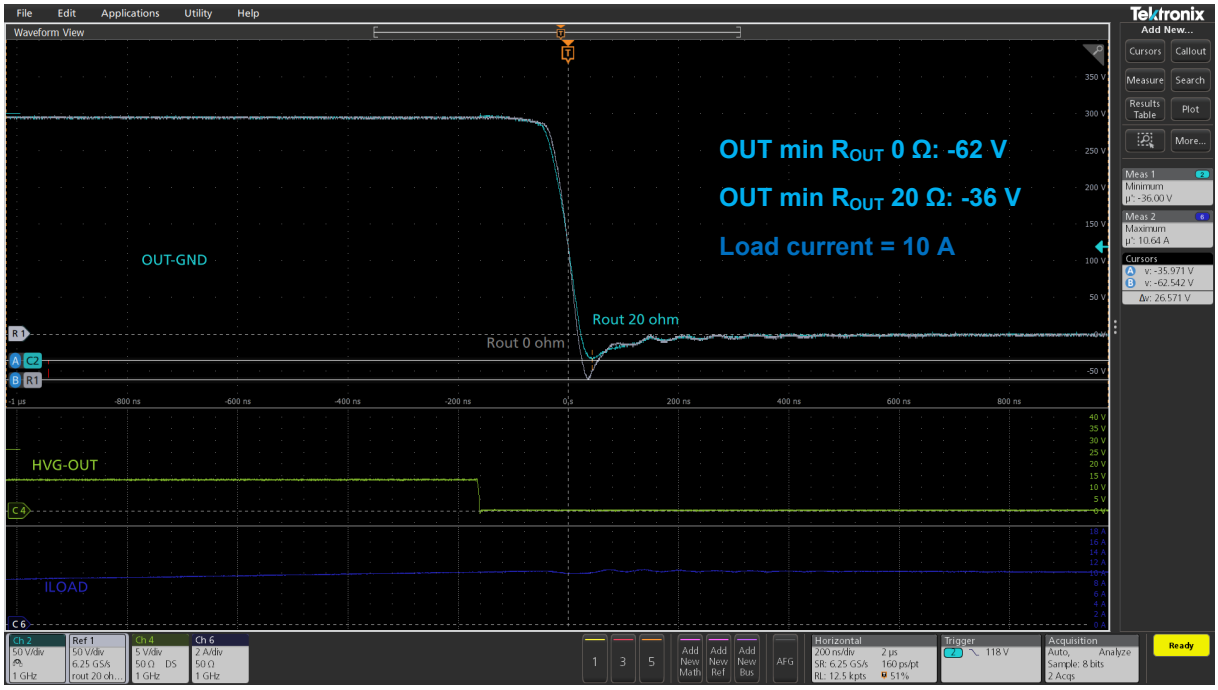


Figure 18 shows the different below-ground value measured with or without the R_{OUT} resistor added to the half-bridge topology of Figure 17, with a parasitic inductance of 190 nH on the low-side transistor collector. It is clearly visible that without the resistor on the output the measured below-ground is almost double.

Figure 18. **Effect of the insertion of a resistor on output on below-ground measurement**



4 Below-ground ruggedness of ST gate drivers

ST has developed its gate drivers by adopting design solutions aimed at minimizing parasitic currents generated by events like the below-ground.

The result is new lines of monolithic drivers such as the L649x half-bridge driver family and the three-phase driver STDRIVE601, which are particularly robust and resilient versus below-ground.

The following sections provide some examples of measurements of output below-ground related to the above-mentioned devices.

An inductive load has been energized with an outgoing current to cause a below-ground as described in Below-ground phenomenon.

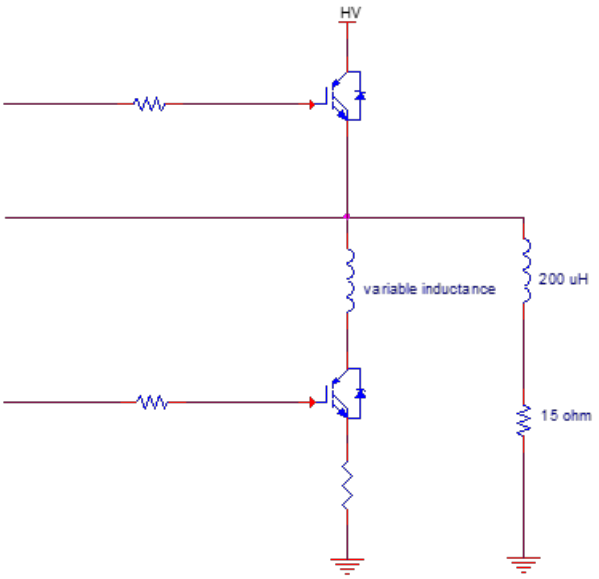
The below-ground on the output is generated through an inductor inserted between the power transistor's collector and the OUT node. By changing the value of the inductance, three scenarios have been simulated:

1. Small value inductance: case of a good PCB layout, may be the intrinsic stray inductance of few nH to tenths of nH
2. Medium value inductance: case of a bad PCB layout
3. Large value (up to 820 nH) inductance: catastrophic, nonrealistic case of PCB layout used to test the ruggedness of the driver.

One sample of STDRIVE601 and one sample of L6491 were tested for below-ground with the following test setup (simplified schematic shown in Figure 19):

- STDRIVE601 and L6491 mounted on their respective evaluation board
- VCC = 15 V
- HV = 300 V
- CIN/CP+ tied to GND
- $LIN_{1,2,3}$ internal pull-up
- $HIN_{1,2,3}$ connected to pulse generator (double pulse to generate high-side hard turn-off)
- Temperature = 25°C

Figure 19. Simplified schematic of setup to generate below-ground on L6491 and STDRIVE601 drivers



The next sections show some waveforms collected for both drivers in the three scenarios mentioned above.

4.1 Below-ground generated on L6491

Figure 20. **Below-ground generated on L6491 (case 1)**

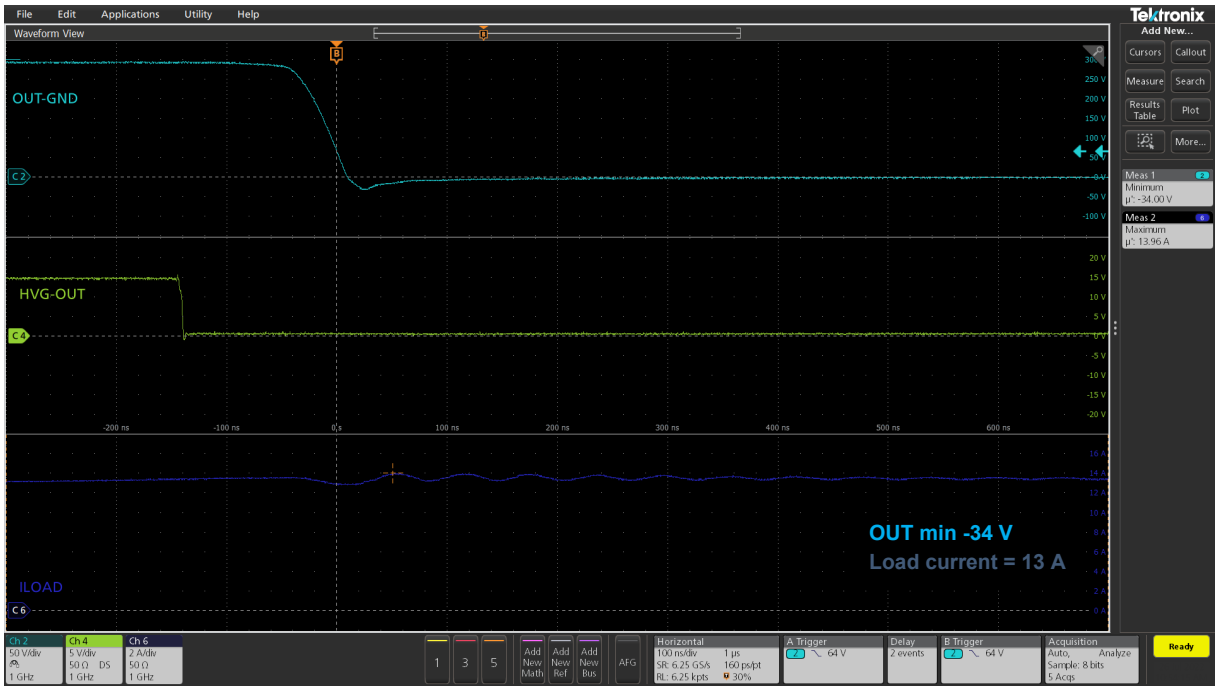


Figure 21. **Below-ground generated on L6491 (case 2)**

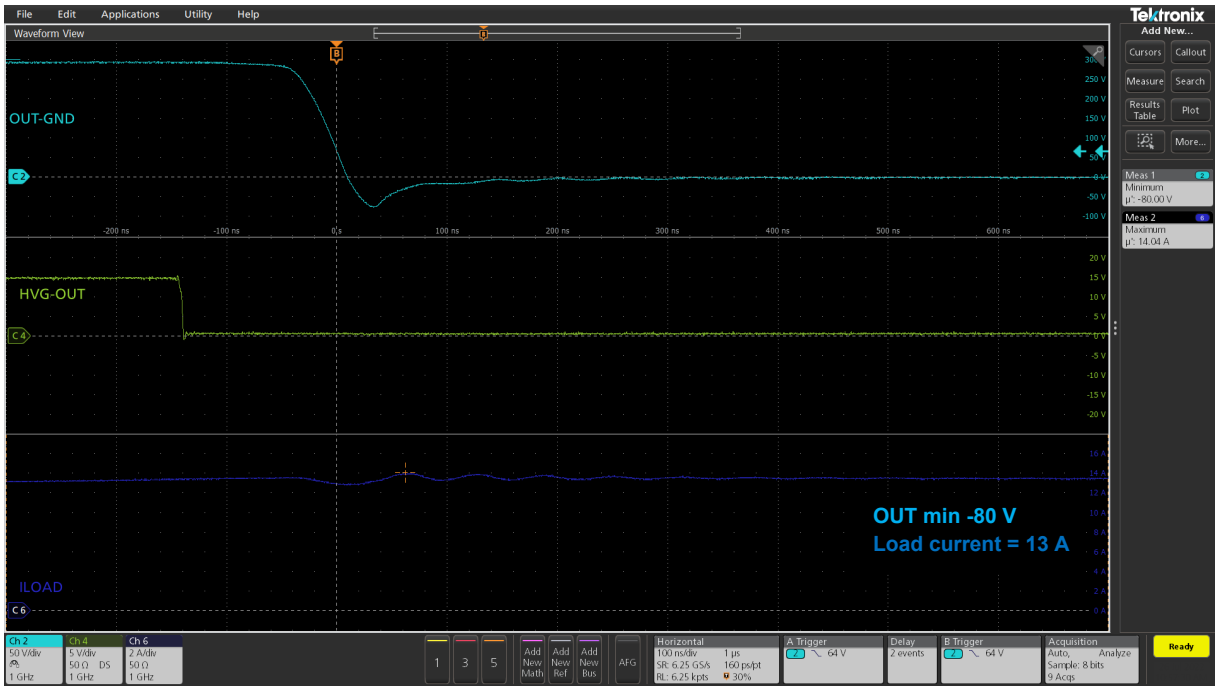
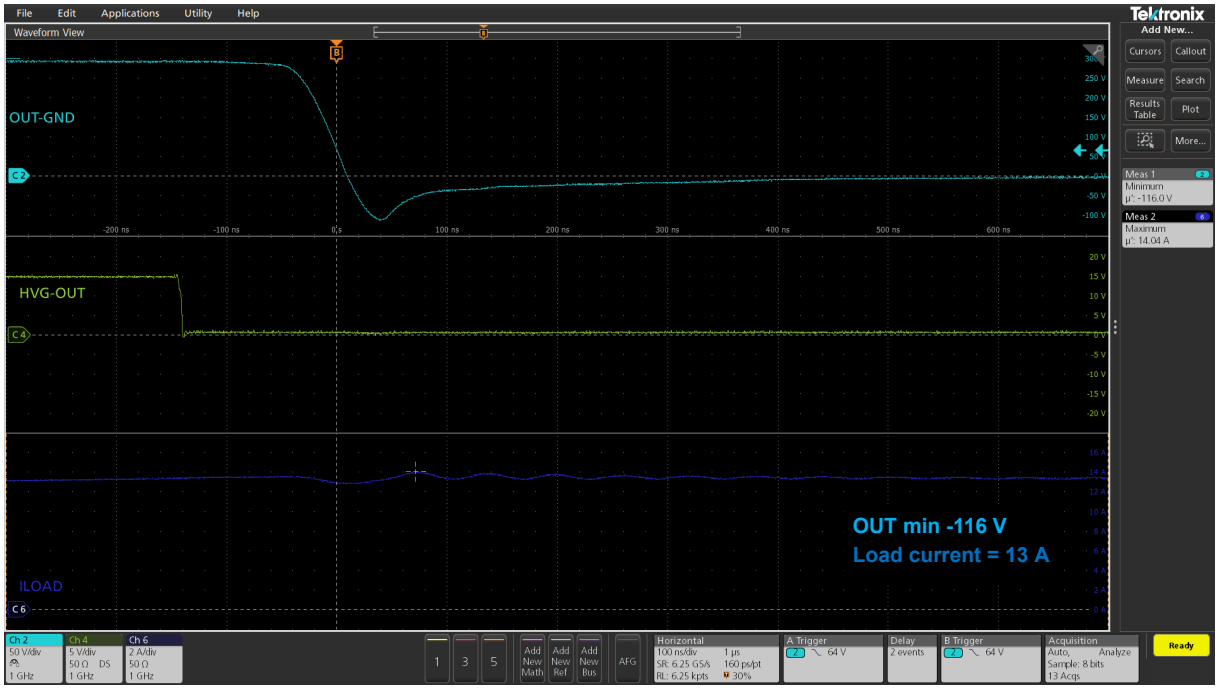


Figure 22. **Below-ground generated on L6491 (case 3)**



4.2 Below-ground generated on STDRIVE601

Figure 23. **Below-ground generated on STDRIVE601 (case 1)**

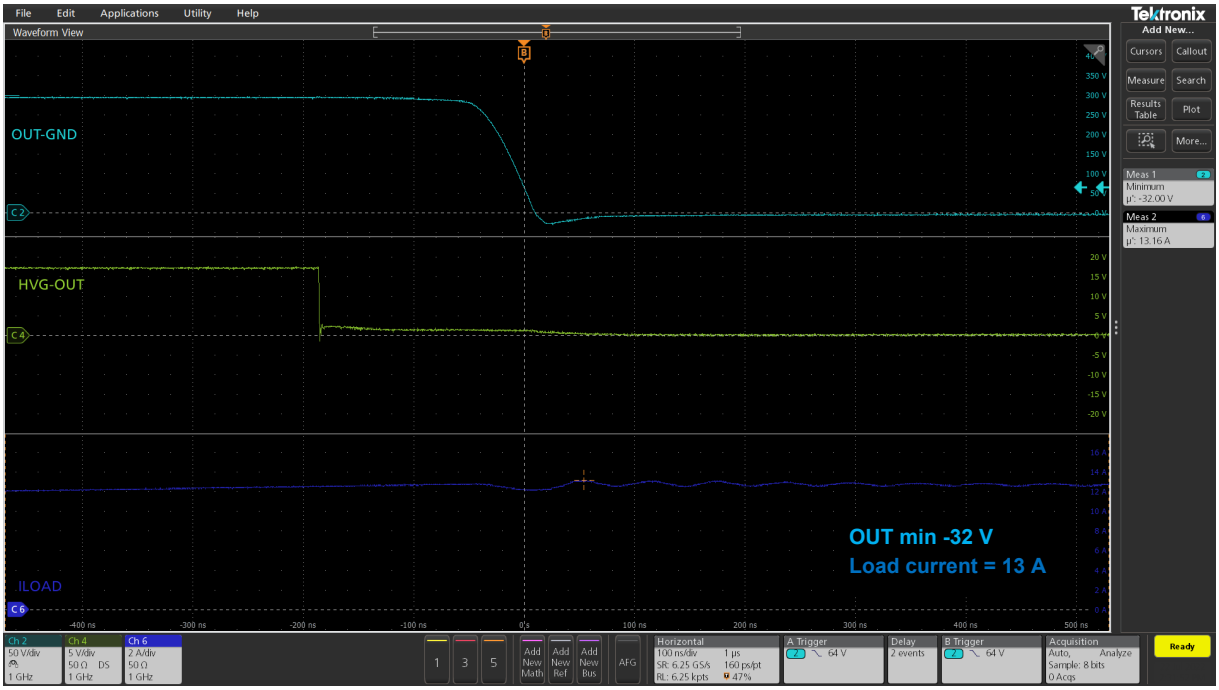


Figure 24. **Below-ground generated on STDRIVE601(case 2)**

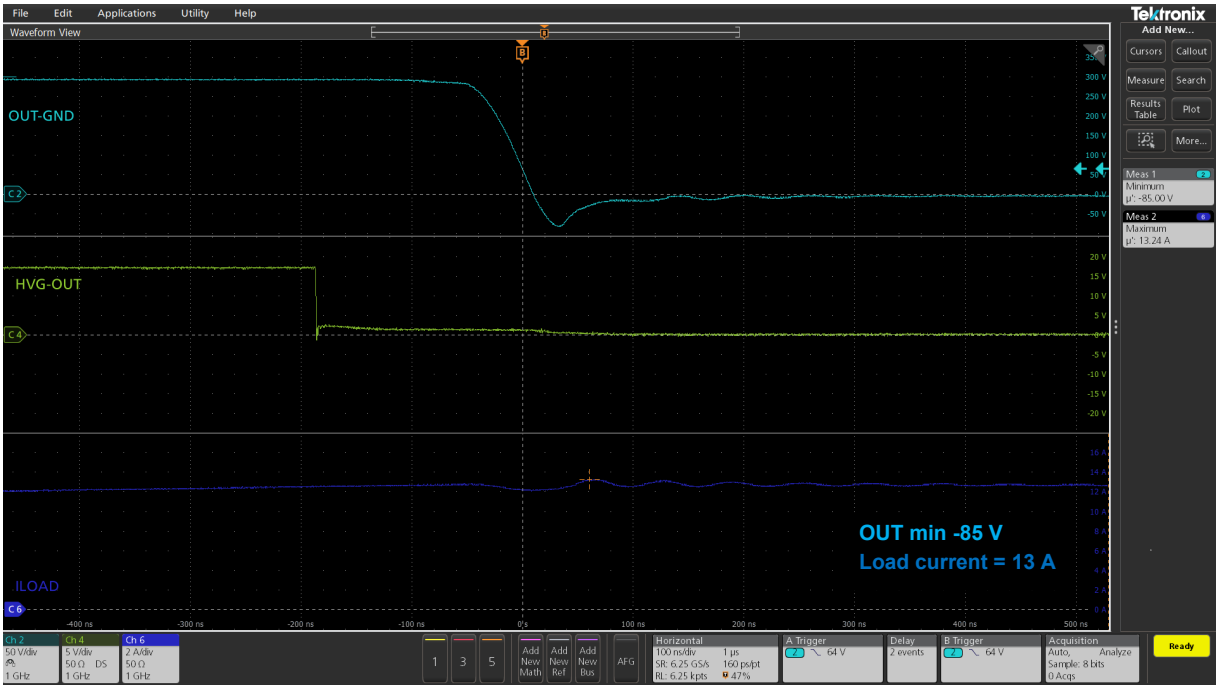
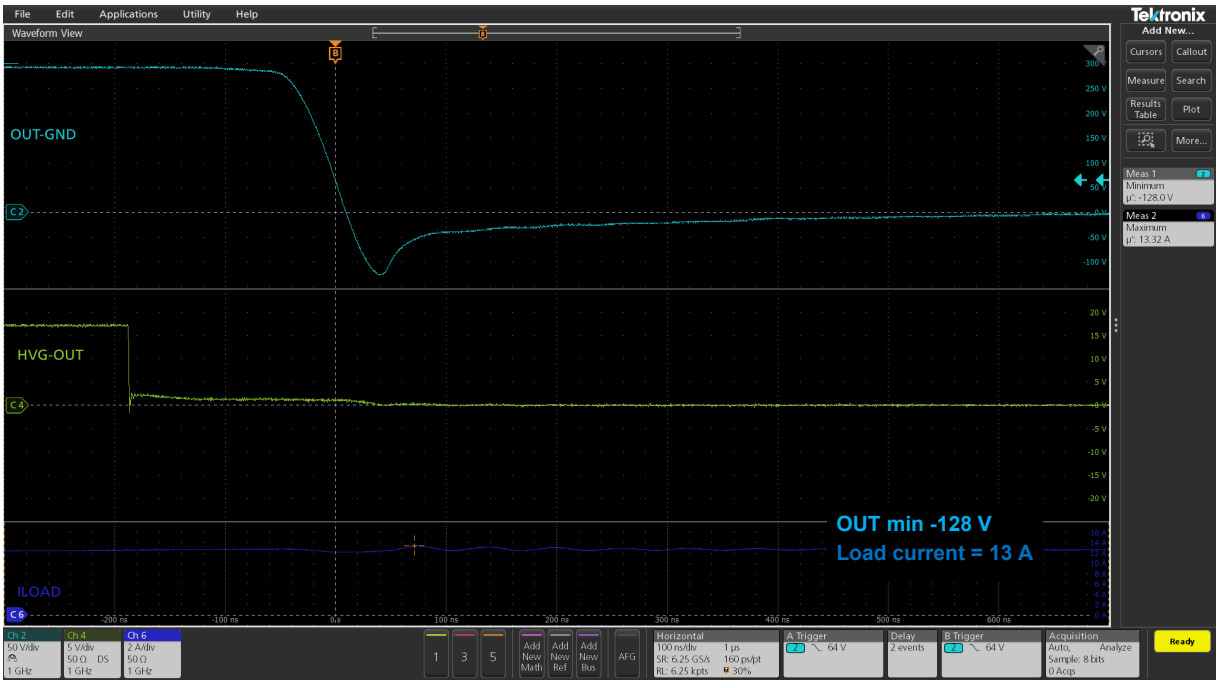


Figure 25. **Below-ground generated on STDRIVE601 (case 3)**



4.3 Conclusion

The results show that both STDRIVE601 and L649x family drivers can withstand very high values of below-ground without any damage.

Table 1. STDRIVE601 and L649x below-ground measurements (load current = 13 A)

Layout	L6491 below-ground [V]	STDRIVE601 below-ground [V]
Good layout (case 1)	-34	-32
Bad layout (case 2)	-80	-85
Catastrophic layout (case 3)	-116	-128

In real applications below-ground events are very short and can last up to dozens of nanoseconds. As visible, both ST drivers in these conditions are very robust with a very good margin against breakdown due to below-ground.

Revision history

Table 2. **Document revision history**

Date	Version	Changes
19-Mar-2023	1	Initial release.

Contents

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