Application note

STPMIC1 auto turn-on

Introduction

The STPMIC1 is provided with an auto turn-on feature that allows the device to be turned ON automatically as soon as VIN rises above a valid threshold voltage.

See section “VIN conditions and monitoring” in STPMIC1 datasheet for more details.

1 Auto turn-on VIN sequence

An auto turn-on event is normally triggered only after the device exits from the NO_SUPPLY state (VIN<$V_{IN\_POR\_Fall}$) and VIN continues increasing, crossing also the “V_{INOK_Rise} threshold”.

In more detail, as soon as the VIN rises above the V_{INOK_Rise} threshold, the STPMIC1 goes to PRELOAD_NVM state and loads the AUTO_TURN_ON bit from NVM.

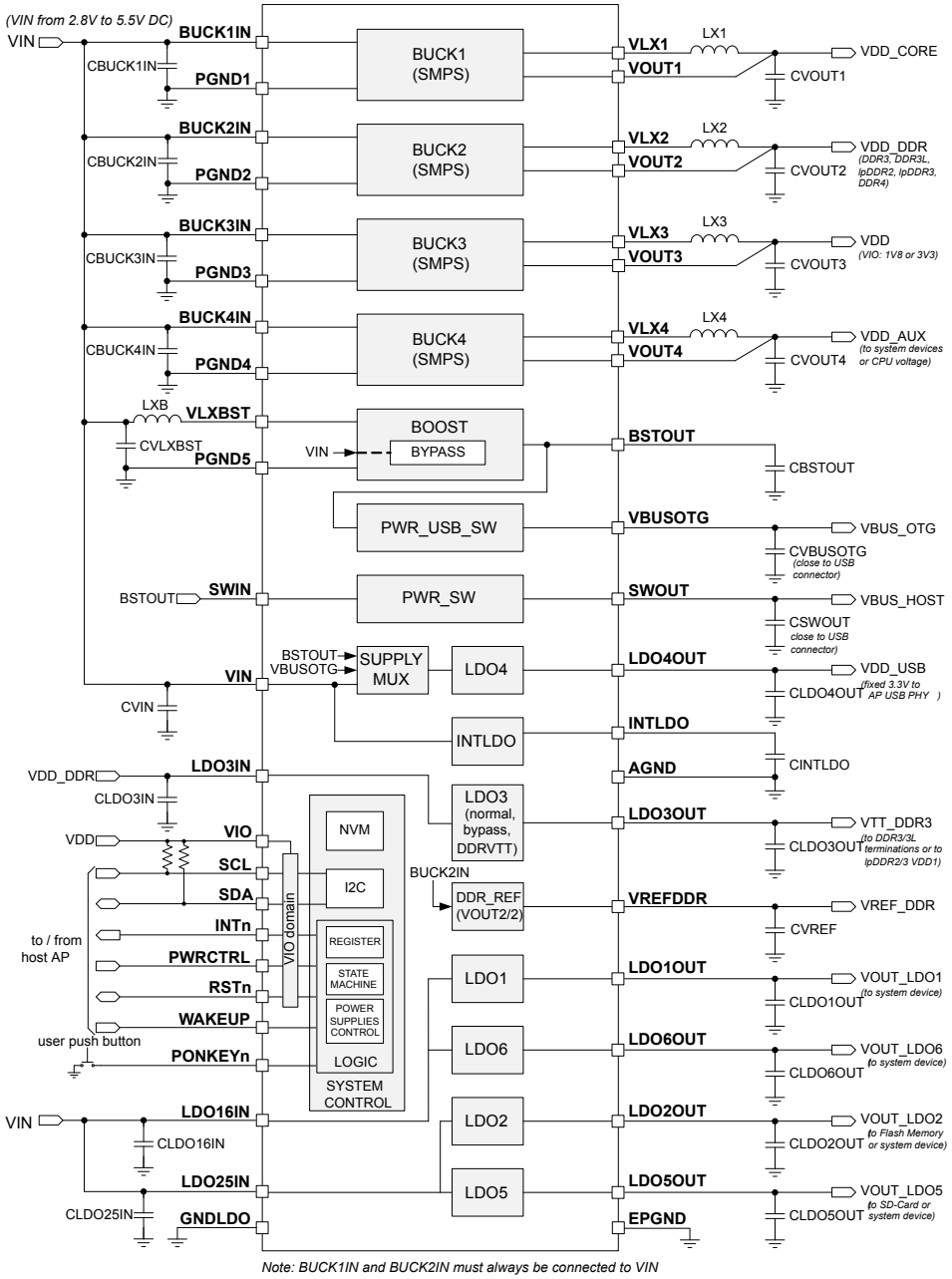
If the AUTO_TURN_ON bit is set, the STPMIC1 goes directly into CHECK&LOAD then goes to POWER_UP followed by the POWER_ON sequence. Otherwise, the device remains in PRELOAD_NVM state and all the regulators output stays disabled.

1.1 INTLDO internal voltage and auto turn-on sequence

The STPMIC1 internal circuitries are supplied by the INTLDO voltage generated by an internal LDO (supplied from the VIN voltage pin) and compensated by the external CINTLDO output capacitor (see Figure 1).

The INTLDO regulator takes part in the regular auto turn-on sequence occurring when the VIN voltage is applied at startup. The CINTLDO capacitor needs to be discharged at every VIN startup cycle.

Figure 1. Block diagram



Note: BUCK1IN and BUCK2IN must always be connected to VIN

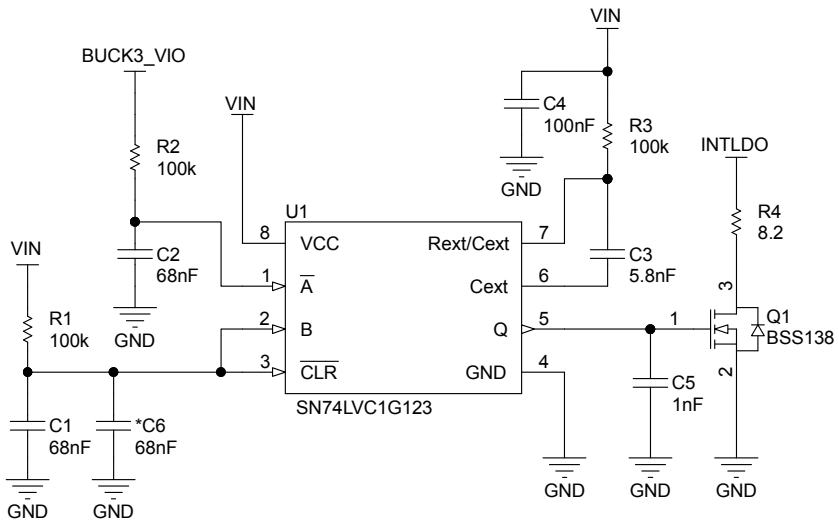
1.2 CINTLDO charge status and VIN bounces

The CINTLDO charge status is important also in case of unwanted VIN voltage bounces, which may occur after a correct auto turn-on sequence is completed.

In fact, if a voltage bounce event occurs, causing the VIN to go below the "V_{INOK_Fall} threshold" for a short time but fast enough to keep the CINTLDO capacitor still charged, when the VIN rises again above the V_{INOK} threshold, the auto turn-on sequence timing is violated, and the device disables all the outputs rails and does not respond to any command until the CINTLDO is discharged and the turn-on sequence is restarted.

1.2.1 Auto turn-on suggestion against VIN bounces

Figure 2. INTLDO additional circuit example



Passive components example:

- R1 = R2 = R3 = 100 kΩ
- R4 = 8.2 Ω
- C1 = C2 = 68 nF
- C3 = 5.8 nF
- C4 = 100 nF
- C5 = 1 nF
- *C6 = to insert for additional power ON delay

The proposed above additional circuit allows the PMIC to perform the auto turn-on sequence in case of possible VIN brownout reaching the following thresholds in a short time (< 2 ms):

VIN < V_{INPOR_Fall} threshold

Note: *(V_{INPOR_Fall} = 2.1 V typ.)*

V_{INPOR_Fall} < VIN < V_{INOK_Fall}.

Note: *(V_{INOK_Fall} = V_{INOK_Rise} -V_{INOK_HYST} where V_{INOK_Rise} and V_{INOK_HYST} are NVM programmable)*

Following the truth table valid for the SN74LVC1G123:

Table 1. SN74LVC1G123 truth table

Inputs			Outputs
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L
X	X	L	L
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

On the $\overline{A}$ pin of the SN74LVC1G123, one 3.3 V output channel of the PMIC1 (that is, Buck 3 output of figure 2 example) is applied, which is monitored to trigger the PMIC power OFF caused by the VIN brownout.

The values of R2 and C2 determine the delay between the negative slope of $\overline{A}$ and the pulse generated on Q (when $\overline{CLR}$ and B are high).

VIN of PMIC1 is applied to the pins B = $\overline{CLR}$ and VCC.

The values of R1 and C1 determine the delay between the positive slope of B = $\overline{CLR}$ and the pulse generated on Q (when $\overline{A}$ is low).

The duration of the pulse generated on Q output depends on the values of R3 and C3 used on pins Rext/Cext and Cext. The pin Rext/Cext is connected to VIN, and the C4 is an additional cap used as VIN filter.

The output Q of SN74LVC1G123 drives Q1 NMOS.

In order to perform the auto turn-on sequence in case of possible VIN brownout, the INTLDO capacitor needs to be discharged below its internal POR threshold allowing the NVM content to be reloaded and restarting the turn-on sequence.

This is achieved by connecting the INTLDO pin to the NMOS drain, close to GND for a pulse period defined by R3/C3.

The following scope plots show the behavior of the PMIC1 when a VIN bounce occurs:

Figure 3. VIN brownout under the V_{INPOR_Fall} after power-on (without the proposed circuit)

Figure 4. VIN brownout under the V_{INPOR_Fall} after power-on (with the proposed circuit).

Figure 5. VIN brownout to V_{INPOR_Fall} < VIN < V_{INOK_Fall} after power-on (without the proposed circuit)

Figure 6. VIN brownout to V_{INPOR_Fall} < VIN < V_{INOK_Fall} after power-on (with the proposed circuit)

Revision history

Table 2. **Document revision history**

Date	Version	Changes
29-Nov-2022	1	Initial release.

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