Guidelines for cycling endurance and data retention of page EEPROMs

Introduction

Reliability and endurance are key requirements for datalogging or event recording applications. The products listed in Table 1 meet the very high level of quality needed for these applications.

Table 1. Applicable products

Root part number reference	Commercial part numbers
M95P32-I	M95P32-xxxxx
M95P32-E	
M95P16-I	M95P16-xxxxx
M95P16-E	
M95P08-I	M95P08-xxxxx
M95P08-E	

1 Cycling performance

1.1 Cycling budget

Page EEPROMs can write data with:

- *Page Program* operation, which needs erased bytes (FFh) to program data
- *Page Write* operation, made up of a *Page Erase* operation followed by a *Page Program* operation

For more information about *Page Program* and *Page Write* operations refer to AN5747 "*Page EEPROM memory architecture*".

Table 2. Glossary

Parameter	Definition
Cycle	Page write operation (1 to 512 bytes) or erase operation (page, sector, block, or chip erase)
Cycling	Cumulated number of cycles

Note: A program operation executed between two erase operations does not count as a cycle.

As specified in the related datasheets, the cycling budget is 500 k per page over the full temperature and supply voltage range, which makes page EEPROMs very flexible.

This cycling budget represents the sum of page write and erase operations over a page:

- A page write of 1 byte or a page write of 512 bytes represent one cycle over the page
- A page erase of 512 bytes represents one cycle over the page, whatever the amount of page program operations.
- A sector erase (4 KB) represents one cycle for each of the 8 pages erased
- A block erase (64 KB) represents one cycle for each of the 128 pages erased
- A chip erase represents one cycle for each page of the memory

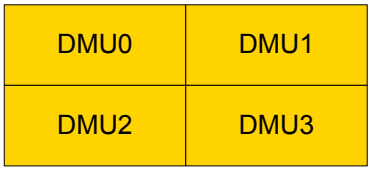
The cycling budget is easy to calculate, and allows byte cycling thanks to the page write operation. The error correction code (ECC) has no effect on it.

For more information about ECC refer to the AN5747.

1.2 Cycling qualification method

The qualification cycling pattern is defined to reach three weeks (~ 500 h cycling time), as defined in JEDEC JESD47. During the qualification phase, the parts are cycled and then read to locate the failing bits, if any. The device architecture embeds data memory units (DMUs), as illustrated in the figure below.

Figure 1. M95P32 DMU architecture



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In the M95P32 devices, each DMU is cycled from 1% (5 k cycles) to 100% (500 k cycles) of the specification with different (page, sector, and block) erase operations . DMUs are not cycled at the same time: this makes it possible to check if cycling a DMU has any impact on the others. The full content is always verified with a read operation.

1.3 Overall number of cycles

The number of cycles can be defined for each page or for the overall number of cycles decoded by the whole memory:

- The cycling value defined in the datasheet is the maximum number of cycles for each page: 500 K.
- The overall number of cycles is the maximum number of qualified cycles: 1 billion.

2 Cycling strategies

A good cycling strategy can optimize the endurance of page EEPROM products.

A power-down during a page write cycle can corrupt the whole addressed page. For this reason, it is advised to separate the areas containing the read-only parameters from those with the cycled items, and to make them as much as possible independent from each other. The two types of data must not share the same pages.

For more information about power loss and data corruption, refer to AN5747.

It is recommended to gather data related to the same cycling rates, referred to as data class in the following sections.

2.1 Strategy 1: counting pages

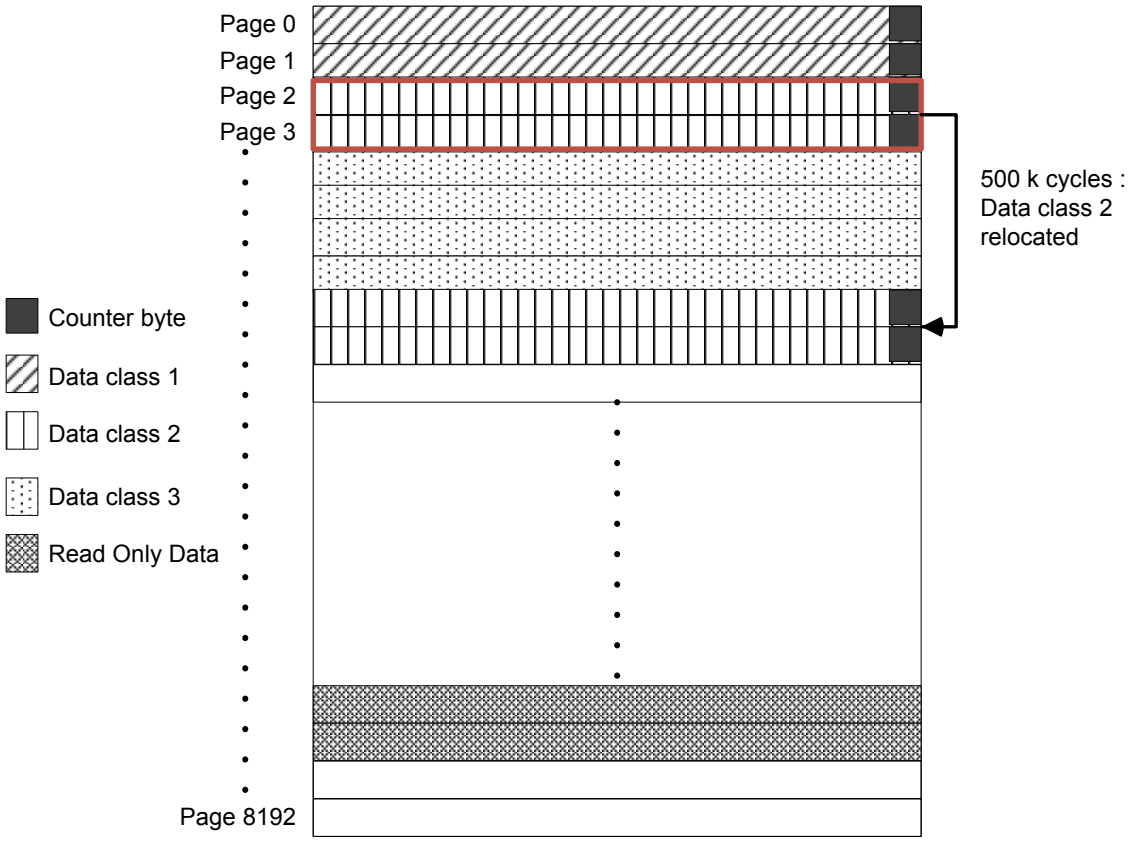
The first cycling strategy is monitoring the write endurance of each page with a dedicated counter byte. If a page reaches the 500 k cycles, the whole data class is relocated to another physically independent memory address.

Example:

In Figure 2, data class 1 cycles every hour, data class 2 cycles every minute. When a page of data class 2 reaches 500 k cycles, the whole data class (page 2 + page 3) is relocated.

The read-only pages and the data classes remain separated.

Figure 2. Counting pages cycling strategy



2.2 Strategy 2: data class budget

This approach recommends to allocate enough memory for a data class. The allocated memory is calculated with the total amount of cycles the data class goes through during the whole application lifetime.

If different data classes are cycled, several parts of the memory must be allocated for each data class type.

Example:

In an application running on M95P32, 32 bytes are cycled every minute, and 4 bytes every 10 minutes. The application lifetime is 10 years.

Two data classes can be identified:

- **dataClass#1**: $\text{years} \times \text{days} \times \textit{hours} \times \text{minutes} = \text{DataClass\#1 application cycling budget}$
  $10 \times 365 \times 24 \times 60 = 5\,256\,000 \ \ \text{cycles}$
- **dataClass#2**: $\text{years} \times \text{days} \times \textit{hours} \times \text{minutes} = \text{DataClass\#2 application cycling budget}$
  $10 \times 365 \times 24 \times 6 = 525\,600 \ \ \text{cycles}$

The page cycling endurance of the M95P32 products is 500 k, hence:

- to fit the 5,256,000 cycles, dataClass#1 needs at least 11 pages (5256000/500000), which represents 478,182 cycles per page
- to fit the 525,600 cycles, dataClass#2 needs at least 2 pages (525600/500000), which represents 262,800 cycles per page

The following figure shows how these data classes can be allocated in a 32 Mbit page EEPROM.

Figure 3. Cycling with data class budget

The cycle begins at pointer position 0. At each cycle, the pointer is incremented to write the next page. When the last page is reached, the position is reset. So, the 11 pages are cycled 478,182 times. This strategy distributes the cycling over several locations, avoiding an excessive stress on the same area.

3 Data retention

3.1 Definition

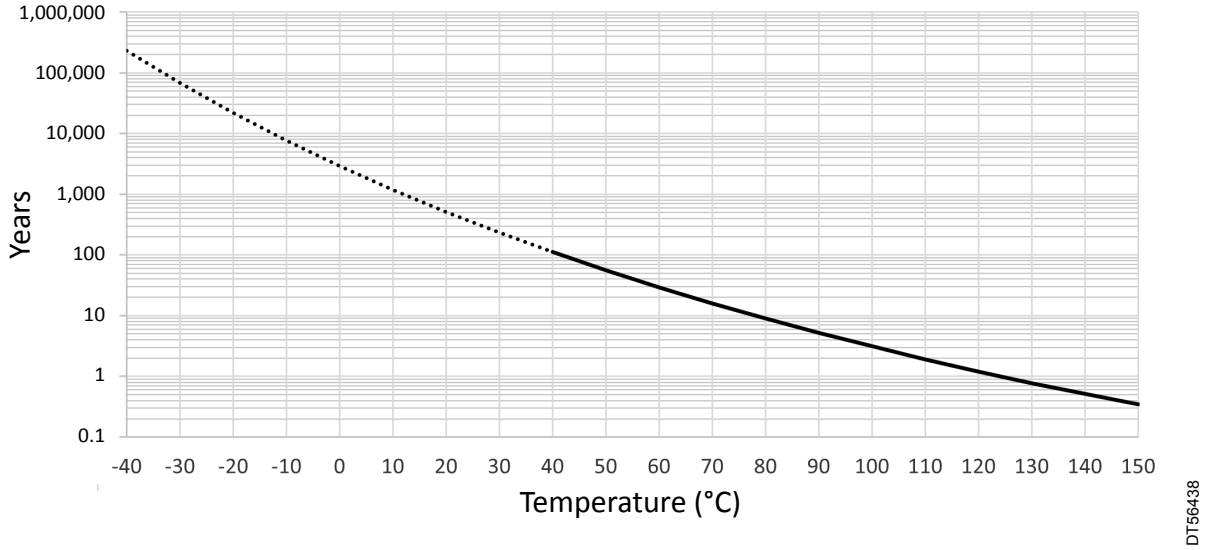
Bytes are written at t = t_0, then no page write or erase operations are executed on them. The data retention is the time after t_0 during which the bytes can still be correctly read (the device can be supplied or not).

3.2 Temperature dependence

Page EEPROMs data retention is depends upon the temperature, the higher the temperature, the lower the data retention time.

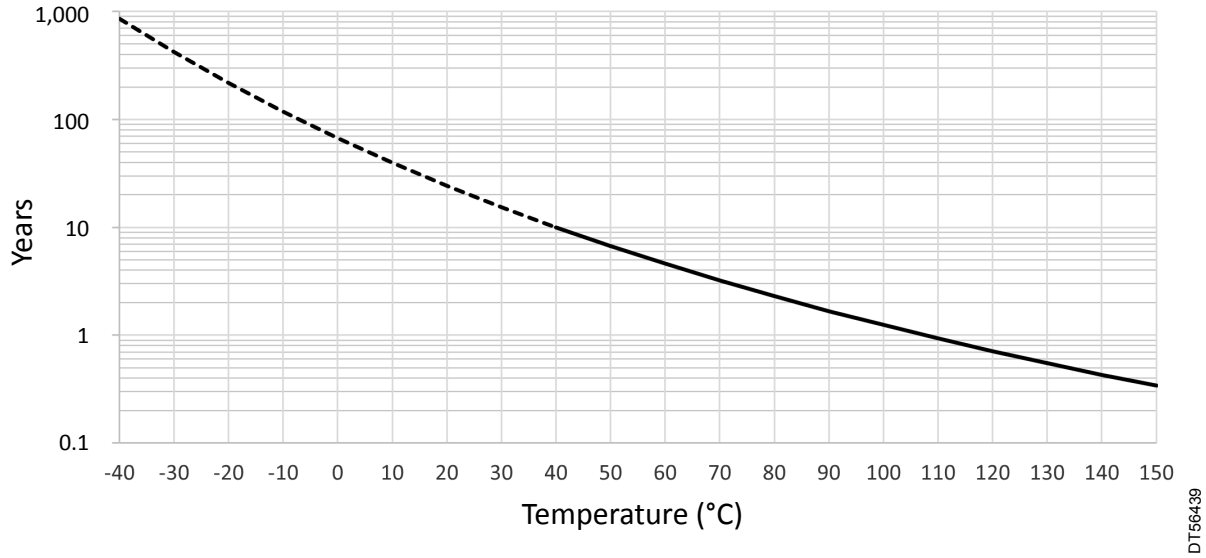
Figure 4 and Figure 5 show the data retention as a function of the temperature for, respectively, read-only data and cycled data.

Figure 4. Data retention vs. temperature (read-only data)



At 40 °C, the read-only data programmed in a page EEPROM product can be correctly read for 100 years.

Figure 5. **Data retention vs. temperature (cycled data)**



At 40 °C, if the page is cycled, the data programmed can be correctly read for 10 years.

3.3 Qualification method

The qualification procedure checks that the data remain readable with a safe programming level. The parts are stored in an oven at 150 °C for 3000 hours, with no DC voltage on pin VCC, then the memory content is checked.

The data retention follows an Arrhenius law, this permits to extrapolate, from the tests performed at different temperatures, the device performance. These limits are above the safe value defined in datasheets.

3.4 Application data retention

To assess the data retention, it is recommended to evaluate the amount of time during which the end application remains within a same temperature range. A good data retention evaluation should:

- Define the time (in years) during which the device remains within a temperature range (the typical temperature profile of the end application)
- Estimate the data retention value for each temperature range with the following equation:

$$\sum_{i=1}^{n} \frac{\text{Number of years at temp}(i)}{\text{Number of years specified for temp}(i)} \leq 1 \quad (1)$$

If the result is lower than or equal to 1, the application data retention time is within the maximum data retention capability of the device.

Example

An application operates for 14 years at 30 °C, and for 6 years at 50 °C. The application does not cycle pages intensively, and its lifetime is 20 years. Equation 1 helps the user to determine if the maximum data capability is reached with the application temperature range.

Table 3. Example of data retention capability calculation

Temperature (°C)	Time at temperature (years)	Data retention capability (years)(1)	Data retention usage(2)
30	14	232	6.0%
50	6	56	10.7%
-	-	-	**Total**: 16.7%

1. *The maximum data retention is determined according to Figure 4.*
2. *The data retention capability is calculated according to equation 1.*

The data are safe for 20 years, with only 16.7% of the capability used. This means that the data are safe for a longer time, demonstrating the excellent data retention capability of the page EEPROM products.

4 Conclusion

The budget of 500 k cycles per page is defined by the number of page write and erase operations executed over the page. Page program operations and ECC are irrelevant. The cycling budget does not depend upon the temperature and voltage ranges.

To guarantee this cycling budget, page EEPROM products go through a robust qualification process, respecting the JEDEC JESD47 guidelines. This qualification method shows that these products can reach a total cumulated cycle of 1 billion.

To optimize the cycling endurance two strategies are available:

1. The page counting, monitoring the write endurance of each page with a dedicated counter byte.
2. The data class budget, distributing the cycling budget of data over several locations, thus avoiding excessive stress on the same area.

The second strategy is recommended when the application budget cycle is known. The first one, more flexible but less easy-to-use, is recommended if the application cycling budget is unknown.

The retention capability demonstrates the high quality of page EEPROMs. This quality is achieved thanks to a severe qualification process and the ECC, which guarantees 100 years of retention for pages not intensively cycled and 10 years for intensively cycled pages.

The user can calculate the application data retention capability (see Section 3.4 Application data retention), to ensure that data are safely stored.

Revision history

Table 4. **Document revision history**

Date	Version	Changes
16-Feb-2023	1	Initial release.
05-Sep-2023	2	Scope extended to M95P08 products, hence updated Table 1. Applicable products. Minor text edits across the whole document.

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