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AN5885

Application note

Designing with the L99H92

Introduction

The L99H92 is a sophisticated H-Bridge MOSFET controller IC designed to control up to 5 N-Channel MOSFETs in full H-Bridge or dual half-Bridge configuration with reverse battery protection. It has a SPI and two configurable current sense amplifiers; L99H92 incorporates SPI control for functional programming and high-level diagnostics.

The L99H92 is optimally intended to drive higher current motor control systems in an automotive environment. This document walks the engineer through the design decision process for developing a higher current motor control application.

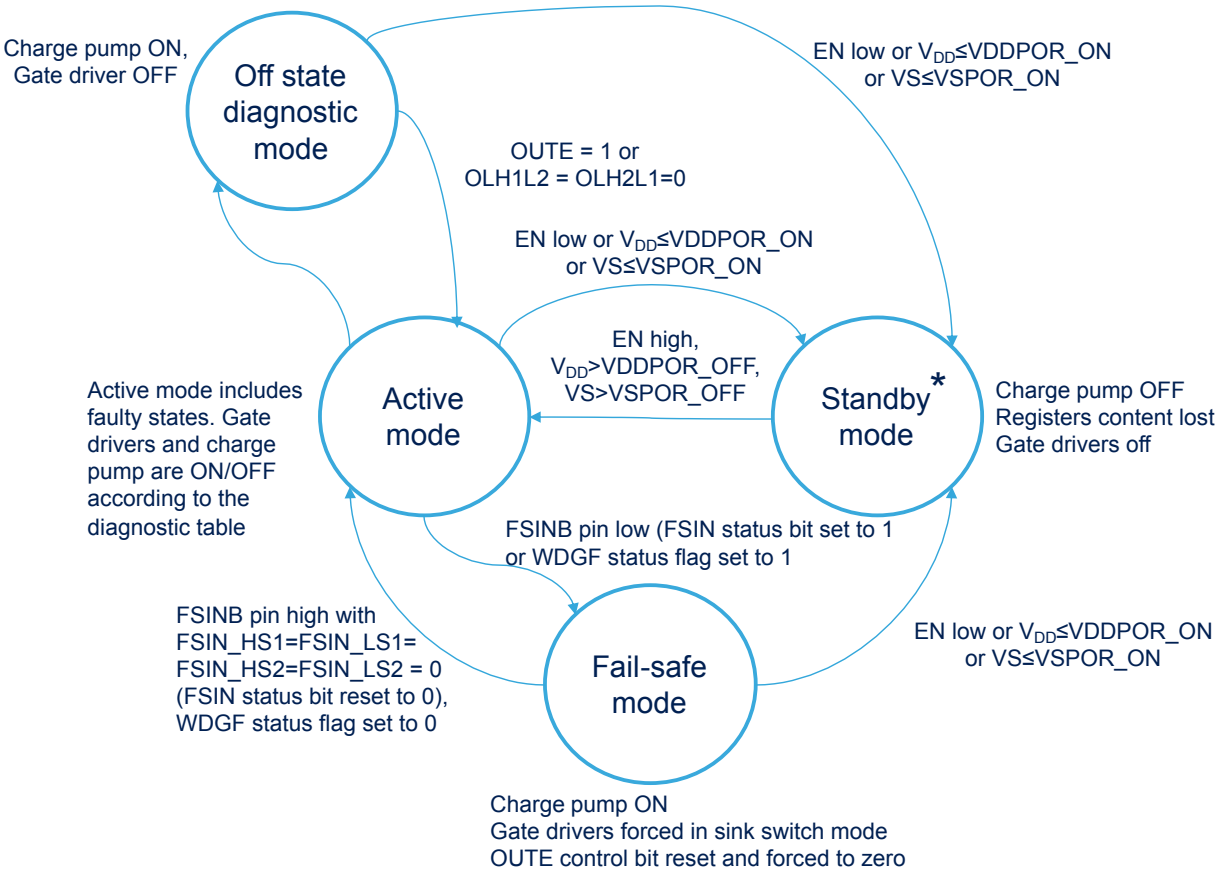
1 Functionality

The L99H92 is an H-Bridge MOSFET controller IC that uses both direct inputs and a SPI bus to manage the H-Bridge functionality. The following is a brief synopsis of the L99H92 basic operation. More details can be found in the datasheet.

1.1 Functional states

This L99H92 does not have a state machine. It does, however, function in four regions: off state/diagnostic, standby, active and fail-safe modes. The functionality can be best described using the following diagram.

Figure 1. Functional states



1.2 Direct input control

What is managed by direct inputs are:

- **Enable pin**
  - When this pin is low all registers are reset to the default setting and the MOSFET drivers are set to passive off mode.
  - When enable goes high and VDD > V_{DDPOR_ON} and VS > V_{SPOR_ON} the L99H92 enters in active mode. If one of these conditions is not met, the device stays in standby mode.
  - When the EN pin is left floating, because of the internal pull-down resistor, the device enters in standby mode.

- **PWM (PWM/IN1) and direction (DIR/IN2) pins**
  - When the OUTE control bit is set and FSINB pin is high, the external MOSFETs are controlled by the PWM/IN1 and DIR/IN2 pins.
  - If INPMODE = 0, the device works in full-bridge mode. In this case the active full-bridge diagonal is selected by DIR/IN2 input while the driving PWM signal must be applied to PWM/IN1 input (PWM/IN1 = PWM, DIR/IN2 = DIR).
  - If INPMODE = 1, the device works in dual half-bridge mode. The two half-bridges must be driven separately by PWM/IN1 and DIR/IN2 inputs (PWM/IN1 = IN1, DIR/IN2 = IN2).
- **Fail-safe input not pin (FSINB)**
  - The L99H92 features an asynchronous, logic independent fail-safe input pin working as a redundant switch-off path for all the MOSFETs.
  - The fail-safe input not pin (FSINB), active low, has an internal pull-down resistance: as soon as the FSINB pin falls below the VFSINBLTH threshold for a time longer than t_{FSINB_filt}, the FSINLL and the FSIN status bits are set and the device is put in fail-safe mode.
  - The gate drivers are forced in sink switch mode to switch off actively all the MOSFETs with the maximum available current, regardless of the programmed gate discharge current.

1.3 Gate drivers

1.3.1 Outputs driving signals (PWM/IN1 and DIR/IN2)

When the OUTE control bit is reset with the FSINB pin high, all the gate drivers are disabled and the turned on MOSFETs are passively shut off through the internal resistance connected between gate and source of each MOSFET (RGSHx and RGSLx). Regardless of the OUTE control bit value, when the FSINB pin is pulled low all the MOSFETs are actively shut off by the gate drivers forced in sink switch mode.

Table 1. Truth table

OUTE bit	AFWE	FWS	FSINB	DIR	PWM	HS1	LS1	HS2	LS2
X	X	X	0	X	X	OFF	OFF	OFF	OFF
0	X	X	1	X	X	OFF	OFF	OFF	OFF

Once the OUTE control bit is set and the FSINB pin is high, the external MOSFETs are driven by the input pins PWM/IN1 and DIR/IN2. Both input pins, PWM/IN1 and DIR/IN2, have an internal pull-down current (IPWM_in and IDIR_in) to put the outputs in a well-known condition in case any of the pins will no longer be driven by the microcontroller. Depending on the value of the INPMODE control bit, the device can work as a full-bridge driver or dual half-bridge driver:

- If INPMODE = 0 (default value), the device works in full-bridge mode. In this case the active full-bridge diagonal, fixing the rotational direction of the motor is selected by DIR/IN2 input while the driving PWM signal has to be applied to PWM/IN1 input.

Depending on the active free-wheeling enable control bit value (AFWE) and the freewheeling selection control bit value (FWS), four different freewheeling strategies are available: active or passive and freewheeling on either high-side or low-side MOSFETs. The DIR input pin sets the active diagonal.

The AFWE control bit enables or disables active free-wheeling and the FWS control bit sets the free-wheeling path (HS or LS).

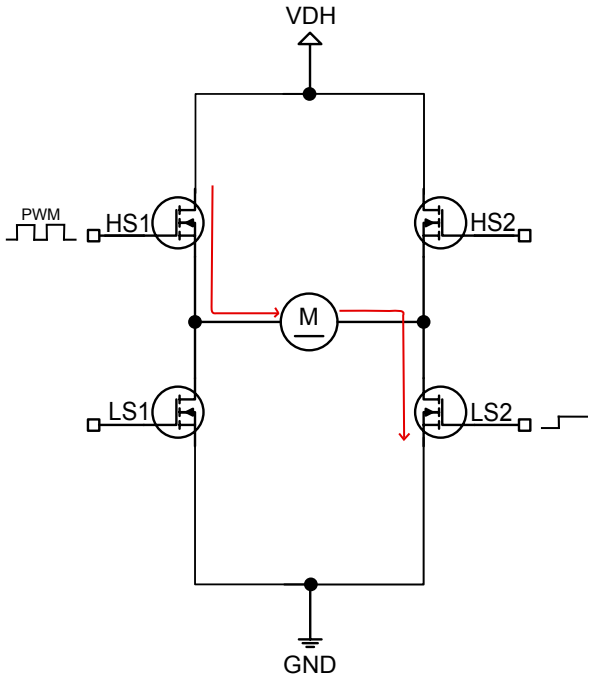
Table 2. Free-wheeling path when DIR = 0

OUTE bit	AFWE	FWS	FSINB	DIR	PWM	HS1	LS1	HS2	LS2
1	0	0	1	0	0	OFF	OFF	OFF	ON
1	X	X	1	0	1	ON	OFF	OFF	ON
1	0	1	1	0	0	ON	OFF	OFF	OFF

When DIR = 0 (CW rotation) and when PWM = 1, independently on how AFWE and FWS are configured, the MOSFETs HS1 and LS2 are activated:

- In the case where FWS = 0, the freewheeling is applied on the low side part, so the PWM signal is applied on the high side 1 that turns off when PWM = 0, while the low side 2 MOSFET is ON.

Figure 2. PWM signal applied on HS1



- Instead, when FWS = 1 the freewheeling (active or passive depending on how AFWE is set) is applied on the high side part of the bridge, meaning that the PWM signal is applied on the low side 2 MOSFET (turns off with PWM = 0) while the high side 1 MOSFET is ON.

Figure 3. PWM signal applied on LS2

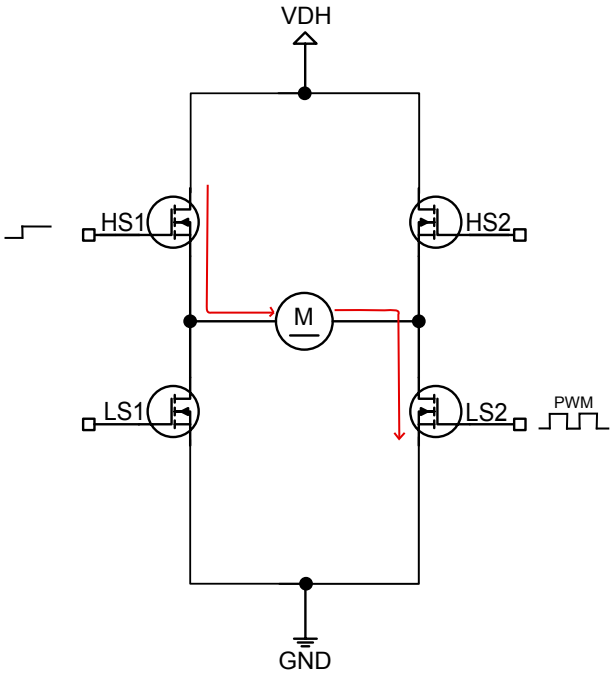


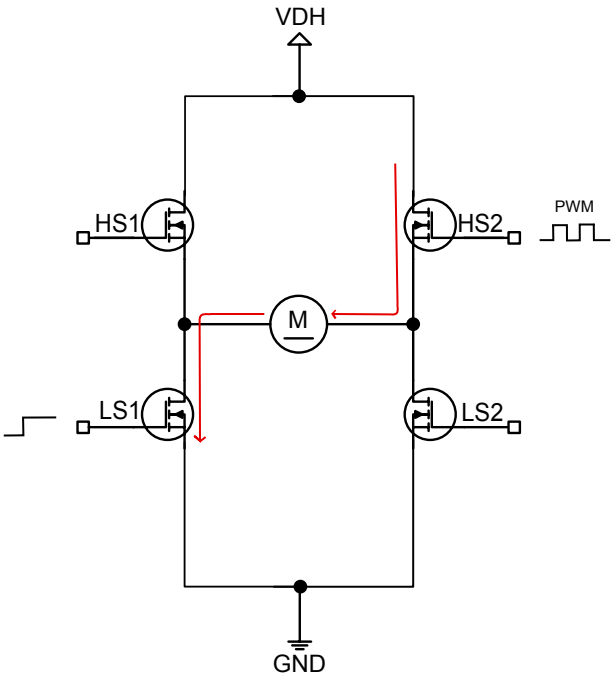
Table 3. **Free-wheeling path when DIR = 1**

OUTE bit	AFWE	FWS	FSINB	DIR	PWM	HS1	LS1	HS2	LS2
1	0	0	1	1	0	OFF	ON	OFF	ON
1	X	X	1	1	1	OFF	ON	ON	OFF
1	0	1	1	1	0	OFF	OFF	ON	OFF

When DIR = 1 (CCW rotation) and when PWM = 1, independently on how AFWE and FWS are set, the MOSFETs LS1 and HS2 are activated:

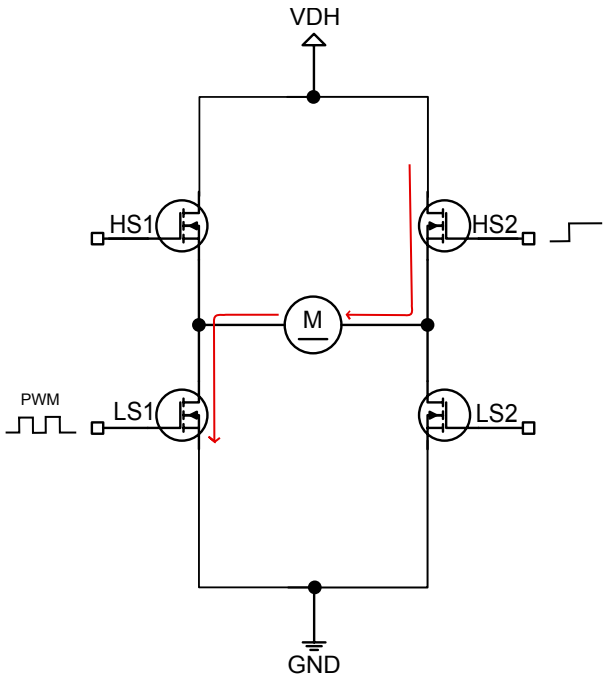
- In the case where FWS = 0, the freewheeling is applied on the low side part, so the PWM signal is applied on high side 2 that turns off when PWM = 0, while the low side 1 MOSFET is ON.

Figure 4. **PWM signal applied on HS2**



- Instead, when FWS = 1 the freewheeling (active or passive depending on how AFWE is set) is applied on the high side part of the bridge, meaning that the PWM signal is applied on the low side 1 MOSFET (turns off with PWM = 0) while the high side 2 MOSFET is ON:

Figure 5. PWM signal applied on LS1



– If INPMODE = 1, the device works in dual half-bridge mode. The two half-bridges can be driven separately by IN1 and IN2 input pins and can be individually disabled through DIS1 and DIS2 control bits.

Table 4. Dual half-bridge mode

Device in active mode with INPMODE = 1 (DUAL HALF - BRIDGE MODE)				
Inputs			Outputs (in case of no faults); x = 1, 2	
FSINB	OUTE bit	DISx bit	HSx	LSx
1	1	0	Inx	$\overline{Inx}$
1	0	x	OFF(1)	OFF(1)
All the other cases			OFF	OFF

1. *In this case, the MOSFET is passively switched off through the internal resistive connection between the gate and related source. In all the other cases where the MOSFET is off, it is actively switched off and forced off by the gate driver working in sink switch mode.*

Note: "Inx" means ON if the logic level on Inx pin input is high and vice versa."$\overline{Inx}$" means OFF if the logic level on Inx pin input is high and vice versa (x = 1, 2).

1.4 SPI control

The L99H92 uses the ST-SPI protocol to communicate with a microcontroller. The ST-SPI is a standard used in ST automotive ASSP devices. The ST-SPI allows usage of generic software to operate the devices while maintaining the required flexibility to adapt it to the individual functionality of a particular product. In addition, fail-safe mechanisms are implemented to protect the communication from external influences and wrong or unwanted usage. The device serial peripheral interface is compliant to the ST-SPI standard rev 4.1.

1.4.1 SPI commands

What is managed by SPI command are:

- Freewheeling control
- VDS monitoring
- Charge pump configuration
- Over/undervoltage recovery actions
- Gate charge and discharge current configurations
- Current sense amplifier configuration
- Watchdog control

1.4.2 SPI diagnostics

The in-frame response SPI protocol provides the general health and well-being of the H-Bridge in a global status byte on the SDO pin every time the host micro provides the op-code and address during a command SPI frame. More detailed diagnostics are available in the status registers. The contents of the address given is returned when the data bits are clocked in.

The diagnostics available in total are:

- Global error
- SPI frame error
- Reset event
- Thermal events
- Under/overvoltage event
- Watchdog timeout
- VDS fault
- Charge pump low event

More details can be found in the L99H92 datasheet.

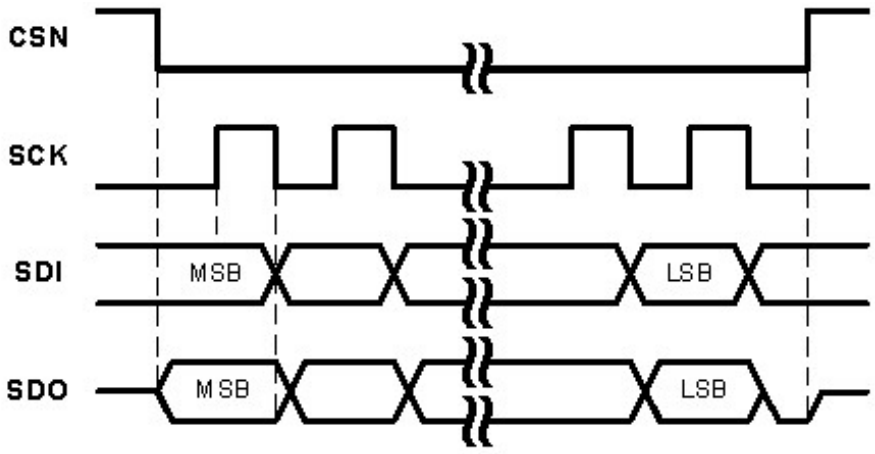
1.4.3 SPI parameters

The ST-SPI can be driven by a microcontroller with a classical SPI peripheral running in the following configuration:

- CPOL = 0
- CPHA = 0

The ST-SPI bus clocks in data on the rising edge and clocks out data on the falling edge (see the Figure 6). The CSN pin is held low during SPI transmission.

Figure 6. SPI protocol description



The following requirements must be respected:

- The clock signal must be low when the CSN falling edge occurs.
- The SDI data is latched at all the following rising CLK edge into the internal shift register.
- After communication start, the SDO will leave tri-state mode and will present the MSB of the data shifted out to SDO.
- At the following falling clock edges data is shifted out through the internal shift registers to SDO.
- The communication frame is finished with the rising edge of the CSN.

A SPI-SDI frame is 24 bits long and it is so composed:

- OC (op code) → 2 bits
- Address → 6 bits
- Data byte 2 → 8 bits
- Data byte 1 → 8 bits

The first two transmitter bits contain the operation code, which represent the command/instruction that is performed. The following 6 bits represent the address on which the command/operation will be performed.

A SPI-SDO frame is 24 bits long and it is so composed:

- GSB (global status byte) → 8 bits
- Data byte 2 → 8 bits
- Data byte 1 → 8 bits

The first eight transmitted bits contain device related status information and are latched into the shift register at the time of the *communication start*.

The GSB byte is transmitted at every SPI transaction.

For the definition of the full structure and the register content of the SPI, please, refer to the L99H92 datasheet.

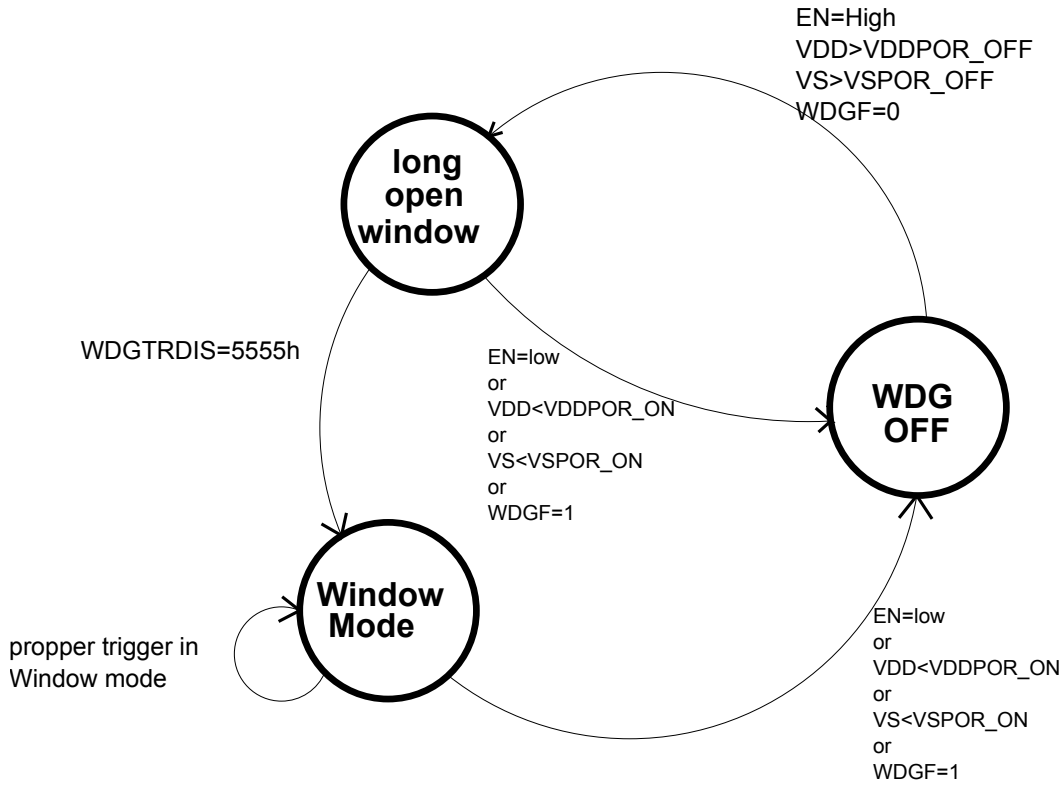
1.5 Watchdog function

The task of the watchdog is to monitor the microcontroller during normal operation. To perform this function that some different tasks have been implemented (see the Figure 7).

- **Long open window.** By default, as soon as the device enters in active mode (EN = high, VDD > V_{DDPOR_OFF}, VS > V_{SPOR_OFF}, WDGF = 0), the watchdog is enabled and start running with a “long open window”. This is to provide more time to the microcontroller for the L99H92 initialization and allows the watchdog disabling procedure, if required, to be run.
- **Window mode.** To enter in “window mode” configuration, the microcontroller must write the word 5555h into the watchdog trigger/disable register (WDGTRDIS) before the end of the long open window. In window mode the microcontroller must send the watchdog trigger bits by the watchdog trigger/disable register (WDGTRDIS) within the watchdog open window. Any correct watchdog trigger SPI frame starts a new window. If no correct watchdog service is sent from the microcontroller, the device is put in fail-safe mode, all gate drivers switch to a sink condition and the watchdog time-out bit (WDTO) is set.
- **Fail-safe mode.** In case of watchdog failure (EN = low or VDD < V_{DDPOR_OFF} or VS < V_{SPOR_OFF} or WDGF = 1) or no correct watchdog service, the device is put in fail-safe mode and the WDGF flag is set. In this case the OUTE control bit is reset and the gate drivers are forced in sink switch mode in order to switch off actively all the MOSFETs with the max available current. To reactive the gate drivers, the WDGF flag must be cleared and the OUTE control bit must be set, both via SPI.
- **Watchdog disabling.** To disable the watchdog, the microcontroller must write a specific key, consisting in two consecutive valid SPI frames (2F6Bh and 1097h) to be sent in the right order before the end of the long open window. Just one attempt to disable the watchdog is allowed in a long open window. If not successful, a watchdog fault is generated, and it is no possible to disable the watchdog until the next long open window.

The watchdog register is a particular register as the data to be written is different from that to be read. For a more accurate description of the watchdog register, please, refer to the L99H92 datasheet, SPI registers section.

Figure 7. Watchdog state diagram

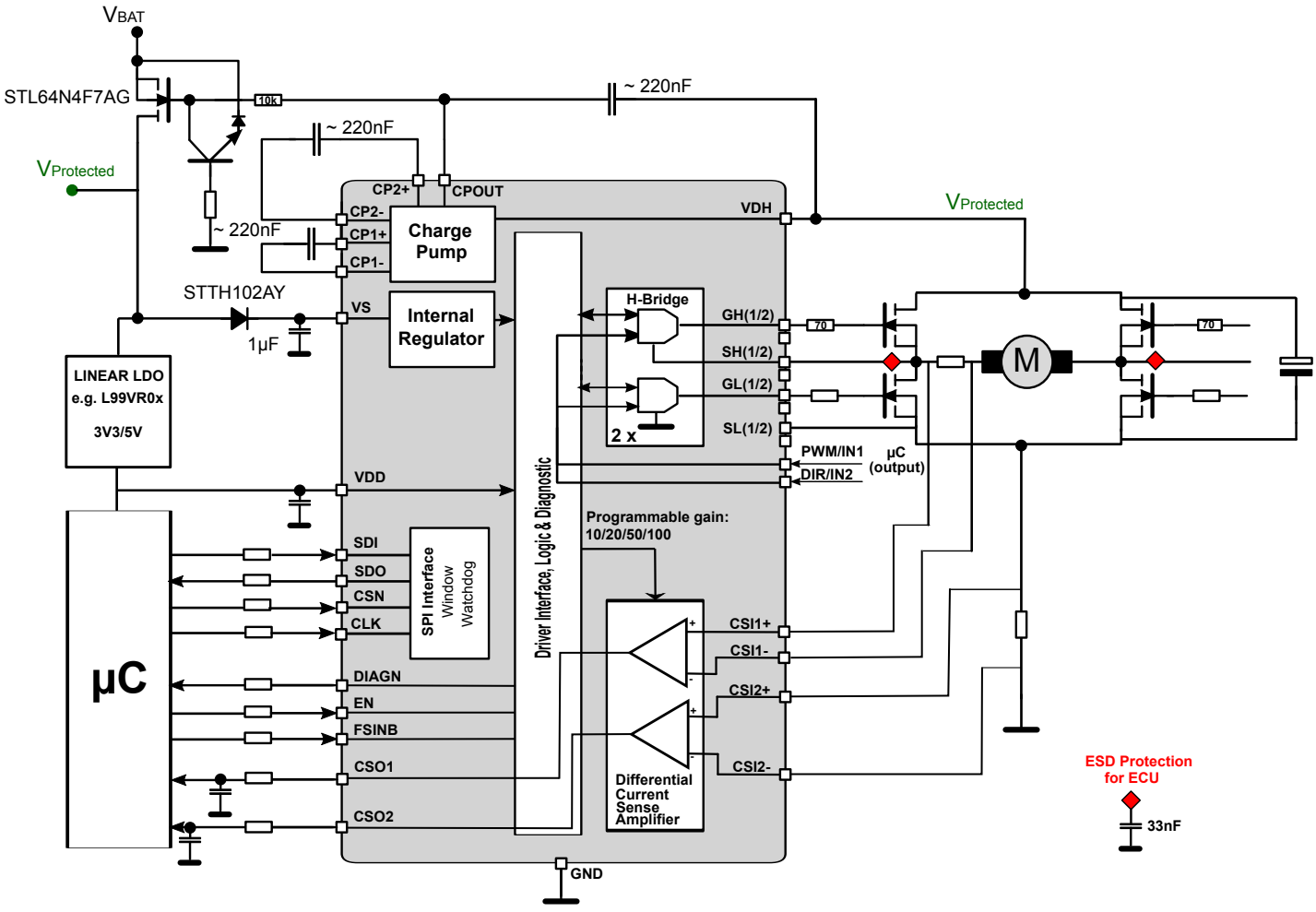


2 Application circuit

There are a few external components that are required to fully use the features of the L99H92. These include charge pump capacitors, gate resistors, sense resistors, MOSFETs for the H-bridge and an additional MOSFET for reverse battery protection if needed.

It is assumed that the application is high current or other less complex solutions would be pursued. When considering high current H-Bridge motor control applications, active recirculation is preferred to minimize the power dissipation in the H-Bridge. Most H-Bridge applications are driving bidirectional motors. As a result, this design guide covers driving bidirectional, higher current motors. For an accurate version of the application schematic and BOM, please, refer to the package of application boards that are available on the ST website.

Figure 8. Application and block diagram



This application note breaks down each individual aspect of the design starting with the hardware selection including circuit board layout guidelines and software considerations.

3 Determining the proper MOSFET for the H-Bridge

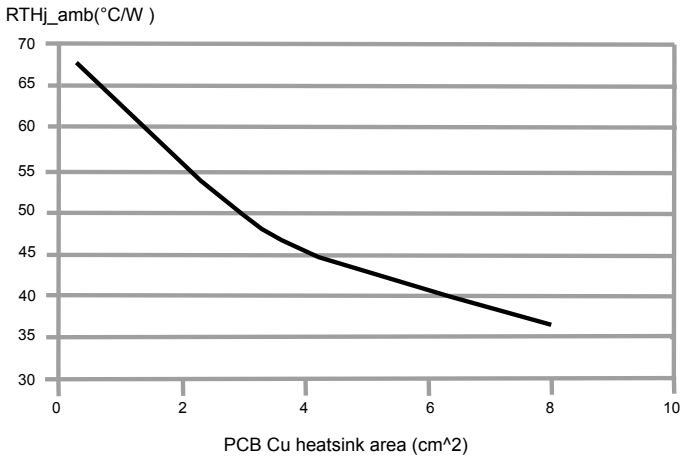
MOSFET selection requires knowing several parameters such as, maximum voltage, maximum current, maximum ambient temperature, and the switching speed required. With that you can narrow your search for the proper MOSFET.

The limiting factor in any surface mounted power device is the capability of the circuit board to dissipate heat. That capability is dependent on several parameters. Circuit boards come in many different flavors. From single sided to multilayer boards, from ½ Oz copper to 10 Oz copper or more.

A two-sided board with 2 ounce copper (70 µm) and thermal vias provide a reasonable amount of heat sinking for a given amount copper area. A four-layer board provides better thermal conductivity.

For a DPAK sized MOSFET on a two-sided board a general rule of thumb would be approximately 35 °C/W with a total of 8 cm^2 of copper area under the part applies to a typical DPAK MOSFET on a two-sided FR4 board: most of the thermal impedance in this system is in the circuit board.

Figure 9. Typical thermal resistance for a DPAK vs. Cu area



Note: Layout condition of Rth measurements (double sided PCB FR4 area = 58 mm x 58 mm, PCB thickness = 1.8 mm, Cu thickness = 2 Oz, copper areas: from minimum pad lay-out to 8 cm^2 on the back side).

When using a DPAK, adding two more (inner) layers improves the thermal impedance to better than 25 °C/W (for 8 cm^2 Cu area) with an optimized layout.

There are two ways of considering the maximum allowable $R_{DS(on)}$. The first method is using the maximum allowable junction temperature to be the upper limit in power dissipation. Junction temperature can be calculated by the following equation:

Simple junction temperature

$$T_{Junction} = P_{Diss} \times R_{th(j-a)} + T_{Amb} \quad (1)$$

Power dissipation comes from two things: conduction losses and switching losses. Conduction losses are a function of the square of the current times the $R_{DS(on)}$ of the switch. $R_{DS(on)}$ changes with temperature. For a typical MOSFET, the $R_{DS(on)}$ doubles between 25 °C and 175 °C. A reasonable equation for $R_{DS(on)}$ over temperature then looks like:

$R_{DS(on)}$ as a function of junction temperature

$$R_{DS(on)}(T_J) = R_{DS(on)@25°C}\left(1 + \frac{T_J - 25°C}{150°C}\right) \quad (2)$$

We insert this into Eq. (1) above and add switching losses then solve for $R_{DS(on)}$:

Max allowable $R_{DS(on)}$ when using junction temperature alone

$$R_{DS(on)\max} = \frac{150°C\left(T_{J\max} + T_{Amb\_\max} - P_{SW}R_{th(j-a)}\right)}{I_{load}^2 R_{th(j-a)}\left(125°C + T_{J\max}\right)} \quad (3)$$

Where:

- T_{Jmax} = maximum rated temperature of the FR4 circuit board
- T_{Amb_max} = maximum ambient temperature for the application
- $R_{th(j-a)}$ = estimated thermal resistance from junction to ambient
- P_{SW} = switching losses (refer to the Eq. (10))

Just using this equation alone can get you in trouble. The concern with higher power in surface mounted power devices is the temperature of the circuit board itself. A typical DPAK MOSFET has a thermal resistance junction to case (Rth(j-c)) around 2 °C/W. The circuit board is then the next 33 °C/W (using the 2-sided board example). Simple resistor division indicates that the circuit board under the part will not be much different in temperature than the Junction. MOSFET junction temperatures can safely reach 175 °C. Even at 4 W, that drops the temperature down to 167 °C at best at the tab. Most FR4 cannot handle that heat. As a result, we start with the max circuit board temperature as the limiting parameter and work backwards.

Circuit board temperature

$$T_{PCB} = T_{Junction} - P_{DISS} \times R_{th(j-c)} \quad (4)$$

Combining the Eq. (1) with Eq. (4) provides for the maximum power each MOSFET can dissipate using the circuit board as the limiting factor:

Maximum power dissipation

$$P_{diss\_max} = \frac{T_{PCB\_max} - T_{Amb\_max}}{R_{th(j-a)} - R_{th(j-c)}} \quad (5)$$

Where:

- T_{PCB_max} = maximum rated temperature of the FR4 circuit board
- T_{Amb_max} = maximum ambient temperature for the application
- $R_{th(j-a)}$ = estimated thermal resistance from junction to ambient
- $R_{th(j-c)}$ = published thermal resistance from junction to case

We are looking for the maximum allowable $R_{DS(on)}$ for a given system. Given the thermal resistances and circuit board limitations the maximum 25 °C $R_{DS(on)}$ that can be safely used in a system is calculated by:

Maximum acceptable $R_{DS(on)}$

$$R_{DS(on)\_max} = \frac{150°C \times \left(T_{PCB\_max} - T_{Amb\_max} - P_{SW} \times R_{th(j-c)}\right)}{I_{load}^2 \times \left[R_{th(j-a)} \times \left(T_{PCB} + 125°C\right) - R_{th(j-c)} \times \left(125°C + T_{Amb\_max}\right)\right]} \quad (6)$$

Where:

- I_{load}^2 is the square of the maximum expected motor current at T_{Amb_max}.
- $R_{DS(on)\_max}$ is the highest the MOSFET 25 °C $R_{DS(on)}$ can be not to dissipate too much heat to hurt the circuit board.
- P_{SW} is the losses due to switching (refer to the Eq. (10)).

Note: This ignores any benefits due to duty cycle while including switching losses. As a result, this is an absolute worst-case condition.

It is important to note that motor run/stall currents change with temperature. The hotter the motor the lower typically the current becomes, as the winding resistance goes up with heat.

3.1 Layout guidelines

Power dissipation capability in the copper is reduced as you get further away from the device.

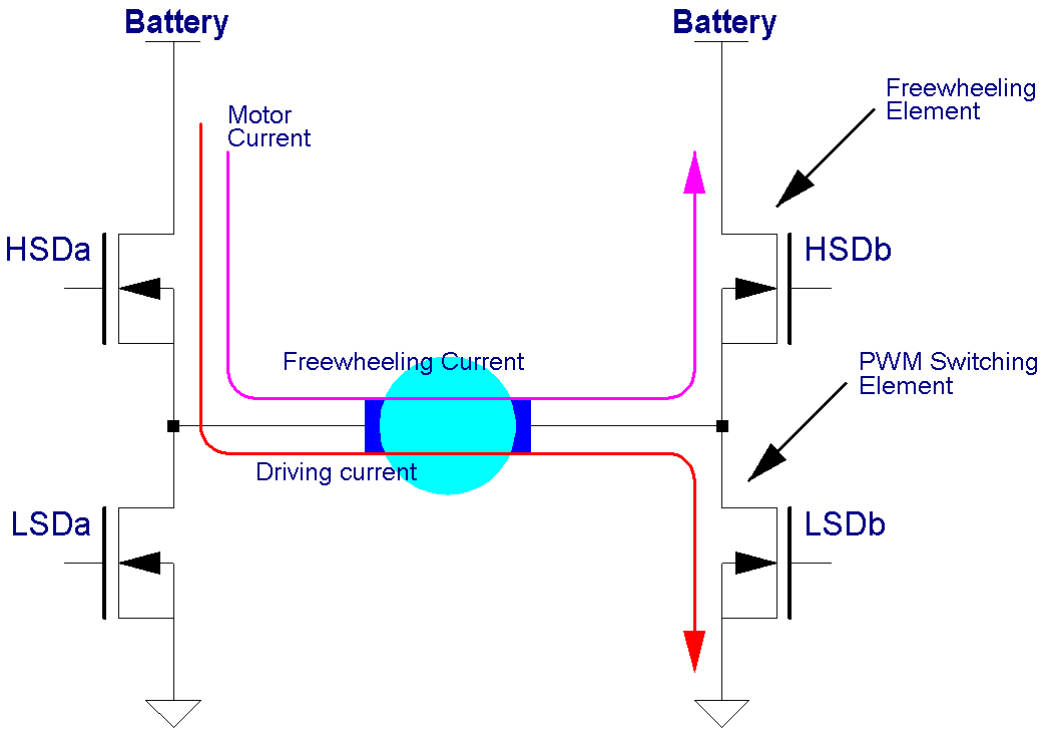
3.2 MOSFET power dissipation calculations

With a general idea of the thermal impedance of the application, MOSFET selection turns to power generation. There are two components to MOSFET power dissipation: conduction losses and switching losses. Conduction losses are only present when the switch is active. Switching losses only contribute when PWMming and then only on the switching component.

3.2.1 Conduction losses

Conduction losses are simply I^2R losses. In an H-Bridge configuration there are two elements that are on at the same time. While driving the load the high side of one leg and the low side of the other leg (or vice versa) are active and conducting load current. If PWMming, then the conduction losses in the switching element is reduced by the duty cycle as the freewheeling element shares in the conduction losses at 1 - %duty cycle.

Figure 10. Currents in an H-Bridge (low side PWM)



The MOSFET switch power equations when low side PWMming would look like:

Power dissipation in the always-on high side switch (HSDa)

$$P_{Cond\_HSDa} = I^2 \times R_{ON(HSDa)} \quad (7)$$

Power dissipation in the PWMmed driving low side switch (LSDb)

$$P_{Cond\_LSDb} = I^2 \times R_{ON(LSDb)} \times Duty \quad (8)$$

Power dissipation in the freewheeling high side switch (HSDb)

$$P_{Cond\_HSDb} = I^2 \times R_{ON(HSDb)}\left(1 - Duty\right) \quad (9)$$

Where:

- P_{Cond_XSDx} = conduction losses in each of the H-Bridge elements. When driving an inductive (motor) load P_{Cond_HSDb} is included.
- I = load current
- R_{ON_HSDa} = $R_{DS(on)}$ of the conducting high side switch

- R_{ON_LSDb} = $R_{DS(on)}$ of the conducting (PWMmed) low side switch
- R_{ON_HSDb} = $R_{DS(on)}$ of the freewheeling high side switch
- $Duty$ = % PWM duty cycle of the low side switch.

If there is no PWMming then the third equation (see the Eq. (9)) disappears. When calculating conduction losses in the freewheeling element it is assumed that the load is inductive, and that the system is turning on the freewheeling element during recirculation.

3.2.2 Switching losses

Switching losses are a result of the driver behaving as a linear output for very short periods of time. The MOSFET is not on or off. It is effectively being driven *linearly* from one rail to the other.

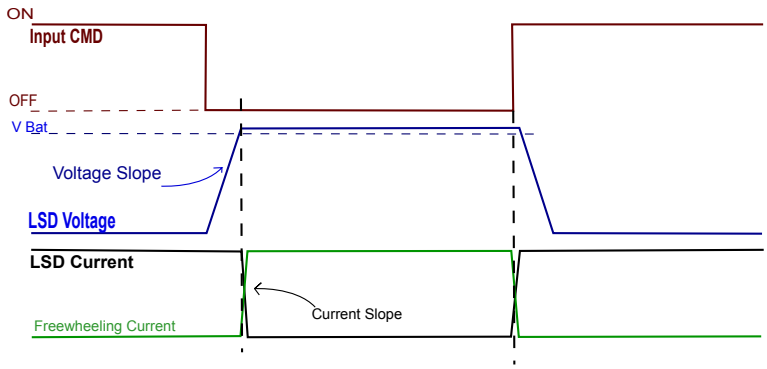
In a PWMmed H-Bridge application there are two elements that are switching. In the example shown in the Figure 10 the low side switch, LSDb, is the driving element and the high side switch, HSDb, is the freewheeling element. However, only the driving element experiences switching losses.

In our example (see the Figure 10) when LSDb turns off, the current slope becomes negative. A negative current slope in the motor inductance causes the voltage at the motor to invert (becomes negative with respect to what it was originally). The voltage climbs until the diode in the freewheeling MOSFET starts to conduct current. That is, there is no current flow in the freewheeling element (high side switch in our example) until the forward voltage of the MOSFET's body diode is satisfied (~0.7 V).

This works in both directions. The current starts or stops flowing in the freewheeling element when the voltage across it is low (see the Figure 11). As a result, there is no linear control occurring at the freewheeling element. Thus, no switching losses.

There is only one switch in the system that experiences switching losses, the PWM switching element (LSDb in our example). Switching losses are different for inductive or motor type loads than they are for resistive loads. For resistive loads, the current is proportional to the voltage across the load (ohm's law). In an inductive load, the current is constant through the entire switching time and only changes once the freewheeling or driving element starts conducting. As a result, the equations that describe the losses during switching are different.

Figure 11. Low side PWM switching curves for an inductive load



A reasonable first order estimation on switching losses is to assume a trapezoidal waveform while ignoring the losses due to the current switching. The current switching losses are typically an order of magnitude less than the losses due to the voltage slope. Inductive switching losses can be estimated in the following equation.

Inductive switching losses

$$P_{Switch} = V_{Bat} I_{Ave} \frac{t_{rise} + t_{fall}}{2} f_{PWM} \quad (10)$$

Where:

- V_{Bat} = supply voltage
- I_{Ave} = average current due to PWMming
- $t_{rise} + t_{fall}$ = rise and fall times during switching
- f_{PWM} = switching frequency

This power equation works for either the high side PWMming or the low side PWMming.

3.2.3 Total losses

The total losses calculated are the sum of the conduction and switching losses from the Eq. (7), Eq. (8), Eq. (9), and Eq. (10). Where the driving (PWMmed) element losses include both conduction and switching. In our example that would be the Eq. (8) and Eq. (10).

Total losses in the PWMmed MOSFET switch

$$P_{MOSFET} = I^2 R_{ON(LSDb)} Duty + V_{Bat} I_{Ave} \frac{t_{rise} + t_{fall}}{2} f_{PWM} \quad (11)$$

It is understood that the $R_{DS(on)}$ is a function of junction temperature. Using the Eq. (2) for $R_{DS(on)}$ in the Eq. (11) obtains a more accurate power dissipation equation in the MOSFET.

Total losses including the temperature effects on $R_{DS(on)}$

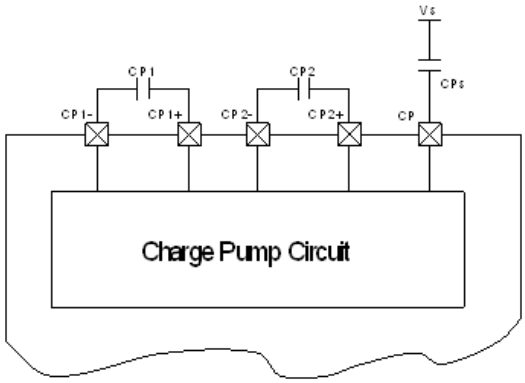
$$P_{MOSFET}\left(T_J\right) = I^2 R_{DS(on)@25°C}\left(1 + \frac{T_J - 25°C}{150°C}\right) Duty + V_{Bat} I_{Ave} \frac{t_{rise} + t_{fall}}{2} f_{PWM} \quad (12)$$

4 Calculating charge pump capacitor values

The L99H92 uses a 2-stage charge pump. This configuration can maintain good gate drive voltages during low voltage operation. There are three charge pump capacitors. Two are for generating the boost and one for storage. The charge pump supplies both the high side and low side MOSFET gate drive circuits.

The datasheet recommends that all three charge pump caps be 220 nF ceramic, 50 V capacitors. Most any application can use these suggested values. It is only in the most extreme cases where there is a large number of very low ohmic MOSFETs in parallel that consideration must be made for the charge pump capacitors.

Figure 12. Charge pump



The charge pump storage (CPs) capacitor should be connected to supply and not ground. As the supply changes the charge pump storage voltage will “float” with it. This is not possible if the cap is tied to ground.

The charge pump frequency is 400 kHz typically and it is independent of the power supply voltage used.

4.1 Average charge pump current draw

The charge pump supplies current to both the high and low side MOSFETs. This guarantees a fully enhanced MOSFET even at very low battery voltages. The only time there is meaningful current draw from the charge pump is during PWMming. That means at most only one low side element and one high side element are PWMming. This occurs when using active freewheeling while driving an inductive load. It should be noted that if you are not driving an inductive type of load then active freewheeling is not recommended.

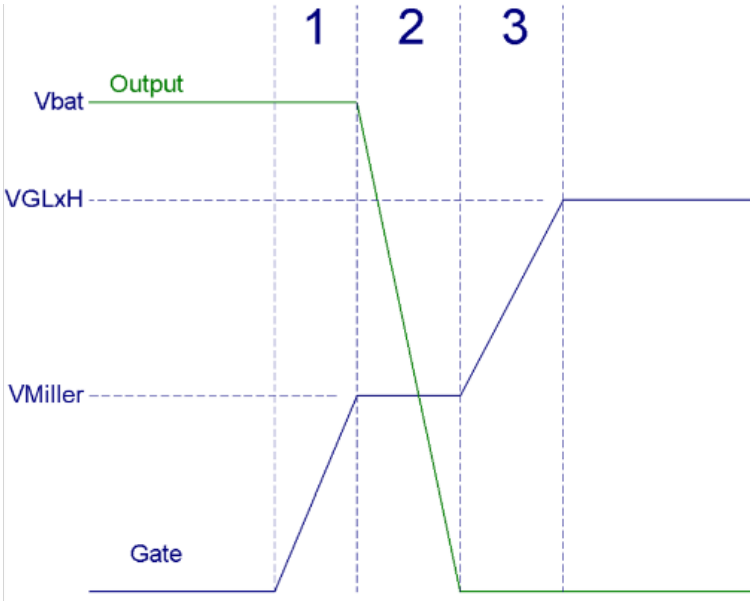
For the example shown in the Figure 10 the switching elements are the LSDb and HSDb MOSFETS. The high side current draw is simple, in that the drain and source voltage do not change. Only the charging of the input capacitance due to the gate voltage rising.

High side switch average charge pump load

$$I_{CP\_HS(ave)} = C_{iss} \times (V_{GHxH} - V_{Bat}) f_{PWM} \quad (13)$$

When considering the low side there are three regions of interest.

Figure 13. **Low side MOSFET gate charge regions**



The equations for these three regions are as follows:

Current sources in the different regions of the low side MOSFET at turn on

$$Region1 = C_{iss} \times V_{GSth} \quad (14)$$

$$Region2 = C_{rss} \times V_{Bat} \quad (15)$$

$$Region3 = C_{iss} \times (V_{GLxH} - V_{GSth}) \quad (16)$$

Adding these three together and inserting the Eq. (13) then multiplying them by the PWM frequency provides the total average current draw from PWMming.

Total charge pump current draw (low side PWM)

$$I_{CP\_ave} = [C_{iss\_HS}(V_{GHxH} - V_{Bat}) + C_{iss\_LS}V_{GLxH} + C_{rss\_LS}V_{Bat}]f_{PWM} \quad (17)$$

Note: Adding the equations from Region1 and Region3 removes the threshold voltage from the equation. We can simplify this further in that C_{rss} is typically orders of magnitude lower than C_{iss}. Therefore, its contribution is not significant.

The charge pump is specified to be able to supply maximally 70 mA ($I_{CP(max)}$) at 13.5 V.

Table 5. **STD65N55F3 dynamic parameters**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
-	Forward transconductance	VDS = 25 V, ID = 32 A	-	50	-	S
C_{iss}	Input capacitance	VDS = 25 V, f = 1 MHz, VGS = 0	-	2200	-	pF
C_{Oss}	Output capacitance			500		pF
C_{rss}	Reverse transfer capacitance			25		pF
Q_g	Total gate charge	VDD = 27 V, ID = 65 A VGS = 10 V	-	33.5	45	nC
Q_{gs}	Gare-source charge			12.5		nC
Q_{gd}	Gate-drain charge			9.5		nC

Using an STD65N55F3 (a 6.5 mΩ MOSFET) as an example of a low ohmic device we have a C_{iss} of 2200 pF. If we bump that up by 50% for absolute worst case the total C_{iss} is 3300 pF. The average DC current from the Eq. (18) is 1.52 mA at V_{Bat} = 12 V:

Calculating the average charge pump current

$$I_{CP\_ave} = (3300pF \times (26V - 12V) + 3300pF \times 12V + 25pF \times 12V) \times 20kHz = 1.59mA \quad (18)$$

This is much lower than the maximum specified charge pump capability of 70 mA.

5 Gate resistance

Gate resistors are used in the H-Bridge applications to control the rise and fall times on the MOSFET switching elements. Rise and fall times influence the power dissipation in the system in terms of switching losses and, also, they contribute to radio frequency interference or RFI. The faster the switching speeds the lower the power dissipation due to switching losses. However, faster switching speeds also generate more RFI. If a shorter time is required two different actions can be taken:

- Change the MOSFET to one with a lower gate capacitance.
- Change the driver to one that can provide more current.

Instead, if a longer time is required more option are available. For example, a solution can be to add more capacitance to the gate by adding an extra capacitor towards ground.

The most common way of controlling the rise and fall times is to add a series resistor to the driver output. Normally the effects of this resistor are:

- Gets the driver, requiring more voltage for the same current, faster out of its current source region into its linear region.
- Once in linear region, the effective source resistance of the driver will be higher, so the time-constant of the charge-up or down of the capacitor will be larger.

The series resistor method is ineffective if the driver is truly a current source: this is the case of L99H92.

The L99H92 gate drivers, thanks to the possibility to drive the MOSFET gates using a programmable constant current, have two main advantages:

- The slew rate of the power stage is controlled allowing a precise EMI management.
- No gate resistors are required reducing the number of components in the bill of material.

The output slew rate depends on how fast the MOSFET gate is charged in the Miller plateau region. In a classical gate driver the charging/discharging current is adjusted adding a resistor between the gate driver output and the MOSFET gate. This way the output slew rate can be limited, but its value depends on the load current.

Using a true current generator, the L99H92 gate driver forces a constant gate current during the entire plateau region regardless of the load current.

The L99H92 implements a rising and falling currents control through the “slew-rate control” (SLEWzx) bits.

The SLEWzx register can be set in two different ways:

- **SLEWzx bits are all set to 0**. In this case the gate drive circuits work in switch mode and they provide the maximum available current. This one is internally limited at 420 mA (typ) according to the specification (IGHx(Ch), IGLx(Ch)), and it is the same for high and low sides.
- **SLEWzx bits are different from 0**. If any value different from zero is programmed on SLEWzx bits, the gate drivers work as current source providing a fixed current as long as the during the MOSFET turning on/off the drain-source voltage is above/below the switch threshold (VDSHxrSW and VDSHxfSW). Once the switch threshold (drain-source voltage drops below 1.14 V, see the Figure 14) is reached, the drivers work in switch mode. Also, the gate drivers source (charge) and sink (discharge) currents can be independently programmed through dedicated control bits to have different output voltage slopes during the turning on and the turning-off of the MOSFETs. The gate current is set in according to the following formula:

I_{GATE} setting

$$I_{GATE} = \frac{SLEWzx[4:0]}{31} * I_{GATEMAX} \quad (19)$$

The rise time to charge the gate is a function of the C_{iss} and the gate current by the equation:

Rise time to charge the gate

$$t_{rise} = C_{iss} \times \frac{V_{Gate}}{I_{Gate}} \quad (20)$$

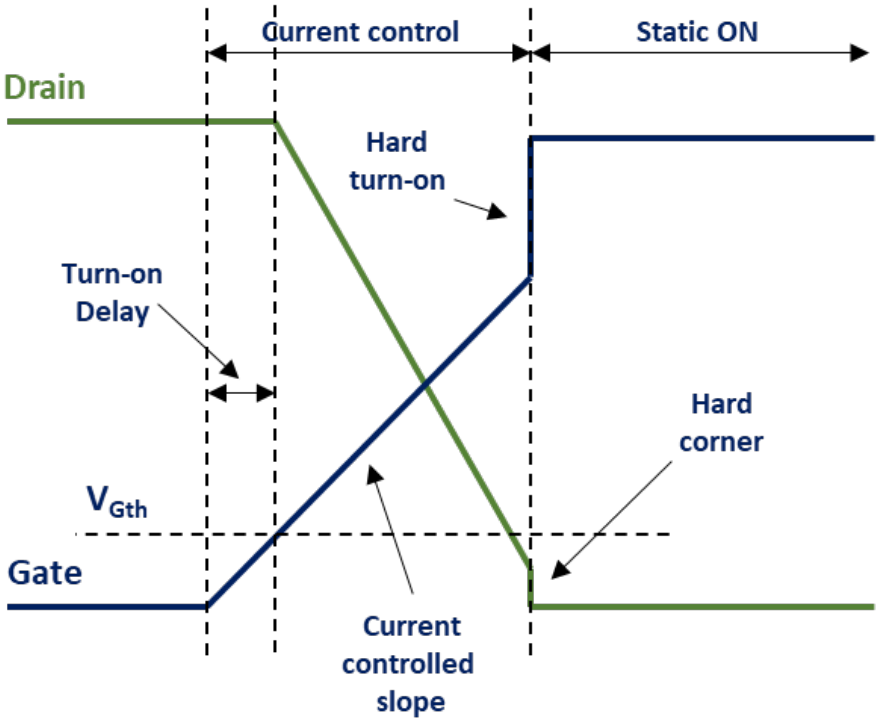
Going one step further and calculating the potential rise time to charge the gate charge we obtain:

Calculating the rise time to charge the gate

$$t_{rise} = 3300pF \times \frac{12V}{170mA} = 233ns \quad (21)$$

So, considering the maximum available current and absolute worst case of capacitor to download, a rise time of 233 ns is necessary to charge the gate.

Figure 14. SLEWzx bits different from 0

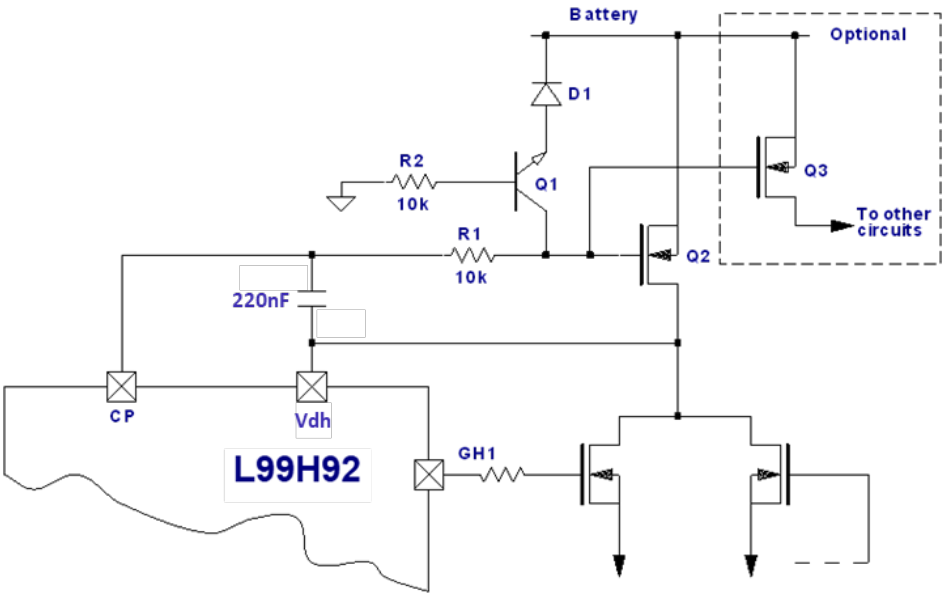


6 Reverse battery component selection

The fifth MOSFET and associated circuitry blocks current when the module is exposed to a negative voltage. This circuit is not intended to stop negative transients. This only provides an accidental reversal of the battery terminals during battery installation. The circuit is simple. We take advantage of the charge pump storage voltage and add an N-Channel MOSFET with the source tied to battery and the drain connected to the upper H-Bridge MOSFET drains.

There are five components to select (R1, R2, D1, Q1 and Q2). They are all necessary for proper and safe operation.

Figure 15. Reverse battery circuit



During a reverse battery condition this circuit turns on Q1 thereby limiting the voltage at the gate-source terminals of Q2 to just over 0.7 V, keeping Q2 (and Q3) off. The resistors are there to limit the current in Q1 during the reverse battery condition. R2 limits the base current in Q1 during reverse battery. R1 limits the Q1 collector current thus allowing a voltage drop between the charge pump output, CP, and the gate of Q2.

D1 is required to block battery voltage during normal operation. The typical reverse voltage capability of a standard small signal NPN transistor is around 7 V. This is not enough to survive normal operating voltages. D1 must have a high enough breakdown voltage to sustain any positive transients this circuit might experience. In automotive, this is typically 100 V (ISO 7637-2).

Q1 must safely drive the current in R1 with the base current created by R2. With 10 kΩ resistor values the base current is ~1 mA. The collector current is similar. This makes for an inexpensive transistor. Due to the charge pump, the collector voltage reaches approximately 13.5 V above battery. The NPN bipolar transistor collector to emitter breakdown voltage (BVCEO) will need to be sufficient to sustain that voltage.

This circuit can be used to protect not only the H-Bridge but also the rest of the module as well from reverse battery. In some cases, the noise at VS can be a concern to other more sensitive circuitry. With that, a second inverted MOSFET (Q3) can be installed in parallel with Q2. This is done by tying the gate and the source to the same nodes of Q2 and allowing the drain to drive the rest of the module. Q3 can be scaled to accommodate the type of loads that it supports. There would be no need, for instance, to have a very low ohmic MOSFET for a simple 1 A or less load.

7 Current sense design

The current sense amplifiers (CSA1 and CSA2) are specially designed for current shunt automotive applications. They are independent, bidirectional, single-supply difference amplifier for amplifying small differential voltages in a wide common mode voltage range. They support the current measurement at two shunts. The CSO outputs are compliant to the VDD power supply rail and have a programmable offset set by CSA1OO and CSA2OO control bits. If these bits are reset, the output offset is set to VO0, otherwise it is set to VO1. The current sense amplifiers input stage is supplied by the charge pump, so when the charge pump is disabled the CSAs is disabled as well.

By default, both current sense amplifiers are enabled, to reduce current consumption they can be disabled independently through control bits DCSA1 and DCSA2.

The inputs (CSI1+/CSI1- and CSI2+/CSI2-) are constructed as a transconductance stage. Therefore, a series resistor (for filtering etc.) should not exceed 50 Ω to keep the additional gain error below 1%.

7.1 Placing the sense resistors

The L99H92 has the option of placing two sense resistors. This option is there to fully mitigate all possible short circuit conditions. Placing one sense resistor in the leg of the H-Bridge and one in the ground, or in the supply, provides confirmation that the currents are flowing where they should. With this configuration a short of any kind can be detected.

Table 6. Fault detection methods

Fault		Description
Short to ground at either leg	1	VDS fault on High side switch Ground sense resistor reports zero current Leg sense resistor reports zero current
	2	VDS fault on High side switch Ground sense resistor reports zero current Leg sense resistor reports high current prior to VDS fault
	3	NO VDS fault Ground sense resistor reports zero current Leg sense resistor reports normal current
Short across the load	1	Possible VDS fault on either active elements Ground and leg sense resistors report high current (prior to VDS fault)
Short to supply at either leg	1	VDS fault on low side switch No current in leg sense resistor prior to VDS fault Ground sense resistor reports high current prior to VDS fault
	2	VDS fault on ground sided elements Leg sense resistor reports high current prior to VDS fault Ground sense resistor reports high current prior to VDS fault
Shorted MOSFET	1	VDS fault on opposite switch in same leg High current in ground sense resistor prior to VDS fault No current in leg sense resistor
	2	Normal operation… Not detectable in one direction only

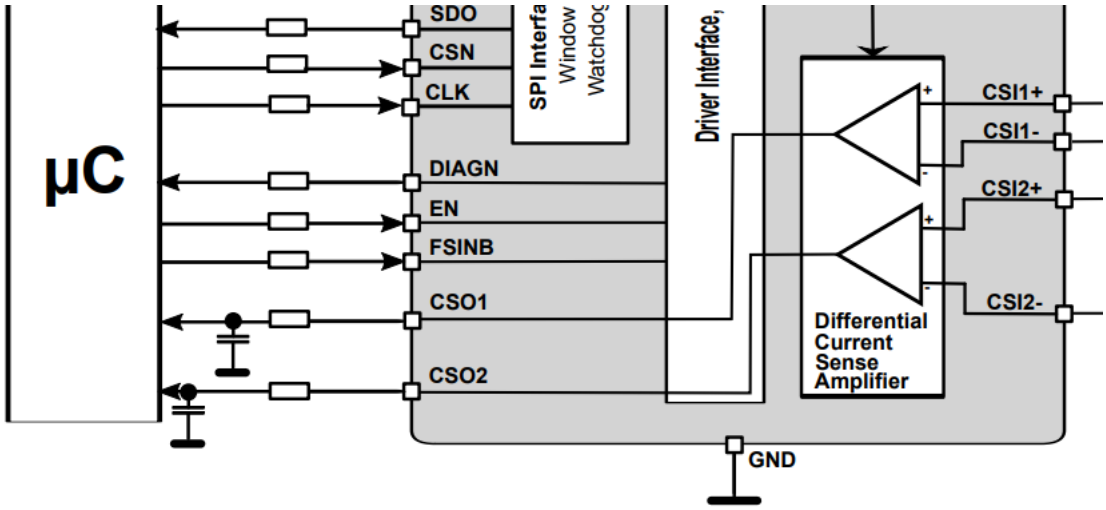
A sense resistor in the ground (below the lower MOSFETs) or supply (above the upper MOSFETs and above the VDH pin) shows no current when freewheeling. Placing a sense resistor in the motor “leg” allows for sensing freewheeling current. One other method would be to place two low side sense resistors, one on each leg. Then, freewheeling current could be sensed.

7.2 Selecting a current sense resistor value

The main concerns regarding current sense resistors are power dissipation and voltage drop. The goal is to accurately measure current without too much power dissipation or inaccuracy due to ADC tolerances.

An easy rule of thumb would be to choose the largest sense resistor size that the minimum gain and ADC voltage limits allow. Then, if power dissipation is an issue back off on the value and, if necessary, increase the gain.

Figure 16. Current sense feedback circuits



The transfer equation from sensed current to ADC value can be calculated by the following equation:

Motor current to ADC count equation

$$Count_{ADC} = (R_{sense} I_{Motor} A_v + V_{Ox}) \frac{2^{n_{ADC}}}{V_{Ref}} \quad (22)$$

Where:

- V_{Ref} = ADC reference voltage
- V_{Ox} = V_{O0} or V_{O1} based on CSA1OO and CSA2OO control bits
- I_{Motor} = motor current to be measured
- A_V = gain setting for the current sense amplifier
- n_{ADC} = number of bits in the ADC

The current sense amplifiers provide a VDD/2, if the CSA1OO and CSA2OO control bits are correctly set, value for a zero-current condition. This allows for bidirectional current sensing. This also reduces the voltage excursion for the output of the total voltage range of the L99H92 CSO pins or ADC V_{Ref}, whichever voltage is less. For a given gain and maximum current the maximum sense resistor value can then be defined by:

Current sense resistor upper limit

$$R_{sense(max)} < \frac{V_{\mathrm{CSOh}}}{2 \times I_{max} \times A_v} \quad (23)$$

Where:

- V_{CSOh} = maximum L99H92 current sense output (CSO) voltage

Note: The maximum voltage for the current sense output is determined by the L99H92 VDD input voltage and is defined as:

ADC input safe upper limit

$$\mathrm{V_{CSOh}} = \mathrm{V_{DD}} - 250\mathrm{mV} \quad (24)$$

If this value is higher than the maximum measurable ADC input voltage, then the ADC maximum voltage should be used.

- I_{max} = maximum current to be measured
- A_V = gain setting for the current sense amplifier

The maximum power dissipated in the sense resistor can be calculated by:

Maximum expected current sense resistor power dissipation

$$P_{sense\_max} = I_{max}^2 \times R_{sense} \quad (25)$$

For the minimum sense resistor value, the equation is a bit different. Here, the concern is with the ADC accuracy. Typically, an ADC has an accuracy that is expressed in ± counts. That is, the range of counts that a specific input voltage will be within. So, out of 2^n counts (where n represents the number of bits in the ADC) the error is usually small. A 12-bit ADC, for instance, can have an error of ±6 counts. That is 6 counts out of a total of 4096 counts. That error is relatively small at the full range of the ADC. However, if the circuit is measuring just a few counts, at low current for instance, ±6 counts may be 20% of what you are measuring. Even though we are measuring low currents at VDD/2 the number of counts of error still applies.

The minimum sense resistor for a given gain can be expressed in terms of acceptable tolerance for a given ADC error as:

Current sense resistor lower limit

$$R_{sense(min)} > \frac{|Error_{counts}|*V_{Ref}}{2^n*A_V*Tolerance*I_{min}} \quad (26)$$

Where:

- $Error_{counts}$ = tolerance of the ADC in counts
- V_{Ref} = ADC reference voltage
- I_{min} = minimum current to be measured
- A_V = gain setting for the current sense amplifier
- n = number of bits in the ADC
- $Tolerance$ = tolerance required for the minimum current measured

The gain can be set to 10, 20, 50 or 100. A higher gain setting allows for a smaller sense resistor value at a set tolerance. In actuality, the gain can be adjusted depending on the current level being measured. This allows for low current accuracy with a high gain setting and high current measurement capability with a low gain setting. The current level thresholds for specific gain setting can be bounded by the maximum voltage on the CSO pin (maximum gain) and the maximum tolerance in the ADC (minimum gain).

Finding the acceptable gain range

$$\frac{|Error_{counts}|*V_{Ref}}{2^n*R_{sense}*Tolerance*I_{load}} < A_v < \frac{V_{CSOh}}{R_{sense} \times 2 \times I_{load}} \quad (27)$$

The result is that as the current goes down the gain can go up. The above equation is used to determine the gain setting needed for each current range. There will be considerable overlap in current ranges for each gain setting. A large amount of hysteresis is recommended to maintain stability. It is also recommended to stay with as large a gain as is possible. This minimizes the error due to the ADC.

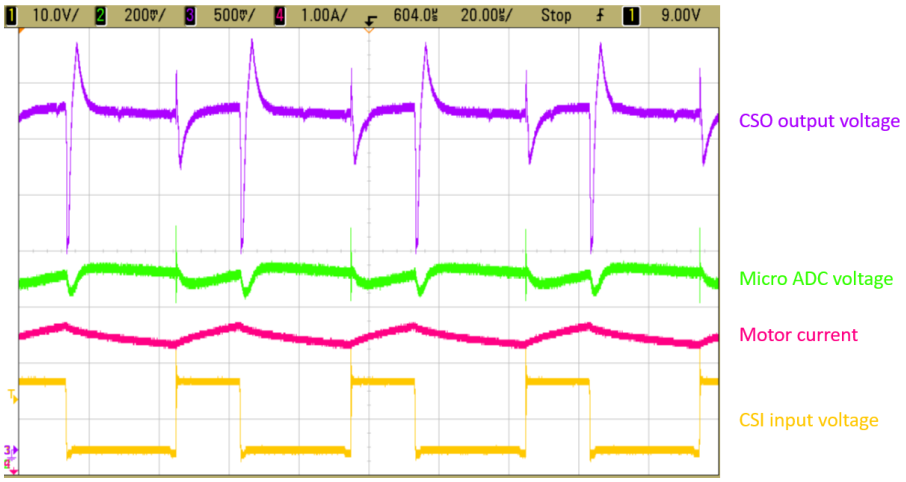
Typically, when regulating to a current it might be best to stay at one gain setting while regulating. Error is only a concern at the regulation set point. As a result, the error due to a low current measurement still tells the PID controller that the current is low, the error is not an issue. As the current approaches the regulation set point the proper gain setting allows for the proper tolerance.

7.3 Load current sensing with PWM control

When PWMming to regulate motor current, the voltage on the PWMmed side of the bridge transits from one rail to the other at the PWM frequency. The current sense amplifier inputs are susceptible to noise if exposed to these transitions.

To illustrate this, the Figure 17 shows PWMming occurring on the “a” side of the bridge where the current sense resistor is placed. The voltage transition that occurs on that leg makes for a noisy current sense feedback.

Figure 17. **Current sense amplifier reaction to voltage swings**



The solution is to maintain the PWM function on the opposite side of the current sense resistor.

The L99H92 can select which leg is PWMmed by selecting which polarity is used (high side or low side PWMming). By PWMming only on the other side of the motor the noise in the current sense amplifier is minimized.

Also, the L99H92 has the possibility to enable the active free-wheeling by the control bit value AFWE and to choose one of the four different freewheeling strategies by the freewheeling selection control bit value FWS: active or passive and freewheeling on either high-side or low-side MOSFETs. The DIR input pin sets the active diagonal, the AFWE control bit enables or disables active free-wheeling and the FWS control bit sets the free-wheeling path (HS or LS).

Figure 18. **Current sense on opposite side of PWM leg**

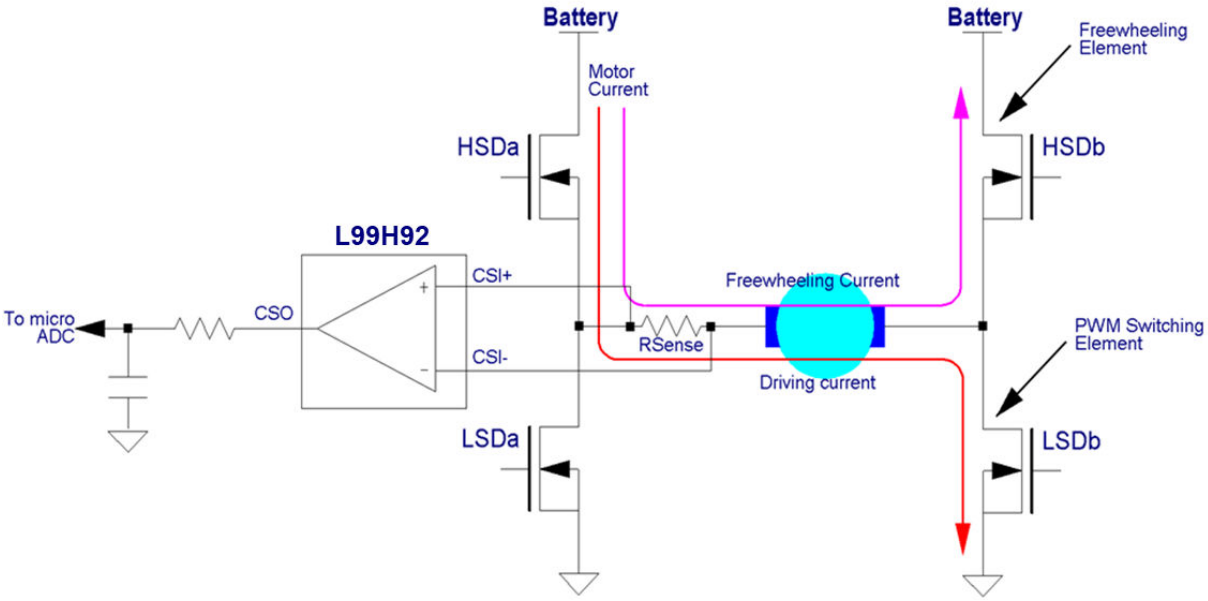
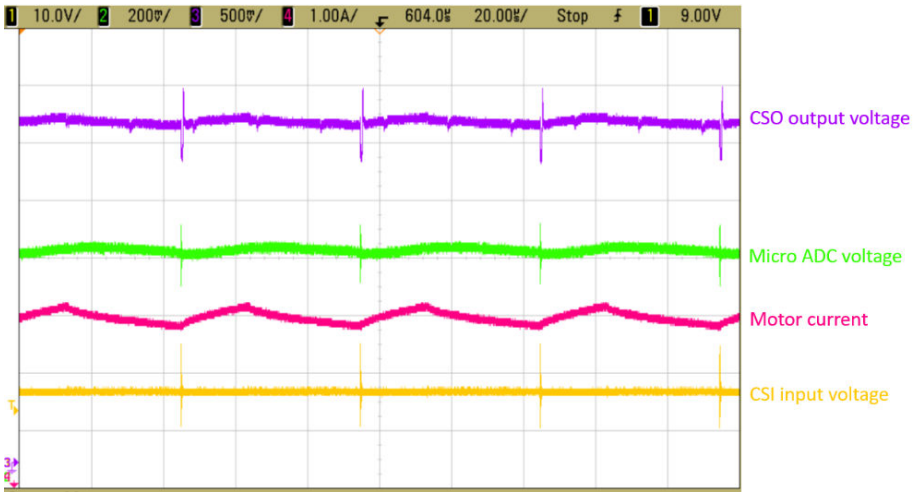


Figure 19. **Current sense amplifier behavior with PWM on the opposite leg**



8 Calibration

There are two steps to calibrating. The first is the input offset. This removes any error due to input offset issues with the current sense op-amp. The second is gain correction. This simple one step operation can calibrate out the error due to both the gain in the op-amp as well as the error due to the resistor value. Between these two calibration steps, all error is accounted for within the limits of the ADC. This includes Rsense tolerance, input offset tolerance, gain tolerance, and ADC reference voltage tolerance.

8.1 Input offset calibration.

Input offset error is a DC error that shifts the current reading result up or down by a fixed amount regardless of the measured current. That error can be expressed by:

Output current measurement with input offset error

$$V_{ADC} = (V_{CSO0} \pm V_{IOFFx}A_{Vx}) + I_{Shunt}R_{Shunt}A_{Vx} \quad (28)$$

Where:

- V_{ADC} = voltage at the ADC input
- V_{CSO0} = V_{O0} or V_{O1} based on CSA1OO and CSA2OO control bits
- V_{IOFFx} = input offset voltage error at a specific gain (x)
- A_{Vx} = gain setting (x = 10, 20, 50 or 100)
- I_{Shunt} = current in the shunt resistor
- R_{Shunt} = shunt resistor value

The DC component is extracted out of that:

DC offset component to measured current due to VIOFFx

$$V_{CSO0}(V_{IOFFx}) = V_{CSO0} \pm V_{IOFFx}A_{Vx} \quad (29)$$

Fortunately, most of the offset error can be eliminated statically. The input offset calibration is performed by reading the actual CSO voltage with the H-Bridge off. Possible motor movement or external biasing might introduce errors while calibrating this parameter.

The calibration procedure takes place with the following steps:

1. Turn off the H-bridge so to reach the condition of “zero current in shunt resistor(s)”.
2. Read ADC and store the value(s) for future reference.

This is the only way that allows to completely reset input offset.

Input offset calibration can be repeated throughout the life of the module. This is advised in that the offset voltage can change with temperature. Input offset calibration needs to be done for each gain setting as well.

The Eq. (28) then changes to reflect this calibration:

Calibrated V_{CSOO} ADC count value

$$Cnt_{VCSOx} = \frac{V_{CSO0} \pm V_{IOFFx}A_{Vx}}{V_{ref}}2^n \quad (30)$$

Where:

- Cnt_{VCSOx} = adjusted digital representation of the V_{CSO0x} after calibration. This value is used to calculate the measured currents and can be recalculated as often as necessary for optimum accuracy
- V_{ref} = ADC reference voltage
- 2^n = ADC bit count, n = 12 for a 12-bit ADC

8.2 Gain error calibration

Gain error calibration removes any error due to the device gain tolerance as well as the tolerance of the sense resistor. Once the input offset calibration is completed a gain error calibration can be done. This can only be done if the sensed current value is known. As a result, gain error correction cannot be done dynamically when the module is in use. This calibration could be performed at the module end of line test and would need to be done once for every gain setting used.

The first step is to measure a reference current with the gain calibration in place. Assuming the offset, gain, and resistor tolerances were zero. This considers the above input offset calibration value of Cnt_{VCSOx} (Eq. (30)).

The ideal ADC count using the reference current, with the DC offset calibrated out, can be calculated by the following equation:

Theoretical ADC count with offset calibrated out

$$CNT_{VCSO\_ref} = I_{ref} R_{Shunt} A_{Vx} \frac{2^n}{V_{Ref}} + Cnt_{VCSOx} \quad (31)$$

The actual ADC count can then be used to generate the gain error correction term. This is calculated by the ratio of the actual measurement at the reference current to the theoretical value.

Gain error correction term

$$A_{Verror} = \frac{CNT_{VCSO\_meas}}{CNT_{VCSO\_ref}} \quad (32)$$

This value, A_{Verror}, is calculated and used for generating gain adjusted ADC thresholds at calibration. To calculate the gain adjusted threshold current values the gain error parameter is inserted into the standard current calculation below. The offset is not included.

Calculating the thresholds with full calibration

$$Cnt_{thesh}(I_{thresh}) = I_{thresh} R_{Shunt} A_{Vx} A_{Verror} \frac{2^n}{V_{Ref}} + Cnt_{VCSOx} \quad (33)$$

The offset (Cnt_{VCSOx}) is removed prior to storing in memory for reference. It is inserted upon recalibration prior to each current measurement. This obtains the most accurate current reading. Of course, this does not need to be done if that level of accuracy is not needed.

Calibrated thresholds without the offset parameter for reference.

$$Cnt_{thesh}(I_{thresh}) = I_{thresh} R_{Shunt} A_{Vx} A_{Verror} \frac{2^n}{V_{Ref}} \quad (34)$$

The calculated results from the Eq. (34) are stored in memory for each threshold desired.

When a new current measurement is requested, an offset calibration can per performed first. That value (Eq. (30)) can then be subtracted from the ADC value measured. The result is then compared to the stored value for that threshold.

At the calibrated current value, the tolerance is typically less than 0.5%. Any additional error is due to the ADC tolerance issues.

9 Off-state diagnostics

Detecting a faulted load prior to turn-on can be advantageous in that it eliminates potential high stress events such as a turning on into a shorted load. While in the off state, the H-Bridge can be checked for open load, short to ground or supply as well verify MOSFET integrity prior to actuation.

Two off-state diagnostic comparators comparing the drop between each half-Bridge output (SHx pin) and related LS MOSFET source (SLx) to a programmable threshold can be used, while all the transistors are switched off, to detect system faulty conditions such as open-load, output shorted to ground or to battery, before even turning on any of the MOSFETs. The outputs of the off-state diagnostic comparators are always available (except in standby mode) and can be read through O1DS and O2DS status bits by SPI.

To enter in off-state diagnostic mode at least the OLH1L2 control bit or the OLH2L1 control bit must be set to one with the device OUTE control bit set to zero. To exit from off-state diagnostic mode either the OUTE control bit is set to one or both the OLH1L2 and the OLH2L1 are set to zero. In off-state diagnostic mode a pull-up resistor is connected to one of the half-Bridge outputs or to both and two pull-down resistors are connected to the two half-Bridge outputs.

Considering that the pull-up resistance is the same as the pull-down resistances, the VDS of the two low side transistors (that is, the two half-Bridge outputs) are expected to be equal to 1/3 VDH if a low resistive load is connected between the two legs.

On the contrary if the VDS of any of the two low sides is lower than VODSL (OLTHH = 0) or higher than VODSH (OLTHH = 1), then a fault condition must be present.

9.1 Off-state open load detection

The configuration circuit to detect an open load is here reported: if a load is connected, see the Figure 20, two resistors to ground of 20 kΩ are in parallel and fix the voltage at the two motor terminals equal to VDH/3. This voltage is compared to a threshold voltage that is VODSL and the two bits O1DS and O2DS are kept to 0. Once the load is removed, see the Figure 21, the input of the comparator is connected to ground by a 20 kΩ resistor. In this case the ground 0 V is compared with a VODSL voltage and the 01DS or O2DS flag is set.

To enter in the off-state diagnostic mode and to perform an open load detection, the below steps must be followed

1. OUTE control bit set to 0 to disable the gate drivers
2. Set the control bits DCSA1 = DCSA = 1 to disable the CSA1/2
3. Set the control bits OLH1L2 = 0, OLH2L1 = 1 and OLTHH = 0 for the SH1 open load detection or OLH1L2 = 1, OLH2L1 = 0 and OLTHH = 0 for the SH2 open load detection
4. Read the O1DS and O2DS bits and check them in according to the Table 7
5. Set the control bits OLH1L2 = OLH2L1 = OLTHH = 0 if the off-state diagnostic must be disabled

Figure 20. Full-bridge open-load-detection (no open-load detected)

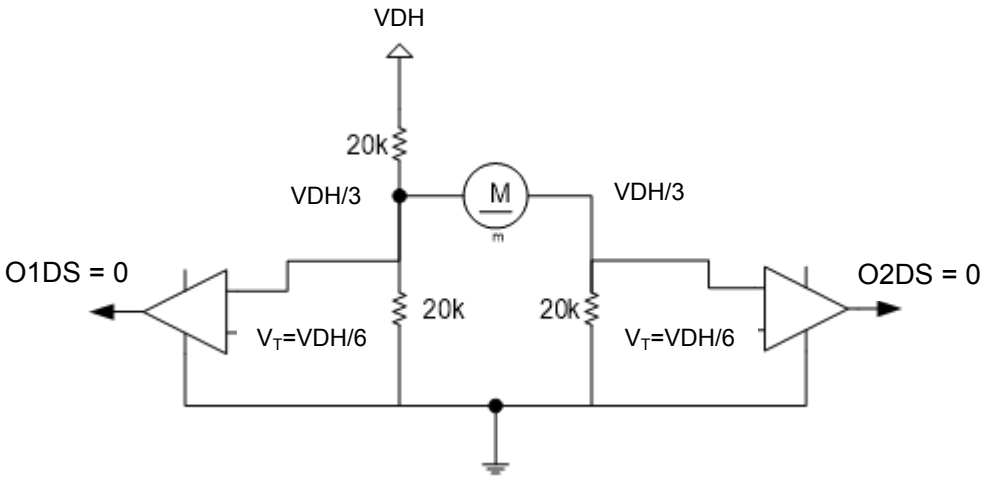
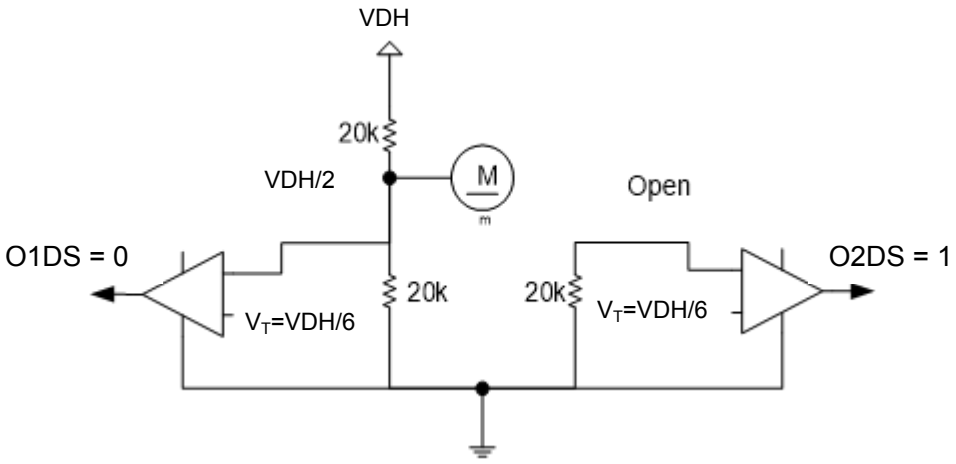


Figure 21. **Full-bridge open-load-detection (open-load detected)**



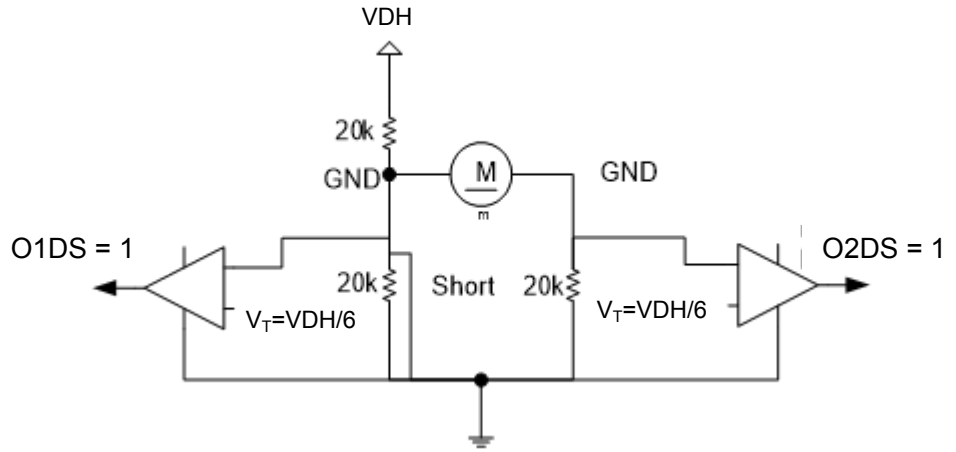
9.2 Short to ground

The configuration circuit to detect a short to ground is here reported: if a load is connected, see the Figure 22, and one of the legs is shorted to ground, the voltage at the two motor terminals equal to 0 V. This voltage is compared to a threshold voltage that is VODSL and the two bits O1DS and O2DS are put to 1.

To enter in the off-state diagnostic mode and to perform an open load detection, the below steps must be followed

1. OUTE control bit set to 0 to disable the gate drivers
2. Set the control bits DCSA1 = DCSA = 1 to disable the CSA1/2
3. Set the control bits OLH1L2 = 0, OLH2L1 = 1 and OLTHH = 0 or the OLH1L2 = 1, OLH2L1 = 0 and OLTHH = 0 for the short to ground detection
4. Read the O1DS and O2DS bits and check them in according to the Table 7
5. Set the control bits OLH1L2 = OLH2L1 = OLTHH = 0 if the off-state diagnostic must be disabled

Figure 22. **Full bridge open-load-detection (short to ground detected)**



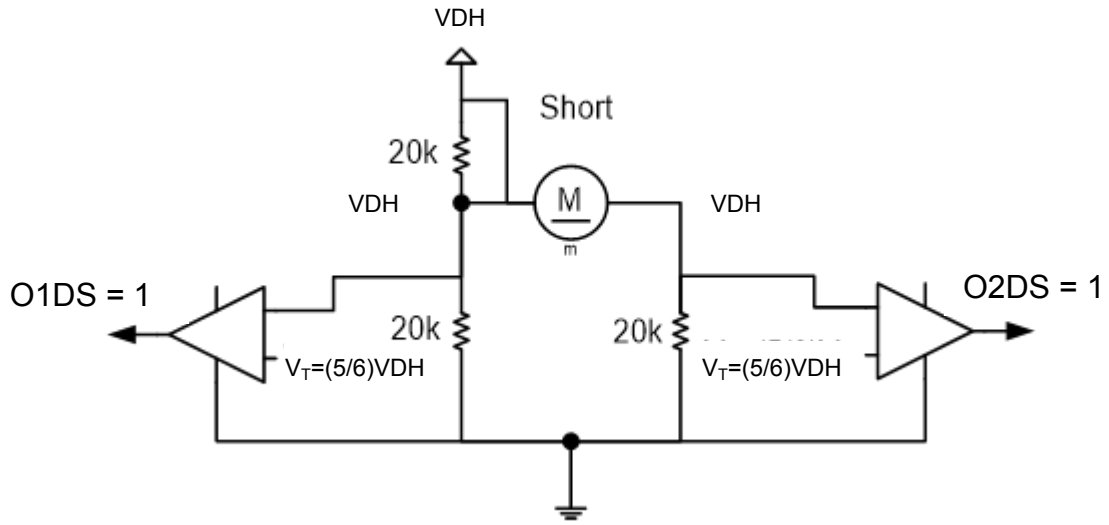
9.3 Short to Battery

The configuration circuit to detect a short to VDH is here reported: if a load is connected, see the Figure 23, and one of the legs is shorted to VDH, the voltage at the two motor terminals equal to VDH. This voltage is compared to a threshold voltage that is VODSH and the two bits O1DS and O2DS are put to 1.

To enter in the off-state diagnostic mode and to perform an open load detection, the below steps must be followed

1. OUTE control bit set to 0 to disable the gate drivers
2. Set the control bits DCSA1 = DCSA = 1 to disable the CSA1/2
3. Set the control bits OLH1L2 = 0, OLH2L1 = 1 and OLTHH = 1 or the OLH1L2 = 1, OLH2L1 = 0 and OLTHH = 1 for the short to battery detection
4. Read the O1DS and O2DS bits and check them in according to the Table 7
5. Set the control bits OLH1L2 = OLH2L1 = OLTHH = 0 if the off-state diagnostic must be disabled

Figure 23. Full bridge open-load-detection (short to VDH detected)



9.4 Off-state diagnostics summary

Below a state diagram of all the steps necessary to perform a full off-state diagnostic. Also, a short summary of the full bridge monitoring in off-state is reported in the Table 7.

Figure 24. Off-state diagnostic state diagram

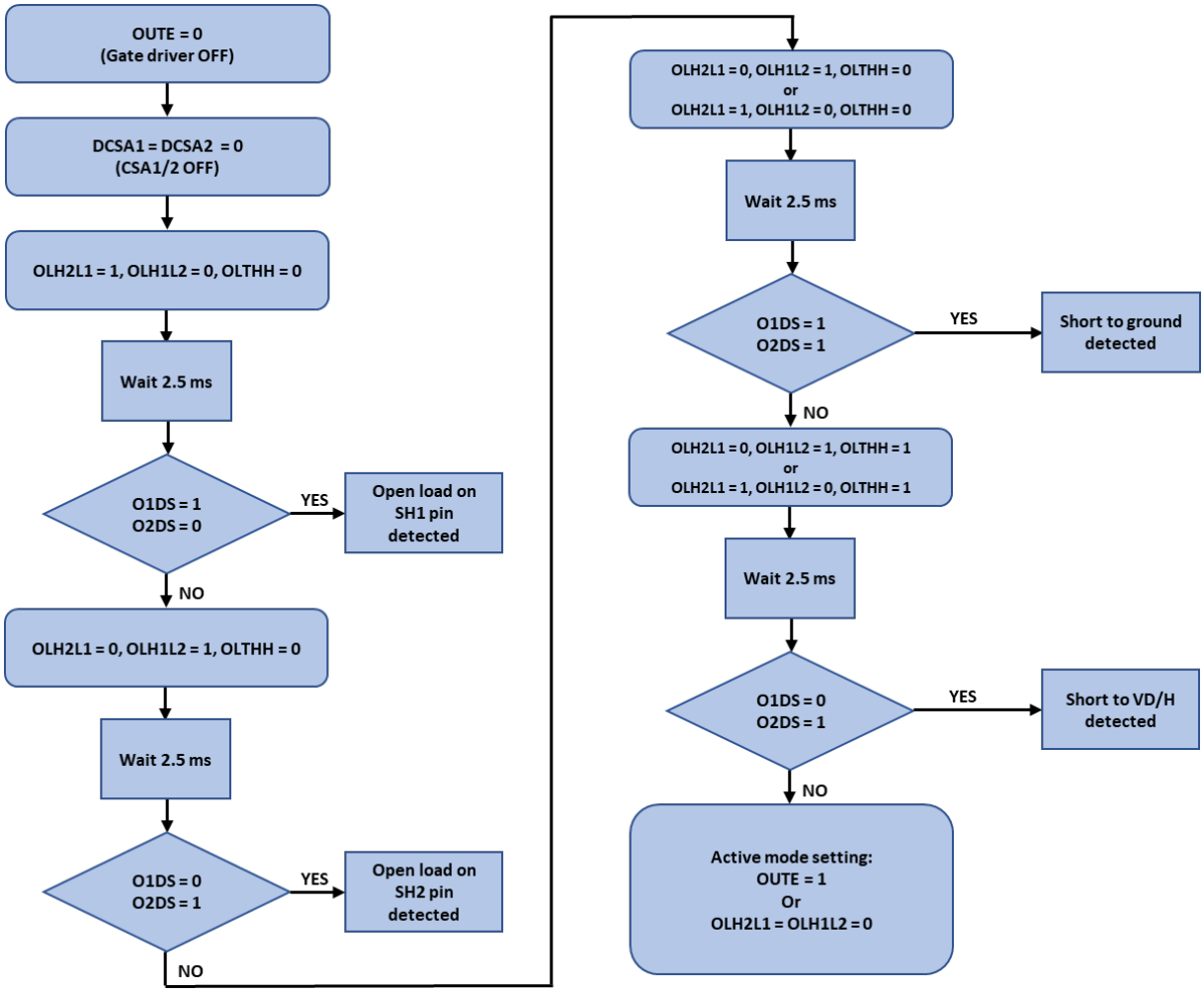


Table 7. Full-bridge monitoring in off-state

Control bits			Failure bits		Comments
OLH1L2	OLH2L1	OLTHH	O1DS	O2DS	
0	0	0	0	0	Off-state diagnostic disabled
1	0	X	0	0	No open-load detected
1	0	0	0	1	Open-load SH2
1	0	0	1	1	Short to GND
1	0	1	1	1	Short to VDH
0	1	X	0	0	No open-load detected
0	1	0	1	0	Open-load SH1
0	1	0	1	1	Short to GND
0	1	1	1	1	Short to VDH

What reported in this chapter applies only to single motor full-bridge configuration, i.e. the case where one full-bridge drives only one motor.

In dual half-Bridge mode (INPMODE = 1), the device can still detect an open-load condition.

In off-state diagnostic mode, it is recommended to wait at least 2.5 ms, starting from any change of OLH2L1, OLH1L2 or OLTHH control bits, before reading stable O1DS and O2DS status bits values.

10 Short circuit detection/drain source monitoring

After performing, and passing, all the off-state diagnostics, the external MOSFETs can be checked to verify that they respond to gate voltage control. It is important that the off-state diagnostics all pass prior to starting these tests.

The voltage-drop over each MOSFET is sensed and compared with a programmable threshold to detect an over-current condition. This monitoring is active only on the MOSFET driven to be turned on.

The used procedure for the check is:

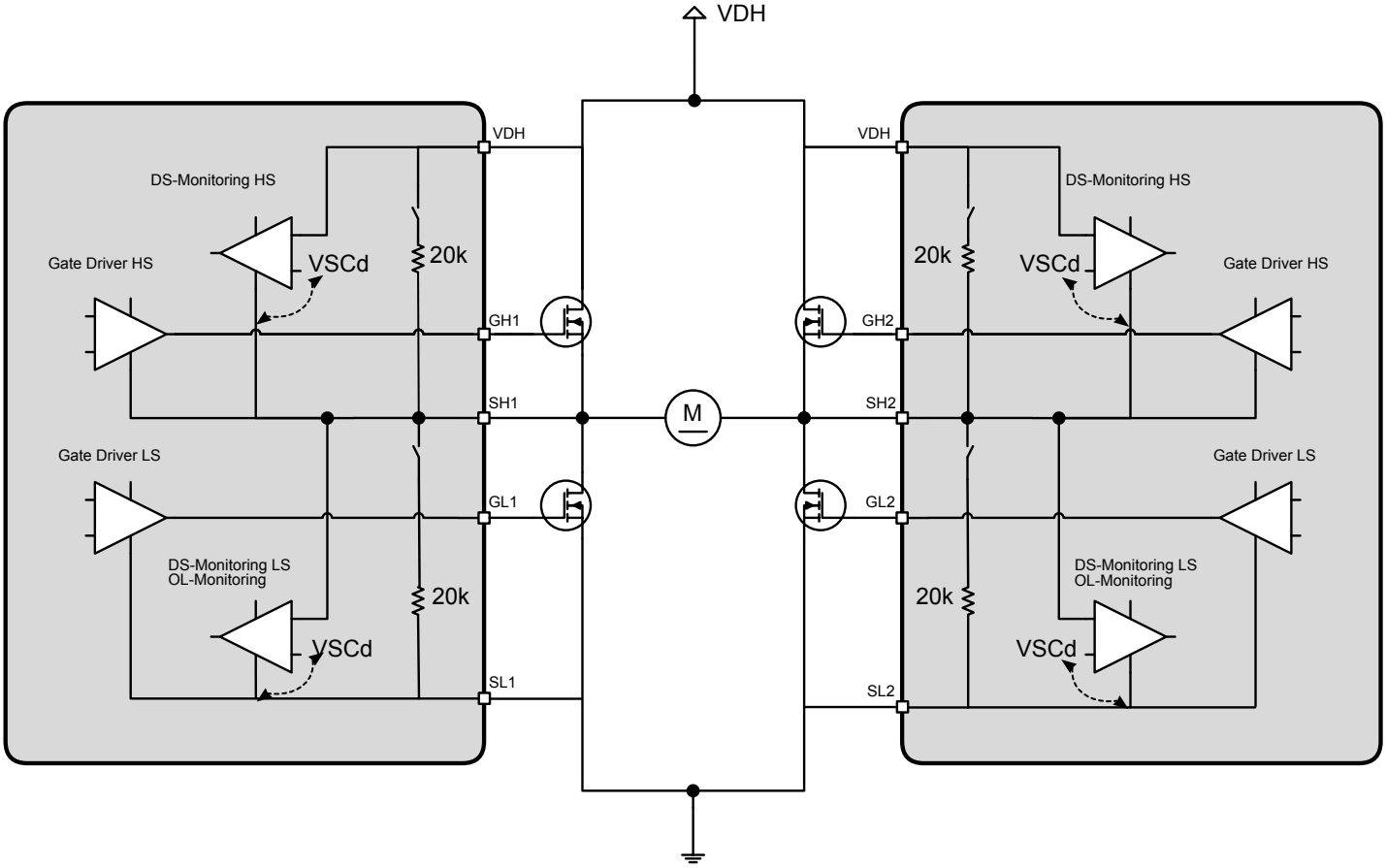
1. When the gate driver starts to turn on a MOSFET, the corresponding drain-source monitoring is masked for the programmed blanking time (DSBTx[2:0]). This is done to give time to the MOSFET to turn on.
2. A filter time (FTx[1:0]) is present to filter noise.
3. After the programmed blanking time, the drain-source monitoring is powered on and the voltage-drop is compared with the programmed threshold voltage (DSMON1[2:0] control bits for full-bridge or leg1 and DSMON2[2:0] control bits for leg2 in dual-half bridge mode)
   a. If the voltage-drop exceeds the programmed threshold for a time longer than the programmed filter time, two different scenarios are possible in according to the DSMON_CONFIG bit setting:
      i. If DSMON_CONFIG bit is set to 1 and INPMODE is set to 0, any VDS monitoring fault will actively switch off all the full-bridge MOSFETs by configuring all the gate drivers in sink switch mode.
      ii. If DSMON_CONFIG bit is set to 0 and INPMODE is set to 1 or 0 the affected/offended half bridge MOSFETs are actively switched off configuring the corresponding gate drivers in sink switch mode.
   b. The drain-source monitoring flag DSHSx or DSLSx of the MOSFET detecting the fault is set. This flag can be cleared by an SPI “read and clear” command only if the fault condition is no longer present.

In dual half-Bridge mode, each half-Bridge has its own programmable threshold (DSMONx[2:0]), blanking time (DSBTx[2:0]) and filtering time (FTx[1:0]).

Few general basic rules about selection of drain-source monitoring parameters are:

- Drain-source threshold voltage should be selected with respect to MOSFET RDS(on), maximal current of a given application and supposed short-circuit current. The selected threshold must be higher than voltage drop over the driven MOSFET during normal operation, which is equal to VSCd > VDS = RDS(ON) * ID, and it should be smaller than voltage drop over the driven MOSFET during over-current condition (VSCd < VDS = RDS(ON) * IOC).
- Drain-source voltage during OFF → ON transition corresponds to a falling transient. Hence, blanking time t_B must be sized to allow VDS settling. On the other hand, the blanking and filtering time must be smaller than PWM ON time. If the MOSFET is switched-off before blanking and filtering time expire, the diagnostic is not performed.

Figure 25. **Short circuit detection/drain source monitoring circuit**



11 Fail-safe and diagnostic input/output

In high current applications a failed MOSFET can cause dramatic thermal events that can be quite serious. In this case it is very important to have the possibility to turn off the MOSFETs without waiting for the timing of an SPI transition. Fortunately, the L99H92 has two pins, one input and one output, that help the microcontroller to immediately deal these cases without the need of SPI transfers.

11.1 Fail-safe input not pin (FSINB)

Refer to the Section 1.1: Functional states for this functionality.

11.2 Diagnostic not output (DIAGN)

The microcontroller can use the DIAGnostic Not (DIAGN) output pin, active low, to detect a device fault, including a device power-on-reset event: the purpose of the DIAGN output pin is to warn immediately the microcontroller that a new fault, which the microcontroller was not yet aware of, has been detected by the device, without the need of periodic SPI transfers. The DIAGN state is valid only for power supply > POR.

The DIAGN output pin has an internal weak pull up resistance. The logic level signal at the pin is the logical NOR combination of all the status flags and status bits linked to the pin through the DIAGCR control register, together with the global status byte RSTB bit.

Once the device comes out of standby mode, the DIAGN pin is pulled low: any valid SPI communication frame will clear the RSTB bit pulling up the DIAGN pin. Any read access to the DSR1 register will reset this signal to high level, until an error coming from a new source occurs pulling again the pin low.

Revision history

Table 8. **Document revision history**

Date	Version	Changes
07-Nov-2024	1	Initial release.

Contents

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