How to optimize the RF board layout for STM32WL3x MCUs

Introduction

The STM32WL3x MCUs are high performance ultra-low power wireless application microcontrollers, which integrate an RF transceiver for low-power wide-area network (LPWAN). They are designed to operate in license-free ISM and SRD frequency bands such as 433, 868 and 915 MHz.

This document describes the precautions needed to achieve the best RF performance of the STM32WL3x.

This document applies to a 4-layer board design based on the VFQFPN48 (6x6x0.9, pitch 0.4 mm) and VFQFPN32 (5 x 5 mm, 0.50 mm pitch) package.

Table 1. Applicable products

Type	Products
Microcontrollers	STM32WL3x product line

1 General information

This document applies to the STM32WL3x Arm®-based MCUs.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Main rules summary

Some general guidelines when routing an RF PCB are listed below:

- RF traces must be short and straight.

Note: Make the transmission lines short and as straight as possible to avoid signal reflection and reduce any high-frequency issues.

- Place and route decoupling capacitors and RF components first as outlined in the steps below:
  1. Place the RF circuit first. This is highly recommended. Decoupling capacitors are essential to avoid high-frequency problems and maintain power integrity. Do not hesitate to add additional decoupling capacitors if needed.
  2. Route RF traces as the next step.
- Do not route high-frequency signals on the edges of the board.

Note: High-frequency signals on the edge of the board tend to radiate due to edge effects.

- Maintain the characteristic impedance (50 Ω) constant.

Note: Avoid discontinuities, such as: different pad sizes on transmission lines, bends, or T-junctions. Maintain the RF width along the whole line.

- Keep supply traces away from any RF signals.

Note: Parasitic capacitance and inductance can induce undesired electric and magnetic coupling between RF signals and supply traces.

- Avoid using vias on RF signals lines.

Note: Vias on RF paths can cause reflections, radiation, and substantial power losses.

- For high-frequency applications, 4-layer PCBs are better than 2-layer PCBs.
- RF return current paths must be free of obstacles or discontinuities.
- Avoid undesired magnetic coupling between inductors by leaving space between them, using magnetic shielding and/or placing them perpendicular to each other.
- Reduce as much as possible any undesired parasitic capacitance and inductance associated with the circuit layout.

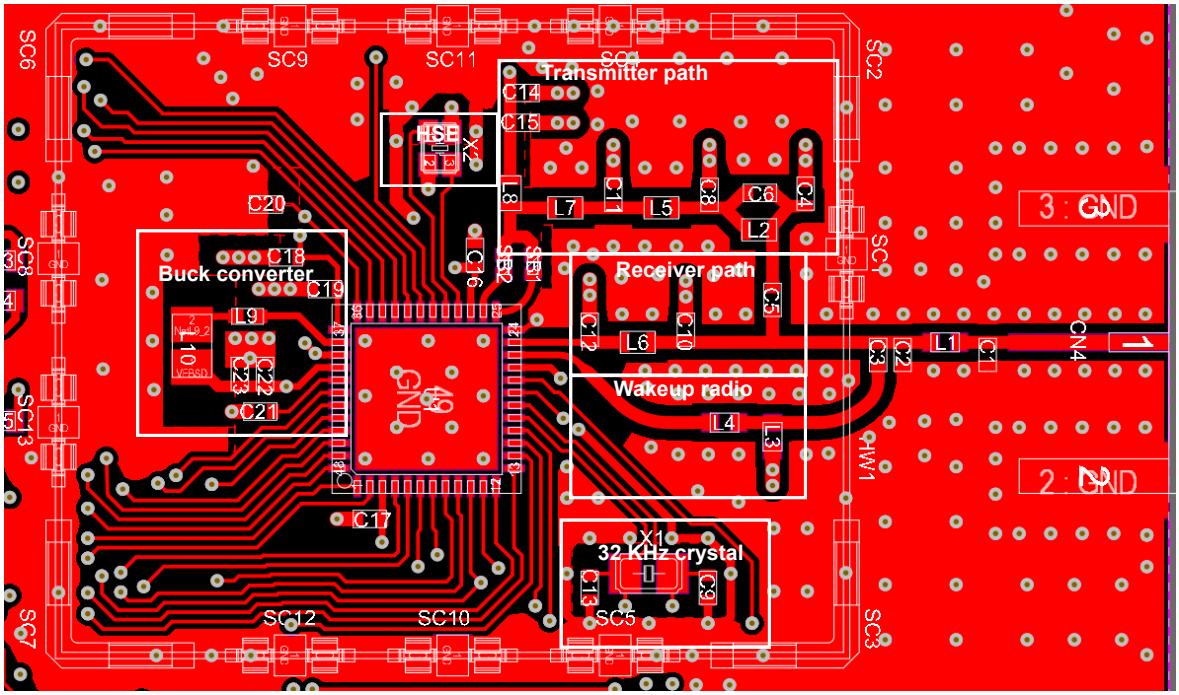
3 STM32WL3 application circuit

This section provides a brief description of the main parts of the application circuit as listed below:

- Transmitter and receiver
- Switching mode power supply (SMPS) buck converter
- External high-speed clock (HSE)
- External low-speed clock (LSE) (optional)
- Low power autonomous wake up receiver (LPAWUR) (optional)

In our reference design, to reduce the cost of the bill of material, the transmitter and the receiver are directly connected to each other, in a direct-tie configuration. This avoids the need for an RF switch. This is illustrated in the figure below.

Figure 1. Reference design board layout



3.1 Transmitter and receiver

The STM32WL3x integrates a power amplifier (PA), a low noise amplifier (LNA) and a wakeup radio.

The PA delivers an output power between -30 dBm to +20 dBm. The output stage topology is single-ended and by using of two dedicated pins (TX and TX_HP), the PA can be configured for three different output power levels.

Power configuration (see the table below):

- High power (HP), optimized up to 20 dBm (TX + TX_HP pin)
- Medium power (MP), optimized up to 16 dBm (TX_HP pin)
- Low power (LP) optimized up to 10 dBm (TX pin)

At each power configuration is associated with a specific bill of material.

On the Nucleo-WL33CCx, the SB1 and SB2 solder bridges allow all three output power configurations as given in Figure 2 and Figure 3.

Table 2. Solder bridge on Nucleo-WL33CCx for power-amplifier configuration

Maximum output power	TX pin	Solder bridge configuration
10 dBm	TX	SB1 open; SB2 closed
16 dBm	TXHP	SB1 closed; SB2 open
20 dBm	TX+TXHP	SB1 closed; SB2 closed

Figure 2. Solder bridge on Nucleo-WL33CCx for power-amplifier configuration

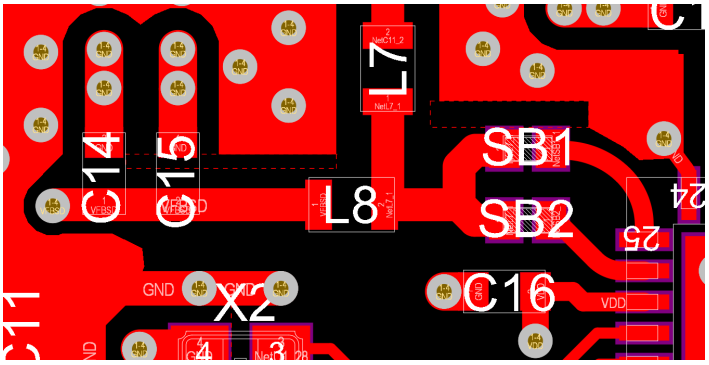


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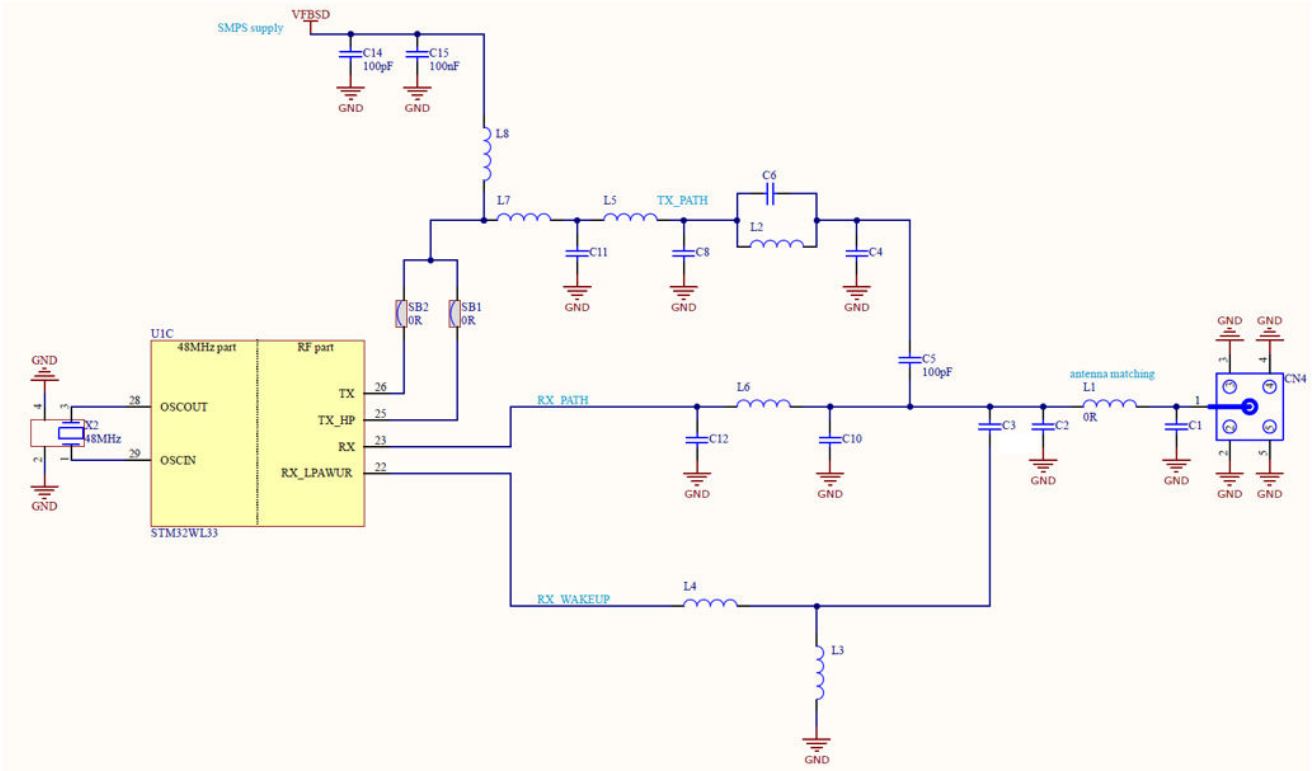
Figure 3. Nucleo-WL33CCx RF part schematic



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3.2 SMPS circuit

The switch mode power supply (SMPS) is a step-down converter which converts the V_{DD} voltage to a programmable voltage used to supply both the integrated PA and the internal LDOs.

Passive components play a fundamental role in the RF performance, so it is strongly recommended to only use the components specified on bill material of reference design.

The placement and routing of these components are critical, and it is important to follow these guidelines to avoid any unwanted coupling with the RF line. This could degrade the sensitivity performance of the reception and increase the levels of the spurious emissions in transmission.

Table 3 lists the pins related to the step-down converter.

Table 3. SMPS pin description

Pin name	Pin number	Description
V_{DDSD}	37	Input supply of the SMPS.(1)
V_{LXSD}	38	Switching node of SMPS.
V_{FBSD}	40	SMPS output voltage.(1)
V_{SSSD}	39	Ground pin of the SMPS.

1. *Connect high-quality bypass capacitors close to this pin and GND.*

Figure 4. Supply and SMPS schematic

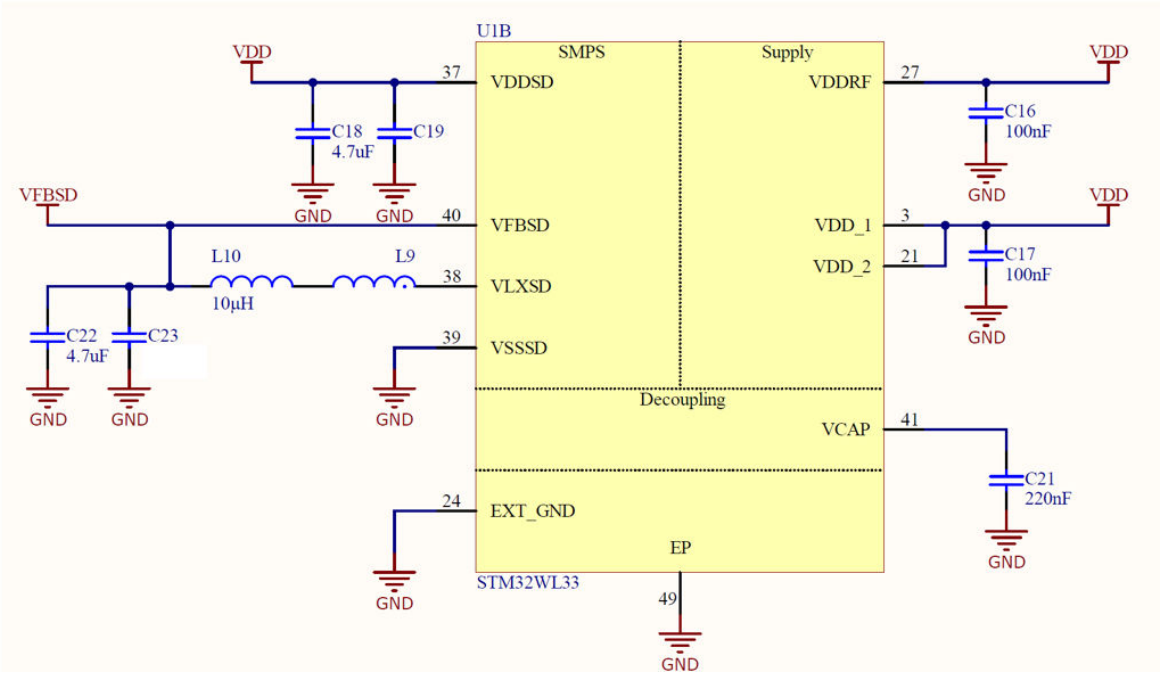


Table 4. SMPS external Component

Designator	Component	Value	Description
C18	Capacitor	4.7 uF	Bypass capacitors to provide a low impedance source to the regulator in addition to supplying the ripple current, and isolating switching noise from other circuits. Connect this capacitor between V_{DDSD} and GND.
C19	Capacitor	-	Output capacitor between V_{DDSD} and GND. Place this capacitor as close as possible to the V_{DDSD} pin. This capacitor is used to guarantee an impedance close to 0 Ω at the operating frequency between the VDDSD pin and the QFN exposed pad.
L9	RF inductor	270 nH(1) 100 nH(2)	Select an inductor with a self-resonant frequency close to the operating RF frequency to filter the noise generated by the converter. Connect this inductor to the V_{LXSD} pin in series to the power inductor.
L10	Inductor	10 µH	Power inductor: DCR 1-Ω and rated current > 100mA.
C22	Capacitor	4.7 µF	Output capacitor between V_{FBSD} and GND
C23	Capacitor	-	Output capacitor between V_{FBSD} and GND. Use the same C19 value to filter the SMPS noise generated at the operating frequency.

1. *For low band: 413-479 MHz*
2. *For High band: 826-958 MHz*

The SMPS can be either used as it is, disabled by software (bypass mode) or not used at all. In the latter case, all components associated the SMPS can be removed from the PCB.

3.3 HSE

The high speed external (HSE) clock can be supplied with a 48 MHz and 50 MHz crystals. The crystal used in the reference design is the NX1612SA-48.000 MHz-EXS00A-CS12140 (8 pF XTAL load). The STM32WL3x includes internal programmable capacitances that can be used to tune the crystal frequency to compensate the PCB parasitic one, to center the initial offset and even to compensate for dynamic temperature drift thanks to its +/-25 ppm possible variation range.

3.4 LSE

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. The crystal used in the reference design is the NX2012SA-32.768KHZ-EXS00A-MU00389 (7 pF XTAL load).

3.5 Low power autonomous wake up receiver (LPAWUR)

The STM32WL3x includes an always-on ultra-low-power wake-up receiver. It detects a specific OOK frame to trigger the wake up of the SOC while in deep-stop mode.

To work correctly, the receiver simply needs a 32 kHz clock which can either be supplied by the internal low-speed internal clock (LSI) block or by the low-speed external clock (LSE).

On the reference board, the path of the LPAWUR is not connected to the SMA connector. To evaluate this feature, a 0-Ω resistor needs to be soldered on the PCB. The matching network of the wake up receiver is tuned for the 826-958 MHz band.

4 PCB stack-up layers

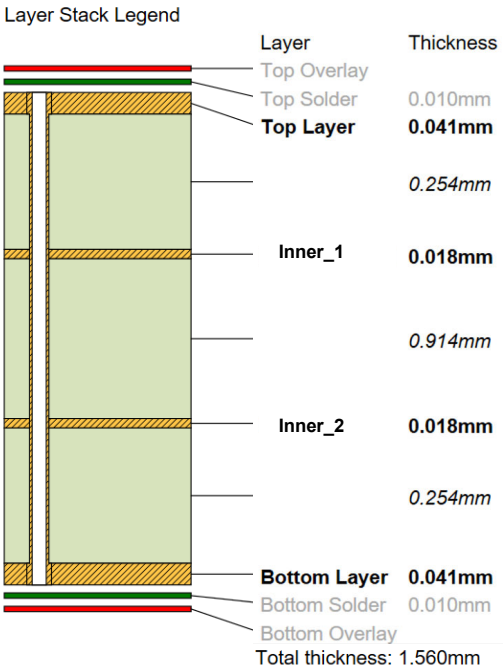
This document provides the guidelines for VFQFPN48 (6x6x0.9, pitch 0.4 mm) and VFQFPN32 (5 x 5 mm, 0.50 mm pitch), four-layers PCB and 0402 SMD RF components. The dielectric selected in our reference design (Nucleo-WL33CCx) is the Ventec VT-47 which ensures a good compromise between cost and performance.

A four-layer PCB is preferred for RF applications as it allows for good EMC performance. A common four-layer PCB, as illustrated in Figure 5, consists of:

- Two layers for the signal
- One layer for power
- One ground plane.

The main advantages of this configuration are the possibility of having a continuous ground plane under the RF traces and to reduce the separation between signal layer (Top layer) and ground plane (Inner_1). In the reference design the distance between the signal layer and ground layer is 0.254 mm.

Figure 5. MB2218 stack-up layers



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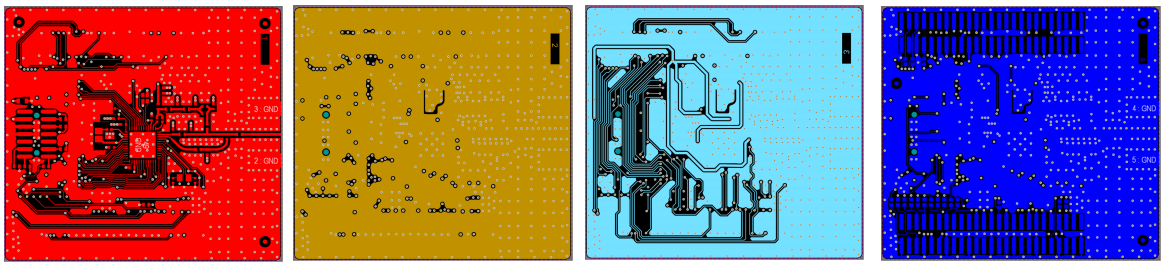
The board routing is as follows and is illustrated in Figure 6.

- Top layer: Used for RF components and transmission lines.
- Inner_1: Continuous ground plane
- Inner_2: Supply traces and digital signal routing
- Bottom layer: Ground plane and digital signal routing.

Figure 6. **MB2218 layers**



Top layer Inner_1 Inner_2 Bottom layer

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5 Layout design guidelines

Controlling the electromagnetic emissions generated by the PCB must be treated as a design problem from the start. Therefore, one of the fundamental aspects to consider during the PCB design is to identify any possible source of emissions.

One of the most common sources responsible for the generation of unwanted emissions is high frequency currents flowing around loops.

The forward and return paths of the high-frequency current can create loops and act as antennas responsible for electromagnetic field emissions. For this reason, it is important to identify the return current path of high-frequency signals and minimize the loop area formed by the signal traces.

Major emission problems occur when the high-frequency return current path meets discontinuities, which cause the return current to flow in large loops increasing the radiation from the boards.

To avoid as much as possible high-frequency current loops on the top layer, the shunt capacitors on the RF path are connected to the ground plane on Inner_1 by vias. In this way, the RF return currents are forced to return to the QFN exposed pad using the Inner_1.

The Inner_1 layer must be used as a ground reference plane for the RF traces on the top layer, and apertures under the RF part must be avoided. Moreover, it is also recommended to avoid discontinuities of the ground plane under the SMPS region. This is to ensure that the high frequency currents generated by the SMPS can easily return to the V_{SSSD} pin which is the ground connection of the SMPS.

On Inner_2 layer, route V_{DD} and high-speed signal traces on this buried layer. The reason is to maximize the ground area on bottom layer to absorb the unwanted emissions generated by high- frequency signal traces routed on Inner_2.

6 Decoupling capacitor

The operating frequency, switching frequency of the SMPS, the high-speed clock frequency and its harmonics (up to the third) must be filtered to avoid up-converted spurs. For this purpose, the capacitors must be selected considering a series resonant frequency (SRF) close to the frequency to be filtered.

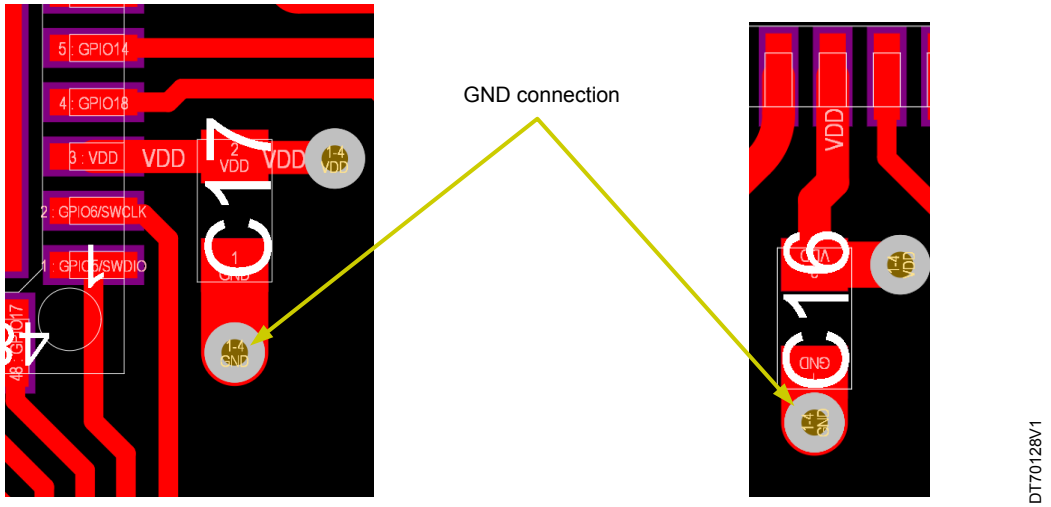
The following are the design considerations for placing decoupling capacitors:

- Place the decoupling capacitors on the same layer as the RF IC.
- The capacitor with the lowest value of capacitance should be placed near the power supply.
- The capacitors which filter the highest frequency should be placed as close as possible to the V_{DD} pins.
- Use small capacitance for high-frequency transients and large capacitance for low-frequency transients.
- Each decoupling capacitor requires a dedicated ground via. Never share ground vias.

6.1 Power supply decoupling on V_{DD1} and V_{DD2}

Bypass capacitors must be placed very close to V_{DD} pins, and the ground pad of the capacitor must be directly connected to the GND plain on Inner_1 by vias to get a low-impedance connection to GND and to reduce as much as possible the current loop. Figure 7 shows the connection of the decoupling capacitors for the V_{DD} pins (pin 3 and 27). A good rule of thumb for V_{DD} line width is a minimum of 150 µm width for each 100 mA of current consumption. This minimizes the potential voltage drop at STM32WL3x V_{DD} pins in RF mode for example and this maximizes battery lifetime.

Figure 7. Bypass capacitor connection on V_{DD} pins



6.2 Power supply decoupling on V_{DDRF}

The decoupling capacitor for V_{DDRF} must offer the low impedance at the frequency of the high-speed crystal reference. The reference design uses the GRM155R71H104KE14 part number which shows 68 mΩ at 48MHz. This is illustrated in Figure 8

Figure 8. Impedance vs frequency GRM155R71H104KE14

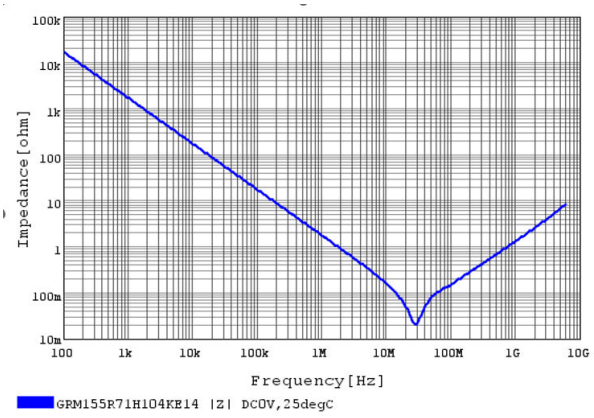


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Figure 9 shows that the impedance measured between the V_{DDRF} pin and the exposed pad is a short circuit at the the crystal frequency of:
(0.23 + j*0.78 Ω at 48MHz).

Figure 9. Impedance on VDDRF at 48 MHz

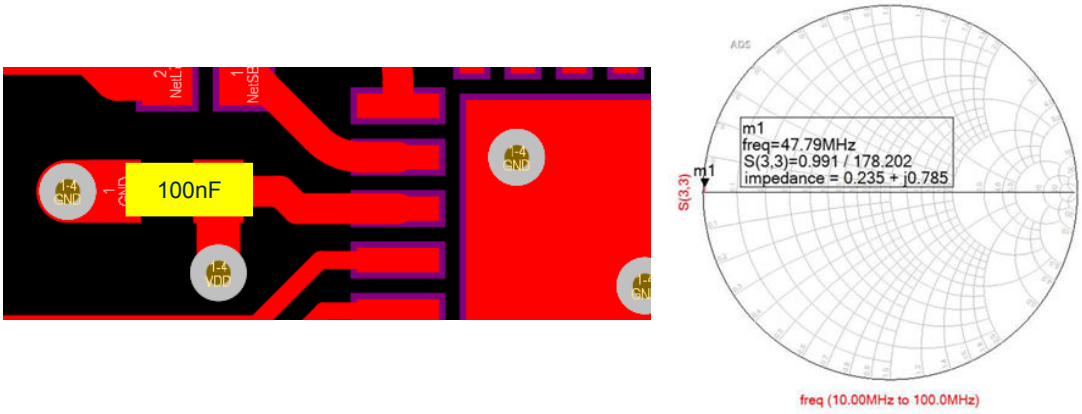

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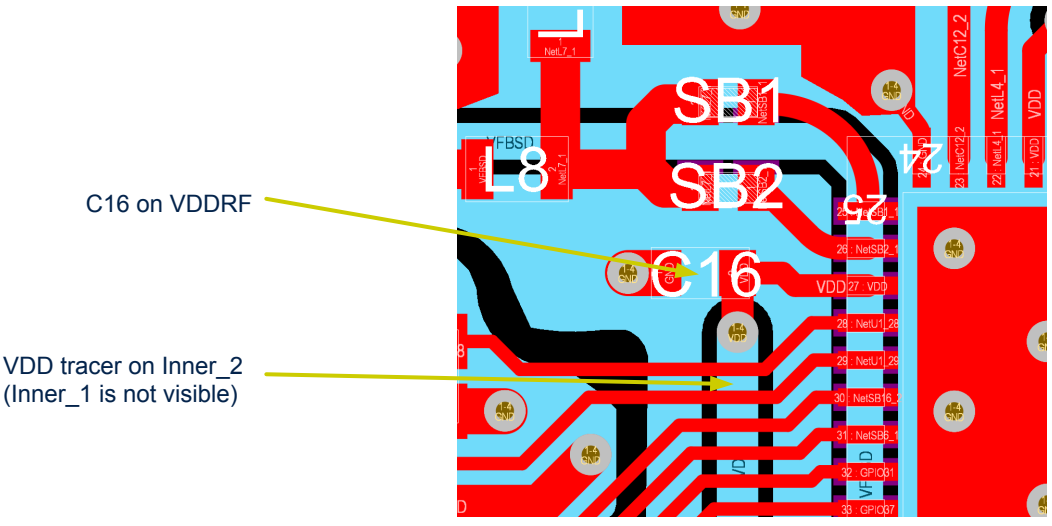
Figure 10 shows the C16 used to filter V_{DDRF} pin and the V_{DD} trace routed on Inner_2.

Figure 10. **VDD trace on Inner_2**



7 Routing for transmitter and receiver

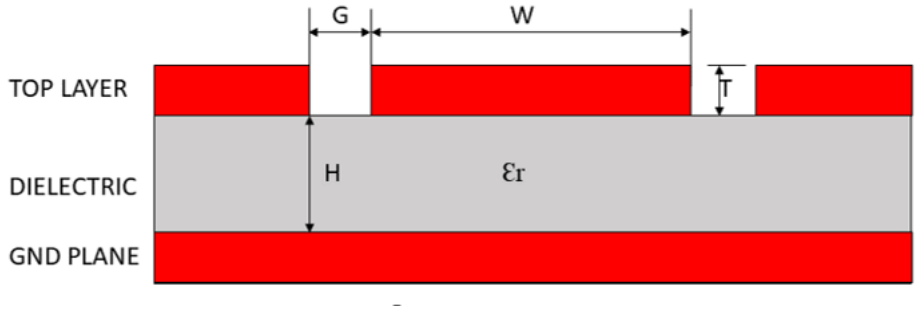
Designing a board with digital and RF parts requires optimal isolation between different circuit blocks. For this reason, grounded coplanar waveguides (GCPW) are used.

GCPW is preferred for following reasons:

- It provides optimal isolation for RF traces and better EMI performance.
- It is easier to support the grounding of shunt elements on RF trace.
- Provides reduced crosstalk with other traces and ensures low energy loss at high frequencies.

The characteristic impedance of the transmission line GCPW is determined by physical dimensions: thickness (T), width (W), clearance (G), and height (H) as illustrated in Figure 11. These dimensions must be kept within tight tolerances to maintain the impedance as close to 50 Ω as is possible. Several online tools allow the GCPW to be designed with a controlled impedance, based on the selected stack-up.

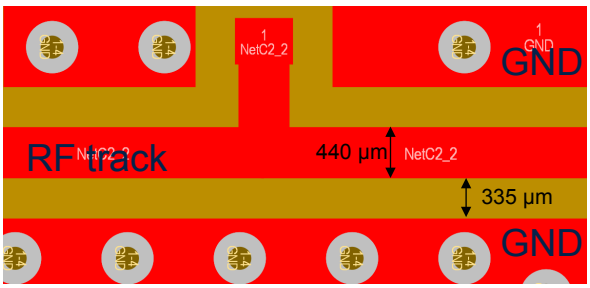
Figure 11. PCB grounded coplanar structure



TX and RX traces routed on the top layer are designed to achieve 50 Ω characteristic impedance with a width of 440 µm. This is illustrated in Figure 12.

- The clearance between the RF track and the GND on the top layer is 335 µm.
- The thickness of the dielectric between the top layer and Inner_1 measures 254 µm.
- The permittivity of the dielectric between the top layer and Inner_1 is 4.4.

Figure 12. RF trace



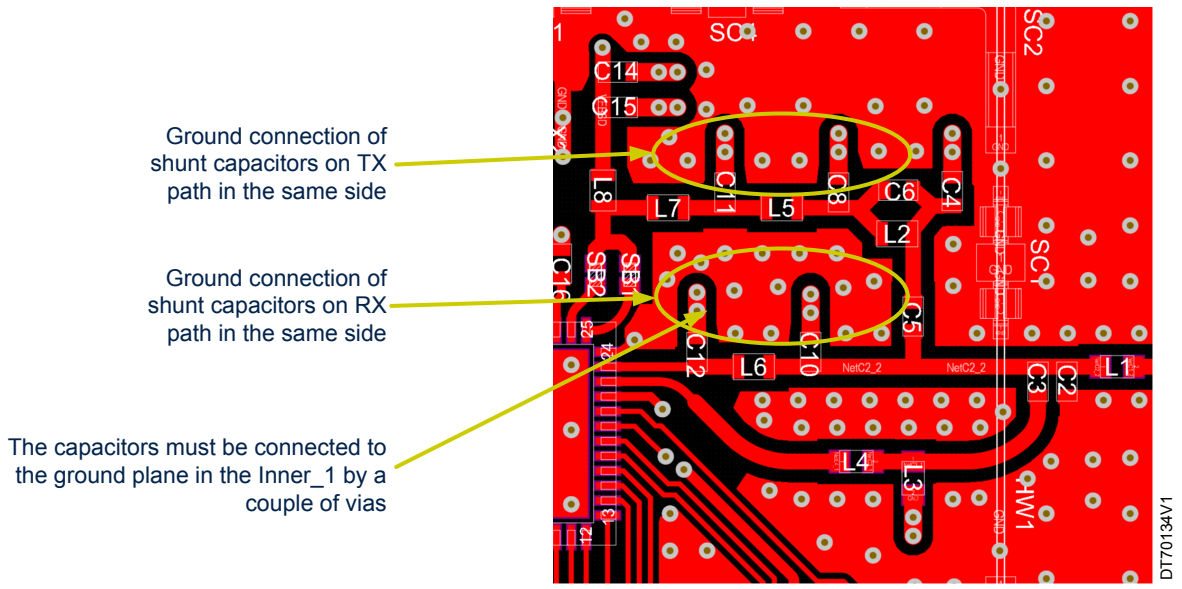
The interconnections between components are not considered transmission lines since their lengths are much shorter than the wavelength, hence, the impedance of these lines is not critical.

To maintain the characteristic impedance constant, make RF transmission lines short and straight and avoid any changes in width. As a result, the recommendation is to design the RF trace with a width equal to the width of the pad of the applied components. In this way, reflections at pad-trace transitions are prevented, and parasitic capacitance to ground is minimized.

There are two solutions to avoid unwanted spurious/harmonics radiation:

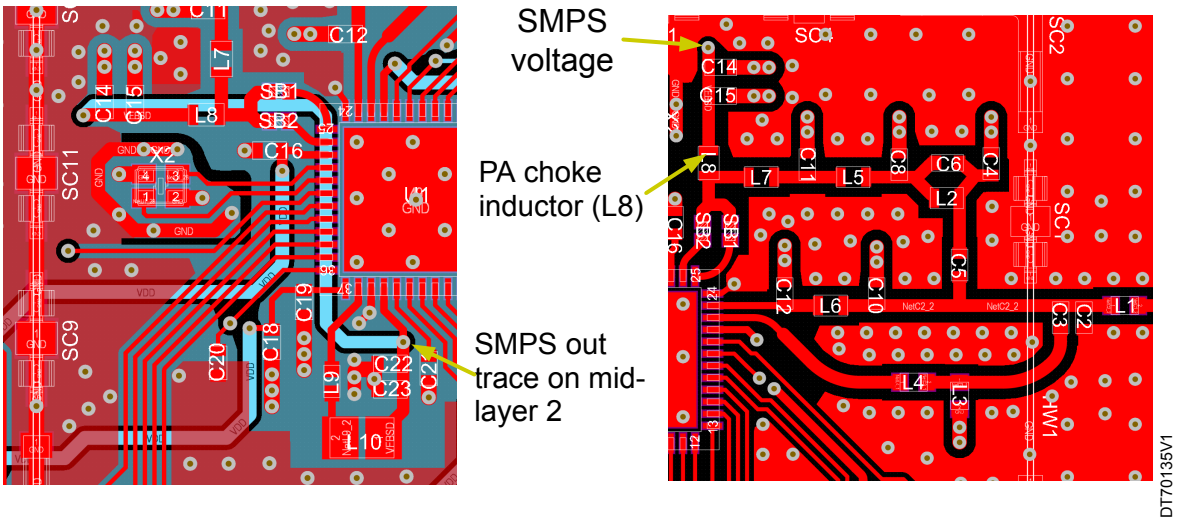
- Avoid connecting GND pads of shunt capacitors to the ground plane on the top layer. The shunt capacitors must be connected directly to the ground plane on Inner_1 through vias (see Figure 13).
- Avoid connecting the ground of shunt capacitors on different sides of the transmission line.

Figure 13. **Shunt capacitors connection**



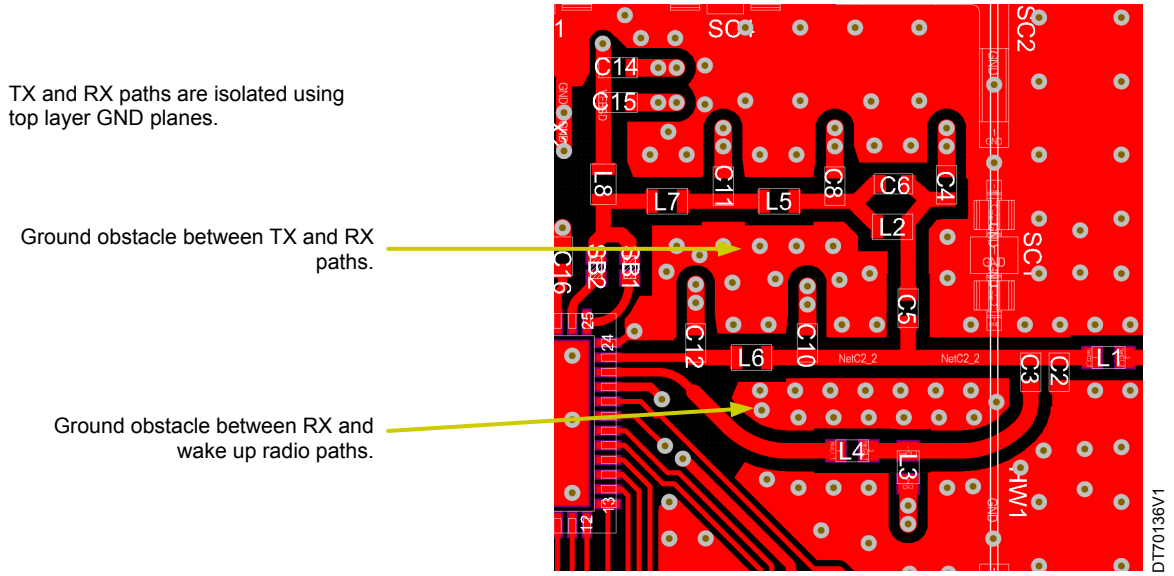
The integrated power amplifier is supplied by the output of the SMPS through a choke inductor and the trace which connects the SMPS to the PA is routed on Inner_2 (see Figure 14).

Figure 14. **SMPS – PA choke inductor connection**



Isolate TX and RX paths, including LPAWuR if used, using top layer GND planes. See Figure 15

Figure 15. Isolation between RF paths



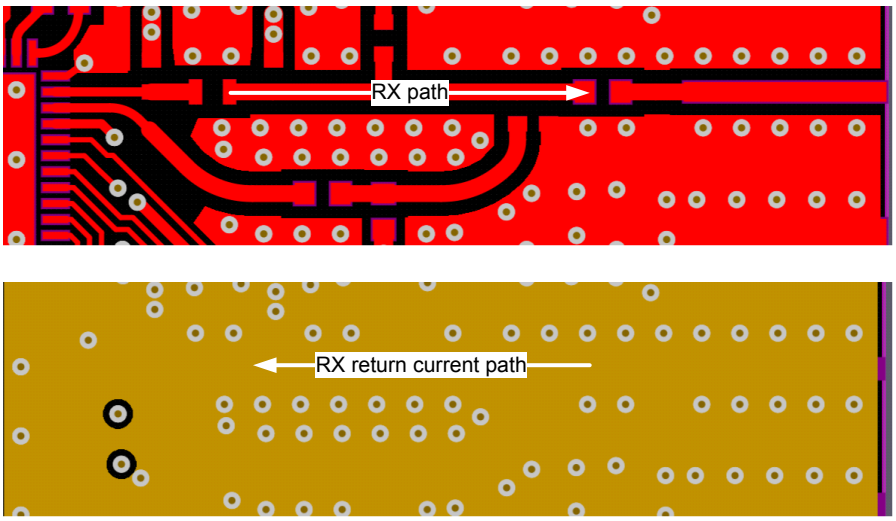
A return path is defined as the conductive path taken by the current returning to the source from the load. Generally, this return path is done on a grounded plane.

If this return path has a slot or an obstacle, the return current must find another route, and this results in a larger loop area that causes losses and EMI problems.

During the design, ensure that the return current can flow directly underneath the signal trace, avoiding any slots or obstacles in the GND plane.

The best solution is to avoid any slots, and vias in the ground reference plane as illustrated in Figure 16.

Figure 16. RF return path



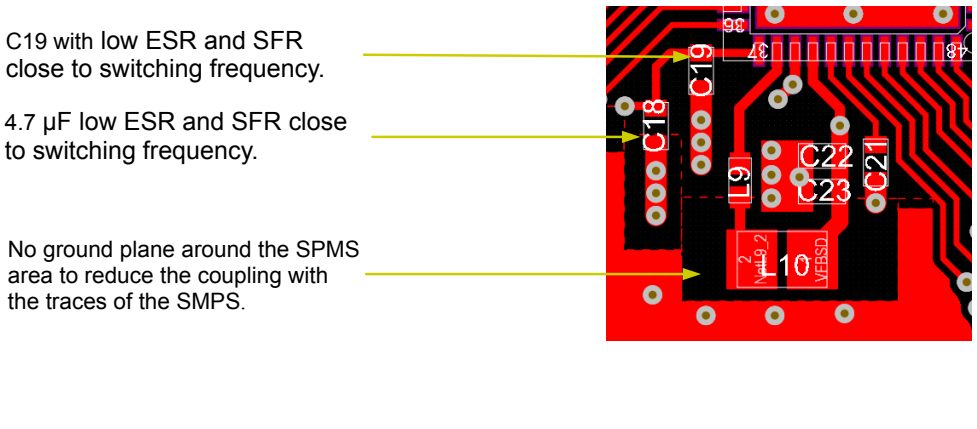
8 SMPS

The SMPS is a source of spurs at the harmonics of the switching frequency. Moreover, if TX and RX paths are directly connected, the performance of the receiver could be degraded by the activity of the SMPS.

The noise generated by the SMPS, can be reduced through the optimization of the power supply decoupling in the RF band; for this reason, it is important guarantee an impedance close to 0 Ω at the operating frequency between V_{DDSD} pin and QFN exposed pad.

- For the V_{DDSD} pin, two capacitors s are used as illustrated in Figure 17:
  - A 4.7 µF capacitor supplies the transient current at each switching period. To reduce voltage ripple on V_{DDSD} pin this capacitor must have a low ESR and SFR close to switching frequency.
  - C19 guarantees an impedance close to 0 Ω at the operating frequency between V_{DDSD} pin and QFN exposed pad. This capacitor must be placed as close as possible to V_{DDSD} pin to minimize the inductive influence of the trace.

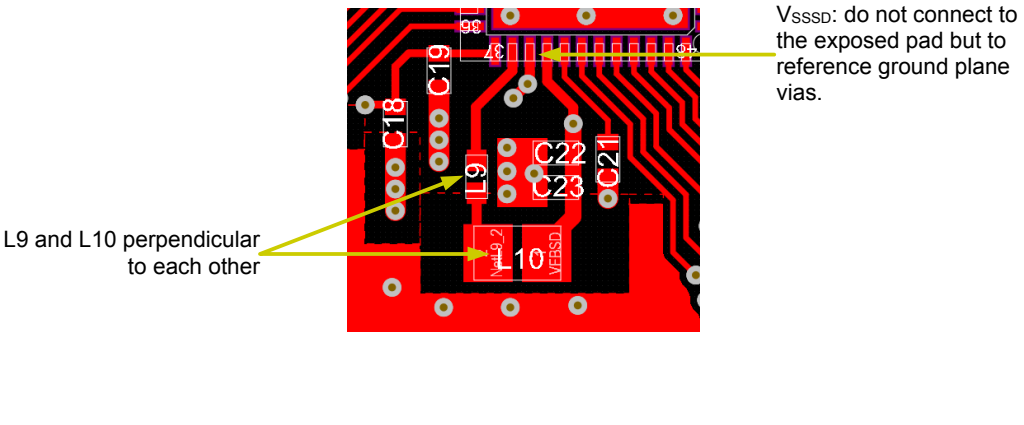
Figure 17. SMPS cut-out region region



- Remove the top GND around the SMPS area and connect them directly to the Inner_1 layer using vias.
- The ground pads of capacitors must be placed as close as possible to the exposed pad, to follow the shortest possible route and oriented to be located inside the SMPS loop.
- Place an RF inductor (L9) in series with the power inductor L10 to filter the noise generated by the SMPS at the operating frequency. Place the power inductor (L10) and the RF inductor (L9) perpendicular to each other to reduce mutual coupling.

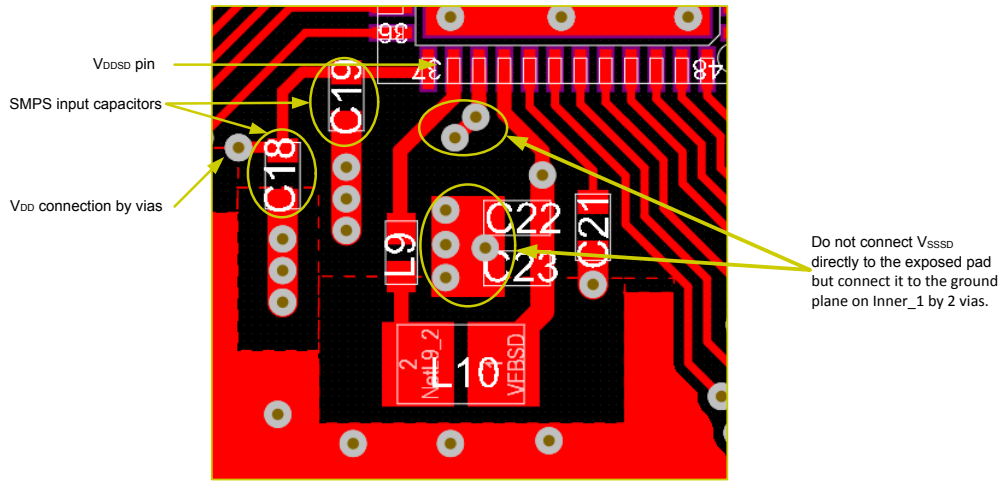
- Do not connect the V_{SSSD} pin to the exposed pad directly but connect it to the ground plane on Inner_1 by vias (see Figure 18).

Figure 18. SMPS inductors and V_{SSSD} pin



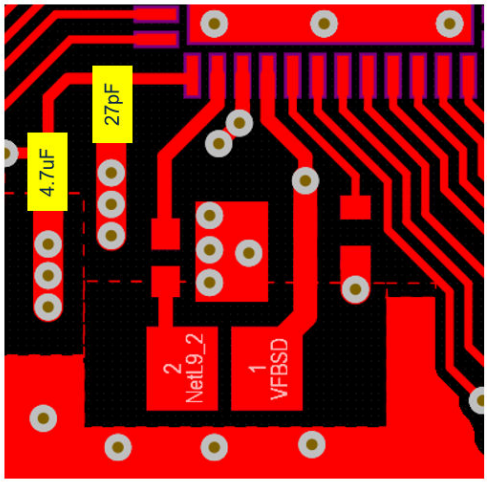
- To avoid any unwanted RF emissions, minimize the switching loop current on the top layer. Use vias to connect the GND pad of the capacitors to the GND Inner_1. Use more vias to reduce the series inductance of the capacitor and to guarantee a good current flow to the GND.
- To maintain a continuous ground plane on Inner_1, avoid any routing under the SMPS area. See Figure 19

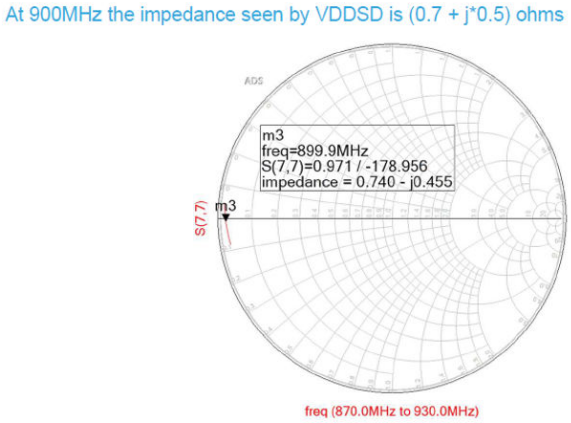
Figure 19. STM32WL3 SMPS ground connection



For high-band operations, use a 27 pF capacitor close to the V_{DDSD} pin. Figure 20 shows the impedance measured between the V_{DDSD} pin and the exposed pad at 900 MHz. The Smith chart shows how this capacitor guarantees an impedance close to zero at 900 MHz.

Figure 20. V_{DDSD} decoupling for 900 Mz band





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9 TCXO and XO

The XO crystal or temperature-compensated oscillators (TCXO) are used by the high-speed external (HSE) clock. Following the indication given below avoids the generation of spurs due to high-speed oscillators:

- Place the crystal as close as possible to the OSCIN OSCOUT pins of the chip to minimize parasitic capacitance due to traces.
- Connect the GND pads of the crystal directly to the ground plane Inner_1 by vias to avoid any unwanted radiator on Top layer.
- Avoid any routing under the crystal.
- To provide a “cleaner” GND for the crystal and avoid unwanted radiators, remove the TOP GND around the crystal and route straight down to the inner layer with through vias.
- Ensure a good separation between the SMPS zone and XTAL zone.

This is illustrated in Figure 21 and Figure 22.

Figure 21. MB2218 top layer

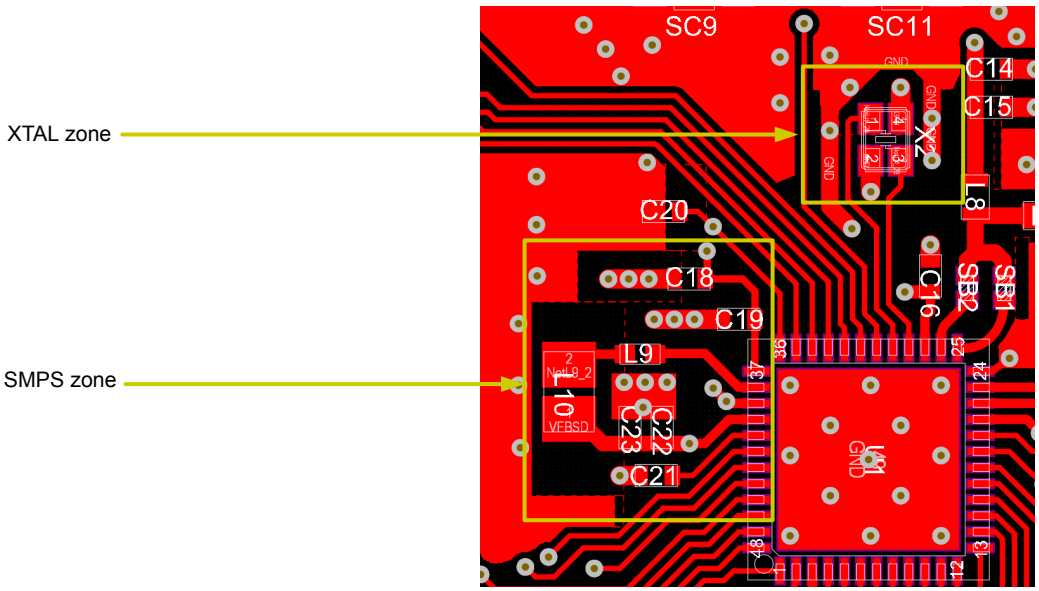
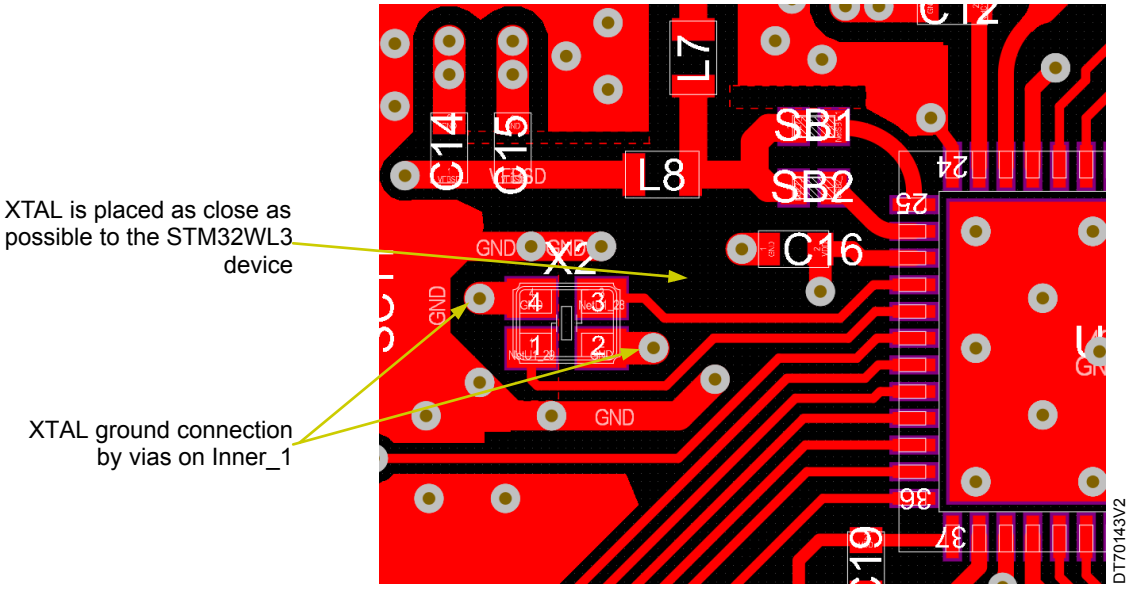


Figure 22. **XTAL placement and ground connection**



Use an isolating ground metal between the crystal and V_{DD} traces:

- To avoi any detuning effects on the crystal caused by the nearby power supply
- To avoid the leakage of the crystal/CLK signal and its harmonics to the supply lines.

Adopt techniques to increase the thermal resistance between the IC and the crystal oscillator as follows:

- a ground barrier on top layer (see Figure 23)
- cut-out regions between the crystal and IC on Inner_1, Inner_2 and bottom layers (see Figure 24)

This Provides additional heat propagation from the STM32WL3x to the crystal oscillator. This is especially true at +20 dBm operations.

Figure 23. **MB2218 top layer, Xtal region**

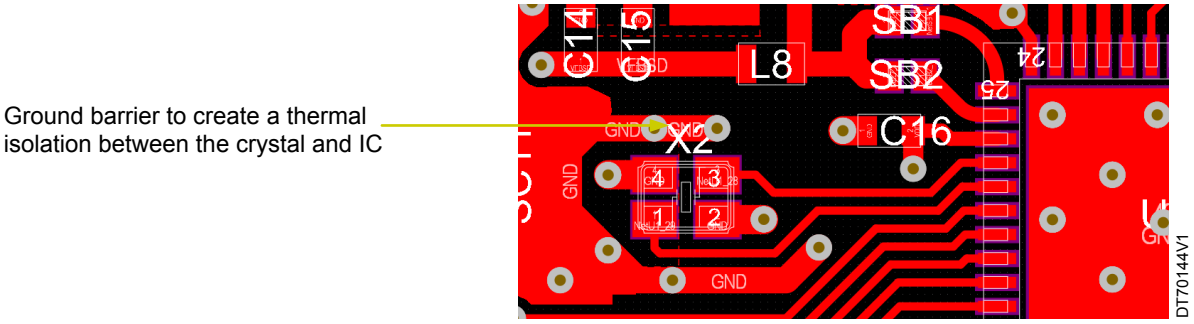
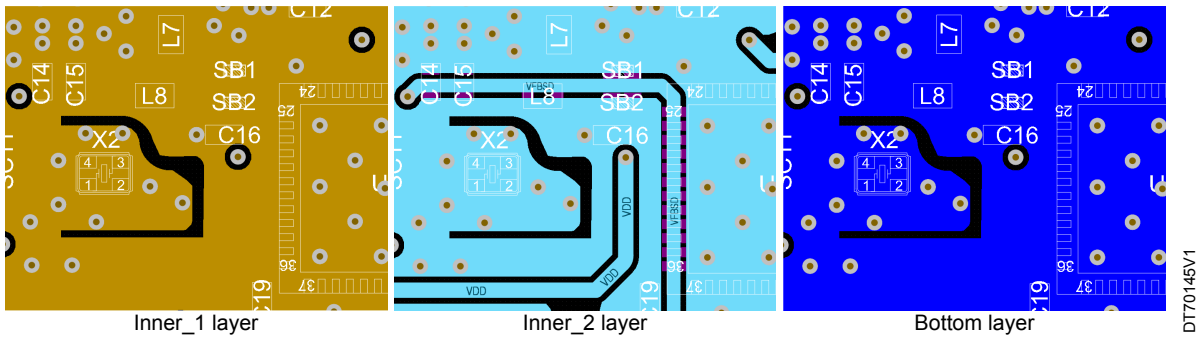


Figure 24. Inner_1, Inner_2 and bottom layer ground plane under the crystal

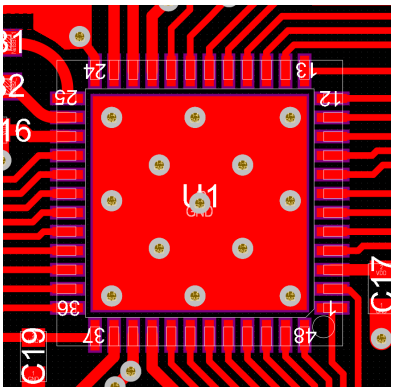


Important: Avoid any routing under the high-speed crystal and close to OSCIN and OSCOUT pins. If some routing under the HSE crystal is necessary, use the Inner_2.

10 Thermal relief pad

The thermal relief pad on the underside of the device provides both thermal relief and a solid ground reference to the chip. Figure 25 illustrates the multiple via connection of the exposed pad to the ground layer on Inner_1. The multiple vias ensure that the total parasitic inductance associated with the vias is minimized by several parallel connections. In addition, distributed vias ensure good thermal dissipation. Use a 4*4 ground-vias matrix to get the best results.

Figure 25. Exposed pad



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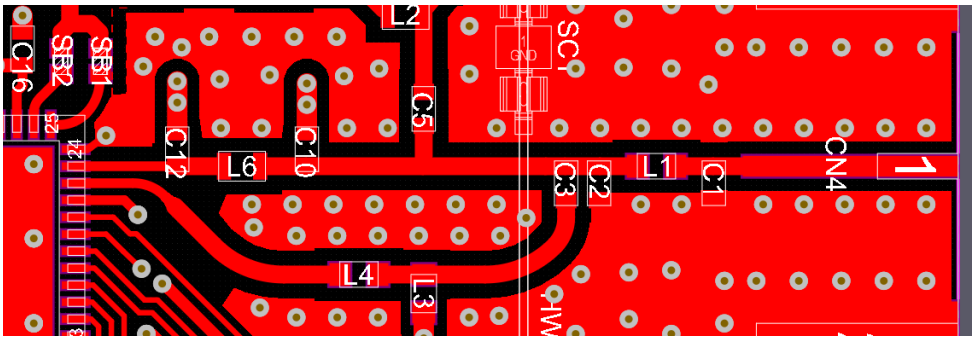
11 Via stitching and shielding

Via stitching is a technique used to tie together large copper areas on different layers, creating a strong vertical connection through the board structure. This helps maintain a low impedance and short return loops. Via stitching can also be used to tie areas of copper that might otherwise be isolated.

To reduce high-frequency issues, put some vias around the RF path, as shown in Figure 26 below.

Figure 26. Via fence around RF path



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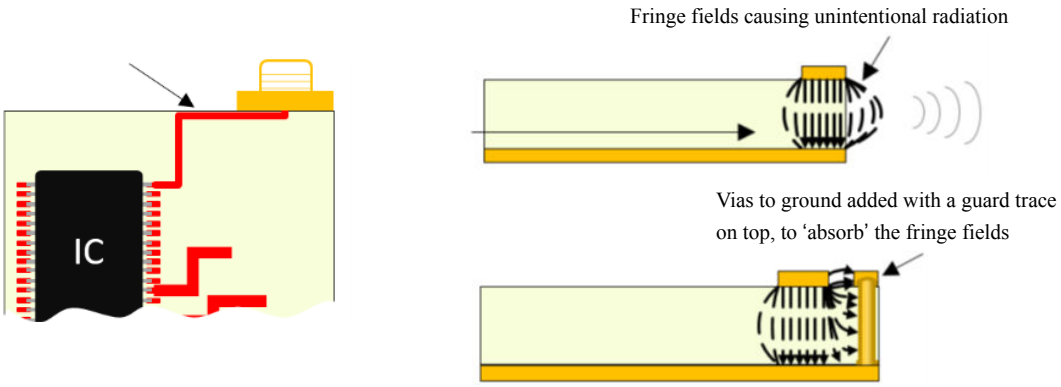
The edge of PCB is a possible source of unwanted emissions, due to the discontinuities in this part of the board. Routing high-frequency signals at board outline may cause unintentional EM radiation due to the fringing phenomenon, also known as the edge effect.

The same precaution must be taken for V_{DD} lines: do no route V_{DD} lines on the PCB edge as they could act as a receive antenna, bringing back RF signals into the chip through supply lines.

Fringing is the bending of the electric flux lines near the edge of the parallel plate capacitors. Normally, the flux lines inside the capacitor are uniform and parallel. But at the edges, the flux lines are not straight and bend slightly outward due to the geometry.

A common practice is to create a ring of stitching vias along the edges of the board to reduce radiation due to fringing fields. This is illustrated in Figure 27

Figure 27. **How to mitigate unintentional EM radiation**



The distance D between each via is determined according to the following equation:

$$\frac{\lambda_g}{20} \leq D \leq \frac{\lambda_g}{10}$$

where the guided wavelength λ_g is defined as:

$$\lambda_g = \frac{c}{f * \sqrt{\varepsilon_{eff}}}$$

where:

- C = the speed of light in vacuum
- f = the highest operation frequency of the RF circuit
- ε_{eff} = the effective dielectric constant of the PCB

12 MB2218 layers

The reference PCB 4-layer layout for the MB2218 is detailed in the figures below.

Figure 28. Top layer of MB2218 reference layout for QFN48

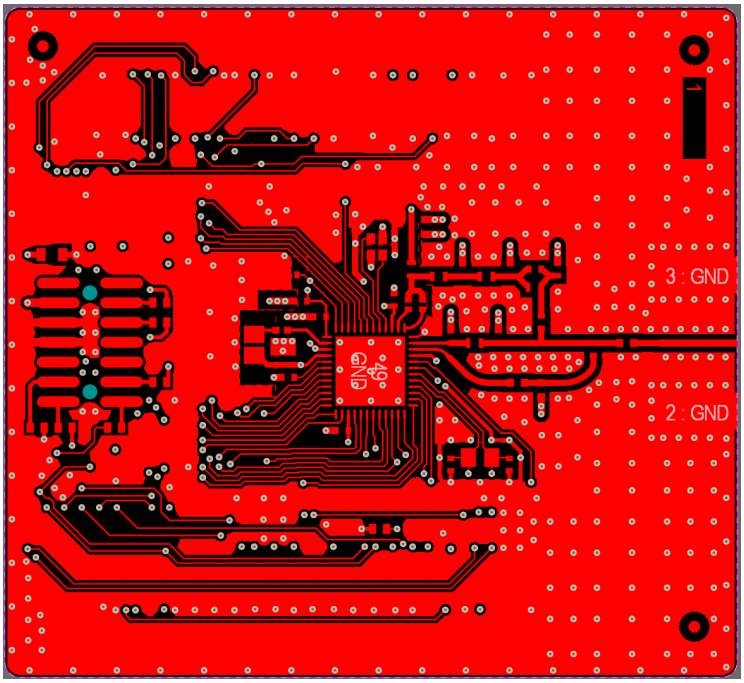


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Figure 29. Inner_1 layer (GND plane) of MB2218 reference layout for QFN48

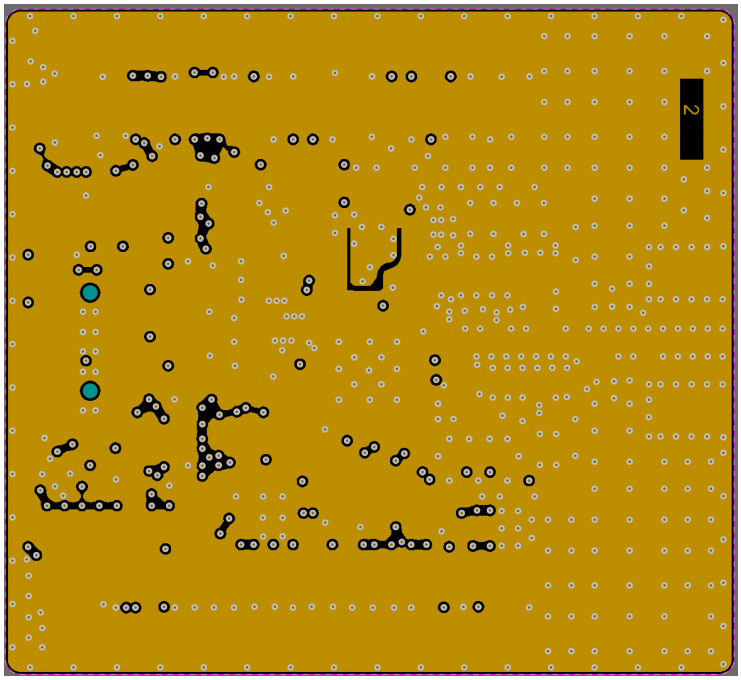

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Figure 30. Inner_2 layer (VCC layer) of MB2218 reference layout for QFN48

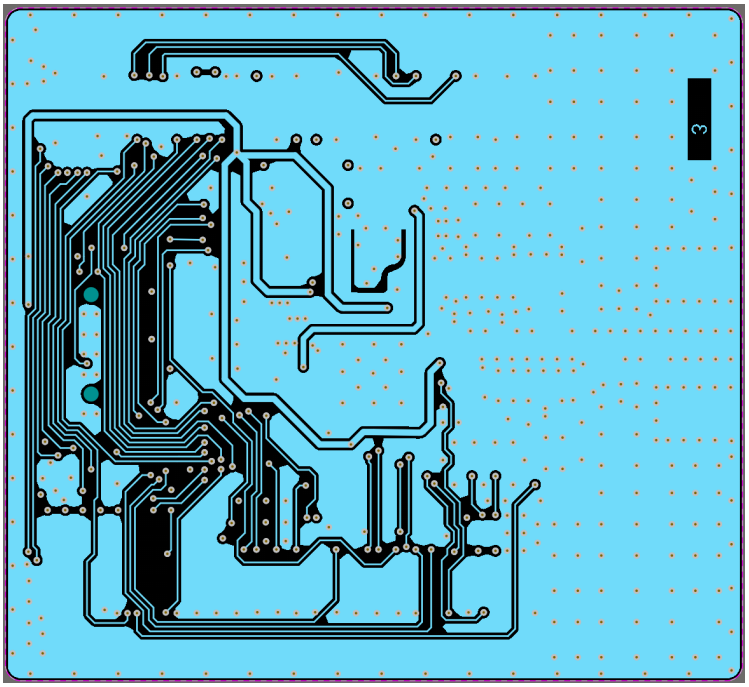

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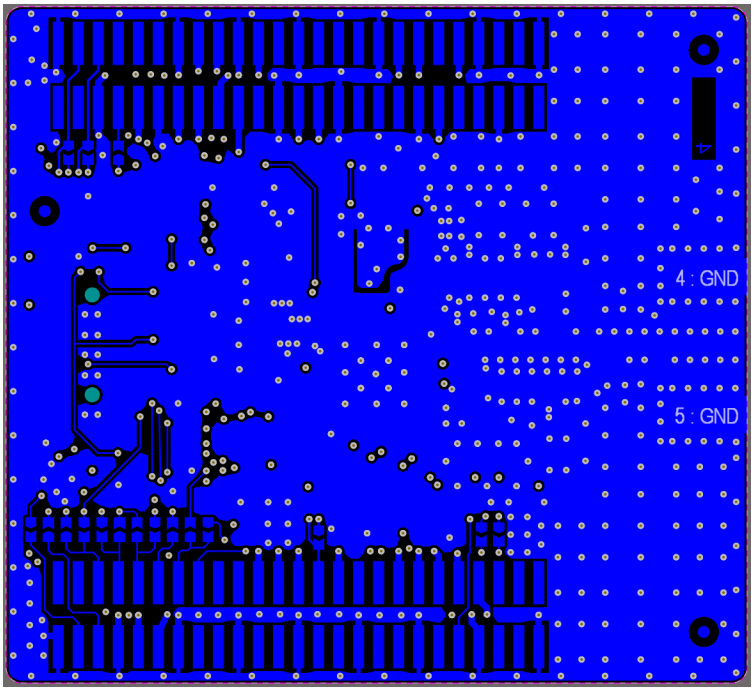
Figure 31. Bottom of MB2218 reference layout for QFN48



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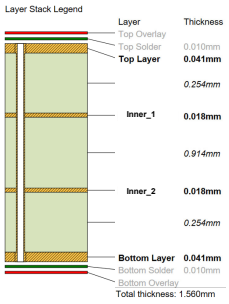
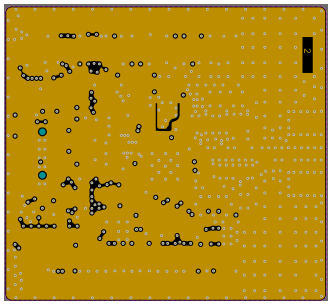
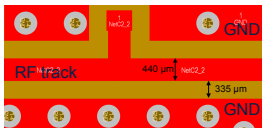
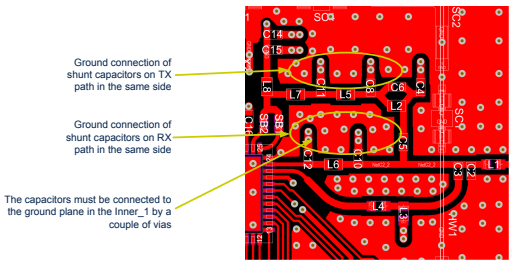
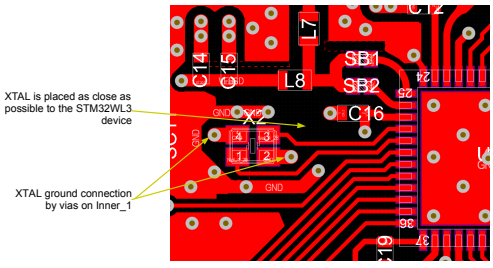
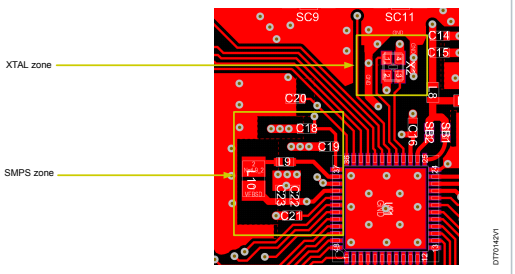
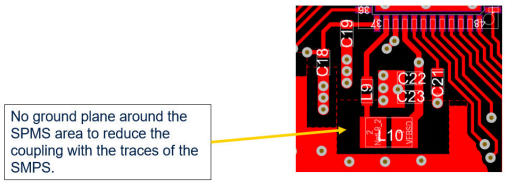
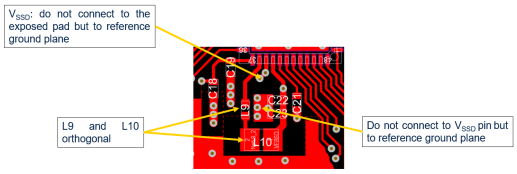
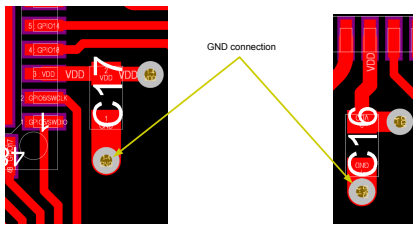
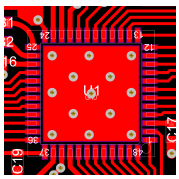
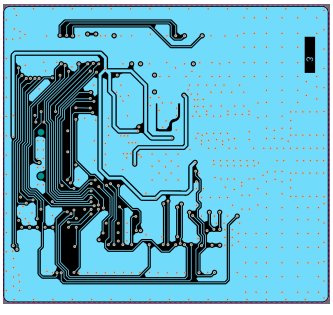
13 Check list

Stackup layers		
1	Check the thickness of the dielectric between the top and the Inner_1 layers is the same as the reference design (0.254 mm).	
2	Check the permittivity Dk at 1 GHz.	
Ground plane		
3	Check if there is a large, continuous ground plane on Inner_1, at least under the RF section.	
4	Ensure that the GND metal edges are closed by "stitching vias" where possible, with a via spacing of less than λ/10 (one tenth) of the highest critical harmonic frequency.	
RF trace		
5	Ensure the 50 Ω grounded coplanar lines used for RF traces are longer than λ/16 of the fundamental frequency.	
6	Ensure that there are vias at the ground metallization near the 50 Ω transmission lines.	
7	Ensure that the RF related components are placed at the furthest possible point from the DC-DC converter.	
8	Ensure that the matching network components are as close to each other as possible	
9	Ensure the ground pins of the shunt capacitors on the matching network are connected to the Inner_1 ground plane by vias.	
XTAL		
10	Ensure that the crystal for the high-speed oscillator is placed as close to the XTAL pins of the STM32WL33 as possible.	
11	Ensure that the XTAL is connected to the ground plane by vias.	
12	Ensure that a ground barrier is present around the XTAL to create a thermal isolation between the crystal and IC.	
13	Ensure a good isolation between the XTAL traces and V_{DD} traces. Avoid to route traces under the XTAL.	

SMPS		
14	Ensure a good isolation/separation between SMPS and XTAL regions to reduce the spurs due to the XTAL.	
15	Ensure the GND plane around the SMPS on the top layer has been removed. Ensure that vias are used to connect all the GND pads of the SMPS components to the ground plane on Inner_1.	
16	Do not connect the V_{SSSD} pin directly to the exposed pad. Connect the V_{SSSD} pin to the reference ground plane by vias. Connect the ground pads of the capacitors C22 and C23 to the ground plane.	
17	Ensure that the VDD filtering capacitors with the smallest values are placed as close as possible to the V_{DD} pins (V_{DD1}, V_{DD2}, V_{DDREF}, V_{DDSD}).	
18	The ground pins of the bypass capacitors must be connected to the Inner_1 ground plane by vias.	
Exposed pad		
19	Connect the exposed pad to the GND plane using multiple vias.	
20	Connect the EXT_GND pin to the ground plane on Inner_1 through a via. Also avoid connecting it directly to the exposed pad of the IC.	
21	Avoid traces on the Inner_1 (GND) between the grounding vias of V_{DD} filtering capacitors and the exposed pad.	
22	For digital signal routing, prefer a buried layer like Inner_2.	
23	Ensure that supply or digital lines are routed far from the PCB edge.	
24	Ensure that the V_{DD} traces are routed on Inner_2 layer. V_{DD} traces can be unwanted radiators. It is important to route these on the inner layers.	
25	Ensure good separation between GPIO traces and the RF line.	-

26	Use a series of GND stitching vias along the PCB edges. The maximum distance between the vias must be less than λ/10, which is a 10th of the harmonic. This distance is required to reduce the PCB radiation at higher harmonics caused by the fringing field of these edges.	-

Appendix A Reference documents

Table 5. Reference documents

Reference	Description
[1]	DS14221 *Multiprotocol LPWAN 32-bit MCU Arm® Cortex®-M0+ 2(G)FSK, 4(G)FSK, ASK, D-BPSK, up to 256KB flash, 32KB SRAM*
[2]	Reference designs for STM32WL3x microcontrollers databrief

Revision history

Table 6. **Document revision history**

Date	Version	Changes
18-Dec-2024	1	Initial release

Contents

List of tables

List of figures