STSPIN32G4 – Buck converter design guidelines

Introduction

The STSPIN32G4 is an extremely integrated and flexible motor controller targeting three-phase brushless motors. The device includes a gate driver to interface with an external power stage, an advanced microcontroller, and a power management circuitry effectively helping designers to reduce bill of material and PCB size.

Among the available features, a Buck regulator is embedded with the STSPIN32G4 that is designed to efficiently provide the gate driver supply voltage (VCC) starting from the motor supply voltage (VM).

This application note clarifies several aspects of the regulator starting from the working principle and its main features. Indications are provided for selection of external components as well as best PCB layout. Finally, some supply strategies are proposed in case the STSPIN32G4 should operate with a reduced input voltage going beyond the Buck operating range.

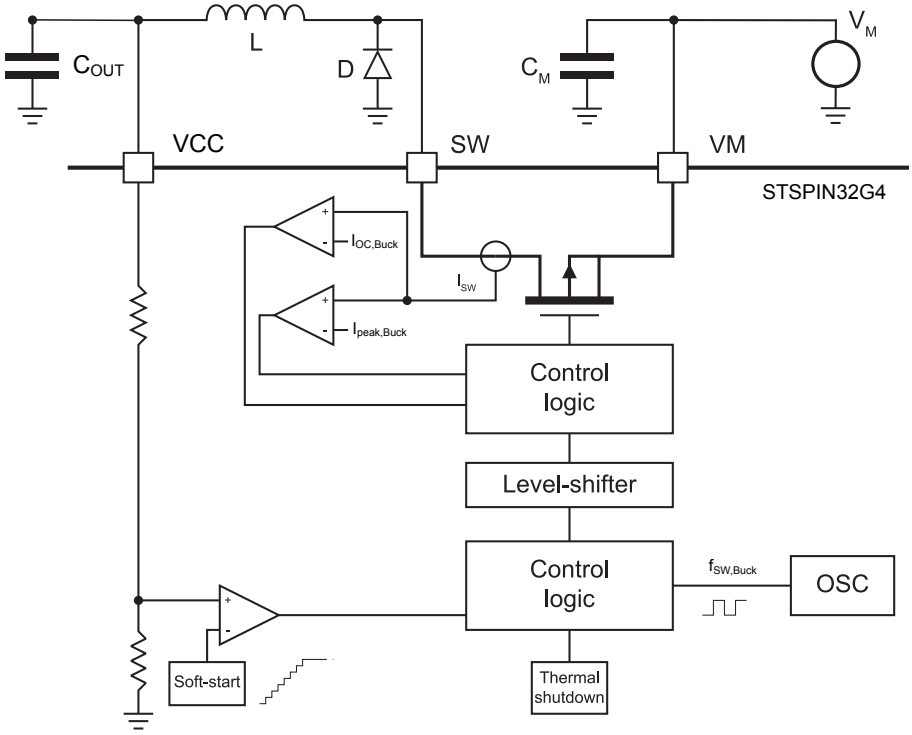
1 Overview

Details of the electrical characteristics and features of the regulator are provided in the STSPIN32G4 datasheet. In brief, the regulator has a current capability of 200 mA and provides configurable VCC output to 8 V (default), 10 V, 12 V and 15 V, soft-start, overcurrent protection and thermal shutdown.

Figure 1 shows a simplified block diagram of the converter and the external components required for proper operations:

- Input capacitor C_M,
- Diode D,
- Inductor L,
- Output capacitor C_{OUT}.

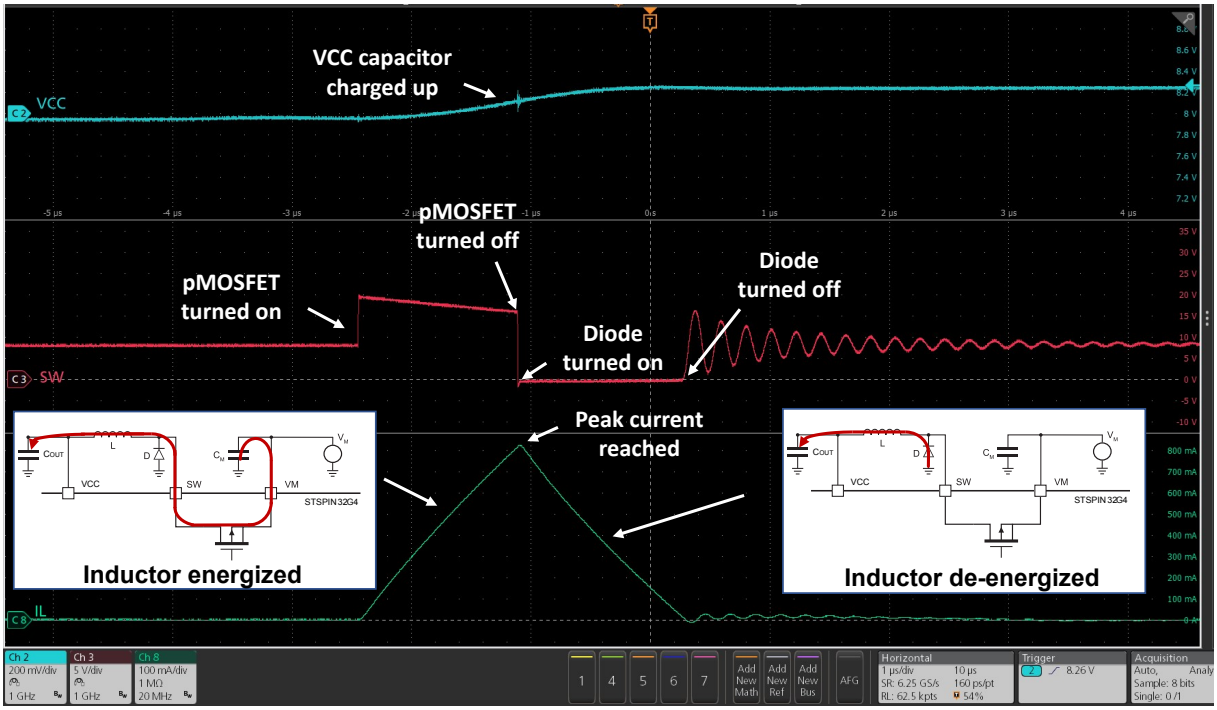
Figure 1. Buck regulator block diagram



1.1 Operating principle

The operating principle of the Buck regulator is based on hysteretic control with pulse-skipping as detailed below with reference to Figure 1 and Figure 2.

Figure 2. **Buck converter switching pulse**



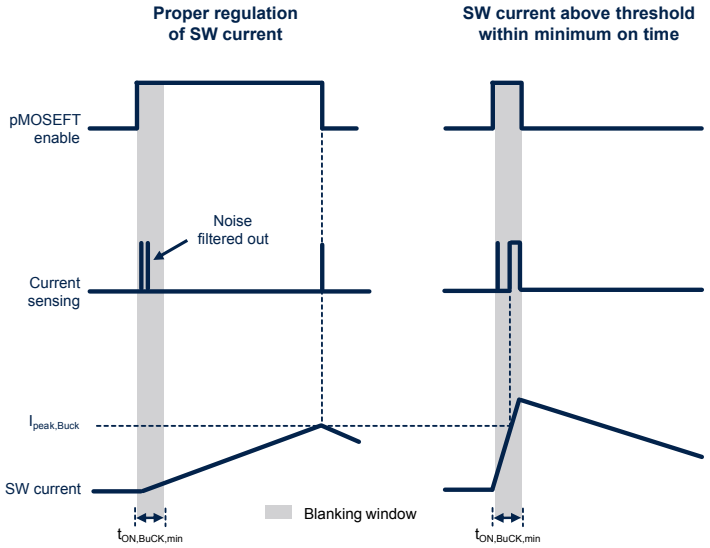
When VCC voltage is lower than the target value, the control logic of the Buck regulator turns on the integrated p-channel MOSFET connecting the SW pin to the VM supply. During this phase, the inductor L is energized and the output capacitor C_{OUT} is charged. The current flowing from the SW pin is sensed by control logic and the MOSFET is turned off reaching $I_{peak,Buck}$ = 750 mA (typ.). At this moment, the inductor current recirculates through the diode D and continues to charge the output capacitor. Depending on operating conditions and selected components, the de-energization of the inductor can complete before a new energization phase begins or not. Indeed, the controller generates a new SW pulse with a frequency of $f_{SW,Buck}$ = 500 kHz (typ.) until the VCC voltage reaches the target value. When target has been reached, no more pulses are generated until the VCC voltage drops below the hysteresis of the internal feedback comparator.

A minimum off-time ($t_{OFF,Buck\ min}$ = 220 ns typ.) for the MOSFET is guaranteed between consecutive SW pulses.

1.2 Minimum on-time

When the integrated MOSFET is turned on at the beginning of a switching cycle, the current flowing through the SW pin is not immediately monitored since the commutation could generate noise, and consequently induce a spurious triggering of the current control. With reference to the left panel of Figure 3, a blanking window is considered during which the output of the current comparators is ignored. Therefore, the SW current monitoring is correctly performed after commutation transients have expired. Because of this blanking window, the SW current can potentially overcome $I_{peak,Buck}$ as shown in the right panel of Figure 3. In this case the MOSFET is immediately turned off after the $t_{ON,Buck,min}$ = 220 ns (max.) and the regulator works at minimum on-time.

Figure 3. **Blanking window and minimum on-time**



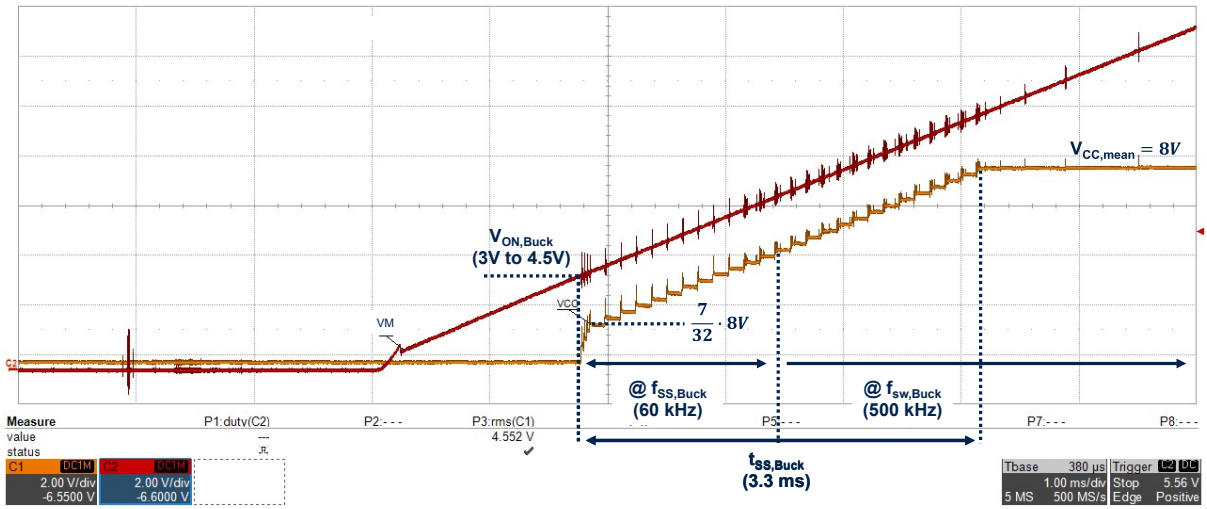
1.3 Soft-start

When the regulator is turned on, at power-up or changing the output voltage, a soft-start ramp is applied at the internal reference voltage. As shown in Figure 4, the regulator turns on when VM voltage overcomes $V_{ON,Buck}$ (from 3 V min. to 4.5 V max.). The starting level of the soft-start ramp corresponds to 7/32 of the VCC set point, then VCC is progressively increased up to the target value.

This behavior helps limiting inrush current from the power supply that would be generated in case of abrupt settling to the target value for charging the output capacitor.

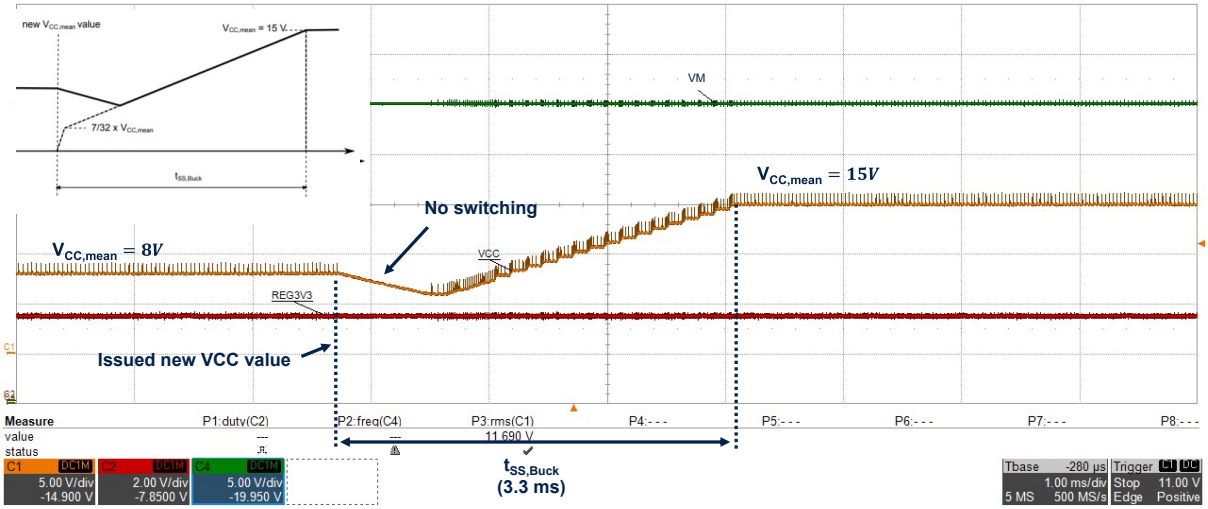
The soft-start ramp lasts $t_{SS,Buck}$ (3.3 ms typ.) and consists of two timeframes; the switching frequency is set to $f_{SS,Buck}$ = 60 kHz (typ.) during the first half of the ramp, then it is increased to the standard operative value $f_{SW,Buck}$ = 500 kHz (typ.).

Figure 4. **Soft-start at power-up**



Soft-start ramp is also applied in case of VCC set point change, as shown in Figure 5. In this case, the switching activity is paused after issuing the new set point because the internal reference is far below the actual output voltage. The decrease of VCC voltage in this timeframe depends on the current consumption from VCC and the output capacitor. Switching pulses restart when soft-start ramp intercepts VCC.

Figure 5. **Soft-start changing VCC setpoint**

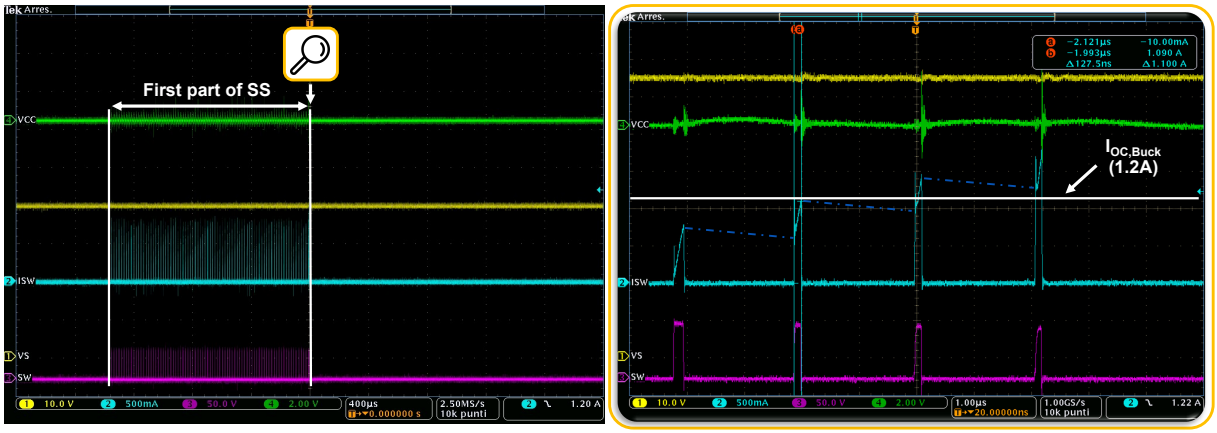


1.4 Overcurrent protection

The regulator integrates a protection in case of overcurrent. As explained in Section 1.2, the regulator can operate at minimum on-time with SW current above the $I_{peak,Buck}$ threshold. In this operating condition, if the SW current becomes higher than $I_{OC,Buck}$ = 1.2 A (typ.), the overcurrent protection triggers, causing the regulator to stop for a disabling time of $t_{disable,Buck}$ = 4 ms (typ.). At the end of this period, the buck regulator restarts performing a soft-start (see Section 1.3).

Possible cases of overcurrent detection are shorts of SW or VCC pin to ground. In the first case the overcurrent is immediately detected while in the latter case, the condition is typically reached when the switching frequency changes from the slower $f_{SS,Buck}$ to the faster $f_{SW,Buck}$ during soft-start. Indeed, as shown in Figure 6, the higher switching frequency prevents complete inductor de-energization so that in few switching pulses the regulator approaches minimum on-time and current increases above $I_{OC,Buck}$.

Figure 6. **Overcurrent detection with VCC shorted to ground**



2 External components selection

Guidelines for external components selection are provided in this section.

2.1 Inductor

The sizing of the inductor value can be done assuming a linear decay for inductor current where the energization and de-energization phases are modeled by the known formula:

Equation 1

$$\Delta t = L \cdot \frac{I_{MAX}}{\Delta V} \quad (1)$$

Being:

- Δt: Energization or de-energization time for the inductor, expressed in seconds
- L: Inductance value of the inductor, expressed in Henry
- I_{MAX}: Maximum value of the current flowing through the inductor, expressed in ampere
- ΔV: Voltage drop across the inductor, expressed in volt

It is recommended that both energization and de-energization phases complete within the converter switching time $1/f_{SW,Buck}$. Indeed, in case the inductor current does not reach zero at every switching pulse, the control could run into a minimum on-time issue and trigger an overcurrent after several cycles, as explained in Section 1.4.

The energization and de-energization times can be derived assuming $\Delta V = V_M - V_{CC}$ during energization and $\Delta V = V_{CC} + V_F$ respectively, being V_F the diode forward voltage. From these considerations, the following constraint on the maximum inductance value is obtained using Eq. (1):

Equation 2

$$\frac{1}{f_{SW,Buck}} > L \cdot \frac{I_{peak,Buck}}{V_M - V_{CC}} + L \cdot \frac{I_{peak,Buck}}{V_{CC} + V_F} \quad (2)$$

At the beginning of soft-start, the output capacitor is fully discharged and $\Delta V = V_M$ during the energization phase and $\Delta V = V_F$ during de-energization phase. As described in Section 1.3, the converter switching frequency is reduced to $f_{SW,SS}$ to accommodate a faster energization time and a significantly slower de-energization time during this initial phase.

Even with a lower switching frequency, the complete de-energization of the inductor could not be easily obtained at first switching pulses due to reduced diode forward voltage leading to very long de-energization time. However, this is typically acceptable as far as VCC voltage rises in few switching pulses, bringing the system in operating regions where complete de-energization is achievable.

The sizing of the inductor always requires that after the minimum on-time of the converter ($t_{ON,Buck,min}$) the inductor current is always lower, with adequate design margin, than the overcurrent threshold ($I_{OC,Buck}$). In this case the most critical condition is the very first pulse with $\Delta V = V_M$ that leads to a constraint on the minimum inductance value:

Equation 3

$$L > \frac{V_M \cdot t_{ON,Buck,min}}{I_{OC,Buck}} \quad (3)$$

Optimal inductance values can be computed considering the above constraints, for different input and output voltages of the converter, as reported in Table 1. The inductance value should be specified from the manufacturer with a tolerance of ±20%.

Table 1. **Optimal inductance values for Buck converter in µH**

		VM										
		75 V	70 V	65 V	60 V	55 V	50 V	45 V	40 V	35 V	30 V	25 V	20 V
VCC	8 V	18	18	18	18	18	15	15	15	15	15	12	12
	10 V	18	18	18	18	18	18	18	18	18	15	15	12
	12 V	18	18	18	18	18	18	18	18	18	18	15	12
	15 V	18	18	18	18	18	18	18	18	18	18	15	10

The maximum theoretical current capability of the regulator can be computed according to the following:

Equation 4

$$I_{CC} \sim L \cdot \frac{VM \cdot I_{peak,Buck}^2}{2 \cdot VCC \cdot (VM - VCC)} \cdot f_{SW,Buck} \quad (4)$$

Values reported in Table 1 guarantee that the Buck converter can provide at least 200 mA. Although it is possible to sink a current greater than the converter capability this is not a recommended operating condition and must be avoided.

From Eq. (4) it is also evident that the Buck regulator cannot provide full current capability during the first half of soft-start ramp due to its reduced switching frequency. For this reason it is recommended to wait at least $t_{SS,Buck}$ time before requesting full performance.

Because of the working mechanism of the converter, which is based on current pulses up to $I_{peak,Buck}$ = 750 mA (typ.), it is important to select an inductor with saturation current above this value. Considering a proper design margin, it is recommended to target 1 A for this parameter.

Since the inductor average current corresponds to the output current, the inductor DC rating should be above 200 mA corresponding to the maximum current capability of the converter.

Suggested part numbers are reported in Table 2 by Würth Elektronik, for each recommended inductance value. A shielded inductor can be used for better performance regarding electromagnetic interference.

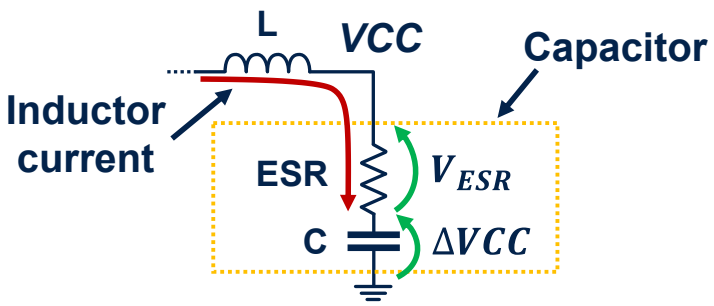
Table 2. **Recommended inductor part numbers**

	Unshielded inductor			Shielded inductor		
Nominal inductance	Part number	Saturation current	Rated current	Part number	Saturation current	Rated current
18 µH	744773118	1.29 A	1.1 A	744778118	1.7 A	1.41 A
15 µH	7447732115	1.01 A	0.64 A	744778115	1.75 A	1.51 A
12 µH	744773112	1.62 A	1.28 A	744778112	2.15 A	1.73 A
10 µH	7447732110	1.23 A	0.8 A	74438357100	4.6 A	2.7 A

2.2 Capacitors

Input and output capacitors should be selected with a value of 220 nF and 10 µF respectively, with a ±10% tolerance. It is important to select Multilayer Ceramic Capacitors (MLCC) because of their reduced Equivalent Series Resistance (ESR). A low ESR of the input capacitor helps to reduce the switching noise generated by the converter on the supply rail VM, while the ESR of the output capacitor plays a central role for VCC ripple magnitude. On each switching pulse the current flowing through the inductor charges the capacitor by $\Delta VCC = \frac{I_{CC}}{f_{SW,Buck} \cdot C_{OUT}}$ however, VCC voltage has an additional transient contribution due to ESR, that is, $V_{ESR} = i(t) \cdot ESR$, as shown in Figure 7.

Figure 7. **Effect of output capacitor ESR**



As evident from Figure 8, when using an electrolytic capacitor that has significant ESR, a transient voltage is generated on VCC at every switching pulse. This transient may reach the comparator threshold so that no more pulses are generated, even though actual VCC voltage is lower than its target. Conversely, no transient appears when using a low ESR ceramic capacitor, as shown in Figure 9, and two switching pulses are correctly performed to raise VCC.

Therefore, a high ESR capacitor produces a higher voltage ripple than expected because of the transient pulses, and a lower VCC mean value due to the sudden comparator triggering.

Figure 8. **10 µF high ESR electrolytic capacitor**

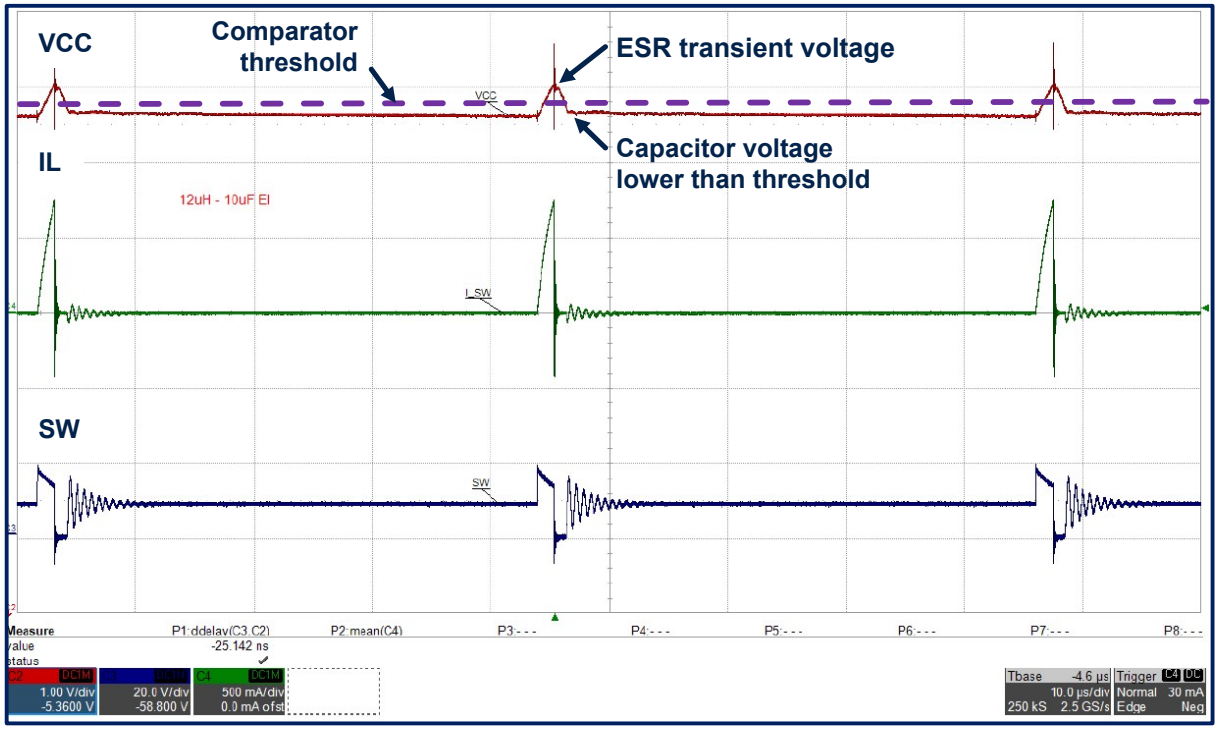
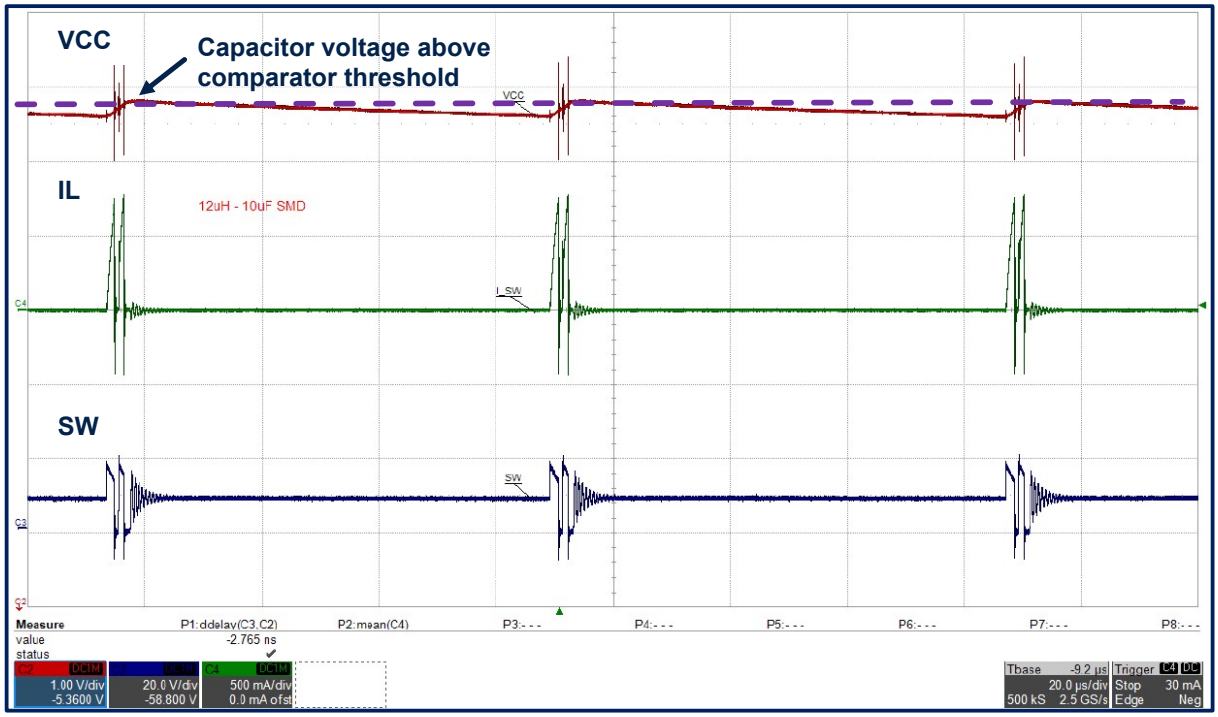


Figure 9. **10 µF low ESR MLCC**



Using an MLCC the peak-to-peak ripple of output voltage is typically bounded to:

$VCC_{PkPk} \cdot VCC_{mean} + 2 \cdot \Delta VCC$

Being:

- VCC_{PkPk}: the percentage referred to target VCC of peak-to-peak ripple (1.875% typ.)
- VCC_{mean}: the average regulated output voltage (8 V, 10 V, 12 V, 15 V typ.)

The recommended output capacitor of 10 µF provides an output ripple that is comparable to comparator hysteresis for the different input and output voltages with suggested inductors. Use of larger values is discouraged since the soft-start ramp could be distorted by reduced current capability, and regulator startup may eventually fail due to overcurrent. Smaller values can be used worsening the output ripple.

When ceramic capacitors are selected, particular attention must be paid on the voltage derating factor. Actual capacitance value decreases when the components are biased with a constant voltage, as is the case of input and output capacitors of the converter. Since the derating factor could reach 50%, a voltage rating at least two times the target VCC voltage for the output capacitor is recommended. An equivalent recommendation is valid for the input capacitor as well.

Considering the temperature range of the STSPIN32G4, class 2 ceramic capacitor X7R (-55 °C to +125 °C with ±15% deviation with temperature) are typically preferred but this can vary with application requirements.

2.3 Diode

A Schottky diode should be selected for reduced on voltage and losses. The diode should have repetitive peak reverse voltage (V_{RRM}) greater than the supply voltage VM and average forward current ($I_{F(AV)}$) above 200 mA. The repetitive peak forward current, which should be greater than $I_{peak,Buck}$, is not a limiting parameter and often not reported in the diode datasheet.

Suggested part numbers by STMicroelectronics are reported in Table 3 for applications up to 75 V and 48 V.

Table 3. **Recommended diode part numbers**

Part number	Max. forward voltage	Forward current	Max. reverse voltage
STPS1H100A	0.77 V	1 A	100 V
STPS0560Z	0.66 A	0.5 A	60 V

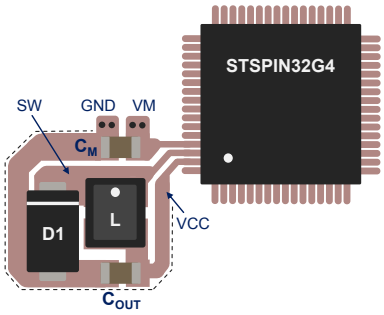
3 Layout recommendations

The PCB layout of the Buck regulator is critical to ensure low electromagnetic interference and noise injection throughout the system due to its switching activity. An example of proper placement and routing is presented in Figure 10. All external components of the regulator are grouped together close to the corner of STSPIN32G4 and on the same layer. This solution minimizes the area of current loops for best performance and at the same time simplifies other routing to the device. The input capacitor was placed as close as possible to STSPIN32G4 with two vias connecting both ground and VM rail for an effective decoupling through other layers. To manage impulsive currents of the converter, all traces should be straight without via holes along the path and with an increased width where possible to reduce parasitic series inductance and consequent bouncing.

The inductor terminal with dot marking should be connected to the switching pin SW achieving a better flux shielding thanks to the specific manufacturing of windings. It is recommended to use a dedicated PCB layer for ground connecting the STSPIN32G4 exposed pad with five vias (8 mil). Local ground of the Buck converter should be split from system ground using a moat in the ground plane as highlighted by the dashed line in Figure 10. The moated area includes all external components and has one aperture close to the STSPIN32G4 to implement a star ground topology. This technique helps for the bounding of high frequency switching currents and minimizes possible noise injection over sensitive circuits in the system like the analog sensing.

It is recommended to not route signals below Buck components (keep-out area), nor cut the ground plane other than shown in the figure. An improvement of layout thermal performance could be needed when using a diode or inductor other than the suggested one, due to higher power losses. In this case, the diode should be moved to the left side without altering the presented topology and a larger copper area can be allocated to the components pads for a better heat exchange.

Figure 10. Suggested layout of Buck converter



4 Working with low input voltage

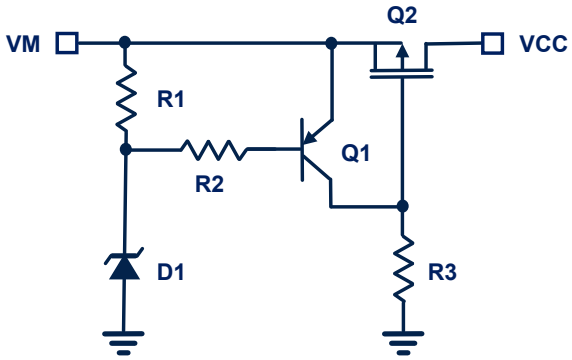
If VM voltage is lower than 15 V, the regulator may not have sufficient voltage drop to properly perform the inductor energization phase within converter timings. When the VM voltage approaches the target VCC, the regulator works at minimum off-time and VCC is lower than the VM of the V_{DROP} voltage depending on used inductor and load condition. Consequently, the driving of power MOSFETs becomes challenging at very low VM voltages since V_{DROP} may induce triggering of undervoltage lockout protection sooner than expected, that is, at VM of roughly $V_{CC(on)}$ (5.5 V max.) + V_{DROP}.

In these cases, two solutions are recommended:

1. Short together VM, SW and VCC pins and disable the Buck regulator.
2. Implement a Buck-Boost regulator as described by AN5748.

However, these solutions are no longer applicable with a varying VM voltage above 20 V due to violation of STSPIN32G4 absolute maximum ratings. To cover this further requirement, an automatic bypass of the Buck regulator could be easily implemented using few additional components, as shown in Figure 11.

Figure 11. Buck converter bypass circuit



Basically, the Q2 pMOSFET turns on when VM is lower than the threshold set via Zener diode D1.

The proposed circuit allows to take advantage of the Buck regulator in case of sufficiently high input voltage while shorting VCC to VM for operating at very low supply levels.

It is recommended a Zener diode with a breakdown voltage and minimum power rating of $V_Z \cdot \frac{VM_{max} - V_Z}{R1}$, being VM_{max} the maximum VM voltage in application. A small signal PNP bipolar transistor can be used for Q1 with a collector emitter breakdown voltage greater than VM_{max} and collector current rating of at least $\frac{VM_{max}}{R3}$. The suggested resistors value is 100 kΩ but this should be tuned depending on selected components. The Q2 pMOSFET should have gate-source maximum voltage of 20 V, on a threshold below 4 V, continuous drain current of 200 mA, and drain-source voltage of at least VM_{max}. Since the on-resistance of this MOSFET determines the voltage drop between VM and VCC; the lower the better.

5 Conclusion

The Buck converter integrated in the STSPIN32G4 was analyzed in this application note.

Several aspects were explained in Section 1 including its working principle, the minimum on-time, the soft-start ramp, and overcurrent protection.

Guidelines for the sizing of external components were provided in Section 2, simplifying the design phase of this regulator. Recommended part numbers are available in Table 2 for the inductor and Table 3 for the diode.

To avoid common mistakes that could impair performance of the entire system, several recommendations for proper PCB layout were provided in Section 3.

Finally, some tips were given in Section 4 to help designers to smoothly adapt the STSPIN32G4 to different power supply requirements of their applications.

Revision history

Table 4. **Document revision history**

Date	Version	Changes
11-Jul-2023	1	Initial release.

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