life.augmented

AN5959

Application note

Migrating within the STM32H5 MCUs

Introduction

The designers of STM32 microcontroller applications must have the possibility to replace one microcontroller type with another one from the same product family or products from a different family easily. The reasons for migrating an application to a different microcontroller can be for example:

- To fulfill higher product requirements, extra demands on memory size, or an increased number of I/Os
- To meet the cost reduction constraints that require to switch to smaller components and shrink the PCB area.

This application note details the steps required to migrate from an existing design between STM32H5 series microcontrollers.

This document provides the full set of features available for the STM32H503, STM32H562, and STM32H563/573 devices, and the equivalent features on the STM32H523/533 devices. This document also provides guidelines on both hardware and peripheral migration.

Migrating between devices within the same family could require hardware or software changes in some cases. Such changes are described in this document.

To understand better the information in this application note, the user must be familiar with the STM32 microcontroller family.

For additional information, refer to the product datasheets and reference manuals.

1 General information

STM32H503, STM32H523/533, STM32H562, and STM32H563/573 MCUs are 32-bit microcontrollers based on the Arm® Cortex® processor.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Table 1. Reference documents

Document number	Title
[1]	STM32H523/533, STM32H562, and STM32H563/573 reference manual (RM0481)
[2]	STM32H503 reference manual (RM0492)
[3]	Getting started with STM32H5 MCU hardware development (AN5711)

2 STM32H503, STM32H523/533,STM32H562, and STM32H563/573 MCU overview

2.1 Memory availability

Table 2 summarizes the memory availability of STM32H503, STM32H523/533, STM32H562, and STM32H563/573 MCUs.

Table 2. Memory availability

Products	Flash memory		RAM size (Kbytes)				Feature level
	Size	Bank	SRAM1	SRAM2	SRAM3	BKPSRAM	
STM32H573	2 Mbytes	Dual	256	64	320	4	With hardware crypto: AES, PKA, SAES, and OTFDEC
STM32H563	Up to 2 Mbytes	Dual	256	64	320	4	N/A
STM32H562	Up to 2 Mbytes	Dual	256	64	320	4	N/A
STM32H523	Up to 512 Kbytes	Dual	128	80	64	2	N/A
STM32H533	512 Kbytes	Dual	128	80	64	2	With hardware crypto: AES, PKA, SAES, and OTFDEC
STM32H503	128 Kbytes	Dual	16	16	N/A	2	N/A

2.2 System architecture

The STM32H5 devices embed:

- High-speed memories (Up to 2 Mbytes of dual-bank flash memory and up to 640 Kbytes of SRAM)
- A flexible external memory controller (FMC) for devices with packages of 100 pins and more
- One Octo-SPI memory interface (at least one Octo-SPI available on all packages) and an extensive range of enhanced I/Os and peripherals connected to three APB buses,
- Three AHB buses and a 32-bit multi-AHB bus matrix.

The following table illustrates the bus matrix differences between STM32H503, STM32H523/533, STM32H562, and STM32H563/573.

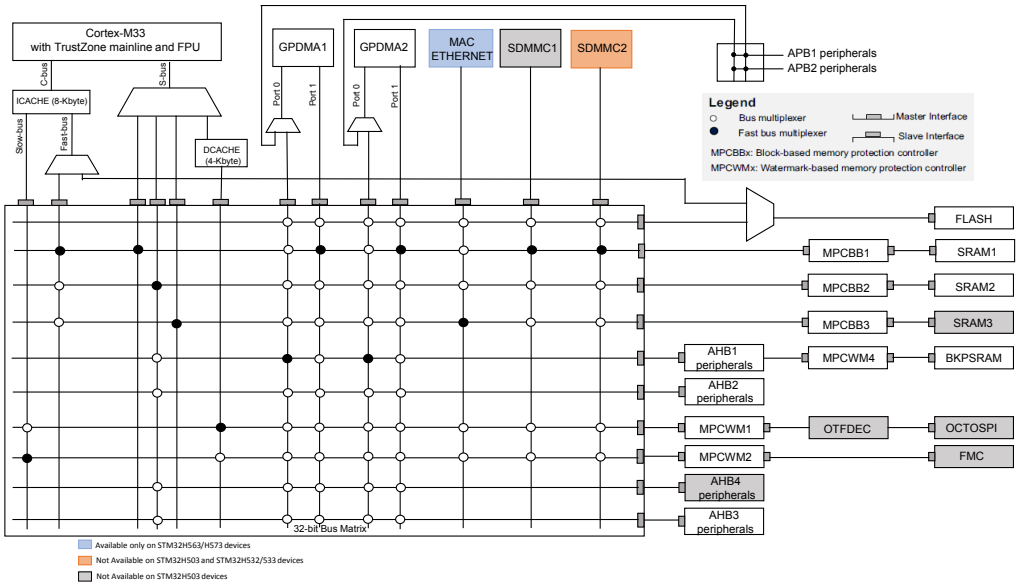
Table 3. Bus matrix

Bus type	STM32H503	STM32H523/533	STM32H562, and STM32H563/573
AHB bus matrix controllers	**Up to 7 controllers**: Fast C-bus, CPU S-bus for internal memories, GPDMA1 (featuring two controller ports), GPDMA2 (featuring two controller ports).	**Up to 11 controllers**: Fast C-bus, slow C-bus, CPU S-bus for internal memories, CPU S-bus for external memories, GPDMA1 (featuring two controller ports), GPDMA2 (featuring two controller ports), SDMMC1.	**Up to 13 controllers**: Fast C-bus, slow C-bus, CPU S-bus for internal memories, CPU S-bus for external memories, GPDMA1 (featuring two controller ports), GPDMA2 (featuring two controller ports), SDMMC1, SDMMC2, Ethernet MAC.
AHB bus matrix receivers	**Up to 6 receivers**: Internal flash memory, SRAM1, SRAM2, AHB1 peripherals (including APB1 and APB2), backup RAM, AHB2 peripherals, AHB3 peripherals.	**Up to 10 receivers**: Internal flash memory, SRAM1, SRAM2, SRAM3, AHB1 peripherals (including APB1 and APB2), backup RAM, AHB2 peripherals, FMC, OCTOSPI, AHB3 peripherals, AHB4 peripherals.	**Up to 10 receivers**: Internal flash memory, SRAM1, SRAM2, SRAM3, AHB1 peripherals (including APB1 and APB2), backup RAM, AHB2 peripherals, FMC, OCTOSPI, AHB3 peripherals, AHB4 peripherals.

The bus matrix provides access from a controller to a receiver, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously.

The system architecture of STM32H503, STM32H523/533, STM32H562, and STM32H563/573 is shown in Figure 1.

Figure 1. STM32H503, STM32H523/533, STM32H562, and STM32H563/573 devices system architecture



DT71848

3 Hardware migration

This section presents the package and pinout compatibility details for the hardware migration.

3.1 Package availability

The table below lists the available packages on the STM32H503, STM32H523/533 devices compared to STM32H562, and STM32H563/573 devices.

Table 4. Available packages

Package (Size in mm x mm)	STM32H503	STM32H523/533	STM32H562, and STM32H563/573(LDO version)	STM32H563/573 (SMPS version)
LQFP48 (7 x 7 mm)	X	X	N/A	N/A
LQFP176 (24 x 24 mm)	N/A	N/A	X	X
LQFP144 (20 x 20 mm)	N/A	X	X	X
LQFP100 (14 x 14 mm)	N/A	X	X	X
LQFP64 (10 x 10 mm)	X	X	X	N/A
UFQFPN32 (5 x 5 mm)	X	N/A	N/A	N/A
UFQFPN48 (7 x 7 mm)	X	X	N/A	N/A
UFBGA176 (10 x 10 mm)	N/A	N/A	X	X
UFBGA169 (7 x 7 mm)	N/A	N/A	X	X
VFQFPN68 (8 x 8 mm)	N/A	N/A	X	N/A
UFBGA144 (10 x 10 mm)	N/A	X	N/A	N/A
UFBGA100 (7 x 7 mm)	N/A	X	N/A	N/A
WLCSP	WLCSP25	WLCSP39	N/A	WLCSP80

X = available, N/A = not available

3.2 Pinout compatibility

The STM32H523/533 devices in the LQFP64, LQFP100, and LQFP144 packages have the same pins as the STM32H563/573 and STM32H562 devices. This means that users can experiment with different peripherals and achieve higher performance (higher frequency) during the development process, giving them more flexibility.

For the LQFP48, LQFP64 and UFQFPN48 packages, the STM32H503 devices are fully pin-to-pin compatible with the STM32H523/533 and with the STM32H562/563 for LQFP64 package.

For more details, see the corresponding application note[3].

4 Boot mode compatibility

4.1 System bootloader

The system bootloader is in the system memory, programmed by STMicroelectronics during the production.

It is used to reprogram the flash memory using one of the following serial interfaces.

The following table shows the communication peripherals supported by the system bootloader. For more details, refer to the application note *STM32 microcontroller system memory boot mode* (AN2606).

Table 5. Bootloader communication peripherals

System bootloader peripherals	STM32H503 I/O pin	STM32H523/533 I/O pin	STM32H562, and STM32H563/573 I/O pin
DFU	PA11/PA12		
USART1	PA10/PA9		
USART2	PA15/PA5	PA3/PA2	PA3/PA2
USART3	PA3/PA4	PD9/PD8(1)	PD9/PD8
CAN	FDCAN1 (PB5/PB15)	FDCANx (PB5/PB13)(2)	FDCANx (PB5/PB13)
I2C1	N/A	PB8/PB9 (3)	N/A
I2C2	PB3/PB4	N/A	N/A
I2C3	N/A	PA8/PC9(4)	PA8/PC9
I2C4	N/A	N/A	PD12/PD13
I3C1	PB6/PB7	PB6(5)/PB7	PB6/PB7
SPI1	PA7/PA0/PA8/PB8	PA7/PA6/PA5/PA4	PA7/PA6/PA5/PA4
SPI2	PB1/PB14/PB10/PB12	PC1(6)/PB14/PB10/PB12 or PB15/PB14/PB10/PB12	PC1/PB14/PB10/ PB12
SPI3	PC12/PC11/PC10/PD2	PC12/PC11/PC10/PA15(3)	PC12/PC11/PC10/PA15

1. *Only for LQFP100, LQFP144, UFBGA144 and UFBGA100*
2. *On STM32H5xx devices, FDCAN bootloader does not use an external quartz, and uses instead HSI and PLL.*
3. *Not available for LQFP48, UFQFN48, WLCSP39*
4. *PC9 is replaced by PB4 on LQFP48, UFQFN48 and WLCSP39.*
5. *PB6 is replaced by PB8 on LQFP48, UFQFN48 and WLCSP39.*
6. *PC1 is replaced by PB15 on LQFP48, UFQFN48 and WLCSP39.*

5 Peripheral migration

5.1 Cross-compatibility between STM32 products

STM32 microcontrollers embed a set of peripherals that can be classified in the following groups:

- Group 1: peripherals by definition common to all products
  Those peripherals are identical, so they have the same structure, registers, and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- Group 2: peripherals shared by all products but with only minor differences (in general to support new features)
  The migration from one product to another is very easy and does not need any significant new development effort.
- Group 3: peripherals that have considerable changes from one product to another (new architecture or new features for example)
  For this group of peripherals, the migration requires a new development at the application level.

The following table summarizes the available peripherals in STM32H5 series microcontrollers as well as their compatibility..

Table 6. STM32 peripheral compatibility between products

Peripherals		STM32H503	STM32H523/533	STM32H562, and STM32H563/573
Core		Cortex®-M33	Cortex®-M33	Cortex®-M33
Maximum CPU frequency		Up to 250 MHz	Up to 250 MHz	Up to 250 MHz
Flash memory		128 Kbytes	512 Kbytes	2 Mbytes
SRAMs	System	32 Kbytes (16+16)	272 Kbytes (128+80+64)	640 Kbytes (256+64+320)
	Backup	2 Kbytes	2 Kbytes	4 Kbytes
Timers	General purpose	1 (32 bits) and 1 (16 bits)	2 (32 bits) and 4 (16 bits)	2 (32 bits) and 8 (16 bits)
	Advanced control	1 (16 bits)	2(16 bits)	2 (16 bits)
	Basic	2 (16 bits)	2 (16 bits)	2 (16 bits)
	Low power	2 (16 bits)	2 (16 bits)	6 (16 bits)
	SysTick timer	1	2	2
	Watchdog timers (independent, window)	2	2	2
Communication interfaces	**SPI/I2S**	Up to 3x SPIs, including three multiplexed with full-duplex I2S and up to 3x additional SPI from 3x USART when configured in synchronous mode	Up to 4 SPIs, including three multiplexed with full-duplex I2S	Up to 6x SPIs. Including three multiplexed with full-duplex I2S and up to 5x additional SPI from 5x USART when configured in Synchronous mode (one additional SPI with OCTOSPI)
	I2C	2 (Fm+ interfaces SMBus/ PMBus)	Up to 3 (Sm and Fm interfaces (SMBus/ PMBus)	4 (Sm, Fm, and Fm+ interfaces (SMBus/ PMBus)
	I3C	2	2	1
	USART/UART	Up to 3 x USARTs	4 / 2	6 / 6
	LPUART	1	1	1
	USB	USB FS	USB FS	USB FS

Peripherals		STM32H503	STM32H523/533	STM32H562, and STM32H563/573
Communication interfaces	UCPD	No	Yes	Yes
	CAN	1 FDCAN	2 FDCAN	2 FDCAN
	SAI	No	No	2
	SDIO/SDMMC	No	1	2
	DCMI	No	Yes	Yes
	PSSI	No	Yes	Yes
	Ethernet	No	No	Yes (not available on STM32H562)
Flexible memory controller (FMC)		No	Yes (8,16-bit data bus width, no SDRAM)	Yes (8,16-bit data bus width with SDRAM)
OCTOSPI		No	1	1
DMA		2 GPDMA(Privileged/ unprivileged support/ linked-list)	2 GPDMA (featuring two controllers ports) TrustZone® support/linked-list	2 GPDMA (featuring two controller ports) TrustZone® support/ linked-list
CORDIC coprocessor		No	No	Yes
Filter mathematical accelerator (FMAC)		No	No	Yes
Real-time clock (RTC)		Yes	Yes	Yes
Random number generator (RNG)		Yes	Yes	Yes
SAES(1), AES		No	Yes	Yes
Public key accelerator (PKA)(1)		No	Yes	Yes
HASH (SHA-512)		SHA-256	Yes	Yes
On-the-fly decryption engine (OTFDEC)		No	Yes	Yes (2)
GPIOs		Up to 49	Up to 112	Up to 140
ADC (12 bits)		1 (12-bit ADC, up to 2.5 MSPS in 12-bit)	2 (12-bit ADC, with up to 5 MSPS)	2 (12-bit ADC, with up to 5 MSPS)
DAC (12 bits)		1xDAC (two channels)	1xDAC (two channels)	1xDAC (two channels)
Comparator (COMP)		1	N/A	N/A
Operation amplifier (op amp)		1	N/A	N/A
RCC		Yes	Yes	Yes
Operating temperatures		Ambient temperature: –40°C to +85°C/105°C, up to +125°C at low dissipation Junction temperature: –40°C to +130°C	Ambient temperature: –40°C to +85°C/up to +125°C Junction temperature: –40°C to +130°C	Ambient operating temperature: –40°C to +85°C / –40°C to +125°C Junction temperature: –40°C to +130°C
Operating voltage		1.71 to 3.6 V	1.71 to 3.6 V	1.71 to 3.6 V
Internal voltage reference buffer		No	Yes	Yes

1. *Available only on STM32H533 and STM32H573 devices*
2. *OTFDEC is not supported on STM32H56x*

Note: For further details, refer to the product datasheets.

Revision history

Table 7. **Document revision history**

Date	Version	Changes
20-Mar-2024	1	Initial release.

Contents

List of tables

List of figures

Disclaimer