AN6000

Application note

How to build the discrete power supply for STM32N6 MCUs

Introduction

This document provides a solution to supply power to STM32N6 MCUs with discrete regulators. The use of the internal SMPS is not covered in this document.

This document is intended for product architects and designers who require information about hardware integration and settings, and it focuses on:

- Reference design block diagram
- Discrete power supply topology
- Power on/off and low-power management
- Voltage regulator module (VRM) electrical specification for supplying the STM32N6 power rails

1 General informations

This document applies to STM32N6 series Arm®Cortex®-M55-based microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1 Referenced documents

Table 1. List of documents

Reference	Name/address	Title
[1]	RM0486	STM32N6 series Arm-based 32-bit MCU reference manual
[2]	DS14791	STM32N657xx Arm® Cortex®-M55, ST Neural-ART Accelerator,H264 encoder, Neo-Chrom 2.5D GPU, 4.2 Mbyte-contiguous SRAM Datasheet *Note: Select the datasheet corresponding to the targeted STM32N6x line.*
[3]	AN5946	How to optimize low-power modes on STM32N6 MCU
[4]	AN5967	Getting started with the hardware development for STM32N6 MCUs

1.2 Glossary

Table 2. Glossary

Term	Meaning
DVFS	Dynamic voltage frequency ccaling
LDO	Low drop out linear regulator
SMPS	Switching mode power supply
VRM	Voltage regulator module

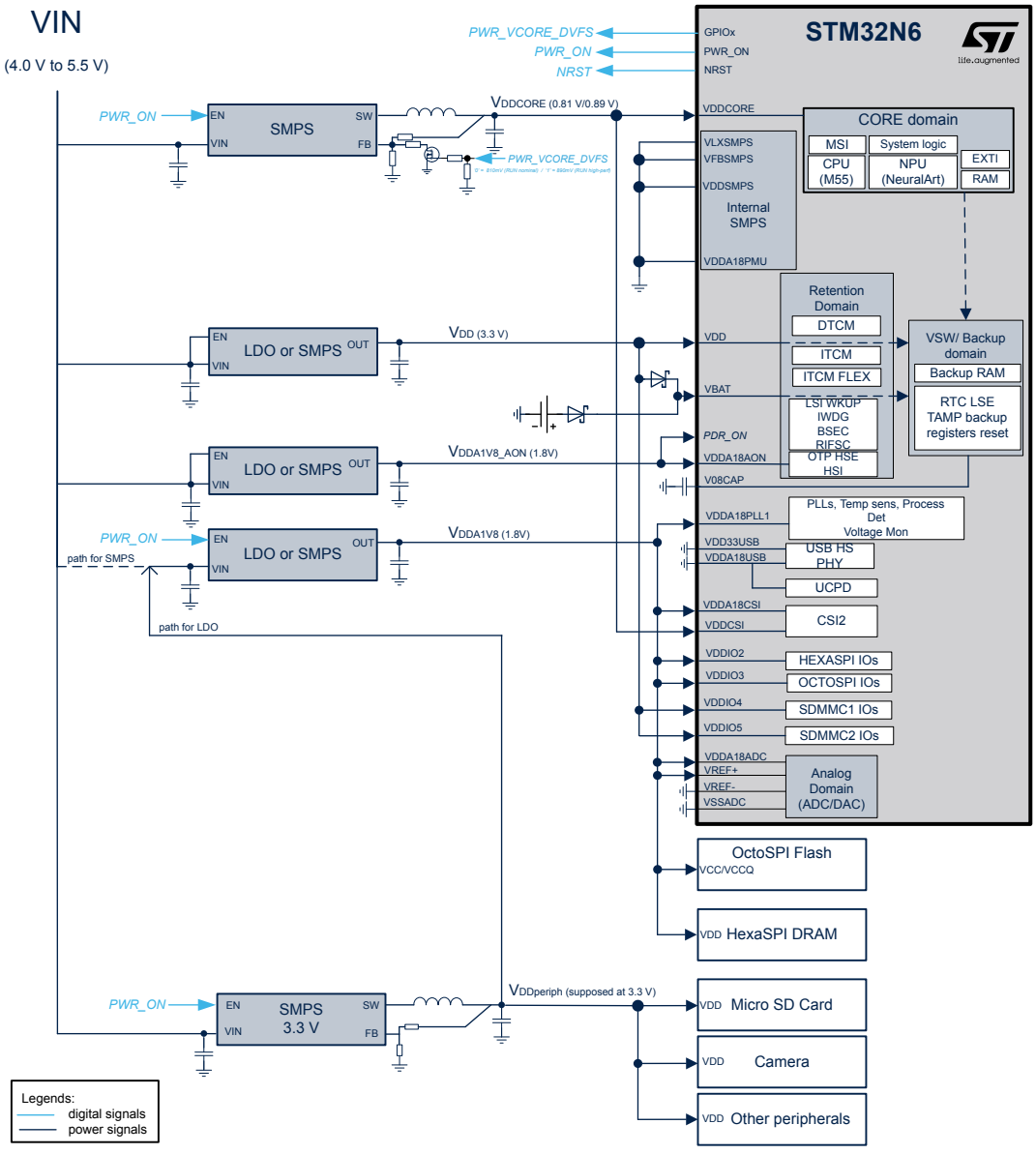
2 Discrete power supplies topologies

2.1 STM32N6 external SMPS, boot flash, DRAM

This reference design targets a system powered by a main supply of 5 V. The STM32N6 device core voltage is powered by external regulators with an I/O voltage of 3.3 V (V_{DD}), a boot flash memory, and a HexaSPI DRAM.

Other peripherals like SD card and camera module are added to illustrate the system.

Figure 1. STM32N6 with power discrete, SD card, and camera



Note: The following are not shown in the diagram:

- *The MCU decoupling scheme is not shown (refer to document [4]).*
- *SMPS and LDO regulator product part numbers and discrete components are not shown, but their electrical specifications are detailed in Section 4: Voltage regulator module specification.*
- *VIN source and related protections, such as ESD, EMI filtering and overvoltage are not shown.*

2.2 Internal or external SMPS topologies selection criteria

To supply the STM32N6 device core domain (V_{DDCORE}), the internal step-down SMPS or an external discrete step-down SMPS can be used. The selection criteria depend on the total power efficiency of the product and the cost of power components needed to design the product.

Design with external regulators

To supply the STM32N6 power domains, LDO or SMPS regulators can be used. The selection criteria between these two topologies are a trade-off between simplicity of integration, power efficiency performance and cost:

- LDO: simplicity of integration and selection, low noise, cheaper than an SMPS but poor power efficiency inferring thermal heating concern.
- SMPS: good power efficiency (lower thermal heating than LDO), but more complex to select and to integrate. More expensive and higher noise than LDO due to switching activity.

For an application powered from a DC source, typically powered from AC to DC wall adaptor, power efficiency is less critical than in battery applications. Nevertheless, thermal heating remains an important criterion and must be minimized as much as possible. This is especially so when the application runs the most power-consuming use case. Reciprocally, an application in Standby mode must have regulators with a low quiescent current for those kept on, and regulators with low leakage current for those turned off.

With an SMPS, the design is more complex and requires the designer to choose the right passive components (inductor, capacitors) to ensure correct system operation. In addition, adding passive components takes up space on the PCB and adds extra cost.

Design with the internal SMPS

Using the internal SMPS (with recommended discrete components) guaranties the electrical performance required to supply the STM32N6 V_{DDCORE} domain (DC accuracy, load transient response, Vripple max). This simplifies integration and design efforts.

To supply the other power domain, in particular the V_{DDA18x} analog power domain, the internal SMPS can be used in series using an additional external SMPS to convert the product input voltage (for example: VIN = 5 V) to 1.8 V to supply both the V_{DDA18x} power domain, and the input supply of the internal SMPS. This choice helps saving a regulator (LDO or SMPS) dedicated to supplying the V_{DDA18x} power domain and to reduce cost. To avoid too much noise at the input of the V_{DDA18x} power domain due to the association of the two SMPS (internal and external SMPS), two passive filters must be added (for example: one ferrite bead at the input of the internal SMPS and LC filter at the input of the V_{DDA18x}), which complicates the integration and takes up more space on the PCB.

The power efficiency of the global solution (internal SMPS and discrete SMPS for V_{DDA18x}) is partly restraint as $\eta total = \eta_{extSMPS} \times \eta_{intSMPS}$.

The internal SMPS description is not in this application note scope.

2.3 Power distribution

For the power distribution of the described system shows in Figure 1, LDO or SMPS regulator topology can be implemented. The choice of the regulators is a trade-off between several criteria described in Table 3:

Table 3. Power discrete topology LDO vs SMPS

Topology	Advantages	Disadvantages
LDO	• Simple integration • Low noise • Efficient if the output voltage is close to the input voltage. • Relevant for domains where power consumption is always low	• Poor power efficiency ($\eta_{tLDO} \sim V_{OUT} / V_{IN}$) • Power losses/heating
SMPS	• High-power efficiency • Low-power dissipation • Faster load transient response • Relevant for domains where power consumption is significant	• More complex to integrate than LDO • Higher noise than an LDO due to the switching activity • Generate EMI and electrical noise • More expensive than LDO

2.3.1 Input voltage

The system example in Figure 1 is powered from a 5 V typical DC voltage source (VIN).

The minimum VIN voltage must be higher than the highest voltage used in the application. For this application that is without USB port, 3.3 V is the highest voltage required (to supply V_{DD}, V_{DD_periph}). Else, 5.2 V is required for application with USB host port. Considering the ideal regulator (no dropout) and ideal power source, the minimum VIN is 3.3 V.

In real conditions, a reasonable 400 mV dropout for 3.3 V regulators (working at full load) and a 300 mV drop on the VIN path (including DC and AC drop and margin) requires a minimum VIN voltage of about 4 V.

The maximum VIN voltage is limited by the regulator powered by VIN having the lowest maximum-rated input voltage. In this application, it is assumed that regulators absolute maximum rating is about 5.5 V.

So, in this application example, the VIN range is 4 V to 5.5 V.

2.3.2 V_{DDCORE} power domain (810 mV/ 890 mV)

V_{DDCORE} is the main STM32N6 device digital core domain. It supplies all digital circuitries including the Arm®Cortex®-M55 CPU, the neural processing unit (NPU), system logic, MSI internal clock, and some analog IP of the MCU (CSI).

The V_{DDCORE} is the most power-consuming domain with order of 1500 mW peak in the worst running conditions, and 10 mW in Stop mode nominal conditions.

Design with a discrete LDO

For the V_{DDCORE} power domain, LDO topology is not recommended due to the high ratio between V_{DDCORE} and VIN (0.81 V/ 5 V ratio of 0.16). A power efficiency of 16% means significantly more energy consumed by the LDO converter than the energy consumed by the STM32N6 device itself.

Design with a discrete SMPS

A step-down SMPS topology is recommended to guarantee a high-power efficiency.

To support the Run high-performance mode (defined in Section 3.3: VDDCORE voltage scaling in Run modes), V_{DDCORE} regulators need to manage two voltage settings: 810 mV for Run nominal mode and 890 mV for Run high-performance mode.

The V_{DDCORE} regulator must comply with strict electrical parameters to fit with the STM32N6's requirement (see Section 4.1: VRM specification for V_{DDCORE} power domain).

2.3.3 VDD power domain (3.3 V/1.8 V)

V_{DD} is the power supply for the STM32N6's V_{DD} domain which includes MCU I/Os, the V_{DDIO1}, V_{DDIO2}, V_{DDIO3} and V_{DDIO4} independent supplies I/Os, the retention domain, and the backup domain.

Note: V_{DDIO1}, V_{DDIO2}, and V_{DDIO3} supplies can have different voltage or be shut down independently.

In the system example in Figure 1, the V_{DD} domain is powered from a 3.3 V source.

The power consumption on the STM32N6's V_{DD} domain (3.3 V) is in the order of 5 mW in nominal running conditions, in Sleep mode, and Stop mode. It can however increase significantly due to I/Os activities; typically when parallel interfaces with I/Os set as output are operating. In other words, the power consumption variation on the V_{DD} domain is mainly impacted by I/Os activities and so it depends on product design: number of I/Os (set as output) operating in parallel, bus frequency, parasitic capacitance on PCB tracks.

Example: if the LTDC interface is instantiated in the application, peaks of current about 100 mA can occur on V_{DD} due to LTDC IOs activity (assuming 24 bits interface = 24 IOs with 30 pF capacitance stray per PCB track at 88 MHz bus frequency). Idd = 0.5 × C × V_{DD} × f × NBios = 0.5 × 30 pF × 3.3 V × 88 MHz × 24 = 105 mA.

Accordingly, it is recommended to use a regulator having 200 mA minimum output rating current; but this value remains application dependent.

The V_{DD} domain can be powered by either an LDO or an SMPS depending on the power efficiency wished and the cost.

Design with an LDO

For the V_{DD} power domain, LDO topology is a good compromise between power losses, voltage noise and cost:

- The ratio between V_{DD} and VIN (3.3 V/5 V ratio) is 0.66. The LDO efficiency is about 66% quasi constant.
- The average current consumption is low (1.5 mA – 6 mA) also for complex use cases.
- In the Standby low-power mode, the V_{DD} domain is kept alive. In general, an LDO has a lower quiescent current than an SMPS, so in Standby mode the LDO has a better power efficiency than an SMPS.

Design with an SMPS

For the V_{DD} power domain, a step down SMPS topology can also be implemented to have a high-power efficiency with very-low-power losses.

The V_{DD} regulator must comply with strict electrical parameters to fit with the STM32N6's requirement (see Section 4.2: VRM specification for V_{DD} power domain).

2.3.4 V_{DDA1V8_AON} power domain (1.8 V)

The V_{DDA1V8_AON} is the power supply of the STM32N6's $V_{DDA18AON}$ system analog domain supplying reset blocks, power management, oscillators, and OTP controller in the retention domain.

The power consumption on the STM32N6's $V_{DDA18AON}$ domain is in the order of 1-5 mW depending on operating conditions, and it mainly depends on oscillators usage. The maximum power consumption is 18 mW (10 mA) during OTP programming operation. In Standby mode, power consumption is in order of 0.07 mW.

This domain can be powered by either an LDO or an SMPS depending on the power efficiency wished and the cost.

Design with an LDO

For the V_{DD1V8_AON} power domain, the average consumption is low in all operating mode, and the LDO topology is recommended:

- The ratio between V_{DD1V8_AON} and VIN (1.8 V/ 5 V = 0.36) is 0.36. The LDO efficiency is about 36% quasi constant.
- The average current consumption is low: low loses/thermal heating is negligible.
- In low-power mode, Standby the V_{DD1V8_AON} domain is kept alive. In general, a LDO has a lower quiescent current than an SMPS, so in Standby mode the LDO has a better power efficiency than an SMPS.

Design with an SMPS

For the V_{DD1V8_AON} power domain, a step down SMPS topology with an ultra-low quiescent current must be implemented due to the low-consumption of this power domain.

The VDDA1V8_AON regulator must comply with strict electrical parameters to fit with the STM32N6's requirement (see Section 2.3.4: V_{DDA1V8_AON} power domain (1.8 V)).

2.3.5 V_{DDA1V8} power domain (1.8 V)

V_{DDA1V8} is the power supply of the STM32N6's VDDA18x power domains which includes: PLLs ($V_{DDA18PLLx}$), CSI ($V_{DDA18CSI}$), USB ($V_{DDA18USB}$), ADC ($V_{DDA18ADC}$, V_{REF+}), and the internal SMPS ($V_{DDA18PMU}$) when used.

The power consumption on the STM32N6's V_{DDA18x} domains is in the order of 2-30 mW depending on operating conditions and decrease below 0.1 mW in Stop mode.

Nevertheless, the V_{DDA1V8} power domain can also be used to supply application peripherals as illustrated in the system example in Figure 1 (the OctoSPI NOR flash memory and the HexaSPI RAM). In that case, particular attention must be kept to select regulator with the appropriate rated output current.

This domain can be powered by either an LDO or an SMPS depending on the power efficiency wished and the cost.

Design with an LDO

For the V_{DDA1V8} power domain, LDO topology is recommended for its intrinsic low-noise figure (no switching activity). Despite poor power efficiency, about 36% due to the ratio between V_{DD1V8} and VIN (1.8 V/5 V = 0.36). Alternatively, if application embeds a 3.3 V SMPS to supply application peripheral, it can be used to supply the LDO input to improve the power efficiency.

Design with an SMPS:

For the V_{DDA1V8} power domain, a step down SMPS topology can be also implemented to have a higher power efficiency (90%) than an LDO. But the switching activity of the SMPS can create some noise on the input of the STM32N6 analog domain.

Regardless of LDO or SMPS topology, the V_{DDA1V8} regulator must comply with strict electrical parameters to fit with the STM32N6's requirement (see Section 4.4: VRM specification for V_{DDA1V8} (analog) power domain).

2.3.6 STM32N6 backup domain VSW and retention domain

The STM32N6 embeds two internal power domains to keep in memory critical data and secret keys:

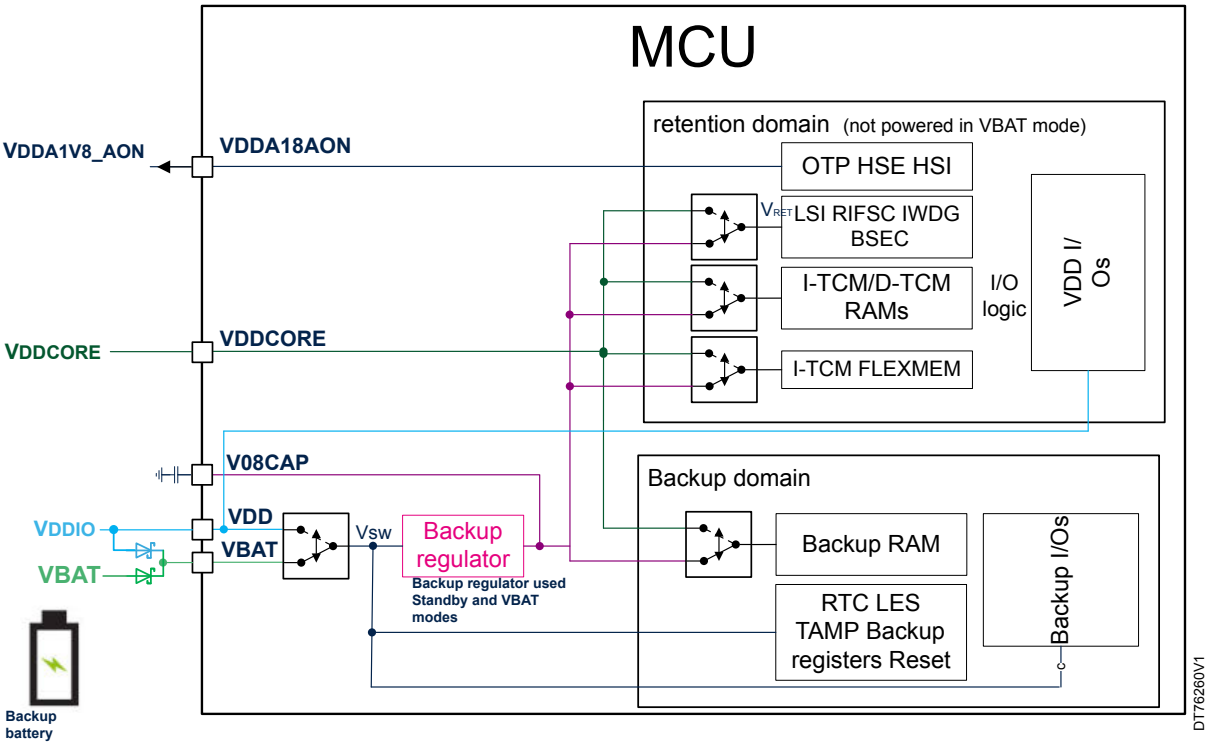
- **The backup domain:** used to supply the RTC, LSE, TAMP registers, backup registers, and backup RAM. They must be retained when V_{DDIO} is turned off to keep critical data or secret keys. The backup domain is powered in all operating modes, including VBAT mode (with V_{BAT} typically powered from a coin cell backup battery).
- **The retention domain:** used to supply OTP controller (BSEC), the independent watchdog (IWDG), the resource isolation framework controller (RIFSC and IAC), I-TCM, D-TCM and I-TCM FLEXRAMs. The retention domain is powered in all operating modes, excluding VBAT mode.

These two domains can be powered by V_{DDCORE} or V_{DD} or V_{BAT} depending on which supply is available and the operating mode of the MCU:

- In Run and Stop mode, the backup domain, and the retention domain are powered from the V_{DDCORE} supply.
- In Standby mode, the backup domain and the retention domain are powered from the V_{DD} supply via the internal backup regulator (decoupling capacitor on V08CAP pin).
- In VBAT mode, (VBAT powered from a backup battery). The backup domain is powered from the V_{BAT} supply via the internal backup regulator.

Note: The retention domain is not powered in VBAT mode.

Figure 2. Backup and retention domains



3 Power management

3.1 Operating modes

The system can switch to a different operating mode depending on the system activity.

Power domains are switched on or off depending on the operating mode. The voltage scaling on V_{DDCORE} can switch in Run nominal mode or in Run high-performance mode according to required performances. So, the corresponding voltage is set in accordance with the system clock frequency.

The STM32N6's PWR_ON signal is a dedicated output allowing to manage the Standby mode.

Table 4. Operating modes

Operating mode	PWR_ON	Description
RUN (nominal or high-performance)	1	• V_{DD}/$V_{DD1V8AON}$ power on • V_{DDCORE} power on (in nominal or high-performance voltage) • V_{DDA1V8} power on • CPU clock on • Peripherals clocks on
SLEEP	1	• V_{DD}/$V_{DD1V8AON}$ power on • V_{DDCORE} power on (in nominal or high-performance voltage) • V_{DDA1V8} power on • CPU clock gated • Peripherals clock on (PERxLPEN bits)
STOP	1	• V_{DD}/$V_{DD1V8AON}$ power on • V_{DDCORE} power on (in nominal voltage) • V_{DDA1V8} power on • CPU clock off • Peripherals clock off (PERxLPEN bits)
STANDBY	0	• V_{DD}/$V_{DD1V8AON}$ power on • V_{DDCORE} power off • V_{DDA1V8} power off • CPU clock power off • Peripherals clock power off
VBAT	0	• V_{DD}/$V_{DD1V8AON}$ power off • V_{DDCORE} power off • V_{DDA1V8} power off • CPU clock power off • Peripherals clock power off

3.2 System power-up/uncontrolled power-down sequence

The system initially has no power source connected. An external power supply source is connected. The VIN voltage rises triggering the system to power up. The system initializes and runs. The external power supply source is then removed triggering an uncontrolled power-down sequence.

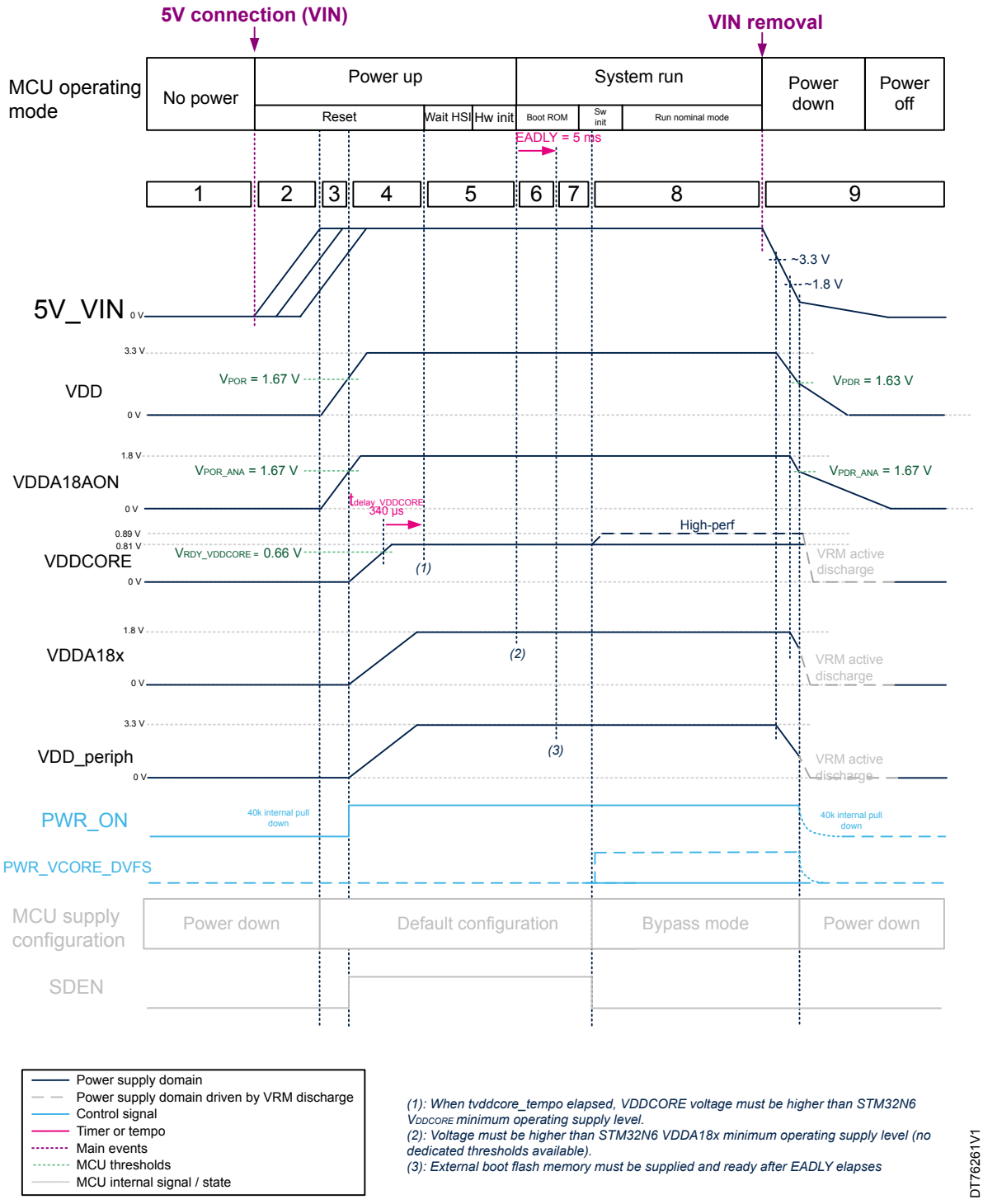
1. The system has no power.
2. A power supply is connected to the system. VIN voltage rises.
3. Once the VIN voltage crosses the V_{DD} and $V_{DDA18AON}$ discrete regulators startup voltage internal threshold, V_{DD} and $V_{DDA18AON}$ regulators starts and V_{DD} and $V_{DDA18AON}$ voltages starts to rise.
4. Once V_{DD} and $V_{DDA18AON}$ voltages cross respectively STM32N6's V_{POR} and V_{POR_ANA} rising both thresholds, the PWR_ON signal is activated and the regulators V_{DDCORE}, V_{DDA18x} and V_{DD_periph} are enabled. Once V_{DDCORE} voltage reaches the STM32N6's $V_{RDY\_VDDCORE}$ threshold, the $t_{delay\_VDDCORE}$ internal temporization is enabled.

5. Once $t_{delay\_VDDCORE}$ elapsed, the HSI oscillator is enabled. Once the HSI oscillator is stable, the system is initialized: option bytes are loaded.
6. Once the option bytes are loaded, the CPU starts to execute the boot ROM: EADLY timer(1) is started.
7. Once EADLY is elapsed, the boot ROM reads, verifies, and executes the boot loader from an external flash memory. For example, the Octo-SPI flash memory as illustrated in Figure 1.
8. The bootloader software must disable the internal SMPS by clearing the SDEN bit in PWR_CR1 register (bypass mode) during execution prior reading, verifying, and executing the application software. The system runs.
9. The main supply is removed, and the VIN voltage drop:
   a. Once the VIN is below 3.3 V, V_{DD} and V_{DD_periph} follow VIN voltage. Then once VIN is below 1.8 V, $V_{DDA18AON}$ and V_{DDA18x} voltages follows VIN voltage.
   b. Once V_{DDIO} or $V_{DDA18AON}$ crosses STM32N6's V_{PDR} and V_{PDR_ANA} falling threshold, the STM32N6 device is internally reset and the PWR_ON signal goes in high impedance and it is forced to 0 by an internal 40K pull-down resistor.
   c. Once the PWR_ON signal is low, the V_{DDCORE}, VDDA18x, and V_{DD_periph} regulators are disabled and their respective internal discharge circuitry are enabled: V_{DDCORE}, V_{DDA18x}, and V_{DD_periph} voltages are forced low.
   d. The system is power off.

1. *The EADLY timer prevents the boot ROM from performing any access to the boot peripheral memory before it is ready at power-up or recovering from Standby mode. Typically, this action is done to wait for a stable supply voltage for the flash memory that is read by boot ROM to get the boot software. EADLY = 5 ms (reset value)*

Note: V_{DDCORE}, V_{DDA18x} voltages must be low before V_{DD} and $V_{DDA18AON}$. See document [1] for details.

Figure 3. Power-up/uncontrolled power-down sequence



3.3 VDDCORE voltage scaling in Run modes

Run nominal mode (default)

In Run nominal mode, the V_{DDCORE} is set to 810 mV. The CPU clock frequency can be set up to 600 MHz and the NPU clock frequency can be set up to 800 MHz. (see “VOS low” in document [1] for details).

Run high-performance mode

In Run high-performance mode, the V_{DDCORE} is increased from 810 mV (nominal value) to 890 mV (high-performance value). The CPU clock frequency can be set up to 800 MHz, and the NPU clock frequency can be set up to 1000 MHz. (see “VOS high” in document [1] for details).

With an external SMPS, the voltage scaling can be performed on-the-fly by the software by setting the PWR_VCORE_DVFS related GPIO for a monolithic discrete SMPS as defined in Figure 1, or by sending a command for a programmable discrete SMPS (eg: via I²C interface).

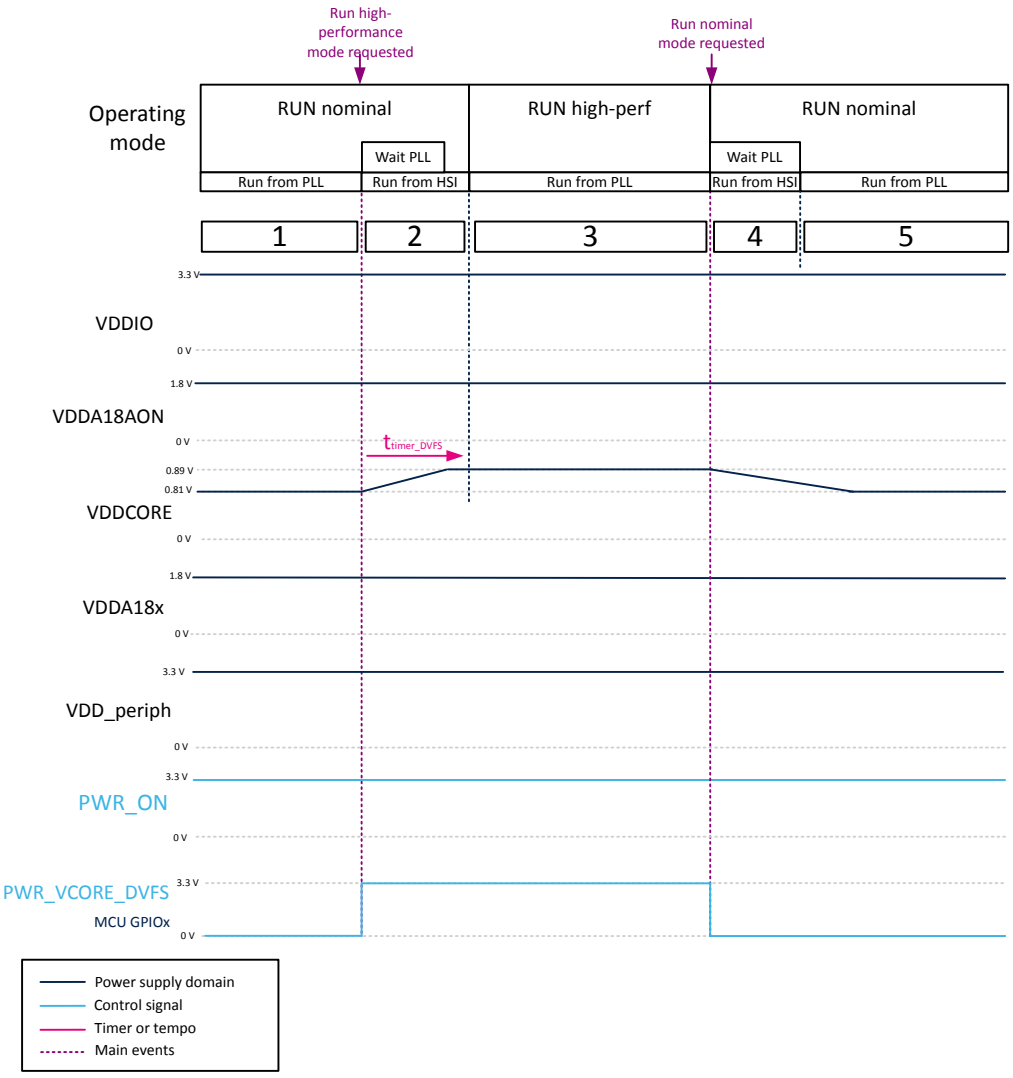
The switch between Run nominal mode to Run high-performance mode is shown in Figure 4 based on the implementation shown in Figure 1:

1. The system is powered up and Run in nominal mode. The system clock is running from PLLs. (for example,: cpu_ck = 600 MHz and npu_ck = 800 MHz)
2. The Run high-performance mode is requested. The software prepares to enter Run high-performance mode:
   a. The CPU clock and NPU clock are set from PLL to the internal oscillator HSI.
   b. The software set high the PWR_VDDCORE_DVFS signal (GPIOx) to switch the V_{DDCORE} SMPS from 810 mV to 890 mV.
   c. The software set a timer t_{timer_dvfs}(1) to wait for V_{DDCORE} to converge to 890 mV.
   d. The software set PLLs for high-performance mode (eg: cpu_ck = 800 MHz and npu_ck = 1000 MHz)
3. Once the timer t_{timer_dvfs} elapsed, and the PLLs are ready, the software set CPU/NPU clocks source back from the HSI oscillator to PLLs. The system runs in high-performance mode.
4. The Run nominal mode is requested. The software prepares to enter Run nominal mode:
   a. The CPU clock and NPU clock are set from PLL to the internal oscillator HSI.
   b. The software set low the PWR_VDDCORE_DVFS signal (GPIOx) to switch the V_{DDCORE} SMPS from 890 mV to 810 mV.
   c. The software set PLLs for nominal mode (eg: cpu_ck = 600 MHz and npu_ck = 800 MHz)
5. Once the PLLs are ready, the software set CPU/NPU clocks source back from the HSI oscillator to PLLs. The system runs in nominal mode.

1. *t_{timer_dvfs}: value is defined according to discrete SMPS regulator slew rate (see Section 5.1: $VRM_{VDDCORE}$ circuitry illustration for DVFS mode)*

Note: If only one peripheral needs to work in high-performance mode, the V_{DDCORE} voltage needs to be set to high-performance mode voltage (890 mV), even if other peripherals keep running in nominal mode.

Figure 4. V_{DDCORE} voltage scaling mechanisms



3.4 Low-power mode management

The STM32N6 supports several low-power modes to reduce power consumption and system clock (see Section 3.1: Operating modes). The modes supported by the system and their advantages/disadvantages are presented in the table below.

Table 5. STM32N6 low-power modes

Operating mode	Advantages	Disadvantages
Sleep	• Very fast recovery duration • All wake-up event available	Only applied to CPU clock gating (little power consumption reduction).
Stop	• Fast recovery duration • Applied to the whole MCU clock gating. (better power consumption than Sleep mode) • All wake-up event available	Same voltage as in Sleep or Run mode (external SMPS does not allow the reduction of voltage in Stop mode).
Standby	Lowest power consumption (all power domains powered off except VDD and VDD1V8_AON).	• Few wake-up events • Longest exit duration

3.4.1 Sleep mode

In Sleep mode, the CPU clock is gated, and the CPU peripheral clocks operates. To reduce power consumption in this mode, it is possible to individually disable or reduce CPU peripherals and memory interface clock (by the PERxLPEN bit field in RCC_xxxxLPENR register, see document [1] for details).

The Sleep mode is close to the Run mode, the high-performance on V_{DDCORE} and the frequency increase is also available. See document [1] for details.

3.4.2 Stop mode

In Stop mode, the CPU clock is stopped and all CPU peripheral clocks are stopped too. Only the CPU peripherals having a PERxLPEN bit operate accordingly. See document [1] for details.

With external SMPS, the Stop mode is equivalent to the Sleep mode as V_{DDCORE} voltage cannot be reduced compared to internal SMPS where V_{DDCORE} voltage can be reduced in Stop mode. See SVOS low and SVOS high in document [1].

3.4.3 Standby mode

This mode is used to achieve the lowest power consumption.

In Standby mode, V_{DDCORE} voltage is powered off in addition to V_{DDA1V8}. PLLs, HSI oscillator, MSI oscillator, and HSE oscillator are also powered off. SRAM and register contents are lost except for backup domain registers (RTC registers, RTC backup register, and backup RAM), and the retention domain. See document [1] for details. Application peripherals are also powered off, except those targetted to wake up the system from Standby mode.

When entering standby mode, the PWR_ON signal is automatically set to 0 by the system to switch off the external SMPS regulator.

Prior entering standby mode, the pwr_on pulse low (POPL timer in PWR_CR1 register) must be set to guaranty a minimum pulse low duration of the PWR_ON signal to prevent the system to wake up prior the V_{DDCORE} voltage goes below $V_{RDY\_VDDCORE}$ falling threshold. This is to ensure that V_{DDCORE} domain is in reset prior allowing to exit from Standby mode.

Figure 5 illustrates mechanisms of Run mode to Standby mode entry and exit based on the implementation shown in Figure 1.

1. The system is powered up and works in Run nominal mode or in Run high-performance mode. The system clock is running from PLLs.
2. The Standby mode is requested:
   a. The software prepares the system to enter in Standby mode (for example, fetching address).
   b. The software set the POPL timer(1) (in PWR_CR1 register). See Section 4.1 for POPL value definition.
   c. Software enter Standby mode (set PDDS in PWR_CPUCR register).
3. The system de-assert the PWR_ON signal and it starts the POPL timer
   a. V_{DDCORE}, V_{DDA18x}, and V_{DD_periph} regulators are disabled.
   b. V_{DDCORE}, V_{DDA18x}, and V_{DD_periph} voltages drop.

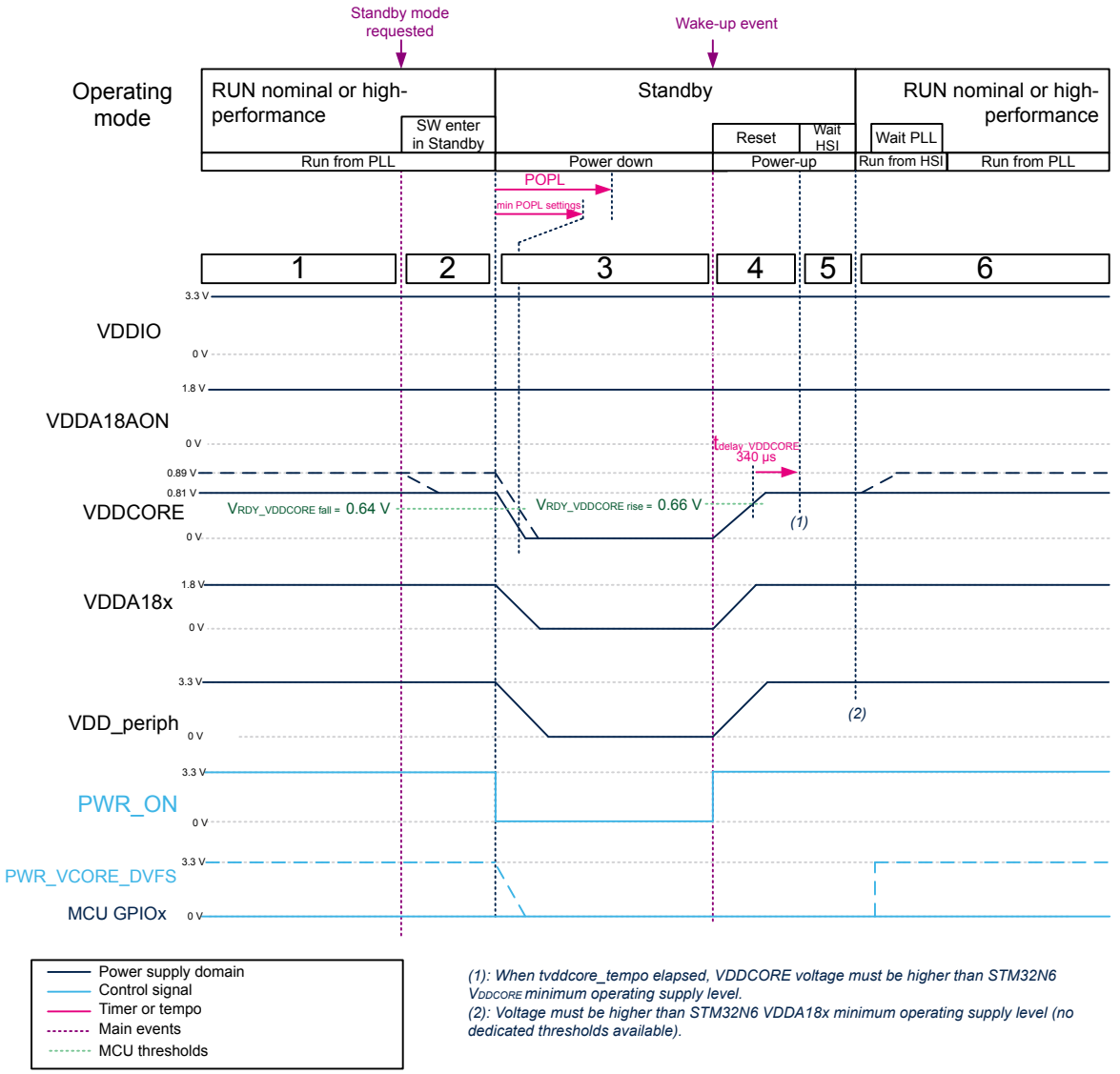
Note: Any wake-up event prior POPL timer elapsed is shifted when the POPL has elapsed.

4. On a wake-up event, the system leaves Standby mode.
   a. The PWR_ON signal is asserted.
   b. V_{DDCORE}, V_{DDA18x}, and V_{DD_periph} regulators are enabled.
   c. V_{DDCORE}, V_{DDA18x}, and V_{DD_periph} voltages rise.
   d. Once V_{DDCORE} voltage reaches the $V_{RDY\_VDDCORE}$ threshold, the $t_{delay\_VDDCORE}$ internal temporization is enabled.
5. Once $t_{delay\_VDDCORE}$ elapsed, the HSI oscillator is enabled.
6. Once the HSI oscillator is stable, the CPU starts and release from Standby mode.

1. *Prior entering standby mode, the pwr_on pulse low (POPL timer in PWR_CR1 register) must be set to guaranty a minimum pulse low duration of the PWR_ON signal to prevent the system to wake up prior the V_{DDCORE} voltage goes below $V_{RDY\_VDDCORE}$ falling threshold. This is to ensure that V_{DDCORE} domain is in reset prior allowing to exit from Standby mode. The POPL duration should be set according to the regulator discharge slew rate when disabled (see Section 4.1: VRM specification for V_{DDCORE} power domain).*

Note: When leaving Standby mode, the program execution is started as after a system reset. Depending on the wake-up source, the program execution can fetch directly to a physical address, such as on TCM for a fast restart (address set in SYSCFG_INITSVTORCR prior Standby entry) or fetch to the boot ROM. See document [1] for details. Figure 5 illustrates the program execution fetches to a physical address on Standby exit (not from boot ROM).

Figure 5. Standby mode mechanism



(1): When tvddcore_tempo elapsed, VDDCORE voltage must be higher than STM32N6 V_{DDCORE} minimum operating supply level.
(2): Voltage must be higher than STM32N6 VDDA18x minimum operating supply level (no dedicated thresholds available).

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4 Voltage regulator module specification

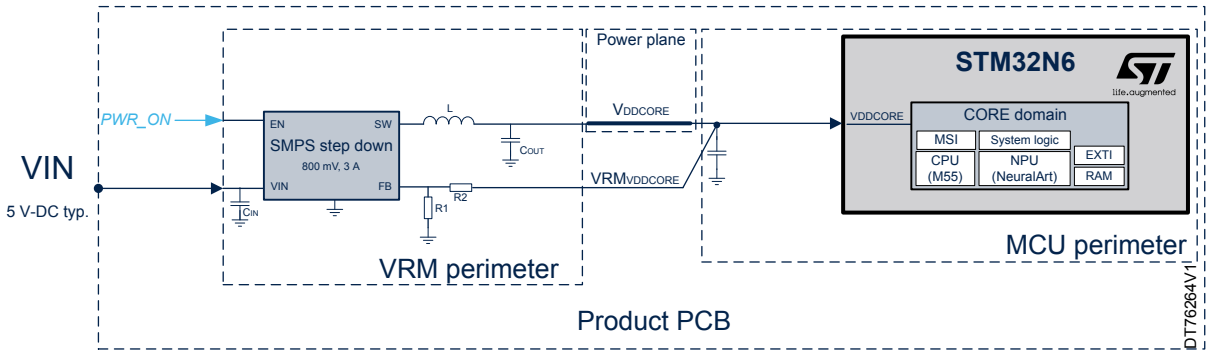
This section provides electrical specifications of voltage regulator modules (VRM) that supply the STM32N6's power domains described in Section 2.3: Power distribution.

A product/application engineer must design the VRM according to these electrical specifications by selecting a regulator IC and the associated discrete components, taking into account all electrical deratings due to product physical environment such as temperature variation, components aging, etc.

This section is only applicable if the STM32N6's decoupling scheme (refer to document [1]) and layout recommendations are carefully followed to minimize the impedance of the power delivery network (PDN).

An illustration of the VRM supplying the Core domain is available in Figure 6. It aims to highlight the perimeter of VRM specifications.

Figure 6. Example of VRM definition



4.1 VRM specification for V_{DDCORE} power domain

As defined in Section 2.3.2: V_{DDCORE} power domain (810 mV/ 890 mV), V_{DDCORE} is the main supply for MCU digital core domain.

Depending on the operating mode wishes, this supply can be set to nominal voltage (810 mV) or to high-performance voltage (890 mV) or switched off in Standby mode. Accordingly, the V_{DDCORE}'s VRM should support two voltages level that can be controlled from the STM32N6 and a discharge circuitry to drop the V_{DDCORE} voltage when VRM is disabled.

Table 6. VRM V_{DDCORE} power domain

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
$VRM_{VDDCORE}$	Output DC voltage in Run nominal mode.	Including line regulation, load regulation and temperature variation	0.790(1)	0.81	0.830(1)	V
$VRM_{VDDCORE-HP}$	Output DC voltage in Run high-performance mode	Including line regulation, load regulation and temperature variation	0.868(1)	0.89	0.912(1)	V
$VRM_{VDDCORE-RIPPLE}$	Output voltage noise/ ripple voltage	IOUT = 1 mA to 2000 mA f = 10 Hz to 5 MHz	-	-	30	mVp-p
VRM_{ICORE}	Rated output current	-	2000	-	-	mA
$VRM_{VDDCORE-TRANS}$	Load transient regulation	I_{OUT} = 5 mA to 700 mA or 700 mA to 5 mA in 1 µs current rise/fall at VRM	-	-	+/-35(2)	mV
$VRM_{VDDCORE-SR-PU}$	Output voltage slew rate at power-up	$VRM_{VDDCORE}$ from $V_{TH\_VDDCORE\ min}$ to $V_{DDCORE\ min}$	0.86(3)	-	-	V/ms

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
$VRM_{VDDCORE-SR-DVFS}$	Output voltage slew rate during Run nominal to Run high-performance mode transition	$VRM_{VDDCORE}$ from PWR_VCORE_DVFS control signal rising (VRM VSEL input) to VRMVDDCORE-OVD min	(4)	-	-	V/ms
$VRM_{VDDCORE\_AD}$	Active output discharge	$VRM_{VDDCORE}$ from the falling edge of the VRM's EN input to $V_{TH\_VDDCORE}$ falling threshold	-	(5)	-	ms

1. *Values differ from STM32N6 datasheet corresponding to a DC and AC IR drop budget through PCB power plans between the VRM output and the STM32N6's V_{DDCORE} BGA supply balls.*
2. *Voltage overshoot/undershoot caused by load transients must not be higher than $VRM_{VDDCORE}$ + $VRM_{VDDCORE-TRANS}$ for a negative current transient and lower than $VRM_{VDDCORE}$ - $VRM_{VDDCORE-TRANS}$ for a positive current transient. Implicitly, output voltage noise/ripple ($VRM_{VDDCORE-RIPPLE}$) is included in the $VRM_{VDDCORE-TRANS}$ value.*
3. *At power-up, once the VRM output crosses the $V_{RDY\_VDDCORE}$ min threshold (0.61 V), the VRM output voltage ($VRM_{VDDCORE}$) must be above VDDCORE min operating condition (0.782 V) in less than $t_{delay\_VDDCORE}$ min (200 µs). Refer to document [2].*
4. *There is no minimum value defined (faster is better). The software should instantiate a timer (duration = t_{timer_DVFS}, see Section 3.3: VDDCORE voltage scaling in Run modes) to wait for Run nominal voltage to Run high-performance voltage transition. The t_{timer_DVFS} duration value depends on how the VRM DVFS is managed: if a programmable VRM (for example: I²C interface) is used, the slew rate value is intrinsic of the VRM IC (defined in the VRM 's product datasheet); if a monolithic VRM is used (as illustrated in Figure 1) then, the slew rate depends on DVFS circuitry as illustrated in Section 5.1: $VRM_{VDDCORE}$ circuitry illustration for DVFS mode.*
5. *As V_{DDCORE} is turned OFF in Standby mode, a regulator having an EN pin is needed to support Standby mode. Additionally, the selection of a regulator with an active output discharge is recommended to allow a fast voltage decrease when the regulator is disabled. Accordingly, the STM32N6's POPL timer must be set with a value higher than $VRM_{VDDCORE-AD}$ duration*

4.2 VRM specification for V_{DD} power domain

As defined in Section 2.3.3: VDD power domain (3.3 V/1.8 V), V_{DD} is the main supply for I/Os voltage interfaces, backup, and retention domains kept powered during Standby mode. Depending on the application V_{DD} is usually 3.3 V or 1.8 V.

This supply is always enabled as long as the VIN voltage is present. Accordingly, a low quiescent current regulator is recommended for Standby mode.

Table 7. VRM VDD power domain

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
VRM_{VDD}	Output DC voltage range	Including line regulation, load regulation and temperature variation	3.1 1.7	3.3 1.8	3.5 1.9	V
VRM_{VDD_N}	Output voltage noise	I_{OUT} = 1 mA to 200 mA F = 10 Hz to 5 MHz	-	-	20	mVp-p
VRM_{IDD}	Rated output current	-	200(1)	-	-	mA
VRM_{VDD_TRANS}	Load transient regulation	I_{OUT} = 1 mA to 200 mA or 200 mA to mA in 1 µs current rise/fall at VRM	-	-	+/-50 mV	mV

1. *The rated output current needs to be adapted if the VRM supplies the V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, V_{DDIO4} in addition to the V_{DD} domain. Refer to Section 2.3.3: VDD power domain (3.3 V/1.8 V).*

4.3 VRM specification for V_{DDA1V8_AON} power domain

As defined in Section 2.3.4: V_{DDA1V8_AON} power domain (1.8 V), V_{DDA1V8_AON} is the main supply for internal oscillators and it is kept powered during Standby mode.

This supply is always enabled as long as the VIN voltage is present. Accordingly, a low quiescent current regulator is recommended for Standby mode.

Table 8. VRMVDDA1V8_AON power domain

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
VRM_{VDD}	Output DC voltage range	Including line regulation, load regulation and temperature variation	1.7	1.8	1.9	V
VRM_{VDD_N}	Output voltage noise	I_{OUT} = 100 µA to 10 mA F = 10 Hz to 5 MHz	-	-	20	mVp-p
VRM_{IDD}	Rated output current	-	10(1)	-	-	mA
VRM_{VDD_TRANS}	Load transient regulation	I_{OUT} = 100 µA to 10 mA or 10 mA to 100 µA in 1 µs current rise/fall at VRM	-	-	+/-50 mV	mV

1. See *Section 2.3.4: V_{DDA1V8_AON} power domain (1.8 V)*

4.4 VRM specification for V_{DDA1V8} (analog) power domain

As defined in Section 2.3.5: V_{DDA1V8} power domain (1.8 V), V_{DDA1V8} is dedicated to supplying all the MCU analog power domain: PLLs ($V_{DDA18PLLx}$), CSI ($V_{DDA18CSI}$), USB ($V_{DDA18USB}$), ADC ($V_{DDA18ADC}$), excluding the internal SMPS ($V_{DDA18PMU}$) as it is not used with external V_{DDCORE} SMPS. Accordingly, a special attention to VRM voltage output noise must be kept in this power domain.

This power domain is switched off during Standby mode, requiring a VRM IC with EN pin control and a discharge circuitry allowing VRM output voltage to drop when the VRM is disabled.

Table 9. VRM V_{DDA1V8} power domain

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
$VRM_{VDDA1V8}$	Output DC voltage range	Including line regulation, load regulation and temperature variation	1.746	1.8	1.9	V
$VRM_{VDDA1V8}$	Output voltage noise	I_{OUT} = 100 µA to 50 mA F = 10 Hz to 5 MHz	-	-	20	mVp-p
$VRM_{IDDA1V8}$	Rated output current	-	50	-	-	mA
VRM_{VDD_TRANS}	Load transient regulation	I_{OUT} = 100 µA to 10 mA or 10 mA to 100 µA in 1 µs current rise/fall at VRM	-	-	+/-30	mV

5 VRM example

5.1 $VRM_{VDDCORE}$ circuitry illustration for DVFS mode

The V_{DDCORE}'s VRM in Figure 1 is a monolithic SMPS with an additional circuitry inserted into a feedback loop. It can control two output voltages (DVFS). This optional circuitry can switch the V_{DDCORE} voltage between 810 mV for Run nominal mode to 890 mV for Run high-performance mode. It is detailed in Figure 7 with design notes to help implementing this circuitry in an application.

Figure 7. VRM VDDCORE DVFS circuitry illustration

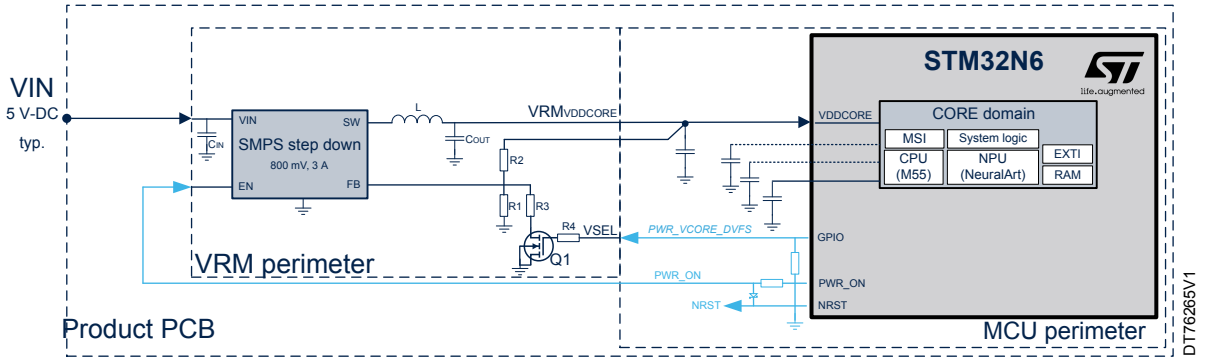


Table 10. VRM VDDCORE truth table

EN	PWR_VCORE_DVFS	VOUT
0	-	0 V (Off)
1	0	810 mV
1	1	890 mV

5.1.1 V_{OUT} (R1, R2, R3, R4) computation example

Assumption: The step down SMPS used in Figure 7 has a feedback voltage equal to V_{FB} = 0.6 V

- When PWR_VCORE_DVFS = 0 (Run nominal mode), the MOFSET Q1 is open and the Q1 drain node is floating. The output voltage $V_{RMVDDCORE}$ is minimum and equal to:
  - $VOUT_{NOM}$ = (R1 + R2) / R1 × VFB = 0.81 V
- When PWR_VCORE_DVFS = 1 (Run high-performance mode), the MOFSET Q1 is closed and Q1 drain node is grounded (Q1 RDSOn value negligible comparing to R3 value). The output voltage $VRM_{VDDCORE}$ is maximum and equal to:
  - $VOUT_{HIGH-PERF}$ = (R1//R3 + R2) / R1//R3 × VFB = 0.89 V

R1 and R2 need to be selected first to reach $VOUT_{NOM}$ = 0.81 V output voltage. In this first step choose R1 or R2 in the range values usually recommended in the SMPS IC datasheet.

In the second step, R3 must be selected to reach $VOUT_{HIGH-PERF}$ = 0.89 V

R4 has a high value to increase the miller plate effect duration to slow the closing duration of the Q1 transistor. Nevertheless, the R4 value must be adapted to reach the $VRM_{VDDCORE-SR-DVFS}$ slew rate constraint.

5.1.2 Electrical parameters for Q1 MOSFET selection

- N-Channel
- I_{DSS} << 2 µA (condition: Vds = 0.8 V, Vgs = 0 V)
- $V_{GS(threshold)}$ < 1.8 V (must be below PWR_VCORE_DVFS I/O voltage, so below the V_{DD} voltage)
- ID min > 2 µA

- VDS > 0.8 V
- Crss recommended below 20 pF(1)

1. *To avoid energy transfers from PWR_VCORE_DVFS signal to Q1 Gate to Drain (through Crss) to feedback node of the SMPS IC during PWR_VCORE_DVFS signal transition. This energy transfer can disturb the feedback node of the SMPS IC making small overshoots and undershoots during PWR_VCORE_DVFS signal transition for a few microseconds.*

Revision history

Table 11. **Document revision history**

Date	Version	Changes
22-Nov-2024	1	Initial release.

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