Migrating between STM32U5 and STM32U3 MCUs

Introduction

The ability to easily replace one microcontroller type with another from the same product family is an important asset for designers of STM32 microcontroller applications.

Migrating an application to a different microcontroller is often needed when product requirements grow. This places extra demands on new features, memory size, or increases the number of I/Os. Cost reduction objectives may also be a reason to switch to smaller components, and shrink the PCB area.

This application note analyzes the steps required to migrate an existing application design from STM32U5 series microcontroller to STM32U3 series microcontroller, or the other way around.

The peripherals, performance, and power consumption are the main aspects to be considered for the migration.

Both STM32U3 and STM32U5 series belong to ultra-low-power family of microcontrollers based on the high-performance Arm® Cortex®- M33 32-bit RISC core, with Cortex® for Arm v8-M. The level of security is very high, as devices of both series embed advanced accelerators for cryptography and advanced features thanks to the Arm® TrustZone®.

While STM32U5 series offer more peripherals and features, better performance and bigger packages, STM32U3 series excel in power consumption thanks to the near-threshold voltage technology. With near-threshold technology, STM32U3 series reduce the active consumption down to 10 uA/MHz, resulting in far longer battery life for any application.

To benefit most from this application note, it is recommended that the reader is familiar with the STM32 microcontroller documentation available on www.st.com.

1 General information

This application note applies to STM32U3 series and STM32U5 series microcontrollers that are Arm® Cortex®-M33 core-based devices.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

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Reference documents

[1] Reference manual *STM32U5 series Arm®-based 32-bit MCUs* (RM0456)

[2] Reference manual *STM32U3 series Arm®-based 32-bit MCUs* (RM0487)

[3] STM32U5 series datasheets and errata sheets

[4] STM32U3 series datasheets and errata sheets

[5] Application note *Getting started with STM32U5 series MCU hardware development* (AN5373)

[6] Application note *Getting started with STM32U3 series MCU hardware development* (AN6011)

[7] Application note *STM32 microcontroller system memory boot mode* (AN2606)

2 Hardware migration guide

The STM32U3 and STM32U5 devices are pin-to-pin compatible and replaceable for the same package sizes.

Three variants of packages are available:

- Legacy with LDO regulator only.
- SMPS with additional power pins for internal SMPS regulator.
- SMPS DSI with additional power pins for internal SMPS regulator and internal DSI transceiver.

Note that legacy SMPS and SMPS DSI packages are not pin-to-pin compatible. For example, a legacy package cannot be replaced by any SMPS package, or an SMPS package cannot be replaced with SMPS DSI package without a change of the application design.

Some functions might not be available on all pins due to unavailability of some peripherals. Refer to Section 3.1 and/or product datasheets for more information.

See Table 1 for an overview of the available packages for both series. If not stated otherwise, checked cells represent the availability of both legacy and SMPS packages.

The WLCSPx packages are not mentioned there, because they are dedicated to individual product lines. Refer to product datasheets for more information.

Table 1. Available packages in STM32U3 and STM32U5

Package (size in mm)	STM32U5				STM32U3
	STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx	STM32U375/385
UFQFPN32 (5 x 5)	-	-	-	-	Legacy only
LQFP48 (7 x 7)	X	X	-	-	X
UFQFPN48 (7 x 7)	X	X	-	-	X
LQFP64 (10 x 10)	X	X	X	-	X
UFBGA64 (5 x 5)	X	-	-	-	X
LQFP100 (14 x 14)	X	X	X	Legacy, SMPS, SMPS DSI	X
UFBGA100 (7 x 7)	X	-	-	-	X
UFBGA132 (7 x 7)	-	X	X	-	-
LQFP144 (20 x 20)	-	X	X	SMPS DSI only	-
UFBGA144 (10 x 10)	-	-	-	SMPS DSI only	-
UFBGA169 (7 x 7)	-	X	-	-	-
TFBGA169 (7 x 7)(1)	-	-	X	-	-
TFBGA216 (13 x 13)	-	-	SMPS DSI only	SMPS DSI only	-

1. *The difference between UFBGA and TFBGA is in package height and ball diameter.*

For more details about available packages, refer to product datasheets and/or documents [5] and [6].

3 Peripheral migration guide

3.1 Peripheral compatibility

Refer to Table 2 for summary of peripheral availability and compatibility on both series.

Table 2. Comparison of peripheral availability and compatibility for STM32U3 and STM32U5

Peripherals		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx	STM32U375/385	Register compatibility
Core		Cortex-M33					-
Maximum core frequency		160 MHz				96 MHz	-
SRAM size (Kbytes)	SRAM1	192		768		192	Partial
	SRAM2	64				64	
	SRAM3	N/A	512	832		N/A	-
	SRAM4	16				N/A	-
	SRAM5	N/A		832	-	N/A	-
	SRAM6	N/A			512	N/A	-
	BKPSRAM	2				N/A	-
Flash memory	Size (bytes)	128K-512K	1M-2M	2M-4M	4M	512K-1M	Partial
	Type	Dual bank					
Cache size (Kbytes)	ICACHE	8		32		8	Yes
	DCACHE1	4		16		N/A	-
	DCACHE2	N/A		16		N/A	-
GTZC	Number of instances	2				1	No
	MPCWM resources	2	5	6		N/A	
	MPCBB resources	3	4	5	6	2	
PWR	LDO + SMPS	Yes				Yes	No
	DSI power pins	N/A		Yes		N/A	-
	LPBAM	Yes				N/A	-
RCC	Clocks	HSI16, HSI48, HSE, MSI (16 ranges), LSI, LSE, SHSI				HSI16 HSI48 HSE MSI (8 ranges) LSI LSE	No
	PLL	Yes				N/A	
GPIO	GPIO	Yes				Yes	Yes
	LPGPIO	Yes				N/A	-

Peripherals		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx	STM32U375/385	Register compatibility
SYSCFG		Yes				Yes	Mostly yes
DMA	GPDMA	Yes (16 channels)				Yes (11 channels)	Mostly yes
	LPDMA	Yes (4 channels)				N/A	-
	DMA2D	N/A	Yes			N/A	-
GFXMMU		N/A			Yes	N/A	-
NVIC		Yes				Yes	Mostly yes
EXTI		Yes				Yes	Mostly yes
CRC		Yes				Yes	Mostly yes
CORDIC		Yes				N/A	-
FMAC		Yes				N/A	-
FSMC		N/A	Yes			N/A	-
OCTOSPI		1	2			1	Mostly yes
OCTOSPIM		N/A	Yes			N/A	-
HSPI		N/A		1		N/A	-
SDMMC		1	2			1	Yes
Analog	ADC 12-bit	1				2	No
	ADC 14-bit	1		2		0	
	DAC 12-bit	2				2	Yes
	VREFBUF	Yes				Yes	Yes
	COMP	1	2			2	Yes
	OPAMP	1	2			2	Yes
Digital filters	MDF	Yes				N/A	-
	ADF	Yes				Yes	Mostly yes
DCMI		Yes				N/A	-
PSSI		Yes				N/A	-
LTDC		N/A		Yes		N/A	-
DSI		N/A		Yes		N/A	-
GPU2D		N/A		Yes		N/A	-
JPEG		N/A			Yes	N/A	-
TSC (number of channels)		Up to 20	Up to 22		Up to 24	Up to 21	Mostly yes
Cryptography	CCB	N/A				Yes	-
	RNG	Yes				Yes	Partial
	AES	Yes				Yes	Yes
	SAES	Yes				Yes	Mostly yes
	HASH	Yes				Yes	Mostly yes
	OTFDEC	Yes				N/A	-
	PKA	Yes				Yes	Mostly yes
Timers	Advanced	2 (16-bit)				1 (16-bit)	Mostly yes
	General purpose	4 (32-bit) + 3 (16-bit)				3 (32-bit) +3 (16-bit)	Mostly yes

Peripherals		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx	STM32U375/385	Register compatibility
Timers	Basic	2 (16-bit)				2 (16-bit)	Mostly yes
	Low-power	4 (16-bit)				4 (16-bit)	Yes
	Graphic	N/A			Yes	N/A	-
	SysTick	2				2	Yes
	Watchdog	IWDG + WWDG					Yes
RTC		Yes				Yes	Mostly yes
TAMP (number of tampers)		Up to 7 (active)			Up to 6 (active)	Up to 5 (passive)	Partial
Communication interfaces	I2C	4		6		3	Yes
	I3C	N/A				2	-
	USART	2	3	4		2	Yes
	UART	2				2	Yes
	LPUART	1				1	Mostly yes
	SPI	3				3	Yes
	SAI	1	2			1	Yes
	FDCAN	1				1	Yes
	USB	USB FS host/device	USB OTG FS	USB OTG HS		USB FS host/device	With STM32U535/545
UCPD		N/A	Yes			N/A	-

In the following chapters, the system architecture and memory mapping of both series are compared. Then, for individual peripherals that are embedded in devices of both STM32U3 and STM32U5 devices but are not the same, the differences are listed and/or explained.

For complete information about other peripherals (that is peripherals available either on STM32U3, or STM32U5 devices), see document [1], [2], [3], and [4].

3.2 System architecture

The system architectures of both series, STM32U3 and STM32U5, are very similar and differ mainly in the number of peripherals and memories available.

STM32U5 devices have (among other features) DCACHE on S-bus, OTFDEC protection for external OCTOSPI memories, SmartRun domain, or direct connection of flash memory and ICACHE for faster code execution.

For more details, see Figure 1 and Figure 2.

Figure 1. System architecture of STM32U3

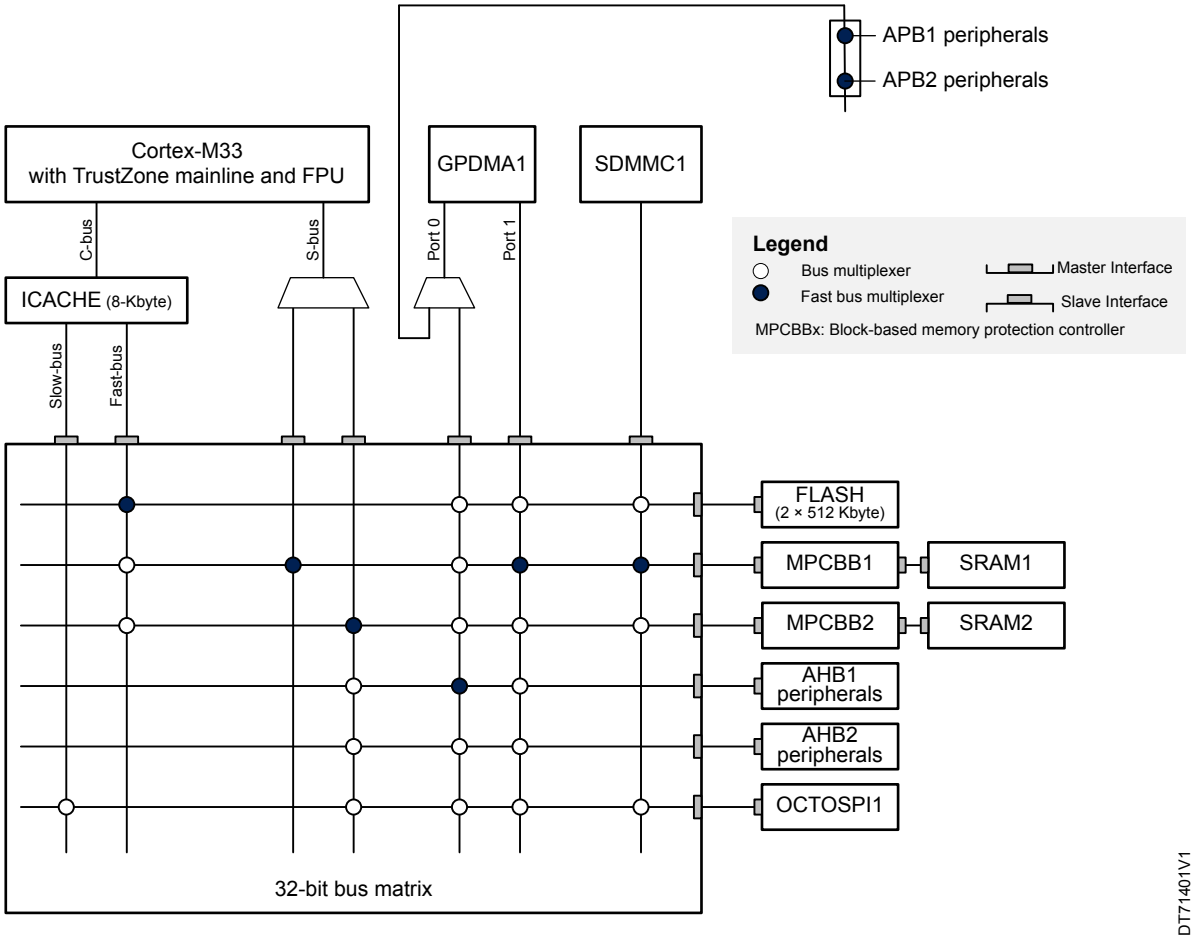
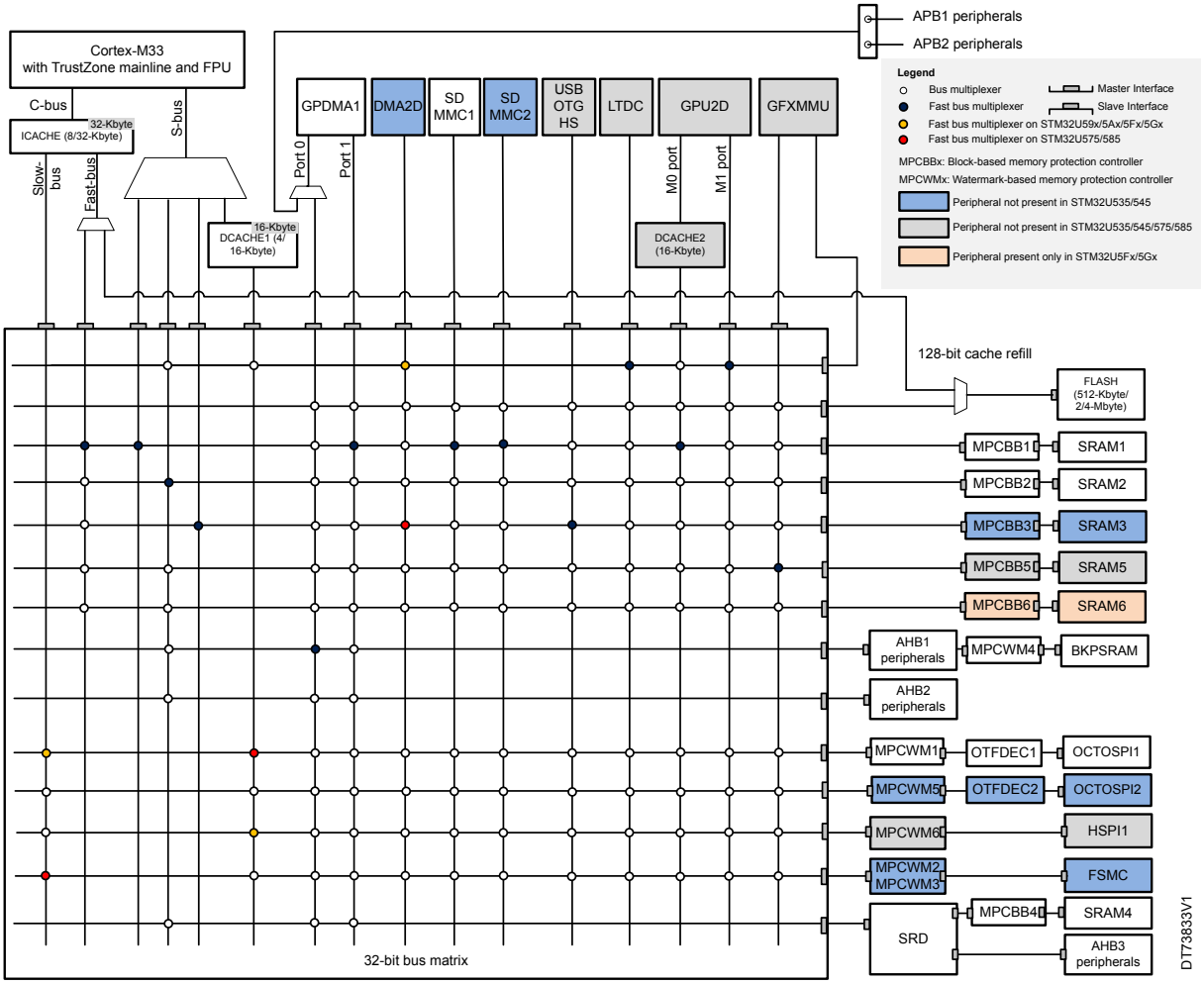


Figure 2. **System architecture of STM32U5**



3.3 Peripheral memory mapping

The main differences in memory mapping between STM32U3 and STM32U5 devices are caused by different sets of embedded peripherals, and additional SmartRun domain on STM32U5 devices (AHB3 and APB3 buses).

In Table 3 summarizes the memory mapping for all peripherals. Peripherals common for both series with different memory mappings are highlighted in bold.

Secure boundary addresses are not compared as the only difference from nonsecure addresses is their base address (`0x4000 0000` for nonsecure and `0x5000 0000` for secure).

Table 3. **Peripheral memory mapping**

Peripheral	STM32U5		STM32U3	
	Bus	Nonsecure boundary address	Bus	Nonsecure boundary address
LPDMA1	AHB3	0x4602 5000 - 0x4602 5FFF	N/A	N/A
ADF1	**AHB3**	**0x4602 4000 - 0x4602 4FFF**	**AHB1**	**0x4003 4000 - 0x4003 4FFF**
GTZC2	AHB3	0x4602 3000 - 0x4602 3BFF	N/A	N/A
EXTI	**AHB3**	**0x4602 2000 - 0x4602 23FF**	**AHB1**	**0x4003 2000 - 0x4003 23FF**
DAC1	**AHB3**	**0x4602 1800 - 0x4602 1BFF**	**AHB2**	**0x4202 8400 - 0x4202 87FF**
ADC4	AHB3	0x4602 1000 - 0x4602 13FF	N/A	N/A
RCC	**AHB3**	**0x4602 0C00 - 0x4602 0FFF**	**AHB1**	**0x4003 0C00 - 0x4003 0FFF**

Peripheral	STM32U5		STM32U3	
	Bus	Nonsecure boundary address	Bus	Nonsecure boundary address
PWR	**AHB3**	**0x4602 0800 - 0x4602 0BFF**	**AHB1**	**0x4003 0800 - 0x4003 0BFF**
LPGPIO	AHB3	0x4602 0000 - 0x4602 03FF	N/A	N/A
TAMP	**APB3**	**0x4600 7C00 - 0x4600 7FFF**	**APB1**	**0x4000 7C00 - 0x4000 7FFF**
RTC	**APB3**	**0x4600 7800 - 0x4600 7BFF**	**APB1**	**0x4000 7800 - 0x4000 7BFF**
VREFBUF	**APB3**	**0x4600 7400 - 0x4600 77FF**	**APB1**	**0x4000 7400 - 0x4000 77FF**
COMP	**APB3**	**0x4600 5400 - 0x4600 57FF**	**APB3**	**0x4004 5400 - 0x4004 57FF**
OPAMP	**APB3**	**0x4600 5000 - 0x4600 53FF**	**APB1**	**0x4000 7000 - 0x4000 73FF**
LPTIM4	**APB3**	**0x4600 4C00 - 0x4600 4FFF**	**APB3**	**0x4004 4C00 - 0x4004 4FFF**
LPTIM3	**APB3**	**0x4600 4800 - 0x4600 4BFF**	**APB3**	**0x4004 4800 - 0x4004 4BFF**
LPTIM1	**APB3**	**0x4600 4400 - 0x4600 47FF**	**APB3**	**0x4004 4400 - 0x4004 47FF**
I2C3	**APB3**	**0x4600 2800 - 0x4600 2BFF**	**APB3**	**0x4004 2800 - 0x4004 2BFF**
LPUART1	**APB3**	**0x4600 2400 - 0x4600 27FF**	**APB3**	**0x4004 2400 - 0x4004 27FF**
SPI3	**APB3**	**0x4600 2000 - 0x4600 23FF**	**APB1**	**0x4000 2000 - 0x4000 23FF**
SYSCFG	**APB3**	**0x4600 0400 - 0x4600 07FF**	**APB3**	**0x4004 0400 - 0x4004 07FF**
HSPI1	AHB2	0x420D 3400 - 0x420D 37FF	N/A	N/A
OCTOSPI2	AHB2	0x420D 2400 - 0x420D 27FF	N/A	N/A
OCTOSPI1	AHB2	0x420D 1400 - 0x420D 17FF	AHB2	0x420D 1400 - 0x420D 17FF
FSMC	AHB2	0x420D 0400 - 0x420D 07FF	N/A	N/A
DLYBOS2	AHB2	0x420C F400 - 0x420C F7FF	N/A	N/A
DLYBOS1	AHB2	0x420C F000 - 0x420C F3FF	AHB2	0x420C F000 - 0x420C F3FF
SDMMC2	AHB2	0x420C 8C00 - 0x420C 8FFF	N/A	N/A
DLYBSD2	AHB2	0x420C 8800 - 0x420C 8BFF	N/A	N/A
DLYBSD1	AHB2	0x420C 8400 - 0x420C 87FF	AHB2	0x420C 8400 - 0x420C 87FF
SDMMC1	AHB2	0x420C 8000 - 0x420C 83FF	AHB2	0x420C 8000 - 0x420C 83FF
CCB	N/A	N/A	AHB2	0x420C 7C00 - 0x420C 7FFF
OTFDEC2	AHB2	0x420C 5400 - 0x420C 57FF	N/A	N/A
OTFDEC1	AHB2	0x420C 5000 - 0x420C 53FF	N/A	N/A
OCTOSPIM	AHB2	0x420C 4000 - 0x420C 43FF	N/A	N/A
PKA +RAM	AHB2	0x420C 2000 - 0x420C 3FFF	AHB2	0x420C 2000 - 0x420C 3FFF
SAES	AHB2	0x420C 0C00 - 0x420C 0FFF	AHB2	0x420C 0C00 - 0x420C 0FFF
RNG	AHB2	0x420C 0800 - 0x420C 0BFF	AHB2	0x420C 0800 - 0x420C 0BFF
HASH	AHB2	0x420C 0400 - 0x420C 07FF	AHB2	0x420C 0400 - 0x420C 07FF
AES	AHB2	0x420C 0000 - 0x420C 03FF	AHB2	0x420C 0000 - 0x420C 03FF
OTG_HS	AHB2	0x4204 0000 - 0x4205 FFFF	N/A	N/A
OTG_FS	AHB2	0x4204 0000 - 0x420B FFFF	N/A	N/A
PSSI	AHB2	0x4202 C400 - 0x4202 C7FF	N/A	N/A
DCMI	AHB2	0x4202 C000 - 0x4202 C3FF	N/A	N/A
ADC1_2	AHB2	0x4202 8000 - 0x4202 83FF	AHB2	0x4202 8000 - 0x4202 83FF
GPIOJ	AHB2	0x4202 2400 - 0x4202 27FF	N/A	N/A
GPIOI	AHB2	0x4202 2000 - 0x4202 23FF	N/A	N/A

Peripheral	STM32U5		STM32U3	
	Bus	Nonsecure boundary address	Bus	Nonsecure boundary address
GPIOH	AHB2	0x4202 1C00 - 0x4202 1FFF	AHB2	0x4202 1C00 - 0x4202 1FFF
GPIOG	AHB2	0x4202 1800 - 0x4202 1BFF	AHB2	0x4202 1800 - 0x4202 1BFF
GPIOF	AHB2	0x4202 1400 - 0x4202 17FF	N/A	N/A
GPIOE	AHB2	0x4202 1000 - 0x4202 13FF	AHB2	0x4202 1000 - 0x4202 13FF
GPIOD	AHB2	0x4202 0C00 - 0x4202 0FFF	AHB2	0x4202 0C00 - 0x4202 0FFF
GPIOC	AHB2	0x4202 0800 - 0x4202 0BFF	AHB2	0x4202 0800 - 0x4202 0BFF
GPIOB	AHB2	0x4202 0400 - 0x4202 07FF	AHB2	0x4202 0400 - 0x4202 07FF
GPIOA	AHB2	0x4202 0000 - 0x4202 03FF	AHB2	0x4202 0000 - 0x4202 03FF
BKPSRAM	AHB1	0x4003 6400 - 0x4003 6BFF	N/A	N/A
GTZC1	**AHB1**	**0x4003 2400 - 0x4003 3FFF**	**AHB1**	**0x4003 2400 - 0x4003 33FF**
GCACHE	AHB1	0x4003 1800 - 0x4003 1BFF	N/A	N/A
DCACHE	AHB1	0x4003 1400 - 0x4003 17FF	N/A	N/A
ICACHE	AHB1	0x4003 0400 - 0x4003 07FF	AHB1	0x4003 0400 - 0x4003 07FF
GPU2D	AHB1	0x4002 F000 - 0x4002 FFFF	N/A	N/A
GFXMMU	AHB1	0x4002 C000 - 0x4002 EFFF	N/A	N/A
DMA2D	AHB1	0x4002 B000 - 0x4002 BBFF	N/A	N/A
JPEG	AHB1	0x4002 A000 - 0x4002 AFFF	N/A	N/A
RAMCFG	AHB1	0x4002 6000 - 0x4002 6FFF	AHB1	0x4002 6000 - 0x4002 6FFF
MDF1	AHB1	0x4002 5000 - 0x4002 5FFF	N/A	N/A
TSC	AHB1	0x4002 4000 - 0x4002 43FF	AHB1	0x4002 4000 - 0x4002 43FF
CRC	AHB1	0x4002 3000 - 0x4002 33FF	AHB1	0x4002 3000 - 0x4002 33FF
FLASH	AHB1	0x4002 2000 - 0x4002 23FF	AHB1	0x4002 2000 - 0x4002 23FF
FMAC	AHB1	0x4002 1400 - 0x4002 17FF	N/A	N/A
CORDIC	AHB1	0X4002 1000 - 0x4002 13FF	N/A	N/A
GPDMA1	AHB1	0x4002 0000 - 0x4002 0FFF	AHB1	0x4002 0000 - 0x4002 0FFF
DSIHOST	APB2	0x4001 6C00 - 0x4001 7BFF	N/A	N/A
LCD-TFT	APB2	0x4001 6800 - 0x4001 6BFF	N/A	N/A
I3C2	N/A	N/A	APB2	0x4001 6C00 - 0x4001 6FFF
GFXTIM	APB2	0x4001 6400 - 0x4001 67FF	N/A	N/A
USB RAM	APB2	0x4001 6400 - 0x4001 6BFF	APB2	0x4001 6400 - 0x4001 6BFF
USB	APB2	0x4001 6000 - 0x4001 63FF	APB2	0x4001 6000 - 0x4001 63FF
SAI2	APB2	0x4001 5800 - 0x4001 5BFF	N/A	N/A
SAI1	APB2	0x4001 5400 - 0x4001 57FF	APB2	0x4001 5400 - 0x4001 57FF
TIM17	APB2	0x4001 4800 - 0x4001 4BFF	APB2	0x4001 4800 - 0x4001 4BFF
TIM16	APB2	0x4001 4400 - 0x4001 47FF	APB2	0x4001 4400 - 0x4001 47FF
TIM15	APB2	0x4001 4000 - 0x4001 43FF	APB2	0x4001 4000 - 0x4001 43FF
USART1	APB2	0x4001 3800 - 0x4001 3BFF	APB2	0x4001 3800 - 0x4001 3BFF
TIM8	APB2	0x4001 3400 - 0x4001 37FF	N/A	N/A
SPI1	APB2	0x4001 3000 - 0x4001 33FF	APB2	0x4001 3000 - 0x4001 33FF
TIM1	APB2	0x4001 2C00 - 0x4001 2FFF	APB2	0x4001 2C00 - 0x4001 2FFF

Peripheral	STM32U5		STM32U3	
	Bus	Nonsecure boundary address	Bus	Nonsecure boundary address
UCPD1	APB1	0x4000 DC00 - 0x4000 DFFF	N/A	N/A
FDCAN1 SRAM	APB1	0x4000 AC00 - 0x4000 AFFF	APB1	0x4000 AC00 - 0x4000 AFFF
FDCAN1	APB1	0x4000 A400 - 0x4000 A7FF	APB1	0x4000 A400 - 0x4000 A7FF
I2C6	APB1	0x4000 9C00 - 0x4000 9FFF	N/A	N/A
I2C5	APB1	0x4000 9800 - 0x4000 9BFF	N/A	N/A
LPTIM2	APB1	0x4000 9400 - 0x4000 97FF	N/A	N/A
DTS	APB1	0x4000 8C00 - 0x4000 8FFF	N/A	N/A
I2C4	APB1	0x4000 8400 - 0x4000 87FF	N/A	N/A
USART6	APB1	0x4000 6400 - 0x4000 67FF	N/A	N/A
CRS	APB1	0x4000 6000 - 0x4000 63FF	APB1	0x4000 6000 - 0x4000 63FF
I3C1	N/A	N/A	APB1	0x4000 5C00 - 0x4000 5FFF
I2C2	APB1	0x4000 5800 - 0x4000 5BFF	APB1	0x4000 5800 - 0x4000 5BFF
I2C1	APB1	0x4000 5400 - 0x4000 57FF	APB1	0x4000 5400 - 0x4000 57FF
UART5	APB1	0x4000 5000 - 0x4000 53FF	APB1	0x4000 5000 - 0x4000 53FF
UART4	APB1	0x4000 4C00 - 0x4000 4FFF	APB1	0x4000 4C00 - 0x4000 4FFF
USART3	APB1	0x4000 4800 - 0x4000 4BFF	APB1	0x4000 4800 - 0x4000 4BFF
USART2	APB1	0x4000 4400 - 0x4000 47FF	N/A	N/A
SPI2	APB1	0x4000 3800 - 0x4000 3BFF	APB1	0x4000 3800 - 0x4000 3BFF
IWDG	APB1	0x4000 3000 - 0x4000 33FF	APB1	0x4000 3000 - 0x4000 33FF
WWDG	APB1	0x4000 2C00 - 0x4000 2FFF	APB1	0x4000 2C00 - 0x4000 2FFF
TIM7	APB1	0x4000 1400 - 0x4000 17FF	APB1	0x4000 1400 - 0x4000 17FF
TIM6	APB1	0x4000 1000 - 0x4000 13FF	APB1	0x4000 1000 - 0x4000 13FF
TIM5	APB1	0x4000 0C00 - 0x4000 0FFF	N/A	N/A
TIM4	APB1	0x4000 0800 - 0x4000 0BFF	APB1	0x4000 0800 - 0x4000 0BFF
TIM3	APB1	0x4000 0400 - 0x4000 07FF	APB1	0x4000 0400 - 0x4000 07FF
TIM2	APB1	0x4000 0000 - 0x4000 03FF	APB1	0x4000 0000 - 0x4000 03FF

3.4 Boot mode compatibility

The principle of selecting boot mode is the same for both series – it depends on option bytes and BOOT0 pin. The only difference is in the names of FLASH option byte registers for storing the boot address. Refer to Table 4 and/or Table 8. The location of the option bytes remains the same.

For both series, boot selection is different when TrustZone is enabled and disabled.

Table 4. Different naming of boot address option byte registers

STM32U5	STM32U3
NSBOOTADD0R	FLASH_BOOT0R
NSBOOTADD1R	FLASH_BOOT1R
SECBOOTADD0R	FLASH_SBOOT0R

See also Table 5 for overview of peripherals and pins used by the system bootloader to reprogram the flash memory on both series. The difference is mainly in available peripherals and pins used by SPI2 and SPI3 which are highlighted.

Table 5. Comparison of peripherals and pins used by bootloader

Peripheral	STM32U5	STM32U3
USART1	PA9/PA10	PA9/PA10
USART2	PA2/PA3	N/A
USART3	PC10/PC11	PC10/PC11
I2C1	PB6/PB7	PB6/PB7
I2C2	PB10/PB11	PB10/PB11
I2C3	PC0/PC1	PC0/PC1
I3C1	N/A	PA1/PB13
I3C2	N/A	N/A
SPI1	PA4/PA5/PA6/PA7	PA4/PA5/PA6/PA7 Note: For WLCSP68-G, PG3/PG4/PG5/PG2 are selected instead of PA4/PA5/PA6/PA7.
SPI2	**PB12/PB13/PB14/PB15**	**PD0/PD1/PD3/PD4**
SPI3	**PB5/PG9/PG10/PG12**	**PA15/PB3/PB4/PB5**
FDCAN	PB8/PB9	PB8/PB9
USB/OTG	PA11/PA12	PA11/PA12

3.5 Global TrustZone® controller (GTZC)

The main difference is the number of instances for each serie: while STM32U3 devices embed one GTZC peripheral, STM32U5 devices embed two GTZC peripherals. The STM32U5 devices offers also watermark memory peripheral controller (MPCWM), protecting external memories, and backup SRAM. Concerning the MPCBB part, the number of its instances and blocks differ from device to device, as these depend on the counts and sizes of internal SRAMs.

Due to the differences mentioned above and different sets of peripherals and memories for each series, the content and size of registers differ significantly. Refer to document [1] and [2] to see GTZC configuration for individual devices.

3.6 SRAMs and RAM configuration controller (RAMCFG)

STM32U5 devices offer more SRAMs and more volatile memory size than STM32U3 devices. For comparison of available SRAMs and its sizes, refer to the Section 3.1.

See Table 6 to find an overview of features of individual SRAMs for both series. Note that due to the continuous memory mapping, the boundary addresses of SRAMs in memory mapping differ. Refer to [1] and [2] for more details.

The most significant difference is the error detection and correction mechanism. While STM32U5 devices use ECC for error detection and single error correction, STM32U3 devices only use hardware parity check for error detection. Also, the wait states of STM32U5 must be correctly set, while STM32U3 does not need any wait states for read/write operations.

Table 6. Comparison of features for individual SRAMs

Feature	STM32U5							STM32U3	
	SRAM1	SRAM2	SRAM3	SRAM4	SRAM5	SRAM6	BKP SRAM	SRAM1	SRAM2
DMA accessibility in Stop 0/1 modes	X	X	X	X	X	X	X	X	X
DMA accessibility in Stop 2 mode	-	-	-	X	-	-	-	X	X
Optional retention in Standby mode	-	X	-	-	-	-	X	-	X
Optional retention in VBAT mode	-	-	-	-	-	-	X	-	-
Erased with RDP regression	X	X	X	X	X	X	X	X	X
Erased or blocked by tamper detection	-	X	-	-	-	-	X	-	X
Optionally erased with system reset	X	X	X	X	X	X	-	X	X
Software erase	X	X	X	X	X	X	X	X	X
ECC	-	X	X	-	-	-	X	-	-
Hardware parity check	-	-	-	-	-	-	-	-	X
Write protection	-	X	-	-	-	-	-	-	X
Wait states	X	X	X	X	X	X	X	-	-

The registers of both series are similar and differ in setting of ECC or hardware parity check, and wait states. For more details, refer to the corresponding chapters in document [1] and [2].

3.7 Embedded flash memory (FLASH)

The sizes of embedded flash memory may differ throughout the devices. For comparison of individual lines of both series, see Section 3.1 and/or corresponding datasheets.

The embedded flash memories of both series are different also in the memory organization and set of features that they support. Refer to Table 7 to see an overview of features for each serie.

Table 7. Overview of flash memory features for STM32U3 and STM32U5 devices

Feature	STM32U5	STM32U3
Memory organization	• Dual bank architecture • Up to 2 Mbytes per bank for main memory • 64.5 Kbytes information block in bank 1	• Dual bank architecture • Up to 512 Kbytes per bank for main memory • 104.5 Kbytes information block
Page size	8 Kbytes	4 Kbytes
Endurance	100 kcycles for up to 256 Kbytes per bank, 10 kcycles for the reset	10 kcycles
Programming and read granularity	128 effective bits + 9 ECC bits	64 effective bits + 8 ECC bits
OTP	512 bytes	
Wait states	• Up to 4 WS with LPM = 0 • Up to 15 WS with LPM = 1	• Up to 2 WS with LPM = 0 • Up to 4 WS with LPM = 1
Read/write protection	• RDP protection (4 levels)	• RDP protection (4 levels)

Feature	STM32U5	STM32U3
	• Write protection (2 areas per bank, 8-Kbyte granularity)	• Write protection (2 areas per bank, 4-Kbyte granularity)
TrustZone support	• Watermark-based secure flash memory area protection • Secure hide protection areas (HDP) • Block-based secure area protection	• Watermark-based secure flash memory area protection • Secure hide protection areas (HDP) • Secure hide protection extension areas (HDP extension) • Block-based secure area protection

Other changes concern the registers of the flash memory peripheral. Even though the functionality is very similar for both series, several registers on STM32U3 were renamed, shrunk/extended or moved. Some registers were even added, for new features like HDP extension, or larger OEM keys. See Table 8 with an overview of changes between the series.

Table 8. Comparison of flash memory registers and option bytes for STM32U5 and STM32U3

Register		Difference
STM32U5	STM32U3	
FLASH_NSKEYR	FLASH_KEYR	Register (NSKEYR <-> KEYR) and field (NSKEY <-> KEY) name change.
FLASH_SECKEYR	FLASH_SKEYR	Register (SECKEYR <-> SKEYR) and field (SECKEY <-> KEY) name change.
FLASH_OPTKEYR	FLASH_OPTKEYR	Field (OPTKEY <-> KEY) name change.
FLASH_NSSR	FLASH_SR	Register (NSSR <-> SR) name change.
FLASH_SECSR	FLASH_SSR	Register (SECSR <-> SSR) name change.
FLASH_NSCR	FLASH_CR	Register (NSCR <-> CR) name change. Size of PNB field differs - 8 bits on STM32U5 compared to 7 bits on STM32U3 (fewer pages).
FLASH_SECCR	FLASH_SCR	Register (SECCR <-> SCR) name change. Size of PNB field differs - 8 bits on STM32U5 compared to. 7 bits on STM32U3 (fewer pages).
FLASH_ECCR	FLASH_ECCCORR	Split of the ECCR register on STM32U5 to two registers on STM32U3: ECCCORR for single error correction and ECCDETR for double error detection. Fields are split accordingly, SYSF_ECC and BK_ECC are present in both. Size of ADDR_ECC differs - 21 bits on STM32U5 compared to 19 bits on STM32U3.
	FLASH_ECCDETR	
FLASH_OPSR	FLASH_OPSR	Register address offset change (0x34 for STM32U5 compared to 0x38 for STM32U3). The size of ADDR_OP differs - 21 bits on STM32U5 compared to 19 bits on STM32U3.
FLASH_OPTR	FLASH_OPTR	Option bit PA15_PUPEN (bit 28) not present on STM32U3. SRAM2_ECC (bit 24) on STM32U5 corresponds to SRAM2_PE (bit 24) on STM32U3 (ECC compared to hardware parity). SRAM3_ECC and BKPRAM_ECC (bits 22 and 23) not present on STM32U3. SRAM_RST (bit 15) on STM32U5 corresponds to SRAM1_RST on STM32U3 and influences only SRAM1 erase. BDRST_STOP (backup domain reset on power-on reset, bit 11) not present on STM32U5.
FLASH_NSBOOTADD0R	FLASH_BOOT0R	Register (NSBOOTADD0R <-> BOOT0R) and field (NSBOOTADD0 <-> ADD) name change.
FLASH_NSBOOTADD1R	FLASH_BOOT1R	Register (NSBOOTADD1R <-> BOOT1R) and field (NSBOOTADD1 <-> ADD) name change.
FLASH_SECBOOTADD0R	FLASH_SBOOT0R	Register (SECBOOTADD0R <-> SBOOT0R) and field (SECBOOTADD0 <-> ADD) name change.
FLASH_SECWMxR1	FLASH_SECWMxR1	Field (SECWM1_PEND <-> SECWM1_END, SECWM1_PSTRT <-> SECWM1_STRT) name change. The size of both fields differs - 8 bits on STM32U5 compared to 7 bits on STM32U3.

Register		Difference
STM32U5	STM32U3	
FLASH_SECWMxR2	FLASH_SECWMxR2	Field (HDP1_PEND <-> HPD1_END) name change. HDP disable done with 1 bit on STM32U5 compared to 8 bits on STM32U3 (keyword needed). Size of HDP1_(P)END differs - 8 bits on STM32U5 compared to 7 bits on STM32U3.
FLASH_WRPxyR	FLASH_WRPxyR	Field (WRPxyR_PSTRT <-> STRT, WRPxyR_PEND <-> END) name change.
FLASH_SECBByRRx	FLASH_SECBByRRx	Different count of registers - x = (1 to 8) on STM32U5 compared to x = (1 to 4) on STM32U3
FLASH_SECHDPCR	FLASH_SECHDPCR	HDP access disable fields - only 1 bit for each HDP area on STM32U5 compared to 8-bit keyword for each HDP and HDP extension area on STM32U3.
FLASH_PRIVCFGR	FLASH_PRIVCFGR	Field (NSPRIV <-> PRIV) name change.
N/A	FLASH_SECHDPEXTR	New register for STM32U3 for enable of HDP extension areas.
FLASH_PRIVBByRx	FLASH_PRIVBByRx	Different count of registers - x = (1 to 8) on STM32U5 compared to x = (1 to 4) on STM32U3.
FLASH_OEM1KEYRx	FLASH_OEM1KEYRx	Different count of registers, or size of the OEM1 key respectively - 64 bits on STM32U5 compared to 128 bits on STM32U3. Register address offset change (0x70 on STM32U5 compared to 0x110 on STM32U3).
FLASH_OEM2KEYRx	FLASH_OEM2KEYRx	Different count of registers, or size of the key respectively - 64 bits on STM32U5 compared to 128 bits on STM32U3. Register address offset change (0x78 on STM32U5 compared to 0x120 on STM32U3).
N/A	FLASH_OEMKEYSR	New register for STM32U3 with OEM1 and OEM2 keys CRC.

For more details, refer to document [1] and [2].

3.8 Power controller (PWR)

Even though both STM32U3 and STM32U5 devices fall into the ultra-low-power family of MCUs and share similar bases, there are many differences between them from the user point-of-view.

Starting with hardware, both series contain LDO regulators and offer packages with embedded SMPS requiring some external circuitry. These requirements are for both the same. Concerning the power pins, some STM32U5 devices require additional DSI supply and offer $V_{DD11USB}$ and/or $V_{DD11DSI}$ domains.

The PWR of STM32U5 devices offer up to 24 pins for up to eight WKUP events, whereas STM32U3 devices have 23 pins (compatible with STM32U5) and up to 10 WKUP events. Two additional events are reserved for I3C reset patterns. These pins can also invoke a wake-up interrupt. On STM32U5, this is limited to Stop 3 mode only.

STM32U5 devices also embed a temperature sensor and backup domain voltage monitor to continuously check operational conditions.

STM32U5 devices provide four voltage ranges, whereas STM32U3 devices only provide two. However, as the STM32U3 devices use subtreshold technology, the V_{CORE} voltage of both ranges is lower than on STM32U5 and so is the power consumption. The EPOD booster of STM32U3 devices must be turned on for frequencies above 24 MHz (compared to 55 MHz on STM32U5).

The consumption is even lower on STM32U3 thanks to the adaptive voltage scaling (AVS) technique. The V_{CORE} is tuned individually on each device to achieve the target frequency of every voltage range and have the lowest consumption at the same time. The exact voltages of STM32U3 voltage ranges might therefore vary.

As the SmartRun domain (SRD) is not present on STM32U3 devices, it does not offer the LPBAM functionality and the number of peripherals autonomous in Stop 0/1/2 modes is limited.

The mentioned differences are summarized in Table 9.

Table 9. Overview of differences of PWR on STM32U3 and STM32U5 devices

Feature		STM32U5 series	STM32U3 series
Power supply domains		V_{CORE}, V_{DD}, backup, analog, V_{DDSMPS}, V_{DDIO2}, V_{DDUSB} (and optional $V_{DD11USB}$), V_{DDDSI}(1) and $V_{DD11DSI}$(1)	V_{CORE}, V_{DD}, backup, analog, V_{DDSMPS}, V_{DDIO2}, V_{DDUSB}
Power supply supervision		BOR, PVD, PVM monitors, out of functional range temperature & backup domain voltage monitors	BOR, PVD, PVM monitors
Voltage ranges		4	2
EPOD booster corner frequency		55 MHz	24 MHz
Adaptive voltage scaling (AVS)		No	Yes
Output pins		CSLEEP, CDSTOP, SRDSTOP	PWR_CSLEEP, PWR_CSTOP
PWR wake-up	WKUPx events	8	10
	Wake-up pins	24 pins	23 pins
	Wake-up interrupt	PWR_S3WU (Stop 3 mode only) - Exit from Stop 3, Standby, and Shutdown modes	PWR and PWR_S - Exit from Sleep, Stop 0/1/2/3, Standby and Shutdown modes
LPBAM		Yes	No
Autonomous peripherals	Stop 0/1	ADC4, DAC, all LPTIMs, all U(S)ARTs, LPUART1, all SPIs, all I2Cs, MDF1, ADF1, GPDMA1, LPDMA1	DAC, LPTIMx (x = 1 to 4), all U(S)ARTs, LPUART1, all SPIs, all I2Cs, all I3Cs, ADF1, GPDMA1
	Stop 2	ADC4, DAC, LPTIM1, LPTIM3, LPUART1, SPI3, I2C3, ADF1, LPDMA1	LPTIM1, LPTIM3, LPTIM4, LPUART1, I2C3

1. *Only on STM32U59x/Ax/Fx/Gx devices.*

Due to these differences and different sets of peripherals available the PWR registers of both series are not compatible. Refer to document [1] and [2] for more details.

3.9 Reset and clock control (RCC)

The first part, reset control, is the same for both STM32U3 and STM32U5 devices. For the clocks and its control, there are many differences.

The main differences are the maximum operational frequency and the absence of PLL on STM32U3 devices. This is compensated by MSI clocks offering frequencies up to maximum frequency, that is 96 MHz (the MSI of STM32U5 offers frequencies up to 48 MHz) with more options of hardware autocalibration (so called PLL-mode). Additionally, using PLL-mode on STM32U3, the multiplication factor for the MSIRCx (x = 0,1) oscillator might be tuned to obtain other frequencies from 3 up to 96 MHz.

The STM32U3 devices also offer additional clock output, MCO2.

Refer to Table 10 for overview of these differences.

Table 10. Overview of differences of RCC on STM32U3 and STM32U5

Features		STM32U5	STM32U3
Maximum frequency		160 MHz	96 MHz
SYSCLK clocks		• HSI16 (16 MHz) • MSIS (0.1-48 MHz) • HSE (4-50 MHz) • PLL1	• HSI16 • MSIS (3-96 MHz) • HSE (4-50 MHz)
Additional clocks		• MSIK (0.1-48 MHz) • LSI (32/0.25 kHz) • LSE (32.768 kHz) • HSI48 (48 MHz) • SHSI (48 MHz) • PLL2 and PLL3	• MSIK (3-96 MHz) • LSI (32/0.25 kHz) • LSE (32.768 kHz) • HSI48 (48 MHz)
PLL		main PLL + 2x PLL for kernel clocks	N/A
Clock output		MCO, LSCO	MCO, MCO2, LSCO
MSI	Oscillators	4 (48/4/3.072/0.4 MHz)	2 (96/24 MHz)
	Frequencies	48, 24, 16, 12, 4, 2, 1.33, 1, 3.072, 1.536, 1.024, 0.768, 0.4, 0.2, 0.133, 0.1 MHz	96, 48, 24.576, 24, 22.5792, 12.288, 12, 11.2896, 6.144, 6, 5.6448, 3.072, 3, 2.8224 MHz
	PLL-mode	LSE	HSE (16 or 32 MHz), LSE

Concerning the kernel clocks, the STM32U5 devices offers more options. See Table 11 for more details.

Table 11. Comparison of available kernel clocks for individual peripherals on STM32U3 and STM32U5

Peripheral	STM32U5	STM32U3
IWDG	LSI	LSI
UCPD1	HSI16	N/A
RTC	• LSI • LSE • HSE/32	• LSI • LSE • HSE/32
LPTIM1/3/4	• LSI • LSE • MSIK • HSI16	• LSI • LSE • MSIK • HSI16
SysTick	• LSI • LSE • HCLK/8	• LSI • LSE • HCLK/8
TIM2/3/4/(5)/6/7	PCLK1 x1 or x2	PCLK1 x1 or x2
U(S)ART(2)/3/4/5/(6)	• PCLK1 • LSE • HSI16 • SYSCLK	• PCLK1 • HSI16
SPI2	• PCLK1 • MSIK • HSI16 • SYSCLK	• PCLK1 • MSIK
I2C1/2/(4/5/6)	• PCLK1 • MSIK • HSI16 • SYSCLK	• PCLK1 • MSIK
I3C1	N/A	• PCLK1

Peripheral	STM32U5	STM32U3
		• MSIK
LPTIM2	• PCLK1 • LSI • LSE • HSI16	• PCLK1 • LSI • LSE • HSI16
FDCAN1	• HSE • PLL1_Q • PLL2_P	• PCLK1 • MSIK
CRS	HSI48	HSI48
OCTOSPI1/(2)	• SYSCLK • MSIK • PLL1_Q • PLL2_Q	• PCLK1 • MSIK
SAES	• SHSI • SHSI /2	HCLK
TIM1/(8/)15/16/17	PCLK2 x1 or x2	PCLK2 x1 or x2
USART1	• PCLK2 • HSI16 • LSE • SYSCLK	• PCLK2 • HSI16
SPI1	• PCLK2 • MSIK • HSI16 • SYSCLK	• PCLK2 • MSIK
I3C2	N/A	• PCLK2 • MSIK
ADF1 (and MDF1)	• MSIK • AUDIOCLK • HCLK • PLL1 • PLL3	• MSIK • AUDIOCLK • SAI1 clock
SAI1/(2)	• AUDIOCLK • PLL1_P • PLL2_P • PLL3_P • HSI16	• MSIK • AUDIOCLK • HSE
ICLK	• MSIK • HSI48 • PLL1_Q • PLL2_Q	• MSIK • HSI48 • HSE • SYSCLK
SDMMC1/(2)	• ICLK • PLL1_P	ICLK
USB or OTG_FS	ICLK	• ICLK • ICLK /2
RNG	• HSI16 • HSI48 • HSI48 /2	• MSIK • HSI48
I2C3	• PCLK3 • MSIK • HSI16 • SYSCLK	• PCLK3 • MSIK
SPI3	• PCLK3 • MSIK	• PCLK3 • MSIK

Peripheral	STM32U5	STM32U3
	• HSI16 • SYSCLK	
LPUART1	• PCLK3 • MSIK • HSI16 • SYSCLK • LSE	• PCLK3 • MSIK • HSI16 • LSE
ADC1/(2/4) and DAC	• HCLK • SYSCLK • PLL2_R • HSE • HSI16 • MSIK	• HCLK /1 to 512 • MSIK /1 to 512 • HSE /1 to 512
DAC sample & hold	• LSI • LSE	• LSI • LSE
HSPI	• SYSCLK • PLL1_Q • PLL2_Q • PLL3_R	N/A
LTDC	• PLL2_R • PLL3_R	N/A
DSI	• PLL3_P • HSE	N/A
OTG_HS	• HSE • PLL1_P • HSE /2 • PLL1_P /2	N/A

Due to different sets of peripherals available, different memory mapping of some common peripherals and different sets of features of RCC on both series, most of the registers are not compatible despite the same name or memory address. Refer to document [1] and [2] for more details.

3.10 System configuration controller (SYSCFG) and infrared interface (IRTIM)

The functionality of SYSCFG is similar for common peripherals. On some STM32U5 devices (STM32U59x/Ax/Fx/Gx), HSPI, OTG_HS PHY and DCACHE2 settings can be additionally changed with registers of SYSCFG.

The only exception is the infrared interface (IRTIM) on STM32U3, which offers more options than IRTIM on STM32U5. See Table 12 for a comparison of these features on both series.

Table 12. Comparison of IRTIM features on STM32U3 and STM32U5

Feature	STM32U5	STM32U3
Carrier signal source	TIM17_CH1	TIM17_CH1
Modulating signal source	TIM16_CH1	TIM16_CH1, USART1, UART4
Adjustable polarity	N/A	X
Settings register	N/A	SYSCFG_CFGR1

The changes in registers are caused only by the aforementioned differences.

3.11 General purpose direct memory access controller (GPDMA)

The GPDMA peripheral is very similar for both series. The principle of the linked list is the same. The difference is in the number of GPDMA channels and their configuration. See Table 13 for comparison of available channels and features.

The GPDMA of STM32U3 devices embed a new feature called peripheral flow-control mode. A peripheral with this feature can terminate a GPDMA block transfer early, before it is transferred completely. This feature is currently supported on GPDMA channels 0 and 1 for `i3c1_rx_dma` and `i3c2_rx_dma` requests. See the corresponding chapter in document [2] for more details about this feature.

Table 13. Overview of GPDMA features for STM32U5 and STM32U3

Feature	STM32U5	STM32U3
Number of channels	• 12 channels with a FIFO of eight bytes (two words) and linear addressing • 4 channels with a FIFO of 32 bytes (eight words) and 2D addressing	• 8 channels with a FIFO of eight bytes (two words) and linear addressing • 2 channels with a FIFO of 32 bytes (eight words) and linear addressing • 2 channels with a FIFO of 32 bytes (eight words) and 2D addressing
Autonomous mode	Sleep, Stop 0/1	Sleep, Stop 0/1
Requests	Compatibility for common peripherals	
Block requests	LPTIM1/3	LPTIM1/2/3
Triggers	Compatibility for common peripherals	
Peripheral flow-control mode	N/A	X

The registers of both series are almost the same, with two exceptions:

- The number of bits in SECCFGR, PRIVCFGR, RCFGLOCKR, MISR, and SMISR corresponds to the number of available channels, and is therefore different.
- Registers C0TR2 and C1TR2 contain additional bit PFREQ (bit 12) to enable peripheral flow-control mode on STM32U3 devices.

3.12 Nested vectored interrupt controller (NVIC)

The interrupt vector is compatible for common peripherals. See Table 14 where all differences in the interrupt vectors between series are listed.

Table 14. List of differences in NVIC on STM32U3 and STM32U5

Address	STM32U5	STM32U3
0x00D4	ADC1_2	ADC1
0x0100	TIM5	Reserved
0x010C	TIM8_BRK/TIM8_TERR/TIM8_IERR	Reserved
0x0110	TIM8_UP	Reserved
0x0114	TIM8_TRG_COM/TIM8_DIR/TIM8_IDX	I3C1 EV
0x0118	TIM8_CC	I3C1 ER
0x0138	USART2	Reserved
0x016C	FMC	Reserved
0x0174	PWR_S3WU	Reserved
0x017C	SDMMC2	Reserved
0x0190	GPDMA1_CH12	Reserved
0x0194	GPDMA1_CH13	Reserved
0x0198	GPDMA1_CH14	Reserved
0x019C	GPDMA1_CH15	Reserved

Address	STM32U5	STM32U3
0x01AC	SAI2	Reserved
0x01D0	I2C4_ER	I3C2 EV
0x01D4	I2C4_EV	I3C2 ER
0x01D8	MDF1_FLT0	Reserved
0x01DC	MDF1_FLT1	Reserved
0x01E0	MDF1_FLT2	Reserved
0x01E4	MDF1_FLT3	Reserved
0x01E8	UCPD1	Reserved
0x01F0	OTFDEC1	Reserved
0x01F4	OTFDEC2	Reserved
0x01FC	DCACHE	Reserved
0x0204	ADC4	ADC2
0x0208	LPDMA1_CH0	Reserved
0x020C	LPDMA1_CH1	Reserved
0x0210	LPDMA1_CH2	Reserved
0x0214	LPDMA1_CH3	Reserved
0x0218	DMA2D	Reserved
0x021C	DCMI_PSSI	Reserved
0x0220	OCTOSPI2	Reserved
0x0224	MDF1_FLT4	Reserved
0x0228	MDF1_FLT5	Reserved
0x022C	CORDIC	PWR
0x0230	FMAC	PWR_S
0x0234	MSI_PLL_UNLOCK	Reserved
0x0234	LSECSS	Reserved
0x0238	USART6	Reserved
0x023C	I2C5_ER	Reserved
0x0240	I2C5_EV	Reserved
0x0244	I2C6_ER	Reserved
0x0248	I2C6_EV	Reserved
0x024C	HSPI1	Reserved
0x0250	GPU2D_IRQ	Reserved
0x0254	GPU2D_IRQSYS	Reserved
0x0258	GFXMMU	Reserved
0x025C	LCD-TFT	Reserved
0x0260	LCD-TFT_ERR	Reserved
0x0264	DSIHOST	Reserved
0x0268	GCACHE	Reserved
0x026C	GFXTIM_GLB_IT	Reserved
0x0270	JPEG_SYNC_IT	Reserved

3.13 Extended interrupt and event controller (EXTI)

The EXTI peripherals of STM32U5 and STM32U3 devices are almost compatible. While STM32U5 devices offer 26 EXTI lines, STM32U3 devices offer only 23 EXTI lines. Refer to Table 15 to compare available lines.

Table 15. EXTI line sources of STM32U3 and STM32U5

EXTI line	Line source	
	STM32U3series	STM32U3 series
0-15	GPIO	GPIO
16	PVD output	PVD output
17	COMP1 output	COMP1 output
18	COMP2 output	COMP2 output
19	V_{DDUSB} voltage monitor	V_{DDUSB} voltage monitor
20	V_{DDIO2} voltage monitor	V_{DDIO2} voltage monitor
21	VDDA voltage monitor 1	VDDA voltage monitor 1
22	VDDA voltage monitor 2	VDDA voltage monitor 2
23	LSECSS or MSI_PLL_UNLOCK(1)	N/A
23	MSI_PLL_UNLOCK(2)	N/A
24	LSECSS(2)	N/A
25	IWDG early interrupt	N/A

1. *Available only on STM32U575/585 line.*
2. *Available on all STM32U5 lines, except the STM32U575/585 line.*

The EXTI registers differ accordingly. They offer settings for 26 or 23 channels.

3.14 Cyclic redundancy check calculation unit (CRC)

Contrary to CRC peripheral on STM32U5 devices, the CRC peripheral on STM32U3 devices offer more possibilities of input and output data reversal (bit/byte/half-word reversal done by byte/half-word/word). This reversal is for both series set in CRC_CR register, and so its structure differs. See Table 16 with comparison of its structure on STM32U3 and STM32U5 devices.

Table 16. Register CRC_CR on STM32U3 and STM32U5

Series/bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STM32U5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REV_OUT	REV_IN[1:0]		POLYSIZE[1:0]		Reserved	Reserved	RESET
STM32U3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RTYPE_OUT	RTYPE_IN	REV_OUT[1:0]		REV_IN[1:0]		POLYSIZE[1:0]		Reserved	Reserved	RESET

3.15 Octo-SPI interface (OCTOSPI)

The OCTOSPI is a peripheral enabling connection of external serial memories available on both STM32U3 and STM32U5 devices. For STM32U3, it is the only interface for external RAMs and flash memories, STM32U5 devices offer also FMC. The access is protected by MPCWM (refer to Section 3.5) and OTFDEC (only for crypto devices) on STM32U5 devices to protect the confidentiality of read-only firmware libraries stored in external SPI NOR flash devices. The STM32U3 devices does not offer such protection for external memories.

The main difference of OCTOSPI itself is the number of available instances. On STM32U3 and STM32U535/45 devices it is only one, while on other STM32U5 devices it is two. Additionally, some advance STM32U5 devices offer a high-speed HSPI interface.

On STM32U5 devices with two OCTOSPI instances, an OCTOSPI manager is available as well. This peripheral enables efficient OCTOSPI pin assignment on the full I/O matrix.

Comparing OCTOSPI implementations on both series, the only difference is an ability to regulate communication on STM32U5 devices. The maximum length of a transaction is limited by the value of the MAXTRAN[7:0] field in the DCR3 register (reserved on STM32U3 devices). They are fully compatible otherwise.

The differences are summarized in Table 17. Refer to the corresponding reference manuals [1] and [2] for more details.

Table 17. Overview of OCTOSPI features on STM32U3 and STM32U5

Feature	STM32U5	STM32U3
Interfaces to connect external memories(1)	OCTOSPI, HSPI, FSMC (+ SDMMC)	OCTOSPI (+ SDMMC)
OCTOSPI memory protection	MPCWM, OTFDEC	N/A
Number of OCTOSPI instances(2)	2	1
OCTOSPIM(2)	X	N/A
OCTOSPI communication regulation	X	N/A

1. *HSPI available only for STM32U59x/5Ax/5Fx/5Gx. FSMC not available for STM32U535/545 line.*
2. *Only one OCTOSPI and no OCTOSPI manager for STM32U535/545 line.*

3.16 Analog-to-digital converter (ADC)

On STM32U5 devices, 1–2 14-bit and 1 12-bit ADCs are available, while on STM32U3 devices two 12-bit ADCs are available. See Table 18 for comparison of features of available ADCs for both series.

Table 18. Overview of ADC features on STM32U3 and STM32U5

Feature	STM32U5		STM32U3
	ADC1/2 (1)	ADC4	ADC1/2
Resolution	14 bits	12 bits	12 bits
Maximum sampling speed (max resolution)	2.5 Msps		2.5 Msps
Dual mode	X(2)	N/A	X
Offset calibration	X		X
Linearity calibration	X	N/A	N/A
Single-end input	X		X
Differential input	N/A		N/A
Injected channel conversion	X	N/A	X
Oversampling	up to 1024x	up to 256x	up to 1024x
Data register	32 bits	16 bits	32 bits
DMA support	X		X

Feature	STM32U5		STM32U3
	ADC1/2 (1)	ADC4	ADC1/2
Parallel data output to MDF/ADF	X	N/A	X
Offset compensation	X	N/A	X
Gain compensation	X	N/A	X
Autonomous mode	N/A	Stop 0/1/2	N/A
Number of analog watchdogs	3		3
Deep power-down mode	N/A		X
Wake-up from Stop mode	N/A	Stop 0/1/2	N/A

1. *ADC2 available only for STM32U59x/5Ax/5Fx/5Gx.*
2. *Only when ADC2 is available.*

Even though the functionality of ADC1/2 on STM32U5 devices and ADC1/2 on STM32U3 devices is similar and the memory location is the same, the structure and even order of registers is different. Refer to corresponding chapters in document [1] and [2] for information about available register settings.

3.17 Multifunction digital filter (MDF) and audio digital filter (ADF)

The multifunction digital filter (MDF) is a high-performance module dedicated to the connection of external sigma-delta (ΣΔ) modulators. This filter is available on STM32U5 devices only. Refer to document [1] for more details.

Contrary to MDF, the audio digital filter (ADF) is available on both series, with one filter and one digital interface. The set of features is almost the same for both series, additional triggers are available on STM32U3 devices, as well as connections to ADC to process data from it directly. This is summarized in Table 19.

Table 19. Overview of ADF features on STM32U3 and STM32U5

Feature	STM32U5	STM32U3
Number of MDF instances	1	N/A
Number of ADF instances	1	1
Number of ADF filters/interfaces	1/1	1/1
Connection to ADC	N/A	X
Sound activity detection	X	X
Trigger sources	EXTI15	EXTI15, TIM1, TIM3, TIM6

The differences in registers are listed in Table 20.

Table 20. Overview of register differences in the ADF peripheral

Register	Field	Comment
ADF_TRGISELR	TRIGSEL[1:0]	Available only on STM32U3 devices (whole register) to select trigger source, bits 1:0
ADF_SADCFGR	SNTHR[x:0]	Field to adjust the signal to noise threshold, 3-bit on STM32U5 vs. 4-bit on STM32U3, starting at bit 0

3.18 Touch sensing controller (TSC)

The maximum number of available touch channels groups on STM32U5 devices is eight, while it is only seven on STM32U3 devices. Therefore, the number of registers and/or register fields dedicated to touch channel groups differ accordingly. The peripherals are compatible on both series otherwise.

3.19 True random number generator

All STM32U3 and STM32U5 devices embed a true RNG peripheral. It can be used to construct a nondeterministic random bit generator (NDRBG).

The version of the RNG embedded in STM32U3 devices is an enhanced version of the one embedded in the STM32U5 devices. It offers better entropy and additional configuration registers for health checks (RNG_HTCR1, RNG_HTCR2 and RNG_HTCR3) and noise source control (RNG_NSCR). Refer to document [2] for more information.

On STM32U3 devices, the RNG is one of the peripherals connected to the CCB (coupling and chaining bridge) increasing security robustness. This way, for example, data coming to PKA RAM or SAES might be replaced by random numbers from RNG. Refer to the CCB chapter in document [2] for more details.

3.20 AES and secure AES hardware accelerators (AES, SAES)

The crypto versions of the STM32U3 and STM32U5 devices embed both AES and secure AES hardware accelerators.

The AES peripheral is the same for both series - full registers compatibility and features list.

The SAES peripheral of STM32U3 devices offers better latency, more chaining algorithms, and a possibility to suspend a message, if another message with a higher priority needs to be processed. This is summarized in Table 21.

Table 21. Overview of SAES features on STM32U3 and STM32U5

Feature	STM32U5	STM32U3
ECB, CBC chaining	X	X
CTR, CCM, GCM chaining	N/A	X
AES 128-bit ECB encryption in cycles	528	480
DHUK and BHK key selection	X	X
Side-channel attacks resistance	X	X
Shared key between SAES and AES	X	X
Key sizes in bits	128, 256	128, 256
Software message suspension	N/A	X

Concerning the registers, the structure of the CR register differs (fields for new functions were added), and eight SUSPRx registers were added on STM32U3 devices.

Additionally, the SAES of STM32U3 devices is connected to CCB (coupling and chaining bridge) which increase security robustness. The SAES peripheral may be chained together with PKA, PKA RAM or CCB itself. For example, writes going to the PKA RAM might be sent to the SAES input register or be substituted by data coming from the SAES output register. Refer to the CCB chapter in document [2] for more details.

3.21 HASH processor (HASH)

The HASH peripherals of both series are very similar, but they differ in supported algorithms (refer to Table 22), and size of some registers (refer to Table 23).

Table 22. Supported algorithms for HASH on STM32U3 and STM32U5

Algorithm	STM32U5	STM32U3
SHA1	X	X

Algorithm	STM32U5	STM32U3
SHA2-224	X	X
SHA2-256	X	X
MD5	X	N/A
SHA2-384	N/A	X
SHA2-512	N/A	X

Table 23. Differences in HASH registers for STM32U3 and STM32U5

Register	Field	Comment
CR	ALGO[x:0]	2-bit for STM32U5, 4-bit for STM32U3
HRx	-	8 registers for STM32U5, 16 registers for STM32U3
CSRx	-	54 registers for STM32U5, 104 registers for STM32U3

3.22 Public key accelerator (PKA)

The PKA peripherals on STM32U5 and STM32U3 crypto devices are very similar. The set of supported algorithms and operations is the same.

The main additional features on STM32U3 devices are hardware protections to monitor the usage of private keys and the integration into the CCB (coupling and chaining bridge) which increase security robustness. The PKA peripheral, along with its dedicated RAM, might be chained together with SAES, or RNG. This way, e. g. write requests to PKA RAM might be substituted by the output of the SAES or RNG peripherals. Refer to the CCB chapter in document [2] for more details.

These differences are also reflected in the registers of the peripheral. The registers contain additional fields for control of the coupling and chaining, as well as additional error flags. Refer to document [2] for more details.

3.23 Timers and low-power timers (TIM, LPTIM)

The additional feature of timers on STM32U3 devices is synchronization with ADC clock to support jitter-free ADC sampling. For this reason, ADSYNC (bit 28) was added to the CR2 register of TIM1, TIM2, TIM3, TIM4, TIM6, TIM7, and TIM15. This bit is reserved on STM32U5 devices.

The low-power timers of both series are fully compatible.

3.24 Real time clock (RTC)

Both STM32U3 and STM32U5 devices contain real time clock (RTC). Both peripherals are very similar. The main difference is an enhancement of the time stamp function on STM32U3 devices. Thanks to two new registers (`TAMP_TSCR` and `TAMP_TSIDR`), it is possible to configure when the time stamp is saved, and after such events happen also to find out the reason why the time stamp was saved.

Another difference is in the behavior of the RTC_OUT2 pin, which works as well in VBAT mode on STM32U5 devices.

The peripherals and their registers are fully compatible otherwise.

3.25 Tamper and backup registers (TAMP)

The anti-tamper detection circuit is used to protect sensitive data from external attacks. This peripheral is implemented on both series, with a different set of available features, see Table 24.

The active tampers are the main additional feature of TAMP on STM32U5 devices. The tamper pins are automatically checked for open circuits and short circuits to increase the security level. Refer to the corresponding chapter in document [1] for more details.

Contrary to it, STM32U3 devices embed TAMP with enhanced time stamp configuration (through RTC registers, see Section 3.24) and more flexible configuration of device resources protection on tamper events. Refer to the corresponding chapter in document [2] for more details.

Table 24. **Overview of TAMP features on STM32U3 and STM32U5**

Feature	STM32U5	STM32U3
Number of tamper pins	8	5
Number of internal tampers	11	9
Backup registers (32-bit)	32	32
Active tampers	X	N/A
Device resources protection configuration	N/A	X
Enhanced time stamp configuration	N/A	X

These differences are reflected in the registers of both series. See Table 25 for an overview of these differences. For more details, refer to the corresponding chapters in document [1] and [2].

Table 25. **Overview of TAMP registers on STM32U3 and STM32U5**

Register		Difference
STM32U5	STM32U3	
TAMP_CR1	TAMP_CR1	Reduced number of fields on STM32U3 for tamper pins/internal tampers.
TAMP_CR2	TAMP_CR2	
TAMP_CR3	TAMP_CR3	Reduced number of fields on STM32U3 for internal tampers, fields name change (ITAMPxNOER <-> ITAMPxPOM).
TAMP_ATCR1	N/A	Registers for configuration of the active tampers on STM32U5, reserved on STM32U3.
TAMP_ATSEEDR		
TAMP_ATOR		
TAMP_ATCR2		
TAMP_IER	TAMP_IER	Reduced number of fields on STM32U3 for tamper pins/internal tampers.
TAMP_SR	TAMP_SR	
TAMP_MISR	TAMP_MISR	
TAMP_SMISR	TAMP_SMISR	
TAMP_SCR	TAMP_SCR	
TAMP_ERCFGR	TAMP_RPCFGR	Register name change (TAMP_ERCFGR <-> TAMP_RPCFGR), additional fields for device resources protection configuration (seven fields on STM32U3, one field on STM32U5).

3.26 Universal synchronous/asynchronous receiver/transmitter (USART/UART, LPUART)

The STM32U3 and STM32U5 devices embed different counts of USART/UART instances. Refer to Section 3.1 for more details. These instances are fully compatible between both series.

The LPUART peripherals are almost fully compatible for both series, with the only exception of the additional TXFIFO and RXFIFO threshold flags of the ISR register that are available on STM32U3 devices. This is summarized in Table 26.

Table 26. LPUART register differences between STM32U3 and STM32U5

Register	Field	Comment
LPUART_ISR	TXFT	TXFIFO threshold flag, available only on STM32U3 devices (bit 27)
	RXFT	RXFIFO threshold flag, available only on STM32U3 devices (bit 26)

3.27 Universal serial bus full-speed interface (USB)

The USB peripherals available on STM32U3 and STM32U5 devices differ from line to line. See Table 27 for comparison of available USB peripherals and their features.

Table 27. Comparison of available USB peripherals for STM32U3 and STM32U5

Feature		STM32U5			STM32U3
		USB FS (STM32U535/545)	OTG FS (STM32U575/585)	OTG HS (STM32U59x/5Ax/5Fx/5Gx)	USB FS (STM32U375/385)
Speed	Host mode	12 Mb/s, 1.5 Mb/s		480 Mb/s, 12 Mb/s, 1.5 Mb/s	12 Mb/s, 1.5 Mb/s
	Device mode	12 Mb/s		480 Mb/s, 12 Mb/s	12 Mb/s
Number of bidirectional endpoints		8	6	9	8
Host mode channels		12		16	12
Size of dedicated SRAM (Kbytes)		2	1.2	4	2
USB 2.0 support		Yes			Yes
OTG revision supported		N/A	2.0		N/A
Battery charging detection (BCD) support		Yes			Yes
Embedded PHY		Yes			Yes

The registers of the USB FS available on the STM32U3 devices are fully compatible with registers of the USB FS of the STM32U535/545 line.

Revision history

Table 28. **Document revision history**

Date	Version	Changes
06-Feb-2025	1	Initial release.
28-Feb-2025	2	Introduction updated.

Contents

List of tables

List of figures