

## Migrating from STM32MP25x to STM32MP21x MPUs

### Introduction

The STM32MP211, STM32MP213, and STM32MP215 devices are part of the STM32 Arm® Cortex® MPUs. They all feature a single Cortex®-A35 core, and a Cortex®-M33 core without a GPU/NPU, nor a video decoder (VDEC).

These devices are referred to as STM32MP21x in this document.

The Cortex®-M33 inside the STM32MP25x devices is identical to the one in the STM32MP21x devices. For an STM32Cube package, this compatibility permits an easy migration from an STM32MP25x device to an STM32MP21x device.

Similarly to the STM32MP25x lines, the high performance Cortex®-A35 core inside the STM32MP21x runs open operating systems such as Linux®. Both provide rich connectivity and the support of a software community. A system configuration migration between different hardware using different device trees is supported with OpenSTLinux.

This application note provides information to facilitate the migration from an STM32MP25x design towards an STM32MP21x one.

**Table 1. Applicable products**

Type	Product lines
Microcontrollers	STM32MP211, STM32MP213, STM32MP215 STM32MP251, STM32MP253, STM32MP255, STM32MP257

## 1 General information

This document applies to STM32MP25x and STM32MP21x Arm<sup>®</sup>-based MPUs.

*Note:* Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

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## 2 References

**Table 2. Referenced documents**

N°	Reference	Title
[1]	DS14556, DS14557	STM32MP21xA/D/C/Fxx datasheet
[2]	DS14284, DS14285	STM32MP25xA/D/C/Fxx datasheet
[3]	RM0457	STM32MP25x reference manual
[4]	AN5489	Getting started with STM32MP25x lines MPUs hardware development
[5]	RM0506	STM32MP21x reference manual
[6]	AN6055	Getting started with STM32MP21x lines MPUs hardware development

### 3 STM32MP25x line overview

The STM32MP25x lines are part of the STM32MP2 series. Depending on the device part number, the system includes a Cortex<sup>®</sup>-M33, and either a single-core, or a dual-core Cortex<sup>®</sup>-A35 and a GPU/NPU.

The full featured system is partitioned in:

- An MPU subsystem based on a dual Cortex<sup>®</sup>-A35 core a with L2 cache
- A second MCU subsystem based on Cortex<sup>®</sup>-M33 with associated peripherals clocked according to the CPU activity

For more information about the full featured system of the STM32MP25x, see [Table 3](#).

**Table 3. Configuration of the STM32MP25x lines**

Lines	Reference manual	Cortex <sup>®</sup> -A35 configuration	Cortex <sup>®</sup> -M33	GPU/NPU Hardware video Encode/Decode	DSI	FDCAN	Ethernet ports	LVDS
STM32MP251	[3]	Single-core	Yes	No	Yes	No	1	No
STM32MP253		Dual-core	Yes	No	Yes	Yes	2	Yes
STM32MP255		Dual-core	Yes	Yes	Yes	Yes	2	Yes
STM32MP257		Dual-core	Yes	Yes	Yes	Yes	3 <sup>(1)</sup>	Yes

1. With a 2-port TSN compliant switch.

## 4 STM32MP21x line overview

The STM32MP21x lines are part of the STM32MP2 series.

The full-featured system is partitioned in:

- An MPU subsystem based on a single Cortex<sup>®</sup>-A35 with a L2 cache
- A second MCU subsystem: Cortex<sup>®</sup>-M33 with associated peripherals clocked according to the CPU activity

For more information about the full-featured system of the STM32MP21x, see [Table 4](#).

**Table 4. Configuration of the STM32MP21x lines**

Lines	Reference manual	Cortex <sup>®</sup> -A35 configuration	Cortex <sup>®</sup> -M33
STM32MP211	[5]	Single-core	Yes
STM32MP213		Single-core	Yes
STM32MP215		Single-core	Yes

The STM32MP21x lines offer a reduced set of peripherals compared to the STM32MP25x devices with some improved performance and features. See the list below.

### Processing

- No Arm<sup>®</sup> Cortex<sup>®</sup>-M0+ and associated peripherals (memory, LPDMA, IWDG5, WWDG2, HSEM, IPCC2)
- External LPDDR4/DDR4/DDR3L SDRAMs with 16-bit interface, compared to 32 bits for the STM32MP25x

### Connectivity

- No PCIe<sup>®</sup> interface
- No USB Type-C<sup>®</sup>
- USB3.0 DRD is replaced by USB2 OTG\_HS Host/Device
- No DSI
- Only one OCTOSPI
- No LVDS
- Ethernet TSN switch is removed. There are only two Ethernet ports, compared to three for the STM32MP25x

### Other

- No video encoder
- Decreased memory size: 448 Kbytes, compared to 640 Kbytes for the STM32MP25x

### Reduced number of peripherals

- Two FDCANs instead of three
- Four MDF audio channels/filters instead of eight
- Two 16-bit PWM timers instead of three
- Six SPIs instead of eight, and three I2Ss
- Eight (LP)U(S)ARTs instead of ten
- Three I2Cs instead of eight
- Three I3Cs instead of four

### Processing

- No GPU
- No NPU
- DDR performance reduced to 800 MHz

### Audio

- No ADF
- Split of audio clocks for SAI, MDF to have independent clock frequency

### Security

- DDR on the fly encrypt/decrypt AES-256 with SCA protection (MCEAXI) included in RISAF DDRMCE
- PKA with SCA/DPA protection and key bus connection
- AES-192 with SCA/DPA protection
- x2 SHA-512 (versus 1)
- Stronger SESIP 3 conformance (RSA/ECC private key store)
- Stronger secure boot encryption (AES-256, ECDSA P-384)
- Monitoring of VDDCPU and VDDCORE is done through an ADC watchdog connected to tampers
- Only 12 tampers (5 outputs, 7 inputs).

### Other

- LCD-TFT: removed rotation feature
- Include Lite-ISP with enhanced statistics in DCMIPP parallel camera interface
- Removed 4 MHz MSI (was used for Arm<sup>®</sup> Cortex<sup>®</sup>-M0+ consumption optimization) and MSI clock is only set to 16 MHz
- FDCAN: CDC update, STNOTECH insertion
- DEBUG: mailbox for JTAG reopening, authentication under reset, DAP-AXI 33-bit addressing
- All three SPI autonomous in LP/LPLV-Stopx (versus only 1)
- x2 vs x3 ADC 12b 4.8MSPS (ADC1/ADC2 independent)
- x1 vs x2 digital temperature sensor

### STM32MP21x 8x8 VFBGA225 package specificities

The 8x8 VFBGA225 package with 98 GPIOs on STM32MP21x has further limitations

- Reduction in number of peripherals:
  - No LPUART1
  - No TIM16, TIM17, LPTIM3, LPTIM4, LPTIM5
  - No CSI interface
- No USB2\_HS signals (single lane USB)
- SDMMC2 is only 4 bits. SDMMC2 is not a boot source for VFBGA225 8x8 package.
- SDMMC3 has no external level shifter control
- Only 8-bit FMC
- Only eight tampers (1 out, 7 in)
- No SAI4\_D1 signal
- No WKUP4 signal
- No RTC\_OUT2/RTC\_LSCO signals
- FMC\_NWE default boot pin changed (from PE14 to PD13)

## 5 Hardware migration

The 10x10 mm VFBGA361 package has been designed to be compatible with all STM32MP2 series devices. For another package size, a good candidate for migration towards an STM32MP21x device can be chosen by considering the following criteria:

- GPIOs: equivalent number of available GPIOs. A precise count must be done for each application use case.
- Size: the package size
- PCB: the PCB technology cost (xFBGA 0.5 mm pitch or xFBGA 0.8 mm pitch)
- DDR: the DDR bus width (16 or 32 bits) which is linked to the maximum Cortex-A and GPU performances.

The following table summarizes the key package parameters for STM32MP25x and STM32MP21x lines.

**Table 5. Packages on STM32MP25x and STM32MP21x lines**

Lines		STM32MP25x lines			STM32MP21x lines			
<b>Product</b>		STM32MP25xxAL	STM32MP25xxAK	STM32MP25xxAI	STM32MP21xxAO	STM32MP21xxAL	STM32MP21xxAN	STM32MP21xxAM
<b>Package</b>		VFBGA361	VFBGA424	TFBGA436	VFBGA225	VFBGA361	VFBGA273	TFBGA289
	Size (mm)	10x10	14x14	18x18	8x8	10x10	11x11	14x14
	Ball pitch (mm)	0.5	0.5	0.8	0.5	0.5	0.5	0.8
<b>GPIOs</b>		144	144	172	98	123	123	123
<b>DDR bus width</b>		16	32	32	16	16	16	16

## 5.1 Power supply aspects

To ensure a better performance and power consumption, the STM32MP25x and STM32MP21x lines provide a separated supply voltage domain for Cortex®-A35 and the core domain.

When the activity requires it, these supplies could be overdriven to increase performance, lowered to reduce leakage, or even shut down.

Similarly to the STM32MP25x, for which it is recommended to use the STPMIC2 power supply management IC, it is indicated to use the STPMIC2L for the STM32MP21x (no  $V_{DDGPU}$ ).

More information about STPMICx can be found on [www.st.com](http://www.st.com).

**Table 6. Power supply comparison between STM32MP25x and STM32MP21x lines**

STM32MP25x lines		STM32MP21x lines		Comments
Supply name	Typical	Supply name	Typical	
$V_{DD}$	1.8/3.3 V	$V_{DD}$	1.8/3.3 V	$V_{DD}$ supply level on STM32MP25x/23x/21x should be carefully controlled within the following ranges: 1.71 V - 1.98 V (typ 1.8 V) 3 V - 3.6 V (typ 3.3 V)
$V_{DDIO1}$		$V_{DDIO1}$		Optional domain for SD card on SDMMC1
$V_{DDIO2}$		$V_{DDIO2}$		Optional domain for eMMC on SDMMC2
$V_{DDIO3}$		$V_{DDIO3}$		Optional domain for OCTOSPI port1
$V_{DDIO4}$		-		Optional domain for OCTOSPI port2 Not applicable on STM32MP21x
$V_{DDCORE}$	0.82 V <sup>(1)</sup>	$V_{DDCORE}$	0.82 V <sup>(1)</sup>	This voltage also applies to $V_{DDDSI/LVDS/CSI}$ .
$V_{DDCPU}$	1.25 V <sup>(1)</sup> 1.35 V <sup>(2)</sup>	$V_{DDCPU}$	0.8 V <sup>(1)</sup> 0.91 V <sup>(2)</sup>	For Cortex®-A35
$V_{DDGPU}$	0.8 V	-	-	Not applicable on STM32MP21x
$V_{DDQDDR}$	-	$V_{DDQDDR}$	-	Different ranges to support available DDR
$V_{DD\_ANA}$	1.8 / 3.3 V	$V_{DD\_ANA}$	1.8 / 3.3 V	This voltage also applies to $V_{DDA18DDR/USB/DSI/LVDS/CSI}$ .
$V_{DD\_PLL}$		$V_{DD\_PLL}$		
$V_{DD3V3\_USB}$	3.3 V	$V_{DD3V3\_USB}$	3.3 V	-
$V_{DDA}$	1.8 / 3.3 V	$V_{DDA}$	1.8 / 3.3 V	-
$V_{BAT}$	3 V	$V_{BAT}$	3 V	-
$V_{O8CAP}$	0.8 V <sup>(3)</sup>	$V_{O8CAP}$	0.8 V <sup>(3)</sup>	Backup regulator decoupling capacitance

1. Support lowering.
2. In overdrive mode.
3. External LDO.

**Table 7. System power modes on STM32MP25x and STM32MP21x lines**

STM32MP25x and STM32MP21x lines							Only STM32MP25x	
Mode	V <sub>DD</sub>		V <sub>DDCORE</sub>		V <sub>DDCPU</sub>		V <sub>DDGPU</sub>	
	State	Control	State	Control	State	Control	State	Control
Run 1	ON	-	ON	-	Overdrive	Hardware/software <sup>(1)</sup>	Overdrive or ON or OFF	Hardware/software <sup>(1)</sup>
					ON	-		
Run 2					OFF	PWR_CPU_ON		
Stop 1	ON	-	ON	-	Overdrive	Hardware/software <sup>(1)</sup>	Overdrive or ON or OFF	Hardware/software <sup>(1)</sup>
					ON	-		
Stop 2					OFF	PWR_CPU_ON		
LP-stop1	ON	-	ON	-	Overdrive	Hardware/software <sup>(1)</sup>	Overdrive or ON or OFF	Hardware/software <sup>(1)</sup>
					ON	-		
LP-stop2					OFF	PWR_CPU_ON		
LPLV-stop1	ON	-	Lowered	PWR_ON or PWR_LP	Lowered	PWR_CPU_ON or PWR_LP	OFF or lowered	PWR_CPU_ON or PWR_LP or Hardware/software <sup>(1)</sup>
LPLV-stop2					OFF	PWR_CPU_ON		
Standby1/2	ON	-	OFF	PWR_ON	OFF	PWR_CPU_ON	OFF	PWR_CPU_ON
V <sub>BAT1/2</sub> <sup>(2)</sup>	OFF using hardware or software							

1. For example, GPIO or I<sup>2</sup>C command to STPMIC.

2. Only Standby1 and V<sub>BAT1</sub> on STM32MP21x (no Arm<sup>®</sup> Cortex<sup>®</sup>-M0+ D3 domain).

## 5.2 Alternate function multiplexing aspects

The STM32MP21x pinout and alternate function multiplexing (AFMux) are derived from STM32MP25x. Thus, there are very few differences.

The below list shows information and differences that may be considered when porting a project from STM32MP25x to STM32MP21x:

- When an IP exists on STM32MP25x and STM32MP21x, the corresponding IP signals are assigned to the same GPIOs on all products.
- Some GPIOs have been removed on STM32MP21x.
- The STM32MP21x 123 GPIO list is based on the STM32MP25x VFBGA361 10x10 package 144 GPIO from which 21 GPIOs have been removed.  
The 21 removed GPIOs are:

PB0	PH6	PZ2
PB4	PI2	PZ4
PB8	PI3	PZ5
PF14	PI7	PZ6
PG6	PI9	PZ7
PH2	PI10	PZ8
PH3	PI11	PZ9

- The STM32MP21x 98 GPIO 8x8 mm package is based on the STM32MP21x 123 GPIO 10x10 mm package from which 25 GPIOs have been removed.  
The 25 removed GPIOs are:

PA12	PB6	PE14	PG14	PI6
PB1	PB7	PG8	PG15	PI8
PB2	PB9	PG9	PH7	PZ0
PB3	PB10	PG10	PH8	PZ1
PB5	PE10	PG13	PI5	PZ3

- FMC (flexible memory controller) parallel NOR non-multiplexed address/data, 8 and 16 bits are not supported on 8x8 mm package as it is the case for STM32MP25x on small packages.
- ANA0 and ANA1 pins have also been removed on 8x8 mm package and on 11x11 mm package.
- Some signals have been remapped to keep the feature:
  - SDMMC2\_CK on PE6 AF14 (to keep SDMMC2 4-bit only)
  - SPI2\_MOSI/I2S2\_SDO on PB13 AF02 (to keep SPI2)
  - I2S2\_MCK on PD14 AF02 (to keep I2S2)
- FMC\_D12 has been remapped on STM32MP21x 11x11 mm and 14x14 mm package to keep FMC 16-bit (from PB8 or PI10 on STM32MP25x to PB2).  
FMC\_D12 is also remapped on STM32MP21x 10x10 mm (to keep FMC 16-bit) but it is not compatible with STM32MP25x 10x10 mm AFMux.
- FMC\_A0 on PA5 is not available on STM32MP21x.
- ADC2 from STM32MP25x has been removed and ADC3 has been renamed as ADC2 in STM32MP21x. As a result, all ADC3\_INNx/INPx signals have been renamed ADC2\_INNx/INPx on STM32MP21x.

- Some signal remapping has been done:
  - Added multiplexing for I2C1 in all places where there was I2C4 on STM32MP25x.
  - Added multiplexing for I2C2 in all places where there was I2C5 on STM32MP25x.
  - Added multiplexing for I2C3 in all places where there was I2C7 on STM32MP25x.
  - Added multiplexing for I3C2 in some places where there was I3C3 on STM32MP25x.
  - Added multiplexing for I3C3 in some places where there was I3C4 on STM32MP25x.
  - Added DCMI D0 on PC10 AF11.
  - Added DCMI HSYNC on PC11 AF09.
- On STM32MP21, the number of IP instances has been reduced, and also some IP instances have been renamed:
  - Two CANs instead of three (removed FDCAN3)
  - Four MDF audio channels/filters instead of eight
  - Two 16-bit PWM timers instead of three (TIM20 PWM removed)
  - Six SPIs instead of eight and three I2Ss (removed SPI6, SPI7, renamed SPI8 to SPI6)
  - Eight (LP)U(S)ARTs instead of ten (removed UART8, UART9)
  - Three I2Cs instead of eight (removed I2C3, I2C4, I2C5, I2C6, and I2C7 and renamed I2C8 to I2C3)
  - Three I3Cs instead of four (removed I3C3 and renamed I3C4 to I3C3)
  - Two ADCs 12b 4.8MSPS instead of three (removed ADC2, renamed ADC3 to ADC2, ADC1/ADC2 independent, and ADC2 VINP18 VDD\_GPU internal channel removed)

### 5.2.1 VFBGA361 10x10 compatibility on STM32MP21x

STM32MP25x and STM32MP21x in VFBGA361 10 x10 mm are fully pin-to-pin compatible.

The following conditions have to be considered:

- Package ballout is identical on STM32MP25x and STM32MP21x.
- However, some package balls on STM32MP25x are not applicable on STM32MP21x, because the features are not present. Those balls are connected according to the below table.

**Table 8. VFBGA361 10x10 ballout compatibility**

STM32MP25x	STM32MP21x	Comments
VDDGPU	VDDCORE	No GPU on STM32MP21x <sup>(2)</sup>
VDDA18COMBOPHY	NC <sup>(1)</sup>	No PCIe <sup>®</sup> /USB3 combo PHY on STM32MP21x
VDDCOMBOPHY	NC <sup>(1)</sup>	//
COMBOPHY_TX1P	NC <sup>(1)</sup>	//
COMBOPHY_RX1P	NC <sup>(1)</sup>	//
COMBOPHY_TX1N	NC <sup>(1)</sup>	//
COMBOPHY_RX1N	NC <sup>(1)</sup>	//
COMBOPHY_REXT	NC <sup>(1)</sup>	//
VDDCOMBOPHYTX	NC <sup>(1)</sup>	//
PCIE_CLKINN	NC <sup>(1)</sup>	No PCIe <sup>®</sup> on STM32MP21x
PCIE_CLKOUTN	NC <sup>(1)</sup>	//
VDDPCIECLK	NC <sup>(1)</sup>	//
PCIE_CLKINP	NC <sup>(1)</sup>	//
PCIE_CLKOUTP	NC <sup>(1)</sup>	//
VDDPCIECLK	NC <sup>(1)</sup>	//
USB3DR_TXRTUNE	OTG_TXRTUNE	USB3DR changed by OTG on STM32MP21x
USB3DR_VBUS	NC <sup>(1)</sup>	//
USB3DR_DM	USB2DR_DM	//
USB3DR_DP	USB2DR_DP	//
VDDA18PLL3	NC <sup>(1)</sup>	-
VDDIO4	NC <sup>(1)</sup>	No OCTOSPIM_P2 on STM32MP21x
VDD33UCPD	NC <sup>(1)</sup>	No UCPD on STM32MP21x
DSI_*	NC <sup>(1)</sup>	no DSI on STM32MP21x
VDDA18DSI	NC <sup>(1)</sup>	//
VDDDSI	NC <sup>(1)</sup>	//
LVDS_*	NC <sup>(1)</sup>	no LVDS on STM32MP21x
VDDA18LVDS	NC <sup>(1)</sup>	//
VDDLVD	NC <sup>(1)</sup>	//

1. NC: Not connected inside the package.

2. In case of using the same board for STM32MP25x or STM32MP21x, it is not recommended to connect together STPMIC output for VDDCORE and VDDGPU from MP25 to supply all pins of STM32MP21x VDDCORE. Use 0Ω resistances to disconnect the STPMIC VDDGPU supply from the STM32MP21x VDDCORE pins and to connect the STPMIC VDDCORE supply to all STM32MP21 VDDCORE pins.

In addition, 21 GPIOs have been removed on STM32MP21x (see Table 8).

Below is the ballout delta between STM32MP25x and STM32MP21x.

- Yellow cells are updated with new signal names.
- Black cells are the 21 removed GPIOs that are NC.
- Grey cells are NC (not connected) due to features not available on STM32MP21x.

Figure 1. Ballout delta between STM32MP25x and STM32MP21x

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A		NC	NC	NC	NC	NC													
B		NC	NC	NC	NC	NC													
C				NC															
D																			
E																			
F	NC	NC	NC	NC															
G			NC	NC															
H			NC	NC															
J	NC	NC	NC	NC															
K																			
L																			
M																			
N																			
P																			
R																			
T																			
U																			
V																			
W																			

## 6 Boot mode selection

The STM32MP25x and STM32MP21x devices always start from an internal boot ROM. The internal boot ROM starts based on the boot pins and on the internal OTP fuses.

- Boot from external flash memory with default OTPs
  - SD card (SDMMC1)
  - eMMC (SDMMC2)
  - SLC-NAND (FMC)
  - Serial NOR or serial NAND flash memory
- Boot from UART or USB device
  - Used to access the device from the STM32CubeProgrammer (STM32CubeProg) to program the external flash memory or internal OTP fuses.

Default pins for the boot interface are the same for the STM32MP25x and STM32MP21x lines except for:

- No OCTOPI2 on STM32MP21x
- FMC\_D[15:8] is not available on the 8x8 package
- FMC\_D12 is remapped on the 10x10, 11x11, and 14x14 packages. Thus, it is not on the default GPIO.

**Table 9. Bootloader interface on STM32MP25x and STM32MP21x**

Interface	STM32MP25x pins	STM32MP21x pins
OCTOSPI_P1	OCTOSPI_P1_CLK PD0 OCTOSPI_P1_NCLK PD1 OCTOSPI_P1_DQS PD2 OCTOSPI_P1_NCS1 PD3 OCTOSPI_P1_IO0 PD4 OCTOSPI_P1_IO1 PD5 OCTOSPI_P1_IO2 PD6 OCTOSPI_P1_IO3 PD7 OCTOSPI_P1_IO4 PD8 OCTOSPI_P1_IO5 PD9 OCTOSPI_P1_IO6 PD10 OCTOSPI_P1_IO7 PD11	Same as STM32MP25x (OCTOSPI1_xx)
OCTOSPI_P2	OCTOSPI_P2_IO0 PB0 OCTOSPI_P2_IO1 PB1 OCTOSPI_P2_IO2 PB2 OCTOSPI_P2_IO3 PB3 OCTOSPI_P2_IO4 PB4 OCTOSPI_P2_IO5 PB5 OCTOSPI_P2_IO6 PB6 OCTOSPI_P2_IO7 PB7 OCTOSPI_P2_NCS1 PB8 OCTOSPI_P2_DQS PB9 OCTOSPI_P2_CLK PB10 OCTOSPI_P2_NCLK PB11	No OCTOSPI_P2
SDMMC1	SDMMC1_D0 PE4 SDMMC1_CK PE3 SDMMC1_CMD PE2	Same as STM32MP25x

Interface	STM32MP25x pins	STM32MP21x pins
SDMMC2	SDMMC2_D0 PE13 SDMMC2_CK PE14 SDMMC2_CMD PE15	Same as STM32MP25x <sup>(1)</sup>
UART4	UART4_TX PH7 UART4_RX PH8	It is not a boot source.
UART5	UART5_TX PA0 UART5_RX PB15	Same as STM32MP25x
USART2	USART2_TX PA4 USART2_RX PA8	Same as STM32MP25x
USART6	USART6_TX PF5 USART6_RX PF4	Same as STM32MP25x
USB	OTG_HSDM OTG_HSDM	Same as STM32MP25x
FMC	FMC_D0 PE9 FMC_D1 PE6 FMC_D2 PE7 FMC_D3 PD15 FMC_D4 PD14 FMC_D5 PB13 FMC_D6 PD12 FMC_D7 PB14 FMC_D8 PB5 FMC_D9 PB6 FMC_D10 PB7 FMC_D11 PD13 FMC_D12 PB8 FMC_D13 PB9 FMC_D14 PB11 FMC_D15 PB10 FMC_CLE PE11 FMC_NCE1 PE12 FMC_NWE PE14 FMC_ALE PE8 FMC_NOE PE15 FMC_RNB PE13	Same as STM32MP25x except: FMC_D12 on PB2 on 10x10, 11x11, 14x14 packages FMC_NWE on PD13 on 8x8 package: Only 8-bit interface

1. SDMMC2 is not a boot source for VFBGA225 8x8 package.

Refer to STM32 wiki articles below:

- [https://wiki.st.com/stm32mpu/wiki/Boot\\_chain\\_overview](https://wiki.st.com/stm32mpu/wiki/Boot_chain_overview)
- [https://wiki.st.com/stm32mpu/wiki/STM32\\_MPU\\_ROM\\_code\\_overview](https://wiki.st.com/stm32mpu/wiki/STM32_MPU_ROM_code_overview)

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## 7 Peripheral migration

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This section presents a full view of the features and peripheral counts of STM32MP25x and STM32MP21x lines. It also presents a peripheral address mapping snap shot for the concerned products.

## 7.1 Peripheral feature comparison

**Table 10. Peripheral comparison between STM32MP25x and STM32MP21x**

Product line		STM32MP257	STM32MP255	STM32MP253	STM32MP251	STM32MP215	STM32MP213	STM32MP211
CPU	Core	Cortex®-A35 FPU neon TrustZone®				Cortex®-A35 FPU neon TrustZone®		
	Multicore	Dual-core			Single-core		Single-core	
	Cache size	2 x 32 Kbytes			32 Kbytes		32 Kbytes	
		2 x 32 Kbytes			32 Kbytes		32 Kbytes	
	Frequency	Up to 1200 MHz				128-Kbyte level 2 cache		
	Overdrive mode	Up to 1500 MHz <sup>(1)</sup>				Up to 1500 MHz <sup>(1)</sup>		
GPU for 3D graphics	-	Vivante - Open GL ES 3.1 - Vulkan 1.1		-		-		
	Frequency	Up to 800 MHz		-		-		
	Overdrive mode	Up to 900 MHz <sup>(1)</sup>		-		-		
MCU	Core	Cortex®-M33 FPU TrustZone®				Cortex®-M33 FPU TrustZone®		
	Cache size	16-Kbyte data cache				16-Kbyte data cache		
		16-Kbyte instruction cache				16-Kbyte instruction cache		
Frequency	Up to 400 MHz				Up to 400 MHz			
Embedded SRAM	CPU system	256 Kbytes <sup>(2)</sup>		512 Kbytes		256 Kbytes		
	Video RAM	128 Kbytes (free for CPU system if video accelerators are not used)		-		-		
	NPU RAM	128 Kbytes <sup>(5)</sup>				-		
	MCU subsystem	256 Kbytes (128 Kbytes are tamper protected)				64 Kbytes (Tamper protected)		
	MCU retention	128 Kbytes				128 Kbytes		
	Backup	8 Kbytes (Tamper protected)				8 Kbytes (Tamper protected)		
SDRAM addressing space	LPDDR 16 bits	Up to 2 Gbytes (LPDDR4)				Up to 2 Gbytes (LPDDR4)		
	LPDDR 32 bits	Up to 2 Gbytes (LPDDR4) <sup>(6)</sup>				-		



Product line		STM32MP257	STM32MP255	STM32MP253	STM32MP251	STM32MP215	STM32MP213	STM32MP211
SDRAM addressing space	DDR 16 bits	Up to 2 Gbytes (DDR3L/DDR4)				Up to 2 Gbytes (DDR3L), up to 4 Gbytes (DDR4)		
	DDR 32 bits	(7)				-		
SDRAM frequency	LPDDR frequency	LPDDR4 up to 1200 MHz				LPDDR4 up to 800 MHz		
	DDR frequency	DDR3L up to 1066 MHz DDR4 up to 1200 MHz				DDR3L up to 1066 MHz, DDR4 up to 800 MHz		
	On-the-fly encryption/decryption	Yes (7)				Yes + AES-256 with SCA protection encode/decode (7)		
Backup registers		512 bytes (128x32 bits, tamper protected)				512 bytes (128x32 bits, tamper protected)		
Timers	General-purpose 16 bits	8 x 16 bits + 4 x 32 bits				8 x 16 bits + 4 x 32-bits (8)		
	Advanced-control	3				2		
	Basic	2				2		
	Low power	5				5 (9)		
Watchdog		7 (5 x independent, 2 x window)				5 (4 x independent, 1 x window)		
Communication interfaces	SPI/I <sup>2</sup> S	8/3 (full duplex)				6/3 (full duplex)		
	I <sup>2</sup> C	8				3		
	I3C	-				3		
	USART + (LP)UART	4 + 5				4 + 4 (10)		
	SAI	4				4 (11)		
	USB host	USB 2.0 host (USBH), 1 port, embedded Hi-Speed, and super-speed 5 Gbps PHY				USB 2.0 host (USBH), 2 ports, embedded Hi-Speed PHY (12)		
	USB OTG	USB 2.0/3.0 dual role (USB3DR), embedded Hi-Speed, and super-speed 5 Gbps PHY				USB 2.0 host/device (OTG), 1 port, embedded Hi-Speed PHY (shared with USBH port 2)		
	SPDIFRX	4 inputs				4 inputs		
	FDCAN	3 (1 x TT-FDCAN), 10 Kbytes shared buffer			-	2 (1 x TT-FDCAN), 10 Kbytes shared buffer		-
SDMMC (SD, SDIO, eMMC)		3 (8 + 8 + 4 bits)				3 (8 + 8 + 4 bits)(13)		
Serial-flash		2 x OCTOSPI				1 x OCTOSPI		



Product line		STM32MP257	STM32MP255	STM32MP253	STM32MP251	STM32MP215	STM32MP213	STM32MP211
-	On-the-fly decryption	Yes <sup>(7)</sup>				Yes <sup>(7)</sup>		
FMC memory controller	PSRAM	4 x CS, up to 4 x 64 Mbytes				4 x CS, up to 4 x 64 Mbytes <sup>(14)</sup>		
	NAND	4 x CS, SLC, BCH4/8				1 x CS, SLC, BCH4/8		
Ethernet		3 ports, R(G)MII, MII	2 ports, R(G)MII, MII	1 port, R(G)MII, MIIP	2 ports, R(G)MII, MII		1 port, R(G)MII, MII	
		TSN switch with 2 external ports	-		-			
LCD-TFT parallel interface		Up to 24 bits, 150 MHz pixel clock (up to 1080p60) Rotation, 3 layers (including 1 secure)				Up to 24 bits, 150 MHz pixel clock (up to 1080p60), no rotation, 2 layers (including 1 secure)	-	-
Display serial interface (DSI)		4 x data lanes 2.5 Gbps each (up to 1536p60)				-		
LVDS display		Dual-link of 4 x data lanes 1.1 Gbps each (up to 1536p60) <sup>(15)</sup>		-		-		
DMA		3 instances, 48 physical channels in total				3 instances (1 secure), 48 physical channels in total		
Cryptography		DES/TDES, AES-256, PKA <sup>(7)</sup>				DES/TDES, AES-256, PKA <sup>(7)</sup>		
Hash		SHA-1, SHA-2, and SHA-3 (up to 512), MD5, HMAC				SHA-1, SHA-2, and SHA-3 (up to 512), MD5, HMAC		
True random number generator		Yes				Yes		
Fuses (one-time programmable)		12288 effective bits				12288 effective bits		
Camera interface	Parallel	Up to 16 bits, up to 120 MHz Path shared with CSI				Up to 16 bits, up to 120 MHz, path shared with CSI		
	CSI-2	2 x data lanes 2.5 Gbps each Path shared with DCMIPP				2 x data lanes 2.5 Gbps each, path shared with DCMIPP <sup>(16)</sup>	-	
	ISP	Yes, basic ISP				Yes, basic ISP		
Multifunction digital filter (MDF)		4 input channels with 4 filters and sound activity detection				4 input channels with 4 filters and sound activity detection		
Audio digital filter (ADF)		1 input channel with 1 filter and sound activity detection				-		



Product line	STM32MP257	STM32MP255	STM32MP253	STM32MP251	STM32MP215	STM32MP213	STM32MP211
ADC	3 x 12-bit ADC				2 x 12-bit ADC		
Number of ADC channels	22/24 <sup>(17)</sup>				24 <sup>(18)</sup>		
Number of tamper pins	up to 16 pins (8 outputs /8 inputs)				up to 12 pins (5 outputs/7 inputs)		
Operating voltage	1.71 to 1.98 V or 3 to 3.6 V				1.71 to 1.98 V or 3 to 3.6 V		
Junction temperature	-40 to 125 °C				-40 to 125 °C		

1. Only for STM32MP2xxD or STM32MP2xxF.
2. Additional 128 Kbytes if video RAM is not used.
3. Additional 128 Kbytes if video RAM is not used, additional 128 Kbytes if NPU RAM is not used.
4. Free for CPU if video RAM is not used (Video decoder statically disabled).
5. Free for CPU if NPU RAM is not used (NPU statically disabled).
6. Not applicable on the VFBGA361 10x10 mm package.
7. Only for STM32MP2xxC or STM32MP2xxF.
8. No TIM16/17 in 8x8 mm package.
9. No LPTIM3/4/5 on 8x8 mm package.
10. No LPUART1 on 8x8 package.
11. SAI4\_D1 missing in 8x8 mm package.
12. No USBHS on 8x8 mm package (only USB\_OTG host/device).
13. SDMMC2 only 4 bits and SDMMC3 without external level shifter control on 8x8 package.
14. Only 8-bit nand and no FMC nor multiplexing on 8x8 mm packages.
15. Except with the VFBGA361 10x10 mm package: single-link of 4 x data lanes 1.1 Gbps each (up to 1050p60).
16. No CSI on 8x8 mm package.
17. 24 channels on VFBGA436 18x18 mm package, 22 channels on other packages.
18. 22 channels on 8x8 mm package (no ANA0/ANA1 pins)



## 7.2 Memory mapping

The peripheral address mapping is very similar between STM32MP21x lines and STM32MP25x lines. Find below an extract of STM32MP25x and STM32MP21x line memory maps. More details can be found in the respective device reference manual.

Figure 2. STM32MP255 memory map

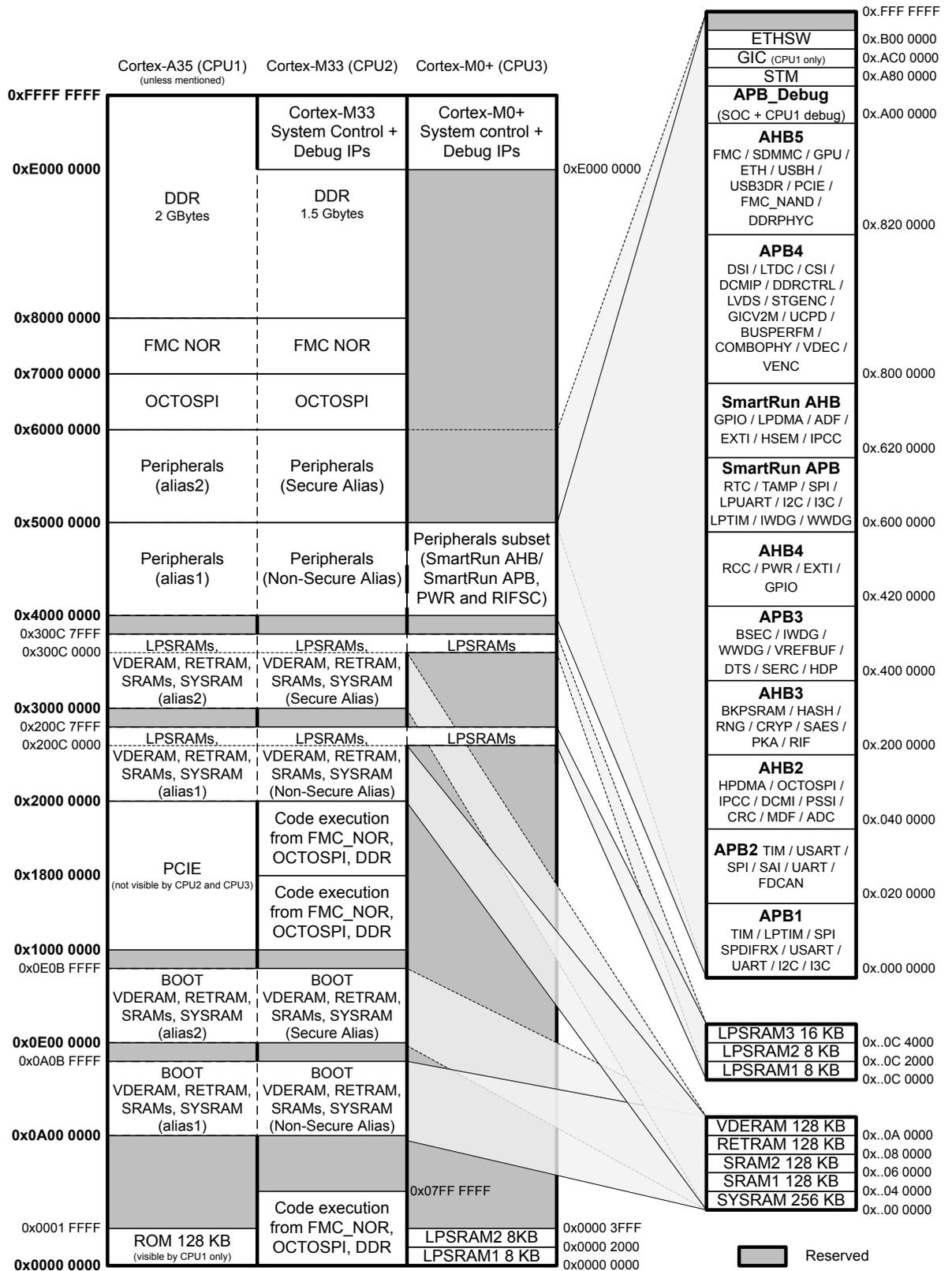
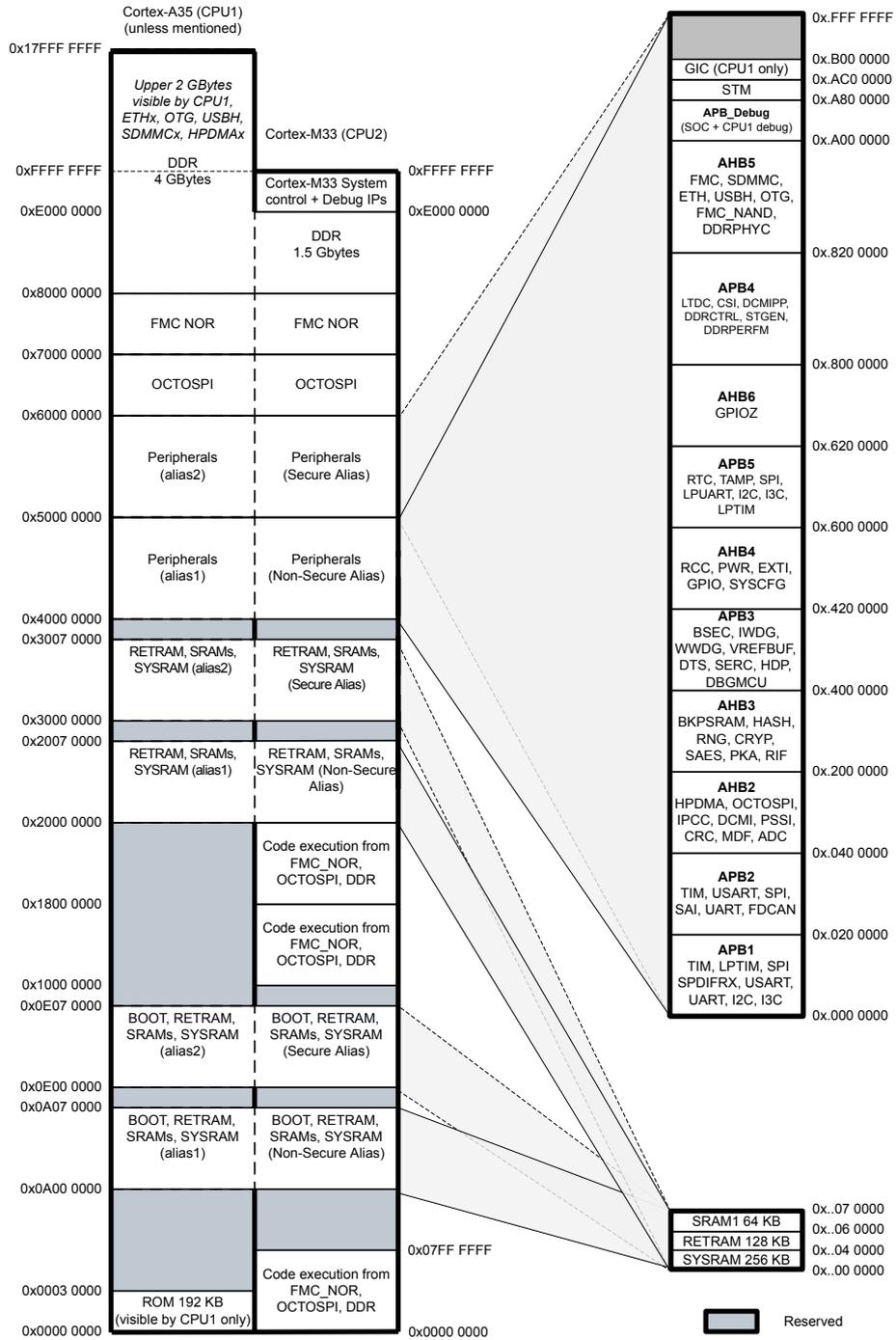


Figure 3. STM32MP215 memory map



DT73107V2

## 8 Application migration strategy

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### 8.1 MPU embedded software: STM32MP21x versus STM32MP25x

STM32MP25x and STM32MP21x platforms are supported by the same MPU embedded software delivery, which automatically adapts the compilation chain and the selected software components according to the machine selection.

### 8.2 Linux application migration

STM32MP21x devices and STM32MP25x devices use the same OpenSTLinux Distribution configured in the Armv8-A 64-bit architecture. The same application can be used on both platforms.

Nevertheless, it is recommended to recompile applications in the STM32MP21x build environment if the Linux kernel and associated distribution parameters have been changed compared to STM32MP25x ones.

### 8.3 MCU application migration

A customer can easily port its STM32MP25x Cortex<sup>®</sup>-M33 application on STM32MP21x Cortex<sup>®</sup>-M33 thanks to STM32CubeMX and STM32CubeIDE tools.

Indeed, STM32CubeMX is adapting the peripheral list according to the selected platform and generating an associated cube project for STM32CubeIDE with peripheral initialization sequence.

## Revision history

**Table 11. Document revision history**

Date	Revision	Changes
05-Sep-2025	1	Initial release.

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