AN6055

Application note

Getting started with STM32MP21x MPU hardware development

Introduction

This application note shows how to use the STM32MP21x MPUs. It describes the minimum hardware resources required to develop an application based on these products.

This document provides an overview of the hardware implementation of the development board, with focus on features like:

- Power supply
- Package selection
- Clock management
- Reset control
- Boot mode settings
- Debug management

Reference design schematics are also included in this application note. They show a description of the main components, interfaces, and modes.

Table 1. **Applicable products**

Type	Products
STM32MP21x	STM32MP211, STM32MP213, STM32MP215

1 General information

This document applies to the STM32MP21x lines MPUs, based on a Cortex® Arm® core with the CoreSight™ debug technology.

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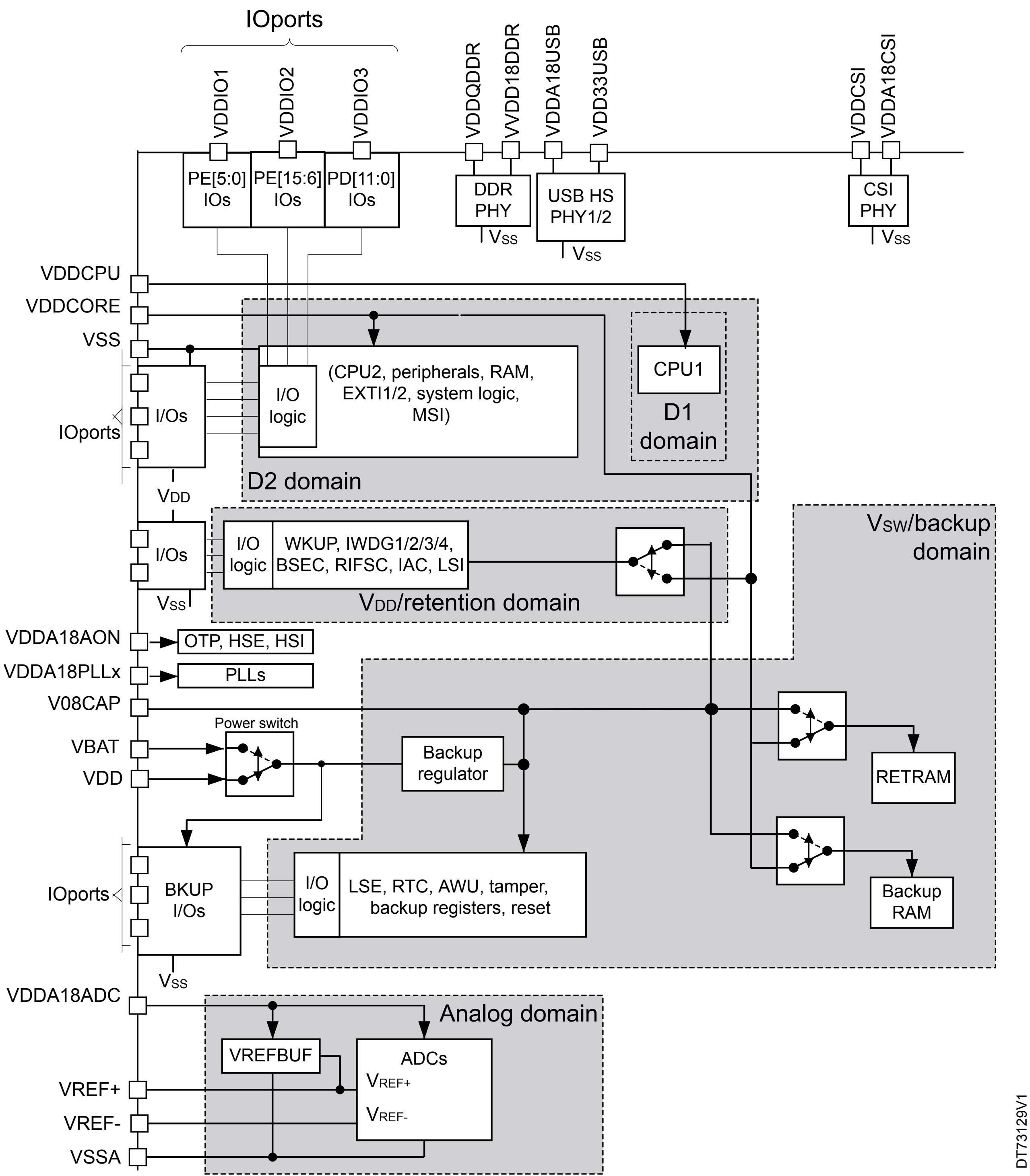
Table 2. Reference documents

N°	Reference	Title
[1]	AN2867	Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs
[2]	AN1709	EMC design guide for STM8, STM32 and legacy MCUs
[3]	AN5275	Introduction to USB DFU/USART protocols used in STM32MP1 and STM32MP2 MPU bootloaders
[4]	AN5723	Guidelines for DDR configuration on STM32MP2 MPUs
[5]	AN5724	Guidelines for DDR memory routing on STM32MP2 MPUs
[6]	AN5727	How to use STPMIC2x for a wall adapter-powered application on STM32MP25 MPUs
[7]	UMxxxx	Discovery kits with STM32MP215 MPUs
[8]	RM0506	STM32MP21x advanced Arm®-based 32/64-bit MPUs
[9]	DS14557	STM32MP21x A/D datasheet
[10]	DS14556	STM32MP21x C/F datasheet
[11]	AN4879	Introduction to USB hardware and PCB guidelines using STM32 MCUs

2 Power supplies

Figure 1. Power supply scheme



2.1 Overview

Note: See details and guaranteed operating points in the product datasheets.
Values in this section are for information only.

- The main I/Os voltage supply (V_{DD}) range is either 1.8 V or 3.3 V typ. There are as well dedicated independent I/Os supplies for some interfaces (V_{DDIO1}, V_{DDIO2}, and V_{DDIO3}).
- There are multiple analog and digital logic voltage supplies, see Section 2.2: Power supply schemes for details.
- The real-time clock (*RTC*) and backup registers can be powered from the V_{BAT} voltage when the main V_{DD} supply is powered off. This internal supply with automatic switch between V_{BAT} and V_{DD} is named V_{SW} supply voltage and is also used to supply PI8, PC13, PZ0, PZ1, PZ3 pins, and, only for TAMP_IN usage, the PC3, PC4, PC5, PF6, PF7, PG1, and PG3 pins.
  V_{BAT} voltage is typically 3 V when used with a coin-cell battery.

2.1.1 Independent ADC supply and reference voltage

To make sure that the conversion of signals is more accurate and can cover a wider range of values, the *ADC* (analog-to-digital converter) and reference have their own power supply that can be filtered separately. This helps to protect them from any interference or noise that may be present on the printed circuit board (*PCB*).

The analog operating voltage supply ($V_{DDA18ADC}$) is 1.8 V typ.

- The *ADC*/*VREFBUF* voltage supply input is available on a separate VDDA18ADC pin.
- An isolated supply ground connection is provided on the VSSA pin.
  In all cases, the VSSA pin must be externally connected to the same supply ground as the V_{SS}.

Warning: *The ADC_INx I/Os must not exceed VDDA18ADC + 0.3 V as specified in the product datasheet.*

External VREF

The user can connect a separate external reference voltage *ADC* input on VREF+. The voltage on VREF+ may range from 1.10 V to $V_{DDA18ADC}$.

Internal VREF

The user can enable in the *VREFBUF* block an internal reference voltage on VREF+.

The voltage on VREF+ can be either 1.21 V or 1.5 V.

The VREF+ pin has an internal reference voltage (VREF) that can be used externally, such as for an analog comparator reference. However, it is important to make sure that the amount of electrical current being used stays within the values specified in the datasheet.

Caution: *When available (depending on package), VREF- must be externally tied to V_{SSA}.*

2.1.2 Battery backup

To retain the content of the backup registers, *BKPSRAM* and *RETRAM*, when V_{DD} is turned off, the VBAT pin can be connected to an optional standby voltage supplied by a battery or another source.

The VBAT pin also powers the *RTC* unit, allowing the *RTC* to operate even when the main digital supply (V_{DD}) is turned off. The switch to the V_{BAT} supply is controlled by the power down reset (*PDR*) circuitry embedded in the *PWR*.

If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}.

2.2 Power supply schemes

Note: See the details and guaranteed operating points in the product datasheets. The values in this section are for information only.

The device is powered by multiple power supplies. Those supplies must be connected to external decoupling capacitors (see Table 3).

I/O supplies

- The V_{DD} is the main supply for I/Os and an internal part, kept powered during the standby mode
  - The voltage range is either 1.8 V or 3.3 V typ.
  - V_{DD} must be present whenever other I/Os supplies are present (except V_{BAT}, which is independent and $V_{DDA18AON}$, which is always present).
- V_{DDIO1}, V_{DDIO2}, and V_{DDIO3} are separate/dedicated I/Os supplies
  - Voltage values are either 1.8 V, 3.0 V, or 3.3 V typ.
  - Each of those supplies can have a different voltage or be shut down independently.
- The VBAT pin can be connected to the external battery
  - The voltage range is 2.3 V to 3.6 V (except when connected to V_{DD}).
  - If the application does not support a backup battery, it is recommended to connect this pin to V_{DD}.
  - If the application supports a backup battery, it is required to add a 2.2 µF capacitor and a resistor. (This is to limit the voltage slew rate when a backup battery is plugged, as explained in Table 3 note 2).
- V_{DDQDDR} is the *DDR* I/O supply
  - The voltage range is 1.283 V to 1.45 V for interfacing DDR3L memories (1.35 V typ.).
  - The voltage range is 1.14 V to 1.26 V for interfacing DDR4 memories (1.2 V typ.).
  - The voltage range is 1.06 V to 1.17 V for interfacing LPDDR4 memories (1.1 V typ.).

Digital logic supplies

- V_{DDCPU} digital CPU domain supply (Arm® Cortex®-A35)
  - It can be shut down during the Run2, Stop2, LP-Stop2, LPLV-Stop2, or Standby mode (using the PWR_CPU_ON signal).
  - The voltage range during run mode is 0.8 V typ. (0.91 V typ in overdrive [(1)])
  - V_{DDCPU} is only present if V_{DD} is already present, as it is dependent on the V_{DD} supply.
  - V_{DDCPU} can be further reduced in specific Stop modes (LP-Stop1 or LPLV-Stop1). This involves either the PWR_ON (for example with the *PMIC*, an external power management IC) or PWR_LP signal.
- The V_{DDCORE} is the main digital voltage
  - V_{DDCSI} must usually be connected to V_{DDCORE}.
  - It can be shut down during the Standby mode (using a PWR_ON signal).
  - The voltage range during run mode is 0.82 V typical.
  - V_{DDCORE} is dependent on the V_{DD} supply, so it is necessary for V_{DD} to be present before V_{DDCORE}.
  - V_{DDCORE} can be further reduced in a specific stop mode (LPLV-Stop1 or LPLV-Stop2). This involves either PWR_ON (for example with the STPMIC, an external power management IC) or PWR_LP signal.

1. Overdrive is only available on some part references. Overdrive affects the maximum Tj and reliability data.

1.8 V analog supplies

- $V_{DDA18AON}$ power supply input for system analogs such as reset, power management, oscillators, and *OTP*, kept powered during the standby mode
  - The voltage range is 1.8 V typ.
- The VDDA18ADC pin is the analog (*ADC*/*VREFBUF*) supply.
  - The voltage range is 1.8 V typ.
  - Additional precautions can be taken to filter analog noise. $V_{DDA18ADC}$ can be connected to a shared 1.8 V supply through an inductor-based filter.
  - The VREF+ pin can be connected to the $V_{DDA18ADC}$ external power supply. If a separate, internal, or external reference voltage is applied to VREF+, a decoupling capacitor must be connected between this pin and VREF- (see Table 3).
    Refer to Section 2.1.1: Independent ADC supply and reference voltage.

The following supplies can be connected to a same source with independent decoupling whenever possible.

- The voltage range is 1.8 V typ.
- The VDDA18PLL1 and VDDA18PLL2 pins are the analog supply for *PLL*s.
- The VDDA18DDR pin is the analog supply for *DDR PHY*.
- The VDDA18CSI pin is the analog supply for *CSI*.
- The VDDA18USB pin is the analog supply for the *USB* HS *PHY*.

3.3 V USB supplies

They must be connected on a same source with independent decoupling whenever possible:

- The voltage range is 3.3 V typ.
- $V_{DD33USB}$ is the *USB* high-speed *PHY* supply.

Caution: *All supply grounds (V_{SS}, V_{SSA}, V_{SSAON}, and V_{REF-}) must be all connected to power planes.*

The following table must be used as a guideline only. The real count and values of the capacitors can be adapted depending on various parameters such as the capacitor size and dielectric, the *PCB* technology, and the product power integrity simulations.

The information in this table does not include capacitors on the supply sources (such as *LDO* or *SMPS*) or external devices (such as *DDR* memory, *SD* card, or *eMMC*, flash memories).

Table 3. Amount of decoupling recommendation by package

This table must be used as a guideline only. The real count and values of capacitors can be adapted depending on various parameters: capacitor size and dielectric, PCB technology, product power integrity simulations, and so on.
The information in this table does not include capacitors on the supply sources (such as LDO or SMPS) or external devices (such as DDR memory, SD card, e.MMC, flash memories, and so on.)

Supply pins	Decoupling point (1)	Value	VFBGA225 (8 × 8)	VFBGA273 (11 × 11)	TFBGA289 (14 × 14)	VFBGA361 (10 × 10)	Comments
VBAT	VSS	2.2 µF (2)(3)	1	1	1	1	Decoupling could be skipped if $V_{BAT} = V_{DD}$
V08CAP	VSS	4.7 µF (2)	1	1	1	1	Internal backup regulator decoupling
VDDCORE	VSS	1 µF (2)	4	4	4	4	-
VDDCSI	VSS	100 nF	1	1	1	1	Supplies must be connected to VDDCORE.
VDDCPU	VSS	1 µF (2)	4	4	4	4	-
VDDQDDR	VSS	1 µF (2)	4	4	4	4	-
VDDA18AON	VSSAON	100 nF	1	1	1	1	-

Supply pins	Decoupling point (1)	Value	VFBGA225 (8 × 8)	VFBGA273 (11 × 11)	TFBGA289 (14 × 14)	VFBGA361 (10 × 10)	Comments
VDDA18PLL1/2, VDDA18DDR, VDDA18USB, VDDA18CSI	VSS	100 nF	5	5	5	5	Supplies must be connected all together.
VDD	VSS	1 µF (2)	3	3	3	3	-
VDDIO1 (4)	VSS	100 nF	1	1	1	1	Usually for *SD* card
VDDIO2 (4)	VSS	100 nF	1	1	1	1	Usually for e.MMC
VDDIO3 (4)	VSS	100 nF	1	1	1	1	Usually for OCTOSPI1
VDD33USB	VSS	100 nF	1	1	1	1	-
VDDA18ADC	VSSA	2.2 µF (2)	1	1	1	1	VSSA must be connected to VSS plane
		100 nF	1	1	1	1	
VREF+	VREF - and VSSA	1 µF (2)	1	1	1	1	VREF- must be connected to VSSA then VSS plane (chained connection)
		100 nF	1	1	1	1	

1. *All VSSx and VSSA must be connected to a common VSS plane.*
2. *Multilayer ceramic capacitor type (MLCC)*
3. *Fulfilling a minimum rise time defined in the datasheet might require a resistor of a few ohms to be connected in series. The total RC must be at least equal to Tr * battery voltage. (For example, RC = 60 µs for Tr = 20 µs/V and a 3 V battery. This could be ensured by a 20 Ω resistor in series for a CR2032 battery type with an internal resistance of a minimum of 8 or 9 Ω). The rise time limitation can also be ensured by a ferrite bead and a capacitor.*
4. *Must be connected to V_{DD} if not used for a dedicated interface supply.*

Note: See package feature details in Section 3.1: Package selection. Not all I/Os are supplied by V_{DD}. See below in Table 4 the summary of the related supplies.

Table 4. I/O power domains

Supply pin	Pin names
VDD	NRSTC1MS, PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PA8, PA9, PA10, PA11, PA12, PA13, PA14, PA15, PB1, PB2, PB3, PB5, PB6, PB7, PB9, PB10, PB11, PB12, PB13, PB14, PB15, PC0, PC1, PC2, PC6, PC7, PC8, PC9, PC10, PC11, PC12, PD12, PD13, PD14, PD15, PF0, PF1 ,PF2, PF3, PF4, PF5, PF8, PF9, PF10, PF11, PF12, PF13, PF15, PG0, PG2, PG4, PG5, PG7, PG8, PG9, PG10, PG11, PG12, PG13, PG14, PG15, PH4, PH5, PH7, PH8, PH9, PH10, PH11, PH12, PH13, PI0, PI1, PI4, PI5, PI6
VDDIO1 (1)	PE0, PE1, PE2, PE3, PE4, PE5
VDDIO2 (2)	PE10, PE11, PE12, PE13, PE14, PE15, PE6, PE7, PE8, PE9
VDDIO3 (3)	PD0, PD1, PD10, PD11, PD2, PD3, PD4, PD5, PD6, PD7, PD8, PD9
VDDA18AON	OSC_IN, OSC_OUT, PDR_ON
VSW (4)	OSC32_IN, OSC32_OUT, PC13, PI8, PZ0, PZ1, PZ3
VDD/VSW(4) (5)	PC3, PC4, PC5, PF6, PF7, PG1, PG3

1. *Usually used for SD cards using SDMMC1.*
2. *Usually used for eMMC or SD card using SDMMC2. On the VFBGA225 8 × 8 package, SDMMC2 is not a boot source.*
3. *Usually used for OCTOSPI1*
4. *VSW is supplied by VBAT in the absence of VDD.*
5. *Pins with two supplies; V_{SW} supply for enabled TAMP_INx additional function, V_{DD} supply for GPIO and other alternate function*

Note: The I/O power domain table does not include analog cells, which have one or more dedicated supplies (such as PHYs).

Table 5. **Supply usage for unused features**

Supply pin	Usual connection	Supply option if not used (1)	Pins or functions	Signals connection if not used	Related block
VDDCSI	V_{DDCORE}	V_{SS}	CSI_xxx pins	All open or all V_{SS}	*CSI*
VDDA18CSI	Global 1.8 V analog supply	V_{SS}			
VDDA18USB	Global 1.8 V analog supply	V_{SS}	USBH_HS_DP/DM pins and USB-OTG_DP/DM pins	All DP/DM to V_{SS}. All TXRTUNE open	*USBH* or *USB-OTG*
VDD33USB	Dedicated 3.3 V supply	V_{SS}			
VDDA18ADC	Dedicated 1.8 V supply or filtered global 1.8 V analog supply	V_{SSA}	*ADC* (internal and external channels)	-	ADC1 or ADC2
	-	-	ANA0/ANA1	V_{SSA}	-
			VREF+ pin	V_{SSA}	
			VREFBUF usage	-	*VREFBUF*

1. *Connection possible only when all related pins/functions are not used.*

2.3 Specific I/O constrains related to voltage settings

V_{DDIO1}, V_{DDIO2}, and V_{DDIO3} have specific register settings and control sequences to be respected when used at 3 V/3.3 V or 1.8 V typ. Refer to the *PWR* section in the product reference manual for details.

See also I/O speed settings for constrains on I/O speed settings for V_{DD}, V_{DDIO1}, V_{DDIO2}, and V_{DDIO3} domains.

2.4 Reset and power supply supervisor

2.4.1 Power-on reset (POR)/power-down reset (PDR)

The device has an integrated POR/PDR circuitry that allows proper operation starting from 1.71 V.

The device remains in the Reset mode as long as V_{DD} and $V_{DD18AON}$ are below a specified threshold, and $V_{POR/PDR}$ is without the need for an external reset circuit. For more details concerning the power on/power down reset threshold, refer to the electrical characteristics in the product datasheets.

2.4.2 vddcore_ok reset

The system has an integrated circuitry that allows proper startup operation of the V_{DDCORE} (D2) domain.

The V_{DDCORE} domain remains in Reset mode when V_{DDCORE} is below the operation threshold vddcore_ok. Once the V_{DDCORE} supply level is above the operation threshold vddcore_ok, the V_{DDCORE} domain is taken out of reset. When the LVDS_D2 bit is set, the V_{DDCORE} supply level can be lowered in LPLV-Stop1 or LPLV-Stop2 modes.

For more details concerning the vddcore_ok reset threshold, refer to the electrical characteristics of the datasheet.

2.4.3 Specific I/O constrains related to voltage settings

V_{DDIO1}, V_{DDIO2}, and V_{DDIO3} have specific register settings and control sequences to be respected when used at 3 V/3.3 V or 1.8 V typ. Refer to the *PWR* section in the product reference manual for details.

See also I/O speed settings for constrains on I/O speed settings for V_{DD}, V_{DDIO1}, V_{DDIO2}, and V_{DDIO3} domains.

2.4.4 vddcpu_ok reset

The system has an integrated circuitry that allows proper startup operation of the V_{DDCPU} (D1) domain.

The V_{DDCPU} domain remains in Reset mode when V_{DDCPU} is below the operation threshold vddcpu_ok. Once the V_{DDCPU} supply level is above the operation threshold vddcpu_ok, the V_{DDCPU} domain is taken out of reset. When the LVDS_D1 bit is set, the V_{DDCPU} supply level can be lowered in LPLV-Stop1 or LPLV-Stop2 mode. For more details concerning the vddcpu_ok reset threshold, refer to the electrical characteristics of the datasheet.

2.4.5 VDD18ADC monitoring mandatory before using the ADC

After boot, it is mandatory to monitor VDD18ADC before using the analog-to-digital converter (*ADC*).

Refer to [8], "Power control (*PWR*)" chapter, "Peripheral voltage monitoring (PVM)" section, for the sequence to use.

2.4.6 VDDCORE and VDDCPU monitoring

The system can monitor V_{DDCORE} and V_{DDCPU} through the use of the ADC2 watchdog if programmed accordingly. The ADC2 watchdogs are connected to the internal tampers. If enabled, they rise a tamper detection when V_{DDCORE} or V_{DDCPU} are outside the ADC2 watchdog-programmed range.

2.4.7 Programmable voltage detector (*PVD*)

The user can monitor the voltage level of the PVD_IN pin using the programmable voltage detector (*PVD*). This can be achieved by comparing the voltage of the PVD_IN pin to the internal V_{REFINT} (Internal voltage reference) level.

The *PVD* is enabled by setting the PVDE bit in the PWR_CR3 register.

A PVDO flag is available to indicate whether the PVD_IN pin is higher or lower than the threshold. This event is internally connected to EXTI1 and can generate an interrupt if enabled through the EXTI1 registers. The *PVD* output interrupt can be generated when PVD_IN drops below the *PVD* threshold. It can also happen when PVD_IN rises above the *PVD* threshold depending on the *EXTI* line rising or falling edge configuration. As an example, the service routine can perform emergency shutdown tasks.

2.4.8 Peripheral voltage monitoring (PVM)

Only V_{DD} and $V_{DDA18AON}$ are monitored by default, as they are the only supplies required for all system-related functions. The other I/O supplies (V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, $V_{DD33USB}$, and $V_{DDA18ADC}$) can be independent from V_{DD} and can be monitored with peripheral voltage monitoring (*PVM*).

A GPVMO flag is available, in the *PWR* control register 1 (PWR_CR1), to indicate if all enabled independent power supplies are higher or lower than the *PVM* threshold. This event is internally connected to the EXTI1 and can generate an interrupt if enabled through the EXTI1 registers. The GPVMO interrupt can occur in two situations: when all independent power supplies that are enabled increase above the *PVM* threshold, or when at least one enabled independent power supply decreases below the *PVM* threshold. The specific situation depends on how the EXTI1 line rising/falling edge configuration is set up. The *PVM* is not available in Standby mode.

The independent supplies (V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, $V_{DD33USB}$, and $V_{DDA18ADC}$) are not considered as present by default, and logical and electrical isolation is applied to ignore any information coming from the peripherals supplied by these dedicated supplies.

- If the independent power supplies are connected to V_{DD} externally, the application must assume that they are available without requiring any peripheral voltage monitoring to be enabled. To remove the power isolation, the corresponding supply valid bits can be set.
- If these supplies are independent from V_{DD}, the peripheral voltage monitoring (PVM) can be enabled to confirm whether the supply is present or not.

2.4.9 Backup regulator voltage thresholds

The backup regulator voltage (V_{08CAP}) can be monitored by comparing it with two threshold levels.

Two flags are available in the PWR control register 2 (PWR_CR2) to indicate if V_{08CAP} is higher or lower than the threshold. Enabling or disabling the monitoring process can be done by using the MONEN bit in the PWR control register 2 (PWR_CR2). As an example, the levels can be used to trigger a routine to perform emergency saving tasks. The monitoring, when enabled, is also available in Standby and V_{BAT} modes. The flags are available on tamper signals.

2.4.10 Application and system resets

An application reset (app_rst) is generated from one of the following sources:

- A reset from NRST pad
- A reset from a *POR*/*PDR* signal (generally called power-on reset)
- A reset from BOR signal (generally called brownout)
- A reset from one of the independent watchdogs (*IWDG*)
- A software reset from the *RCC*
- A failure on *HSE*, when the clock security system feature is activated
- A *RETRAM CRC* error reset
- A *RETRAM ECC* failure reset

A system reset (sys_rstn) is generated from one of the following sources:

- A reset from app_rstn signal (application reset)
- A reset from vcore_rstn signal
- A reset from vcpu_rstn signal when the D1 domain does not exit from Standby

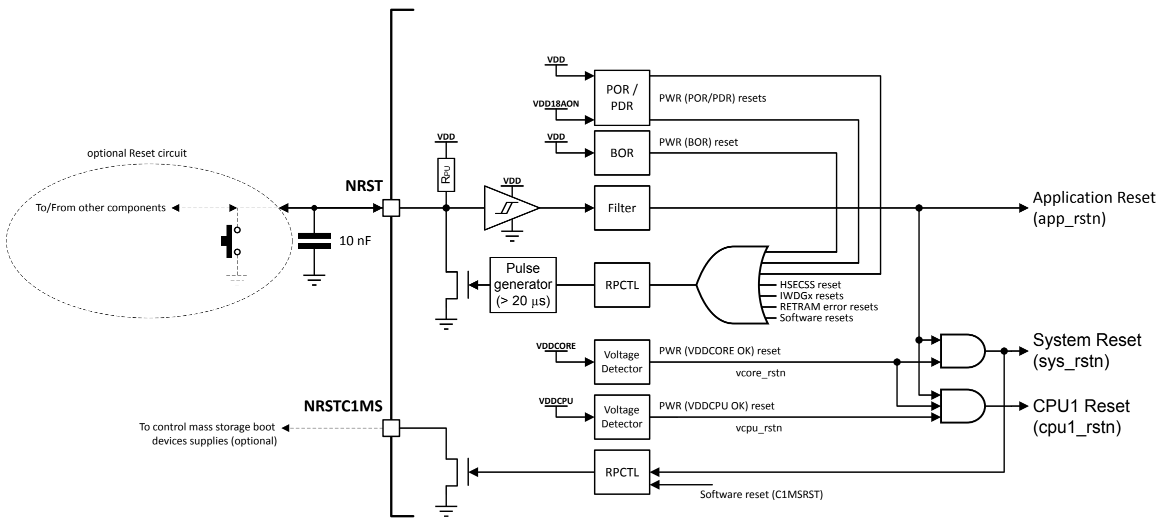
Note: *When the system is in Standby, the V_{DDCORE} and V_{DDCPU} are switched off, but V_{DD} and $V_{DD18AON}$ are still present. So when the system exits from Standby, the vcore_rst signal is activated, generating a nreset reset.*

NRST pin is also activated when app_rstn is internally generated and low-level duration could be adapted using RPCTL.

The NRSTC1MS pin is activated when sys_rstn is generated. The NRSTC1MS pin can be utilized to manage the power supply of external flash memory that is necessary for the initial boot of CPU1. This external flash memory may require a power cycle to ensure a platform reboot, such as in the case of an *SD* card. Low-level duration can be adapted using RPCTL.

For additional information on reset coverage and configuration, consult the *RCC* section of the product reference manual.

Figure 2. Simplified reset pin circuit



1. *This is a very simplified view that provides only an overview of the reset flows. It does not include all details. Details and specific behaviors are described in the product reference manual.*

3 Packages

3.1 Package selection

The package must be selected by taking into account the constraints that are strongly dependent upon the application.

The list below summarizes the more frequent constraints:

- Number of interfaces required
  Some interfaces might not be available on some packages.
  Some interfaces combinations might not be possible on some packages.
  Refer to product datasheets for details.
- *PCB* technology constraints
  Small pitch and high ball density can require more *PCB* layers and a higher *PCB* class requiring stack-up with the microvia (laser via) technology.
- Package height
- *PCB* available area
- Thermal constraints
  Larger packages have better thermal dissipation capabilities.

Table 6. Package availability summary

Size (mm)(1)	8 × 8	10 × 10	11 × 11	14 × 14
Pitch (mm)	0.5	0.5	0.5	0.8
Thickness (mm)	1.0	1.0	1.0	1.2
Sales number	VFBGA225	VFBGA361	VFBGA273	TFBGA289
STM32MP211x	STM32MP211xAO	STM32MP211xAL	STM32MP211xAN	STM32MP211xAM
STM32MP213x	STM32MP213xAO	STM32MP213xAL	STM32MP213xAN	STM32MP213xAM
STM32MP215x	STM32MP215xAO	STM32MP215xAL	STM32MP215xAN	STM32MP215xAM

1. *Typical body size*

Note: Refer to the product datasheets on st.com for an up-to-date reference availability.

Table 7. **STM32MP21xx differences per package**

Features		STM32MP21xxAO	STM32MP21xxAN	STM32MP21xxAM	STM32MP21xxAL
		VFBGA225	VFBGA273	TFBGA289	VFBGA361
Packages	Body size (mm)	8 × 8	11 × 11	14 × 14	10 × 10
	Pitch (mm)	0.5	0.5	0.8	0.5
	Thickness (mm)	xxx	xxx	xxx	xxx
	Ball count	225	273	289	361
GPIO	**With interrupt (total count)**	**98**	**123**	**123**	**123**
Limitations per package	*CSI*	no	yes	yes	yes
	FMC	8-bit, no *FMC* NOR	16-bit with D12 remapped	16-bit with D12 remapped	16-bit with D12 remapped(1)
	ANA0/ANA1	no	yes	yes	yes
	Tamper (in/out)	7/1	7/5	7/5	7/5
	Wake-up pins	5	6	6	6
	RTC_OUT	Only RTC1	x2	x2	x2
	LPUART1	No	Yes	Yes	Yes
	SPI2/I2S2	Yes, with signal remapped.	Yes	Yes	Yes
	TIM16/17	No	Yes	Yes	Yes
	LPTIM3/4/5	No	Yes	Yes	Yes
	SDMMC2	4-bit No external level shifter control. Signal CK remapped. *SDMMC2* not a boot source.	full	full	full
	SDMMC3	No external level shifter control.	full	full	full
	SAI4	Missing D1 (PDM)	full	full	full
	TRACED	Missing TRACED [13, 12, 11, 8]	full	full	full

1. *FMC 8-bit compatible with the STM32MP21x 10 × 10 package.*

3.2 Alternate function mapping to pins

Generally, for each used interface, it is recommended to keep ball choices together as close as possible to ease *PCB* routing and to avoid potential timing issues.

In addition, to fulfill timings, *I3C* signals like *SDA*/*SCL* pairs must be chosen thanks to Table 8.

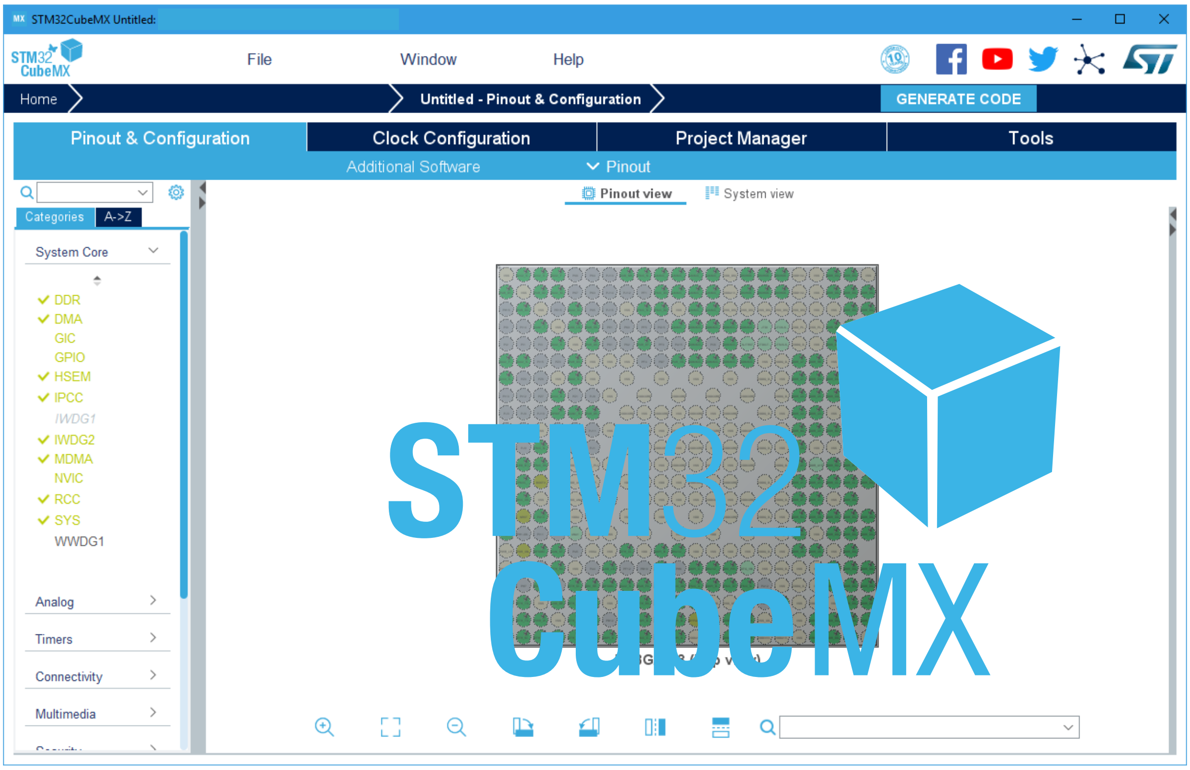
Table 8. Possible combinations of I3C pins

SCL signals	*SDA* signals			
I3C1				
-	-		PI1	PA2
PG13	-		YES	-
PA3	-		-	YES
I3C2				
-	PF0		PG0	-
PF2	YES		-	-
PC12	-		YES	-
I3C3				
-	PZ0	PZ3	PG0	PG2
PZ1	YES	YES	-	-
PC12	-	-	YES	YES
PG1	-	-	YES	YES

To explore easily peripheral alternate functions mapping to pins, it is recommended to use the STM32CubeMX tool available on www.st.com.

Note: *STM32CubeMX might not support all features or options that are described in the product reference manual or datasheet. This is usually due to reduced features in software deliveries such as OpenSTLinux or STM32CubeMP2. This can evolve in future releases of the ecosystem.*

Figure 3. STM32CubeMX example screenshot



1. *This is a screenshot example. It is not specific to the STM32MP21x lines. The appearance can also differ with future STM32CubeMX versions.*

4 Clocks

Different clock sources can be used to drive the subsystems clocks:

- *HSI* oscillator clock (high-speed internal clock signal): 64 MHz typical
- *MSI* oscillator clock (multispeed internal clock signal): 16 or 4 MHz typical
- *HSE* oscillator clock (high-speed external clock signal): 40 MHz typical
- PLL1 dedicated to Arm® Cortex®-A35 core
- PLL2 dedicated to *DDR* subsystem
- PLL4/5/6/7/8 clocks
- PLL_USB to generate the *USB* clock (480 MHz)

The devices have two secondary clock sources:

- 32 kHz low-speed internal *RC* (*LSI RC*) that drives the independent watchdog and, optionally, the *RTC* used for automatic wake-up from the Stop/Standby modes.
- 32.768 kHz low-speed external crystal (*LSE* crystal) that optionally drives the real-time clock (RTCCLK)

Each clock source can be switched on or off independently when it is not used, to optimize the power consumption.

Refer to the reference manual and datasheet for the description of the clock tree, and for details of the possible clock frequencies.

4.1 HSE oscillator clock

The high-speed external clock signal (*HSE*) can be generated from two possible clock sources:

- *HSE* user external clock (see Figure 4).
- *HSE* external crystal (see Figure 5).

See also Section 8.1: Clock for the recommended implementation.

Figure 4. *HSE* external clock

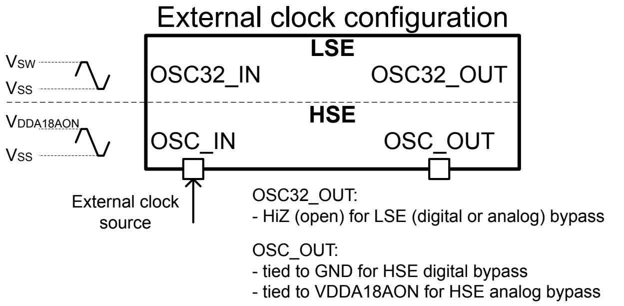
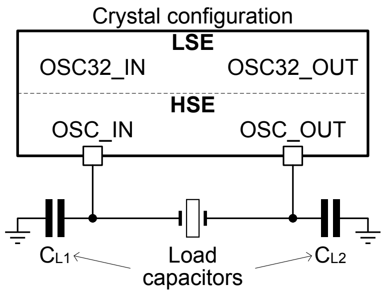


Figure 5. *HSE* crystal



1. *Refer to the application note [1].*

4.1.1 External source (*HSE* bypass)

In this mode, an external clock source must be provided. It can have a frequency from 16 to 48 MHz (refer to the corresponding datasheets for the actual maximum value).

The external digital (V_{IL}/V_{IH}) or analog (amplitude of 200 mV pk-pk minimum) clock signal with a duty cycle of about 50%, has to drive the OSC_IN pin.

Note: To allow USB boot, the boot ROM automatically selects the HSE mode by checking the OSC_OUT connection during the startup phase (that is on the NRST rising edge):

- *OSC_OUT is tied to GND (max 1 kΩ): HSE digital bypass*
- *OSC_OUT is tied to $V_{DDA18AON}$ (max 1 kΩ): HSE analog bypass*
- *OSC_OUT high-Z or connected to a crystal: HSE crystal mode.*

When utilizing a bypass, the external clock generator can be activated through the PWR_ON feature for the purpose of power conservation (that is to say deactivated during Standby). In that case, the OSC_IN clock input must be stable within 10 ms after the PWR_ON rising edge occurs.

4.1.2 External crystal (*HSE* crystal)

The external oscillator frequency ranges from 16 to 48 MHz.

The external oscillator has the advantage of producing a very accurate rate on the main clock. The associated hardware configuration is shown in Figure 5. Using a 40 MHz crystal frequency is a good choice to get accurate *USB* high-speed clocks.

The crystal and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected crystal.

For C_{L1} and C_{L2} it is recommended to use NP0/C0G capacitors selected to meet the load requirements of the crystal. C_{L1} and $C_{L2,}$ have usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}. The *PCB* and pin capacitances must be included when sizing C_{L1} and C_{L2}.

Refer to the application note and electrical characteristics sections in the product datasheet for more details.

4.2 *LSE* OSC clock

The *LSE* can be generated from two possible clock sources (see Figure 6 and Figure 7 below):

- *LSE* user external clock, see Figure 6
- *LSE* external crystal, see Figure 7

Figure 6. *LSE* external clock

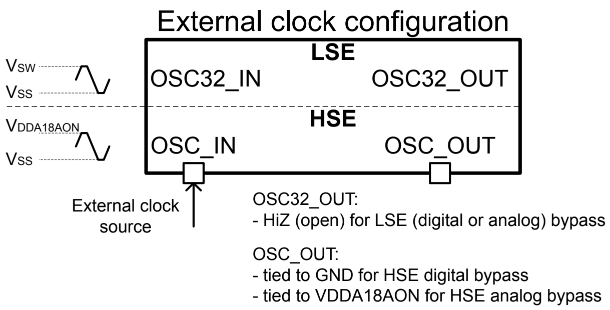
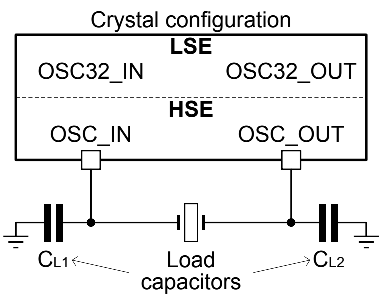


Figure 7. *LSE* crystal resonators



1. crystal resonators: It is strongly recommended to use a crystal with a load capacitance $C_L \leq 12.5$ pF.

4.2.1 External source (*LSE* bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 1 MHz. The external digital (V_{IL}/V_{IH}) or analog (amplitude of 200 mV pk-pk minimum) clock signal with a duty cycle of about 50% has to drive the OSC32_IN pin while the OSC32_OUT pin must be left high-Z (see Figure 6. external clock). The configuration of the bypass mode as well as the selection between the digital and the analog is done within the *RCC* registers.

4.2.2 External crystal (*LSE* crystal)

The *LSE* crystal is a 32.768 kHz low-speed external crystal. It has the advantage of providing a low-power, but highly accurate clock source to the real-time clock peripheral (*RTC*) for clock/calendar or other timing functions.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins. The goal is to minimize output distortion and startup stabilization time. The load capacitance values C_{L1} and C_{L2} must be adjusted according to the selected oscillator. It is recommended to use medium-high or high drive on the *LSE* oscillator.

Refer to the application note and the electrical characteristics sections in the product datasheet for more details.

4.3 Clock security system (CSS)

Details can be found in the product reference manual [8].

4.3.1 CSS on HSE

The clock security system can be activated by software. In this case, the clock detector is enabled after the *HSE* oscillator startup delay, and disabled when this oscillator is stopped. If a failure is detected on the *HSE* oscillator clock, an application reset can be generated.

4.3.2 CSS on *LSE*

The clock security system can be turned on using software. When this happens, the clock detector is turned on after a delay in the *LSE* oscillator startup. The detector is turned off when the oscillator stops. If there is a problem with the *LSE* oscillator clock, the *RTC*/*TAMP* clock source is stopped and the *TAMP* block is notified for security protection and system wake-up.

5 Boot configuration

5.1 Boot mode selection

In the STM32MP21x lines, different boot modes can be selected by means of the BOOT[3:0] pins and *OTP* settings.

Table 9. Boot sources

BOOT[3:0] pins	Alternate *OTP* value							
	0b00 (default)				0b01	0b10	0b11	
	Primary Arm® Cortex®-A35 core	Primary Arm® Cortex®-M33 core	Primary Arm® Cortex®-M33 core (1)		Primary Arm® Cortex®-A35 core	Primary Arm® Cortex®-M33 core	Primary Arm® Cortex®-M33(1) core	
			Arm® Cortex®-A35	Arm® Cortex®-M33			Arm® Cortex®-A35	Arm® Cortex®-M33
0	*UART* and *USB* (2) (3)							
1	*SD* card	-	-	-	*SD* card	*SD* card	-	-
2	e•MMC	-	-	-	e•MMC	e•MMC	e•MMC	Serial NOR
3	Development boot(2)							
4	Serial NOR	-	-	-	Serial NOR	Serial NOR	*SLC* NAND	Serial NOR
5	Serial NAND	-	-	-	-	-	e•MMC (4).	Serial NOR
6	*SCL* NAND	-	-	-	-	-	e•MMC (4)	HyperFlash™
7	-	*SD* card	-	-	HyperFlash™	HyperFlash™	-	-
8	-	e•MMC	-	-	Serial NAND	Serial NAND	e•MMC	HyperFlash™
9	-		Serial NAND	Serial NOR	-		SD card(5).	Serial NOR
10	-		*SCL* NAND	Serial NOR	-		*SD* card(5)	HyperFlash™
11	-	Serial NOR	-	-	*SLC* NAND	SLC NAND	SLC NAND	HyperFlash™
12	Development boot(2)							
13	-	-	e•MMC	Serial NOR	*SD* card(5)	SD card(5)	*SD* card	Serial NOR
14	-	-	*SD* card	Serial NOR	e•MMC (4)	e•MMC (4)	*SD* card	HyperFlash™
15	*UART* and *USB* (3)							

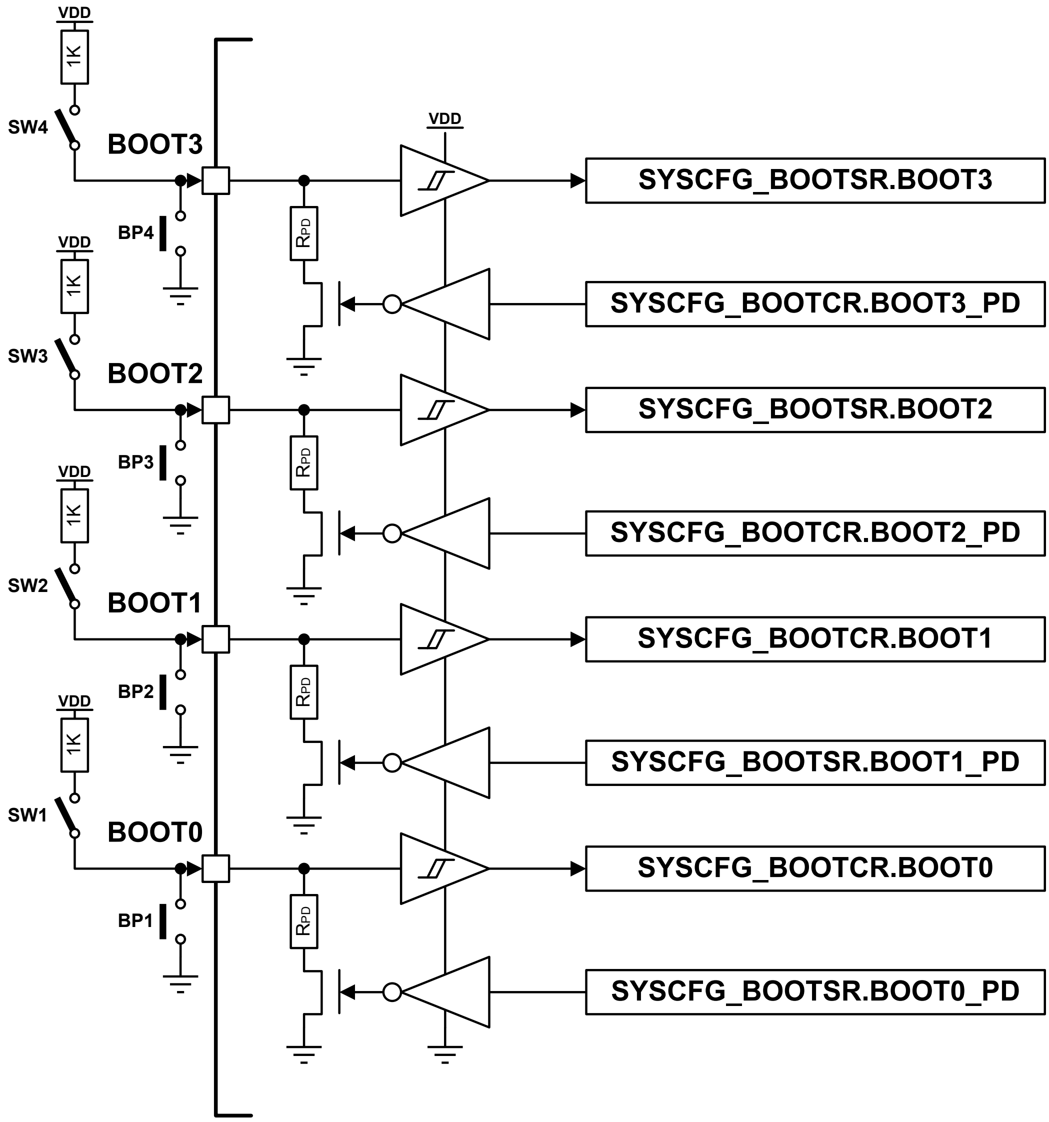
1. *Two flash memory configurations. Indirect Arm® Cortex®-A35 boot (from Arm® Cortex®-M33) or used during Arm® Cortex®-A35 D1 Standby exit.*
2. *Cannot be overridden by OTP.*
3. *Wait for the incoming connection to USART2 or UART5 on the default pins and the USB high-speed device on OTG_HSDP_DP/DM.*
4. *e•MMC on SDMMC1*
5. *SD card on SDMMC2*

The boot *ROM* samples the values on the boot pins after a reset. It is up to the user to set the BOOT[3:0] pins before reset exit to select the required boot mode. The software could also resample the boot pins later (for example by reading the BOOT[3:0]" field in the "SYSCFG_BOOTCR" register). Or the boot *ROM* could do it upon Standby mode exit. Consequently, the boot pins must be kept in the required boot mode configuration all the time.

5.2 Boot pin connection

Figure 8 shows an example of the external connection required to select the boot memory of the STM32MP21x lines devices.

Figure 8. Boot mode selection example



Despite all the recovery cases in software, there is a risk that, with wrong or corrupted flash memory content (such as user mistake, bad flash memory content programmed, power lost), the system might not start (also known as 'bricked').

Note that on empty flash memories, the boot code automatically switches to *UART*/*USB* connection.

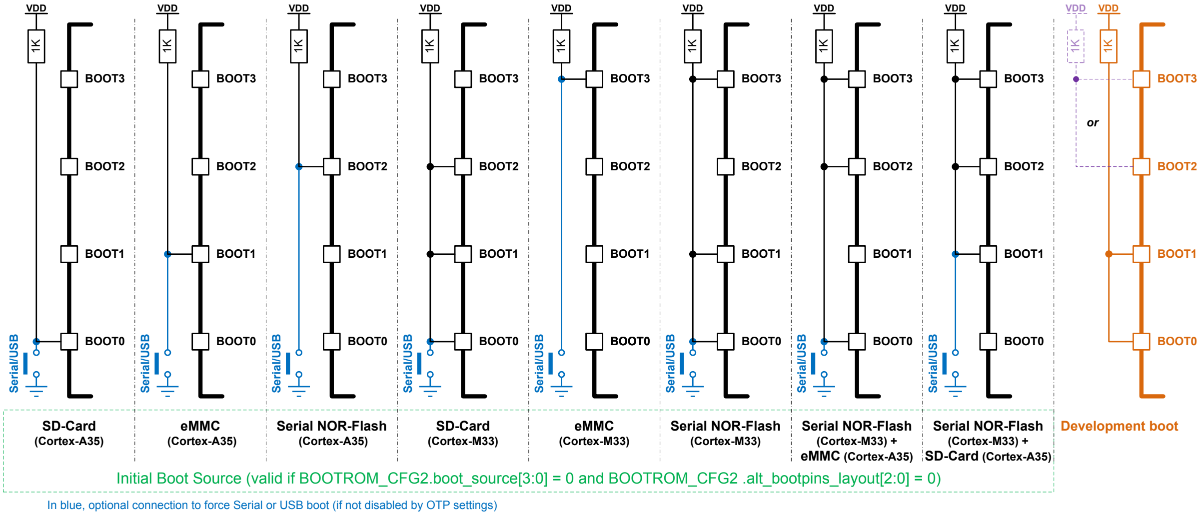
It might be required to have a way to force use of *UART*/*USB* connection in order to enable board flash memory reprogramming (for example: after sale services, firmware update).

There are also cases where initial boot is done on a different flash memory than regular boot (for example the initial boot from SD card, which copies binary data in another flash memory like serial NOR, serial NAND, eMMC, or *SLC* NAND). This is possible as the initial boot code could set relevant *OTP* bits to force future boot from the programmed flash memory (see Figure 10). This allows a simplified and flexible mass production without intervention on boot pins. The typical connections examples for a final board are described in Figure 9. Boot pins typical connection schematics.

The switches could be done by various ways such as pushbutton, solder bridges, connector contacts, test points. They are assumed 'open' by default during normal product boot to avoid current flow in external resistors.

Note that *OTP* configuration could force or forbid any of the boot sources in order to satisfy product security requirements.

Figure 9. Boot pins typical connection schematics



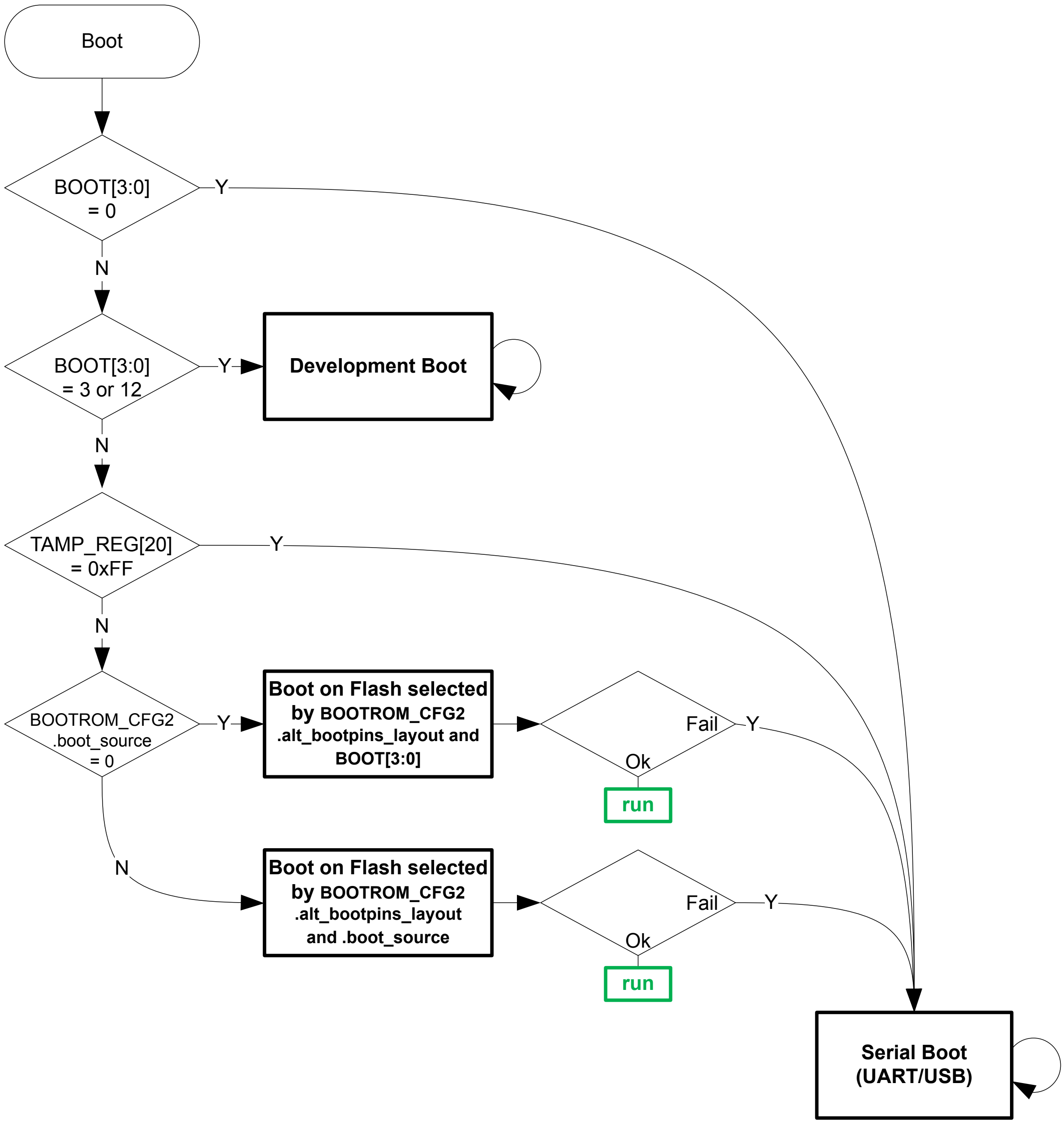
5.3 Embedded bootloader mode

This embedded bootloader is located in the boot *ROM*. During boot, the *OCTOSPI*, *FMC*, *SDMMC*, and *USART* peripherals operate with the internal 64 MHz oscillator (*HSI*).

The OTG_HSDP high-speed device, however, can function only if an external clock (*HSE*) is present with a recommended frequency of 40 MHz (alternatively, 16, 19.2, 20, 24, 25, 26, 28, 32, 36, 40 or 48 MHz could be used with *OTP* settings and/or automatic frequency detection).

For additional information, refer to the *USB* DFU/*USART* protocols used in STM32MP2 series bootloaders [3].

Figure 10. Simplified boot flow



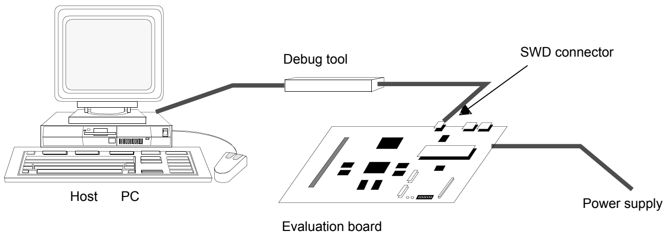
6 Debug management

6.1 Introduction

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a *JTAG*, or *SWD* connector and a cable connecting the host to the debug tool.

Figure 11 shows the connection of the host to the evaluation board.

Figure 11. Host-to-board connection



6.2 *SWJ* debug port (serial wire and *JTAG*)

The STM32MP21x lines core integrates the serial wire/*JTAG* debug port (*SWJ-DP*). It is an Arm® standard CoreSight™ debug port that combines a *JTAG-DP* (5-pin) interface and an *SW-DP* (2-pin) interface.

- The *JTAG* debug port (*JTAG-DP*) provides a 5-pin standard *JTAG* interface to the AHP-AP port
- The serial wire debug port (*SW-DP*) provides a 2-pin (clock + data) interface to the *AHB*-AP port

The two pins of the *SW-DP* are multiplexed with two of the five *JTAG* pins of the *JTAG-DP*.

6.3 Pinout and debug port pins

6.3.1 Internal pull-up and pull-down resistors on *JTAG* pins

To avoid any uncontrolled I/O levels, the STM32MP21x lines embed internal pull-up and pull-down resistors on *JTAG* pins:

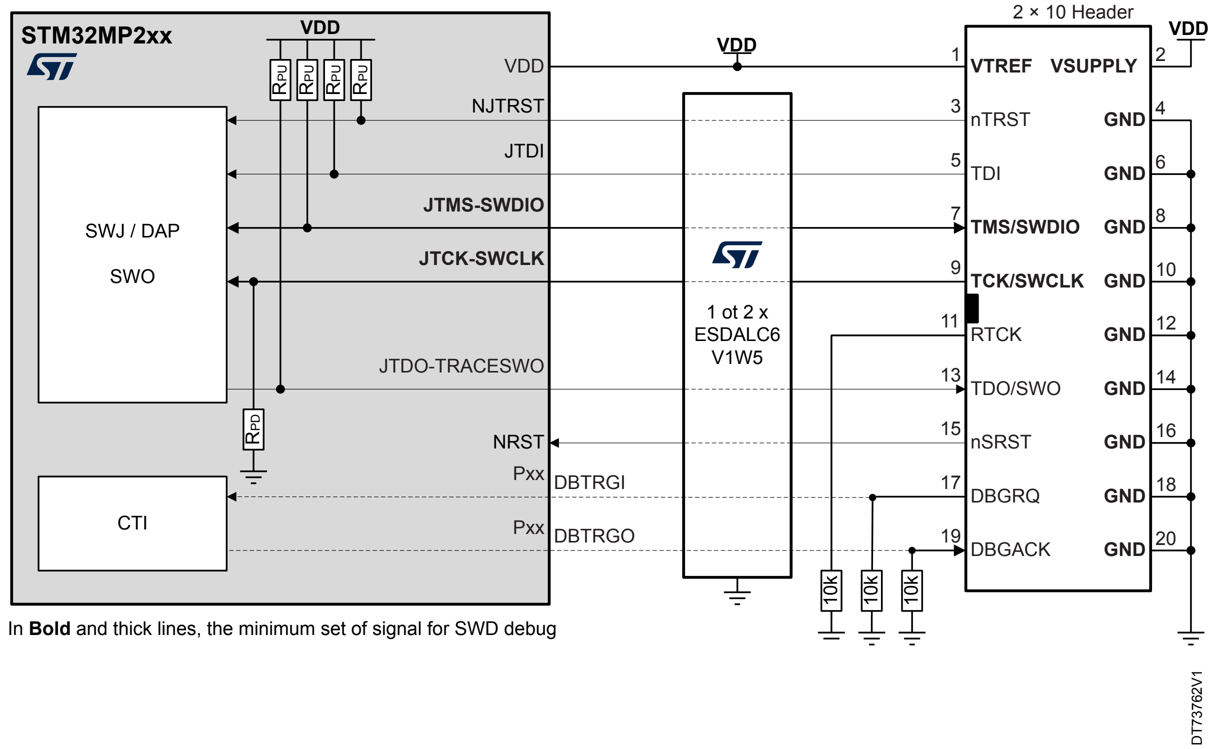
- NJTRST: Internal pull-up
- JTDI: Internal pull-up
- JTDO-TRACESWO: Internal pull-up
- JTMS-SWDIO: Internal pull-up
- JTCK-SWCLK: Internal pull-down

Note:
- *The JTAG IEEE standard recommends adding pull-up resistors on TDI, TMS, and nTRST but there is no special recommendation for TCK. However, for the STM32MP21x lines, an integrated pull-down resistor is used for JTCK.*
- *Having embedded pull-up and pull-down resistors removes the need to add external resistors.*
- *In order to use the RMA (return material acceptance), the JTAG pins (JTDI, JTCK, JTMS) must be accessible. The JTDO pin might be needed too, depending on the tool that is used.*

6.3.2 Debug port connection with standard *JTAG* connector

Figure 12 shows the connection between the STM32MP21x lines and a standard *JTAG*/*SWD* connector.

Figure 12. *JTAG*/*SWD* using Arm® JTAG 20 connector implementation example



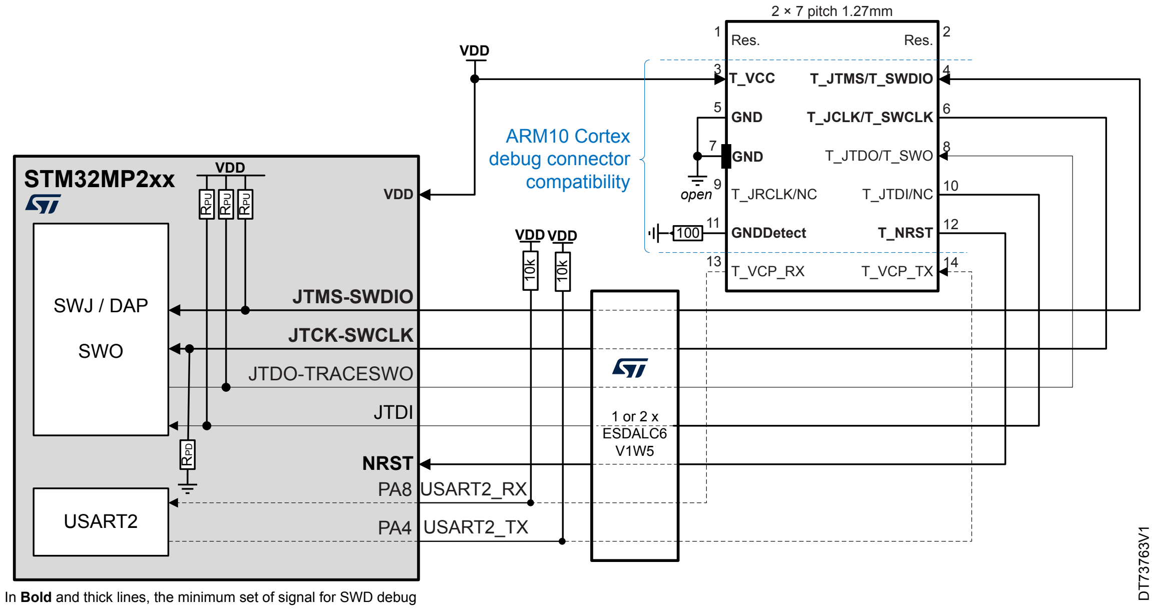
Note: The single wire trace on the TRACESWO pin is only available for Arm® Cortex®-M33 core. To trace all cores activity, a parallel trace port must be used (see Parallel trace and HDP).

6.3.3 Debug port and *UART* connection with STDC14 connector

Figure 13 shows the connection between the STM32MP21x lines and an STDC14 connector including *UART* virtual com port connection.

Reference example for the STDC14 header is FTSH-107-01-L-DV-K-A.

Figure 13. *JTAG*/*SWD*/*UART* VCP using STDC14 connector implementation example



Note:
- *The single wire trace on the TRACESWO pin is only available for Arm® Cortex®-M33 core. To trace all core activities, a parallel trace port must be used (see Parallel trace and HDP).*
- *STDC14 connector is respecting (from pin 3 to pin 12) the Arm10 pinout (Arm® Cortex® debug connector).*

6.3.4 Parallel trace and HDP

Parallel trace

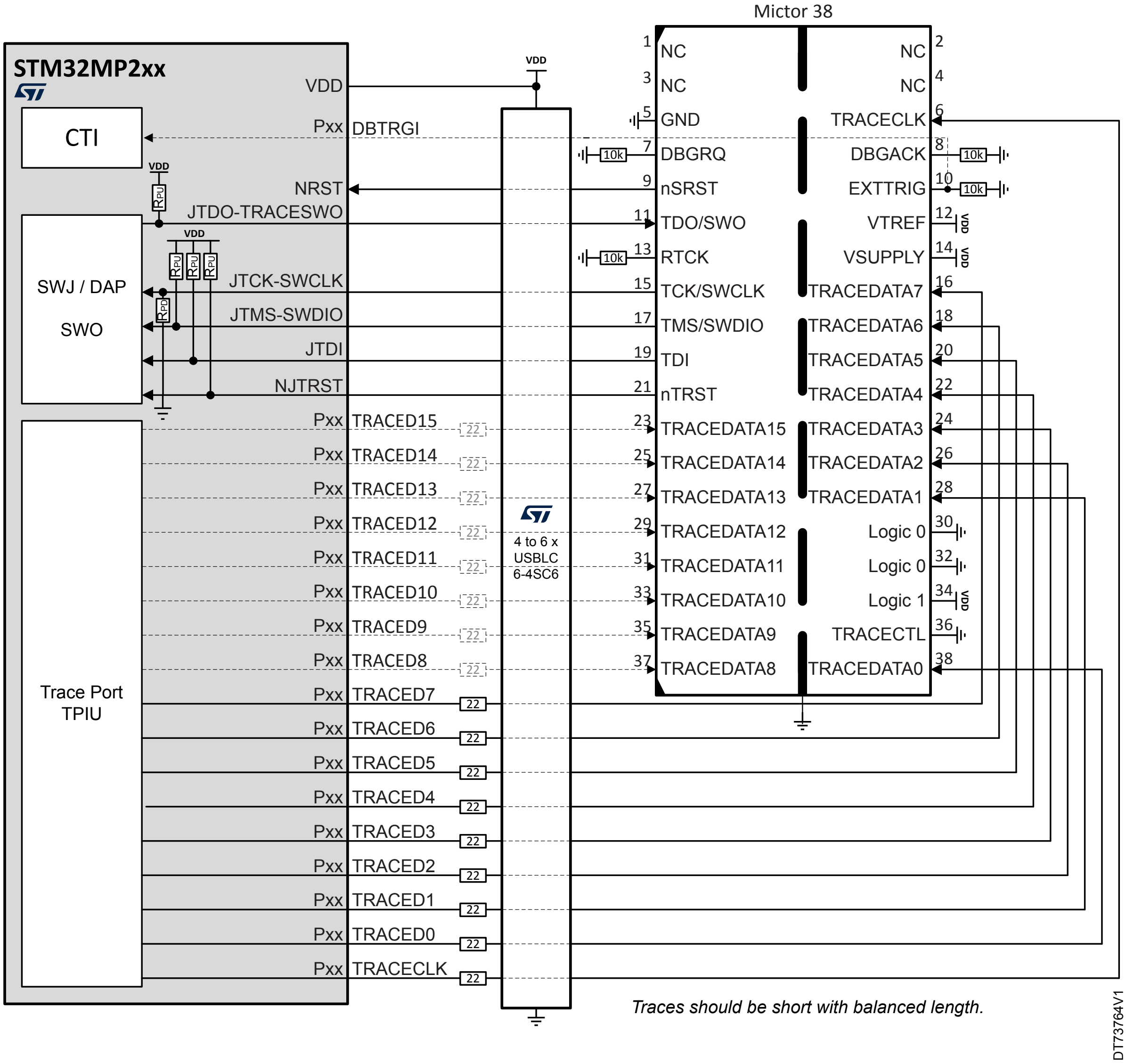
TRACED[15:0] and TRACECLK signals are available as alternate functions on I/Os pins. The number N of trace data can be = 1, 2, 4, 8 or 16 pins. Less trace data mean lower available trace bandwidth, so less information could be traced (such as the number of trace sources, code and/or data tracing) without trace overrun. For each product, a trade-off between available features and the trace bus could lead to have reduced feature while using trace during product development.

The trace is compliant with Arm® CoreSight™ trace. It needs a dedicated tracing tool in order to be interpreted and correlated with the debugging done through *SWD* or *JTAG*.

For more information on the Trace Port interface CoreSight™ component, refer to the product reference manual [8] and the Arm® CoreSight™ technical reference manual.

Note that for efficient tracing bandwidth, TRACECLK must run as fast as possible while maintaining good signal integrity on all parallel trace signals. This is dependent on board and connector choices, *GPIO* strength settings (GPIO_OSPEEDR registers), and V_{DD} voltage.

Figure 14. Parallel trace port with *JTAG*/*SWD* on Mictor-38 implementation example



Note: *Missing TRACED[13,12,11,8] on VFBGA225 8x8 package.*

Hardware debug port (*HDP*)

Some internal signals are available for deep debugging. Internal knowledge and an oscilloscope or logic analyzer are needed. For more information, refer to the product reference manual [8] and datasheets [9] [10].

6.3.5 Debug triggers and LEDs

The CoreSight™ cross-trigger interface (CTI) is available on DBTRGI and DBTRGO pins.

DBTRGI could be generated by the external user signal. It could be programmed also inside CoreSight™ components to start/stop traces or enter specific cores in debug mode (break).

DBTRGO could be generated by CTI to see externally that a trigger condition is reached by one of the CoreSight™ components (core break, trace started, and so on.).

DBTRGO could be made available on PH4, PH5, PZ3 (except VFBGA225 8x8 package).

DBTRGI could be made available on PH4, PH5, PZ3 (except VFBGA225 8x8 package).

6.3.6 Debug LED

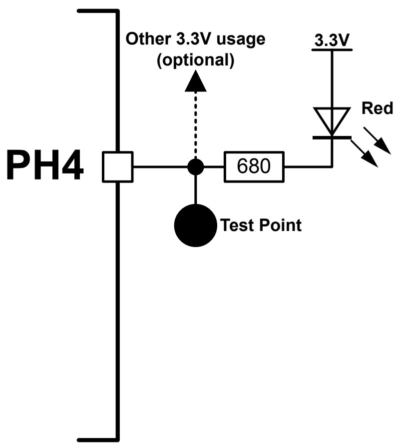
The PH4 pin has a specific BOOTFAILN behavior (see boot documentation for details):

- During the boot phase, in case of boot failure, the PH4 pin is set to low open-drain. The debug LED lights bright. Note that in most cases, without secure boot enabled, this failure is not visible as it immediately falls back to an *UART*/*USB* boot.
- During *UART*/*USB* boot, the PH4 pin toggles open-drain at a rate of few Hz until a connection is started. The debug LED blinks fast.
- With BOOT[3:0] = 0b0000 (development boot), PH4 is set to low open-drain. The debug LED lights bright.
- In all other cases, like normal boot, the PH4 pin is kept in its reset value, that is high-Z until further software setting.

A red LED can be connected to PH4 as shown in Figure 15. V_{DD} = 1.8 V, additional circuitry might be needed.

LEDs are useful for quick visual signaling of system activity. So, it is a good choice to use at least PH4 for quick low level boot error signaling. In most cases, the LED circuitry does not conflict with usage for other purposes (such as USBH_HS_OVRCUR).

Figure 15. PH4 LED connection (valid for VDD = 3.3V)



7 Recommendations

7.1 PCB

For technical reasons, it is mandatory to use a multilayer *PCB* with a separate layer dedicated to the ground (VSS), and another layer dedicated to power supplies like V_{DD}, V_{DDCPU}, and V_{DDCORE}. This provides good decoupling and a good shielding effect.

7.2 Component position

A preliminary layout of the *PCB* must separate the different circuits according to their EMI contribution. The aim is to reduce cross-coupling on the *PCB* that is noisy high-current circuits, low-voltage circuits, and digital components.

7.3 Ground and power supplies (V_{SSx},V_{DDx})

Due to a large power and high frequencies involved in the STM32MP21x devices, it is mandatory to use *PCB* with at least four layers and with dedicated power planes for V_{SSx} and V_{DDx}.

7.4 Advanced *GPIO* configuration

To utilize *ETH* RGMII, *DCMIPP* parallel inputs, *LTDC* parallel outputs, or parallel TRACE outputs (*TPIU*), it is necessary to configure certain settings within the GPIOx_ADVCFG and GPIOx_DELAY registers. Refer to Table 10 below for recommended values.

Table 10. *GPIO* advance configuration recommended settings

<table>
<tr><th rowspan="2">Interface</th><th rowspan="2">Mode</th><th rowspan="2">Signals</th><th colspan="4">GPIOx_ADVCFGR bits</th><th>GPIOx_DELAY field</th></tr>
<tr><th>RET</th><th>INVCLK</th><th>DE</th><th>DLYPATH</th><th>DLY[3:0]</th></tr>
<tr><td rowspan="15">ETH1, ETH2</td><td rowspan="5">RGMII</td><td>ETHx_RGMII_RX_CTL</td><td rowspan="4">1</td><td rowspan="4">0</td><td rowspan="4">1</td><td rowspan="4">0</td><td rowspan="4">0b0000</td></tr>
<tr><td>ETHx_RGMII_RXD[3:0]</td></tr>
<tr><td>ETHx_RGMII_TX_CTL</td></tr>
<tr><td>ETHx_RGMII_TXD[3:0]</td></tr>
<tr><td>Other ETHx_</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0b0000</td></tr>
<tr><td rowspan="10">RGMII_ID (GMAC side internal delays)[1]</td><td>ETHx_RGMII_RX_CLK (on PA14)</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0b0011</td></tr>
<tr><td>ETH2_RGMII_RX_CLK (on PC0)</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0b0100</td></tr>
<tr><td>ETH2_RGMII_RX_CLK (on PF6)</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0b0110</td></tr>
<tr><td>ETH1_RGMII_GTX_CLK</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0b0101</td></tr>
<tr><td>ETH2_RGMII_GTX_CLK</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0b0110</td></tr>
<tr><td>ETHx_RGMII_RX_CTL</td><td rowspan="4">1</td><td rowspan="4">0</td><td rowspan="4">1</td><td rowspan="4">0</td><td rowspan="4">0b0000</td></tr>
<tr><td>ETHx_RGMII_RXD[3:0]</td></tr>
<tr><td>ETHx_RGMII_TX_CTL</td></tr>
<tr><td>ETHx_RGMII_TXD[3:0]</td></tr>
<tr><td>Other ETHx_</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0b0000</td></tr>
<tr><td rowspan="4">DCMIPP parallel</td><td rowspan="2">PIXCLK rising edge sampling</td><td>DCMIPP_PIXCLK</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0b0000</td></tr>
<tr><td>Other DCMIPP_</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0b0000</td></tr>
<tr><td rowspan="2">PIXCLK falling edge sampling</td><td>DCMIPP_PIXCLK</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0b0000</td></tr>
<tr><td>Other DCMIPP_</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0b0000</td></tr>
</table>

Interface	Mode	Signals	GPIOx_ADVCFGR bits				GPIOx_DELAY field
			RET	INVCLK	DE	DLYPATH	DLY[3:0]
LTDC parallel	CLK rising edge sampling	LCD_CLK	0	0	0	0	0b0000
		Other LCD_	1	0	0	0	0b0000
	CLK falling edge sampling	LCD_CLK	0	1	0	0	0b0000
		Other LCD_	1	0	0	0	0b0000
TRACE (*TPIU*) parallel	Edge-aligned data	TRACECLK	1	0	0	0	0b0000
		Other TRACEx	1	0	0	0	0b0000
	Center-aligned data	TRACECLK	1	0	0	0	0b0000
		Other TRACEx	1	1	0	0	0b0000

1. *Use these settings only if a 2 ns internal delay is needed for RGMII timings. Delay values could be slightly tuned if required.*

7.5 I/O speed settings

It is important to set the right output drive on I/Os to have sufficient rise and fall times. Moreover, it helps avoid any additional ringing and noise.

When there are no specific requirements for I/O speed, it is mandatory to set OSPEEDR to 0.

As a first approximation, the following drawings and tables could be used to choose quickly the right setting to apply according to signal frequency and capacitive load. This setting might need to be tailored in case of signal integrity issue.

Whenever an OSPEEDR value of two or three is used, related I/O compensation needs to be enabled in SYSCFG. There are five independent I/O compensations for each of the four independent I/O supplies: V_{DD}, V_{DDIO1}, V_{DDIO2}, and V_{DDIO3}. Refer to the product datasheet and reference manual for more details.

Note that there are four independent I/Os voltage sections (V_{DD}, V_{DDIO1}, V_{DDIO2}, or V_{DDIO3}), which, in some AFMUX settings cases, could be shared between different interfaces.

When V_{DD}, V_{DDIO1}, V_{DDIO2}, or V_{DDIO3} are held at 1.8 V, settings must be done in PWR_CR1.VDDIOxVRSEL (for VDD and VDDIO3) or PWR_CR7.VDDIO2VRSEL (for VDDIO2) or PWR_CR8.VDDIO1VRSEL (for VDDIO1). Without these settings, the I/Os are working in degraded mode.

Note: *To avoid I/O damage due to mis-settings, in addition to PWR settings, there are OTP bits (HSLV_VDDIOx) that must be programmed when a specific domain (V_{DD}, V_{DDIO1}, V_{DDIO2}, or V_{DDIO3}) may be used below 2.5 V on a product. See related sections in the product reference manual for details.*

Note: *In the case of asynchronous or single edge clocked data lanes (such as SDR), the maximum data frequency toggle is effectively half the data rate.*

For example, an SPI running at 10 Mbit/s has a maximum frequency of 5 MHz on the data signal, like output serial data 01010101..., but 10 MHz on the clock signal.

On dual-edge clocked data lanes (such as DDR), the clock and data have the same maximum toggling frequency.

Figure 16. I/O speed summary with various loads and voltages

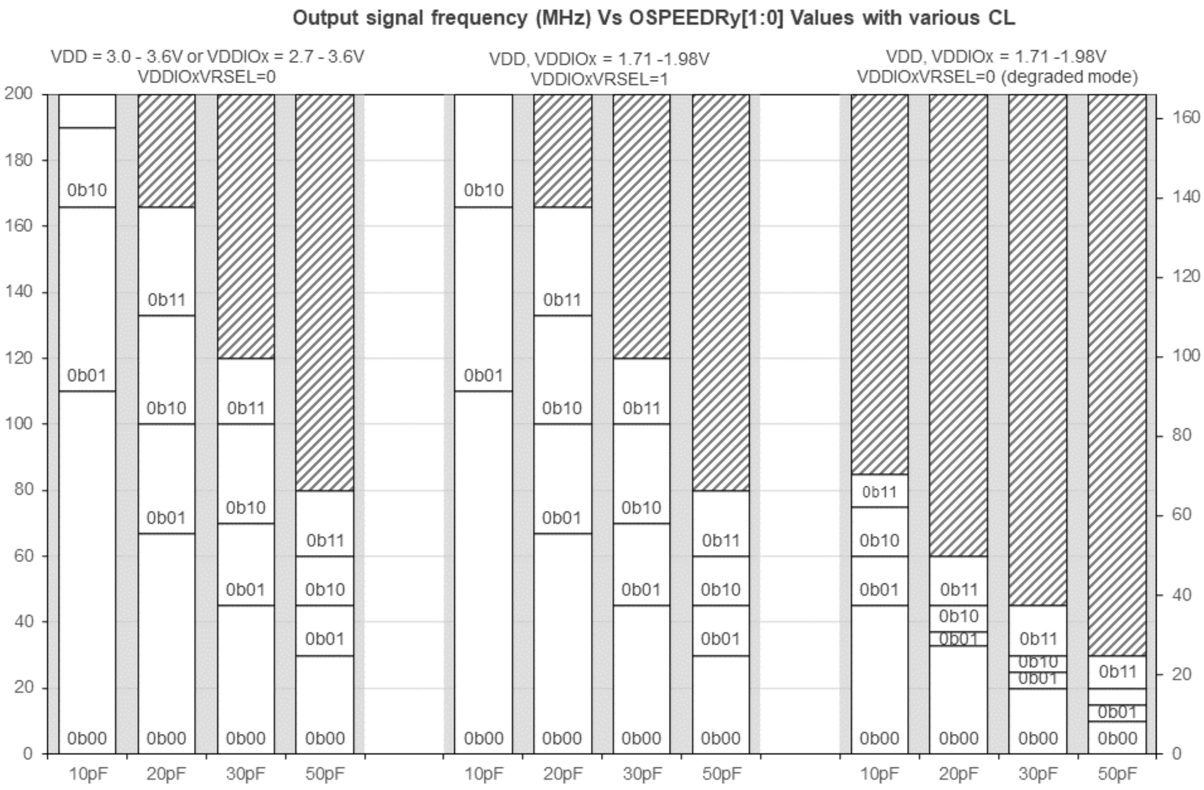


Table 11. OSPEEDR setting example for VDD = 3.3 V typ.[1]

Peripheral	Signals	Toggling rate (MHz)	OSPEEDR C_L = 30 pF		OSPEEDR C_L = 10 pF	
FMC async	Data/Controls	50	1	Medium speed	0	Low speed
FMC sync	CLK	100	2	High speed	0	Low speed
	Data/Controls	50	1	Medium speed	0	Low speed
OCTOSPI1 (SDR)	CLK	133	2[2]	High speed	1	Medium speed
	Data/Controls	66.5	1	Medium speed	0	Low speed
OCTOSPI1 (DDR)	All	66.5	1	Medium speed	0	Low speed
LTDC	CLK	150	3 [2]	Very high speed	1	Medium speed
	Data/Controls	75	2	High speed	0	Low speed
LTDC	CLK	83	2	High speed	0	Low speed
	Data/Controls	41.5	0	Low speed	0	Low speed
TIM/*LPTIM*	All	5	0	Low speed	0	Low speed
I^2C	All	1	0	Low speed	0	Low speed
USART	All	5	0	Low speed	0	Low speed
SPI	CLK	50	1	Medium speed	0	Low speed
	Data/Controls	25	0	Low speed	0	Low speed
SAI	MCLK	15	0	Low speed	0	Low speed
	CLK	1	0	Low speed	0	Low speed
	Data/Controls	0.5	0	Low speed	0	Low speed
SDMMC (SDR)	CLK	133	2 [2]	High speed	1	Medium speed
	Data/Controls	66.5	1	Medium speed	0	Low speed
SDMMC (DDR)	All	52	1	Medium speed	0	Low speed
FDCAN	All	5	0	Low speed	0	Low speed
ETH (MII)	CLK	25	0	Low speed	0	Low speed
	Data/Controls	12.5	0	Low speed	0	Low speed
ETH (RMII)	All	50	1	Medium speed	0	Low speed
	Data/Controls	25	0	Low speed	0	Low speed
ETH (RGMII)	All	125	2 [2]	High speed	1	Medium speed
ETH (MDIO)	*MDIO*	2.5	0	Low speed	0	Low speed
TRACE	All	133	2 [2]	High speed	1	Medium speed
		100	2	High speed	0	Low speed

1. *VDDIOxVRSEL = 0*
2. *Value for a 20 pF load.*

Table 12. **OSPEEDR setting example for VDD = 1.8 V typ.**[1]

[1]Peripheral	Signals	Toggling rate (MHz)	OSPEEDR C_L = 30 pF		OSPEEDR C_L = 10 pF	
FMC async	Data/Controls	50	1	Medium speed	0	Low speed
FMC sync	CLK	100	2	High speed	0	Low speed
	Data/Controls	50	1	Medium speed	0	Low speed
*OCTOSPI*1 (SDR)	CLK	133	2 [2]	High speed	1	Medium speed
	Data/Controls	66.5	1	Medium speed	0	Low speed
*OCTOSPI*1 (DDR)	All	66.5	1	Medium speed	0	Low speed
LTDC	CLK	150	3 [2]	Very high speed	1	Medium speed
	Data/Controls	75	2	High speed	0	Low speed
LTDC	CLK	83	2	High speed	0	Low speed
	Data/Controls	41.5	0	Low speed	0	Low speed
TIM/*LPTIM*	All	5	0	Low speed	0	Low speed
I²C	All	1	0	Low speed	0	Low speed
USART	All	5	0	Low speed	0	Low speed
SPI	CLK	50	1	Medium speed	0	Low speed
	Data/Controls	25	0	Low speed	0	Low speed
SAI	MCLK	15	0	Low speed	0	Low speed
	CLK	1	0	Low speed	0	Low speed
	Data/Controls	0.5	0	Low speed	0	Low speed
SDMMC (SDR)	CLK	133	2 [2]	High speed	1	Medium speed
	Data/Controls	66.5	1	Medium speed	0	Low speed
SDMMC (DDR)	All	52	1	Medium speed	0	Low speed
FDCAN	All	5	0	Low speed	0	Low speed
ETH (MII)	CLK	25	0	Low speed	0	Low speed
	Data/Controls	12.5	0	Low speed	0	Low speed
ETH (RMII)	All	50	1	Medium speed	0	Low speed
	Data/Controls	25	0	Low speed	0	Low speed
ETH (RGMII)	All	125	2 [2]	High speed	1	Medium speed
ETH (MDIO)	*MDIO*	2.5	0	Low speed	0	Low speed
TRACE	All	133	2 [2]	High speed	1	Medium speed
		100	2	High speed	0	Low speed

1. *VDDIOxVRSEL = 1*
2. *Value for a 20 pF load.*

7.6 PCB stack and technology

A trade-off between the *PCB* cost and easy electrical connections has to be made. Below, examples are, either for four or six layers *PCB* with only *PTH* (suited for 0.8mm pitch package), or for six layers *PCB* with both *PTH* and laser drilled vias (suited for 0.5mm pitch package).

Note that some STM32MP21x lines packages with an outer ball pitch of 0.5 mm provide power improved center ball matrix with depopulated matrix. It enables large *PTH* via in between balls.

This ensures better supply connection as well as optimized thermal conductivity than small buried laser drilled vias.

Figure 17. **6-layer *PTH PCB* stack example**

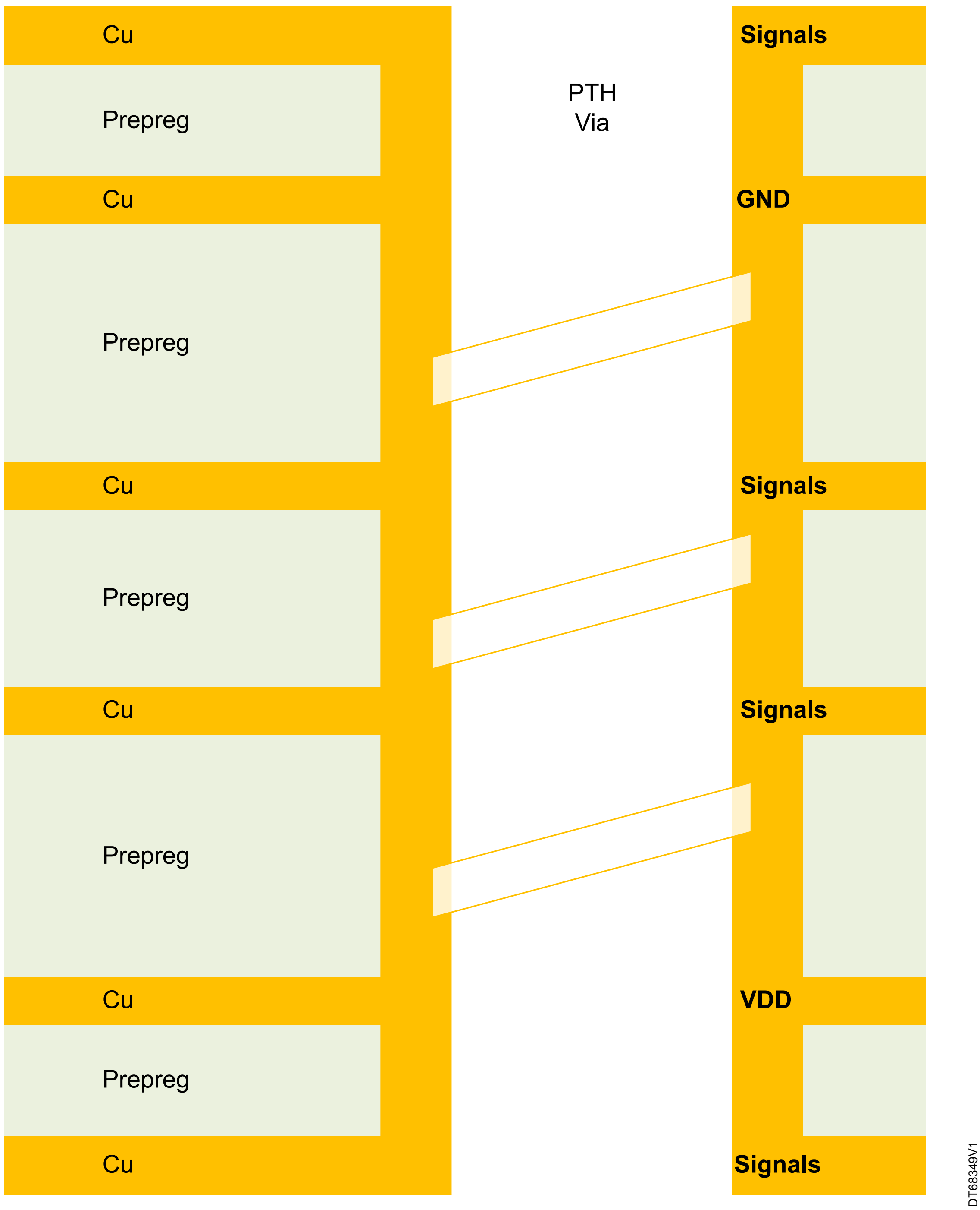


Figure 18. 6-layer *PTH* + laser vias *PCB* stack example

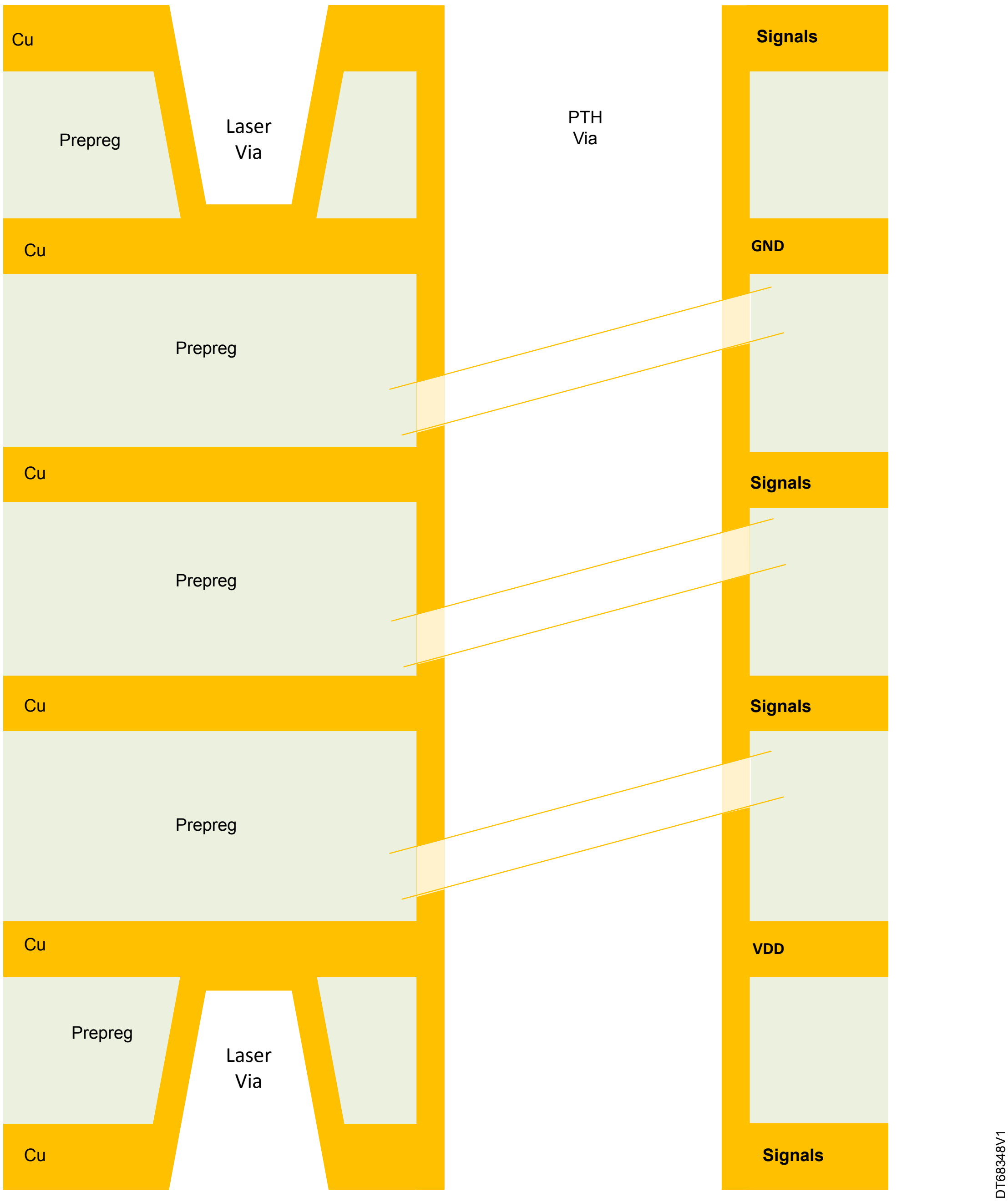


Figure 19. ***PCB* rule for 0.8 mm pitch package (with *PTH*)**

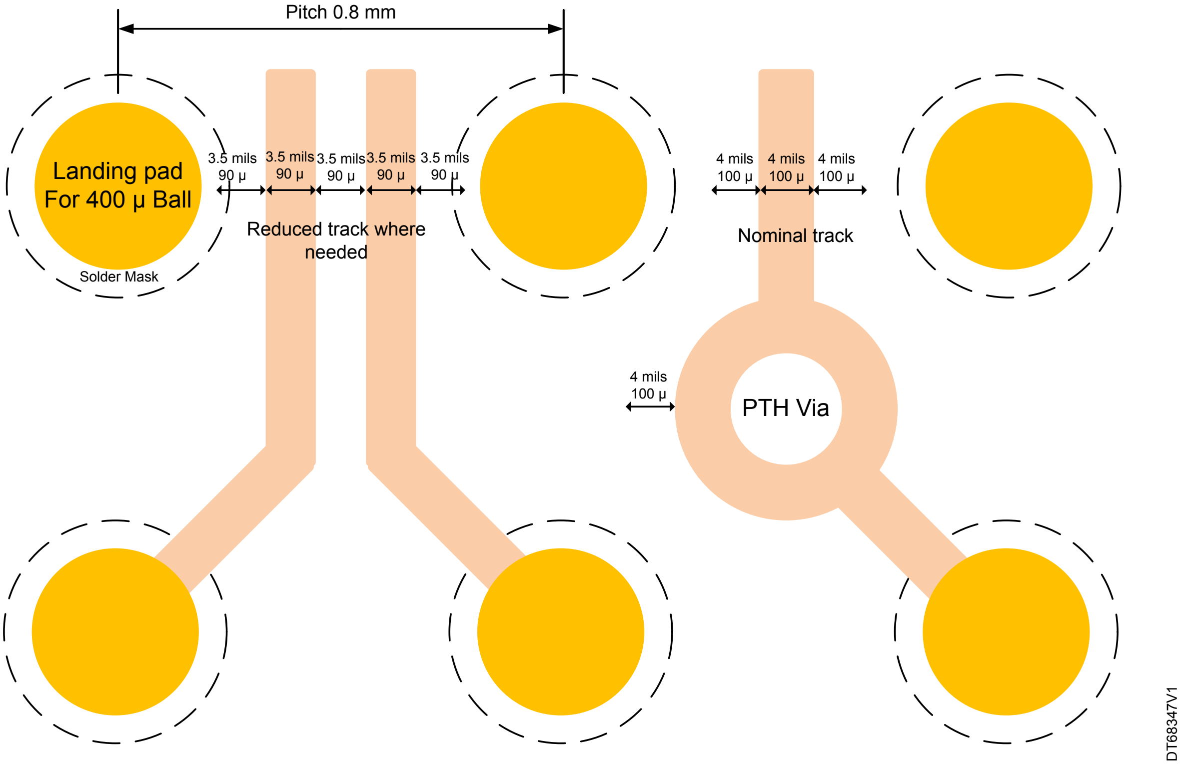
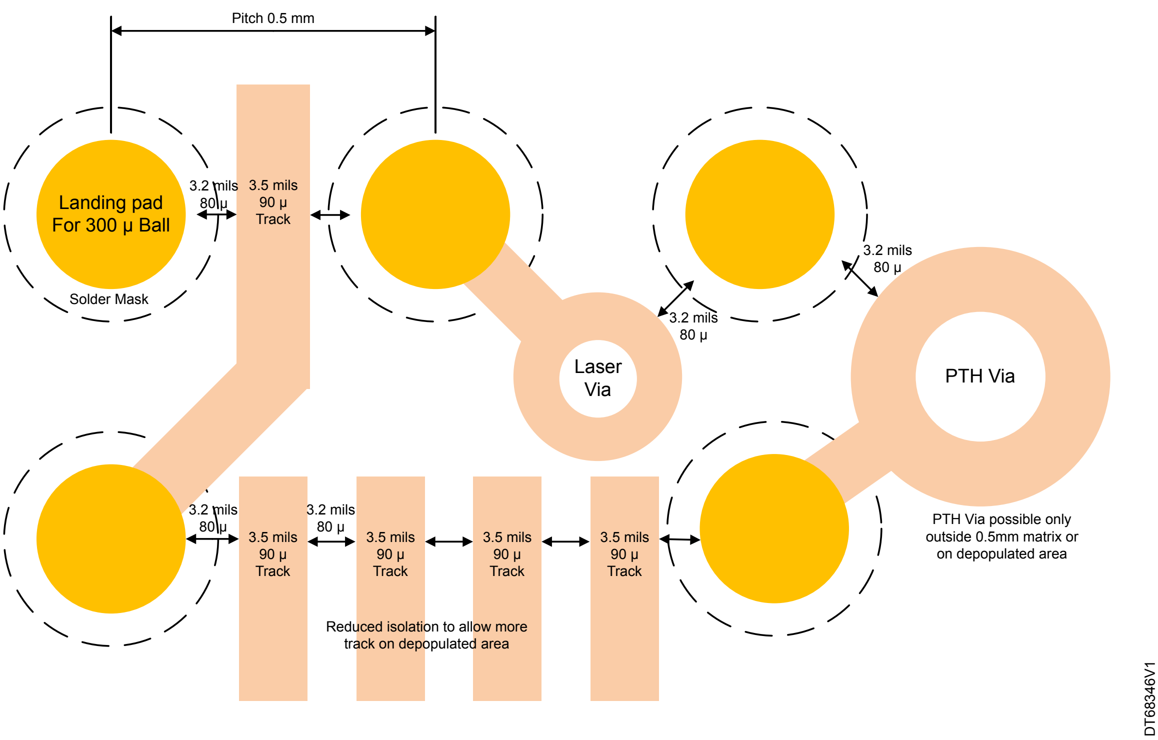


Figure 20. ***PCB* rule for 0.5 mm pitch package (with laser via and *PTH*)**

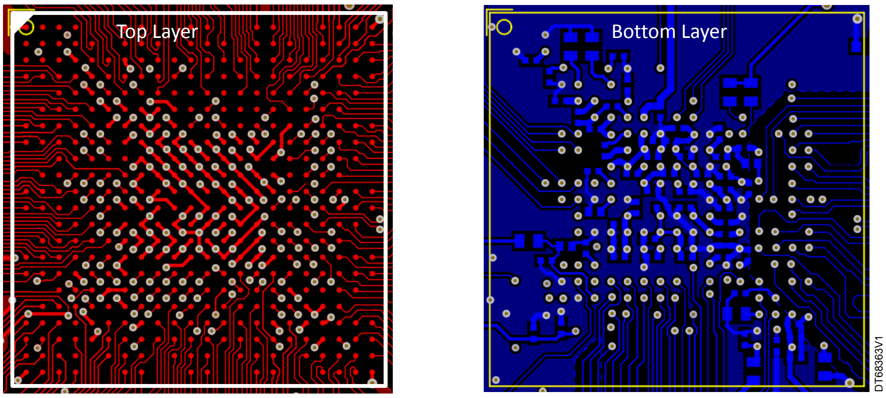


7.7 Decoupling

All the power supply and ground pins must be properly connected to the power supplies. These connections, including pins, tracks, and vias must have as low impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer *PCB*s.

In addition, each power supply pair must be decoupled with ceramic capacitors (most of the time 100 nF or 1 µF, see Table 3. Amount of decoupling recommendation by package). These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the *PCB*. Exact values might depend on the application. Figure 21 shows the typical layout of such a decoupling placement.

Figure 21. Example of decoupling layout



7.8 ESD/EMI protections

Electrostatic discharge (ESD) and electromagnetic interference (EMI) must be taken into account from the beginning of a product development as it can be very complex and expensive to add them later.

ESD and EMI are driven by global standards (such as IEC 61000, JESD 22) which in most countries require a certification to allow mandatory marking to be applied on a product (such as CE, FCC).

ESD and EMI are also driven by standardized interface certification or requirements (for example USB).

Although the STM32MP21x lines embed device level ESD protection, the final product protection must be done by external components, more especially on interfaces having external user access in the final product (such as Ethernet, USB, SD card). Some components provide ESD protection as well as EMI common-mode filtering (for example ECMF02-2AMX6 used on USB). Some examples of ESD/EMI protections are provided in Section 8: Reference design examples.

For more details, refer to the application note [2] about the EMC design guide.

7.9 Sensitive signals

When designing an application, the EMC (electromagnetic compatibility) performance can be improved by closely studying the following points:

- Signals for which a temporary disturbance affects the running process permanently (such as interrupts and handshaking strobe signals, not the case for LED commands)
  For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy or sensitive traces nearby (crosstalk effect) improve the EMC performance. For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (such as clock)
- Sensitive signals (such as high-Z ones)

Signals that do not allow negative injection, such as input/output signals on VSW supply, need to be handled with care to prevent undershoots. To avoid this, a series resistor (usually 22 Ω) can be added close to the signal source to match impedance, or a small capacitor (suited to the impedance and frequency of the signal) can be added near the input/output to reduce ringing. Refer to the product datasheet for more information.

For more details, refer to the application note [2] about the EMC design guide.

7.10 Unused I/Os and features

The STM32MP21x lines are designed for a wide range of applications and often a particular application does not use 100% of the resources.

To increase the EMC performance, unused clocks, counters, or I/Os must not be left free. For example, I/Os must be set to “0” or “1” (external or internal pull-up or pull-down to the unused I/O pins), and unused features must be “frozen” or disabled.

8 Reference design examples

This section provides examples to help the user to connect major and critical interfaces to the STM32MP21x devices.

8.1 Clock

Two clock sources are used for STM32MP21x lines, with the following choices:

- *LSE*: 32.768 kHz crystal for the embedded *RTC*
- *HSE*: 40 MHz crystal or external oscillator as STM32MP21x lines main clock

Refer to Section 4: Clocks.

Figure 22. *HSE* recommended schematics for both oscillator/crystal options

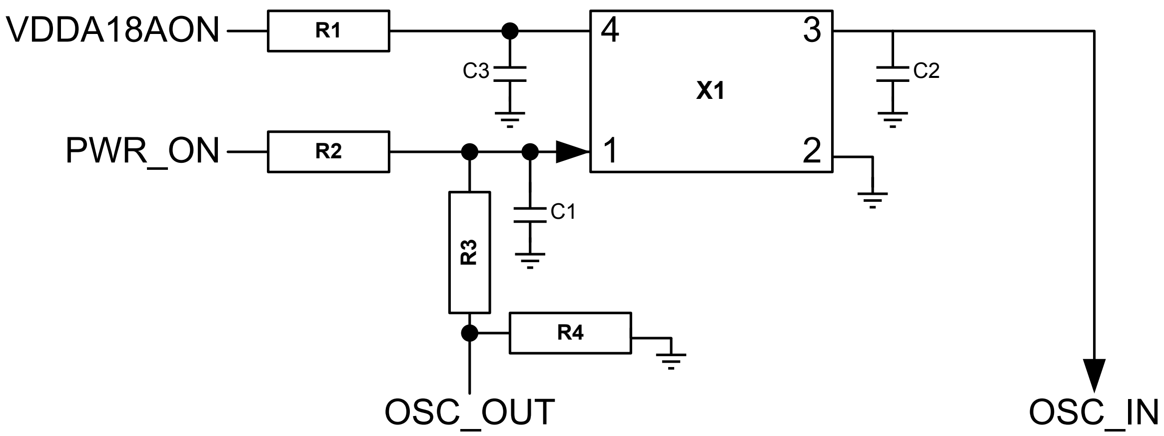


Table 13. HSE BOM for oscillator or crystal

-	Oscillator (OSC_OUT = logic 0)	Crystal (OSC_OUT = crystal pin)
X1	NZ2016SH 40 MHz	NX2016SA 40 MHz
R1	10 Ω	- (open)
R2	10 KΩ / 30 KΩ(1)	- (open)
R3	- (open) / 33 kΩ(1)	0 Ω
R4	1 kΩ	- (open)
C1	- (open)	6.8 pF
C2	- (open)	6.8 pF
C3	10 nF	- (open)

1. *Respectively for VDD = 3.3 V and VDD = 1.8 V. In case of VDD = 3.3 V, a resistor divider formed by R2/(R3+R4) is required as the oscillator pin 1 (Enable) must be limited to a VDDA18AON (1.8 V) voltage, which supplies the external oscillator.*

8.2 Reset

The NRST reset signal in Figure 1 is active low. The reset sources include:

- Reset button
- Debugging tools via the *JTAG* connector

Refer to Section 2.4: Reset and power supply supervisor.

8.3 Boot mode

The boot option is configured by setting permanent wires or switches: SW4 (BOOT3), SW3 (BOOT2), SW2 (BOOT1) and SW1 (BOOT0) and internal *OTP*. Refer to Section 5.

If the *UART* boot uses one of the possible U(S)ARTx_RX pins (see Table 14), to avoid that a floating signal is sent to the host until the boot *ROM* has received and decoded the initialization character, it is required to have a 10 kΩ V_{DD} pull-up resistor on the respective U(S)ARTx_TX pin.

The U(S)ART_RX pin used for the boot or system console must not be left floating to avoid dummy serial character decoding. This could be ensured in either of two ways:

- Defining an internal pull-up resistance in a uBoot/Linux device tree
- Using a 10 kΩ V_{DD} pull-up resistor on the board

The table below shows the default pins used for each boot interface.

Note: Most could be changed using OTP settings. This table is for default OTP settings.

Table 14. Minimum set of default pins used during the boot *ROM* phase

Most can be changed using *OTP* settings. This table is for default *OTP* settings.

<table>
<tr><th>Interface</th><th colspan="3">Type</th><th>Signal</th><th>Pin</th><th>I/O supply domain</th></tr>
<tr><td rowspan="22">FMC</td><td rowspan="14" colspan="2">SLC NAND 8 bits</td><td rowspan="22">SLC NAND 16 bits</td><td>FMC_NOE</td><td>PE15</td><td rowspan="6">V_{DDIO2} [1]</td></tr>
<tr><td>FMC_RNB</td><td>PE13</td></tr>
<tr><td>FMC_NWE [2]</td><td>PE14</td></tr>
<tr><td>FMC_NCE1</td><td>PE12</td></tr>
<tr><td>FMC_ALE</td><td>PE8</td></tr>
<tr><td>FMC_CLE</td><td>PE11</td></tr>
<tr><td>FMC_D0</td><td>PE9</td><td rowspan="16">V_{DD}</td></tr>
<tr><td>FMC_D1</td><td>PE6</td></tr>
<tr><td>FMC_D2</td><td>PE7</td></tr>
<tr><td>FMC_D3</td><td>PD15</td></tr>
<tr><td>FMC_D4</td><td>PD14</td></tr>
<tr><td>FMC_D5</td><td>PB13</td></tr>
<tr><td>FMC_D6</td><td>PD12</td></tr>
<tr><td>FMC_D7</td><td>PB14</td></tr>
<tr><td rowspan="8" colspan="2">-</td><td>FMC_D8</td><td>PB5</td></tr>
<tr><td>FMC_D9</td><td>PB6</td></tr>
<tr><td>FMC_D10</td><td>PB7</td></tr>
<tr><td>FMC_D11</td><td>PD13</td></tr>
<tr><td>FMC_D12</td><td>PB2</td></tr>
<tr><td>FMC_D13</td><td>PB9</td></tr>
<tr><td>FMC_D14</td><td>PB11</td></tr>
<tr><td>FMC_D15</td><td>PB10</td></tr>
<tr><td rowspan="6">OCTOSPI1 port1</td><td rowspan="4">Serial NOR</td><td rowspan="4">Serial NAND</td><td rowspan="6">HyperFlash™</td><td>OCTOSPI1_CLK</td><td>PD0</td><td rowspan="6">V_{DDIO3}</td></tr>
<tr><td>OCTOSPI1_NCS1</td><td>PD3</td></tr>
<tr><td>OCTOSPI1_IO0</td><td>PD4</td></tr>
<tr><td>OCTOSPI1_IO1</td><td>PD5</td></tr>
<tr><td rowspan="2" colspan="2">-</td><td>OCTOSPI1_IO2</td><td>PD6</td></tr>
<tr><td>OCTOSPI1_IO3</td><td>PD7</td></tr>
</table>

Interface	Type		Signal	Pin	I/O supply domain
OCTOSPI1 port1	-	HyperFlash™	OCTOSPI1_IO4	PD8	V_{DDIO3}
			OCTOSPI1_IO5	PD9	
			OCTOSPI1_IO6	PD10	
			OCTOSPI1_IO7	PD11	
			OCTOSPI1_NCLK	PD1	
			OCTOSPI1_DQS	PD2	
SDMMC1	*SD* card or *e*•MMC		SDMMC1_CK	PE3	V_{DDIO1}
			SDMMC1_CMD	PE2	
			SDMMC1_D0 [3]	PE4	
SDMMC2[4]	*SD* card or *e*•MMC		SDMMC2_CK	PE14	V_{DDIO2}[1]
			SDMMC2_CMD	PE15	
			SDMMC2_D0 [3]	PE13	
USART2			USART2_RX	PA8	V_{DD}
			USART2_TX	PA4	
UART5			UART5_RX	PB15	V_{DD}
			UART5_TX	PA0	
USART6			USART6_RX	PF4	V_{DD}
			USART6_TX	PF5	

1. *Some FMC and SDMMC2 pins are shared: use of FMC is exclusive of use of SDMMC2.*
2. *On VFBGA225, FMC_NWE is mapped on GPIO PD13.*
3. *Only used as input by boot ROM.*
4. *On the VFBGA225 8 × 8 package, SDMMC2 is not a boot source.*

8.4 *SWD*/*JTAG* interface

The reference design shows the connections between the STM32MP21x devices and some standard connector (refer to Section 6: Debug management).

Note: *If available, it is recommended to connect the debugger probe system reset pin to NRST. This action permits resetting the application from the debugger.*

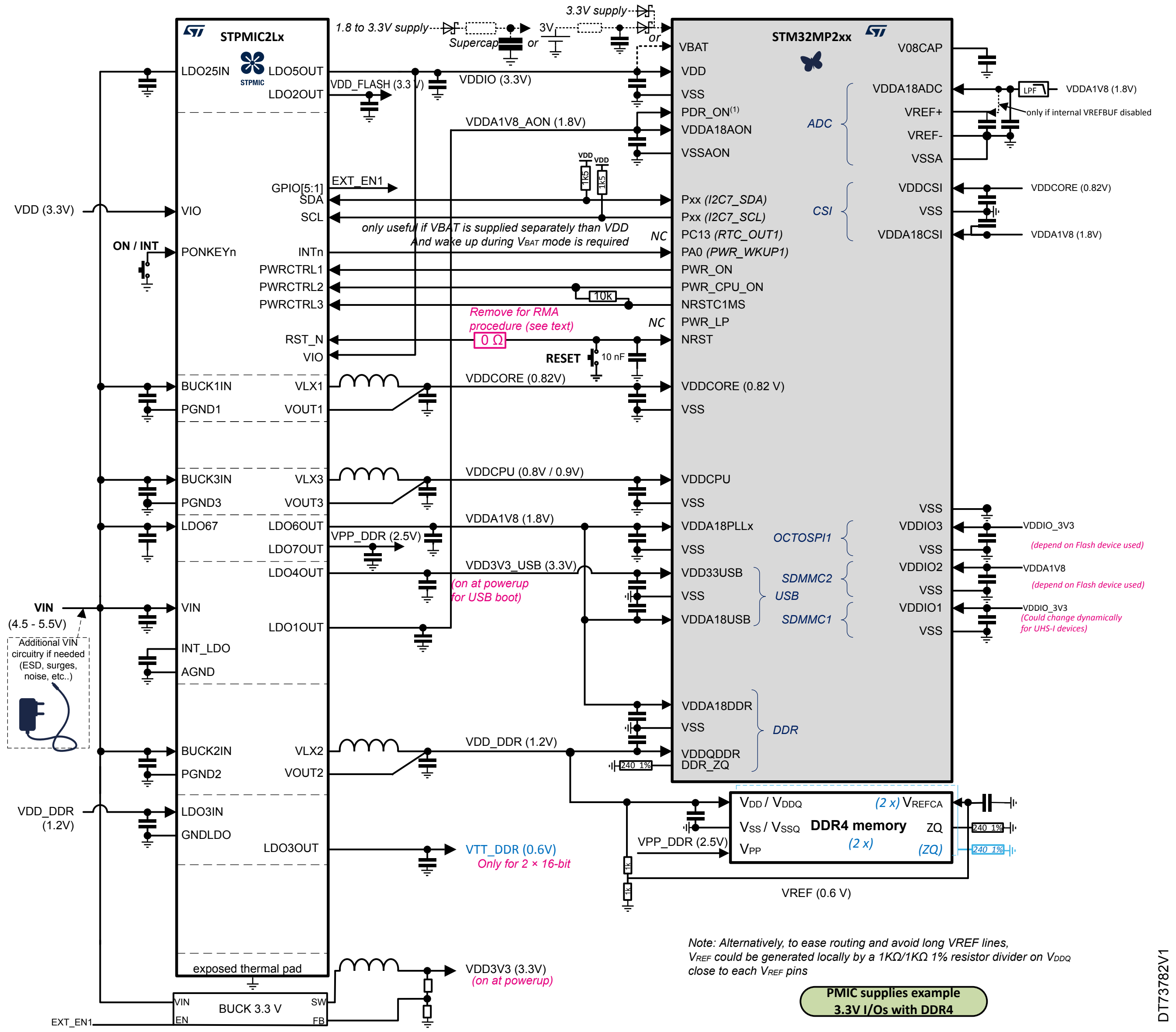
8.5 Power supply

The PMIC automatically applies power cycling when its RST_N pin is activated (for example, button, system reset). However, in the case of entering an RMA state, the power cycling must not be done. A 0 Ω resistance between NRST and PMIC RST_n pins can be provided and removed when using the procedure to enter an RMA state. Refer to Section 2.

8.5.1 Example of PMIC supplies for 3.3 V I/Os and DDR4

This reference design example targets a complex 3.3 V I/Os platform with DDR4 and high integration PMIC. Usually, all platform components can be powered by the PMIC. Full power supply control is supported thanks to PMIC I²C and side band signals. The Sleep mode, the Stop mode, and the Standby mode are supported. See the PMIC documentation for details of the PMIC components.

Figure 23. Example of PMIC supplies for 3.3 V I/Os and DDR4



1. PDR_ON must always be connected to VDDA18AON.

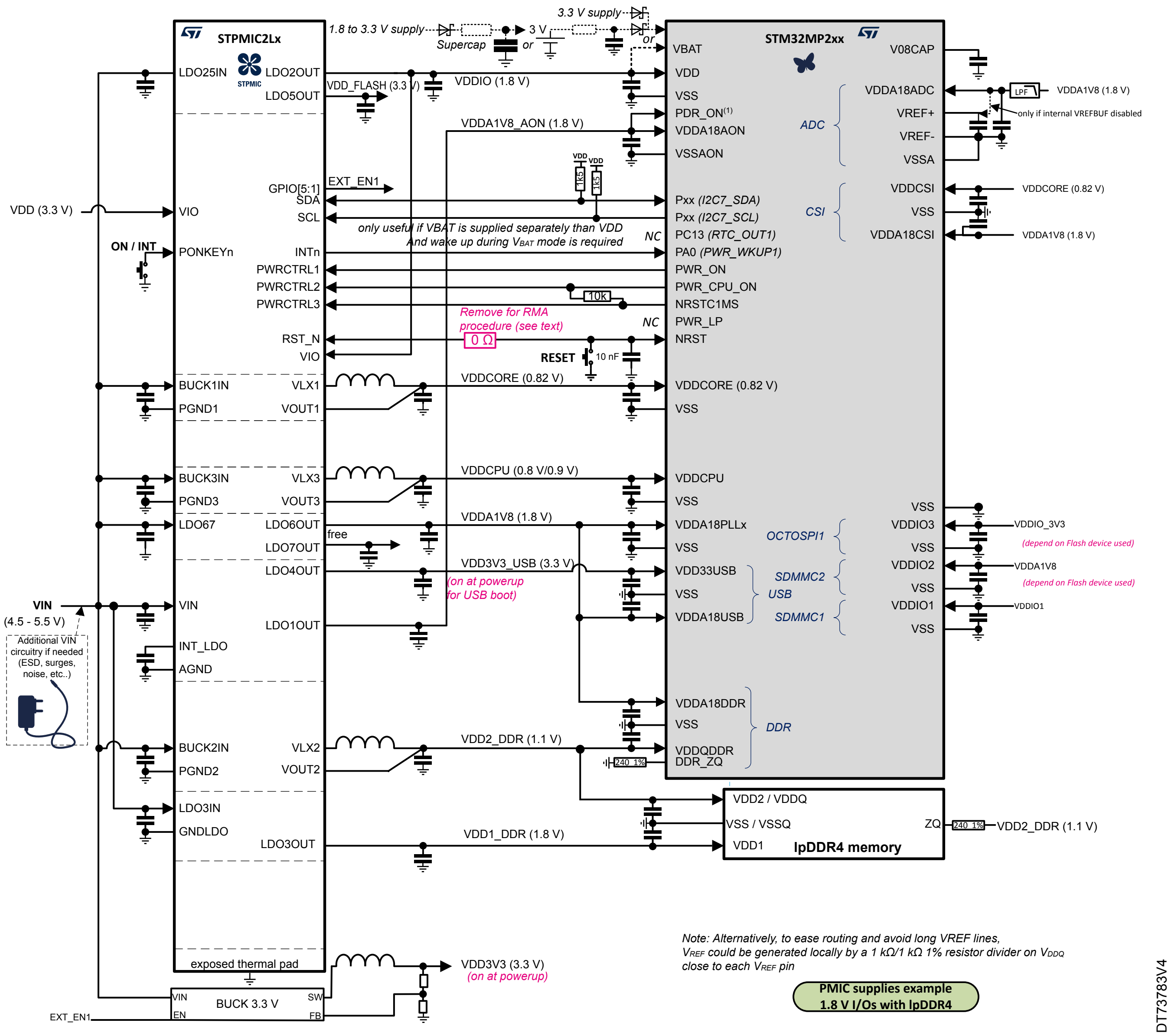
See Table 3. Amount of decoupling recommendation by package.

Note: On a given I²C bus, it is not possible to share I²C devices controlled from both secure and nonsecure software. For example: secure software controls the PMIC in STMicroelectronics standard deliveries, and that PMIC belongs to a distinct and secured I²C controller.

8.5.2 Example of *PMIC* supplies for 1.8 V I/Os with LPDDR4

This reference design example targets a complex 1.8 V I/Os platform with low power LPDDR4 and high integration *PMIC*. Usually, all platform components can be powered by the *PMIC*. The full power supply control is supported thanks to *PMIC* I^2C and side band signals. The Sleep mode, the Stop mode, and the Standby mode are supported as well as very-low power standby with LPDDR4 retention. See *PMIC* documentation for details of *PMIC* components.

Figure 24. Example of *PMIC* supplies for 1.8 V I/Os with LPDDR4



1. PDR_ON must always be connected to VDDA18AON.

Note: SD card supplies are not enabled in the STPMIC25A and STPMIC25B default NVM after shipment. They need to be specifically programmed in the customer production flow (using USB or UART boot) to allow SD card boot. Alternatively, if no SD card UHS-I is required, instead of using LDO7 and LDO8, the SD card supplies (VDDIO_SDCARD and VCC_SDCARD) could be both connected to a 2.7-3.6 V supply enabled with default the STPMIC25x NVM (for example, BUCK7 or LDO2).

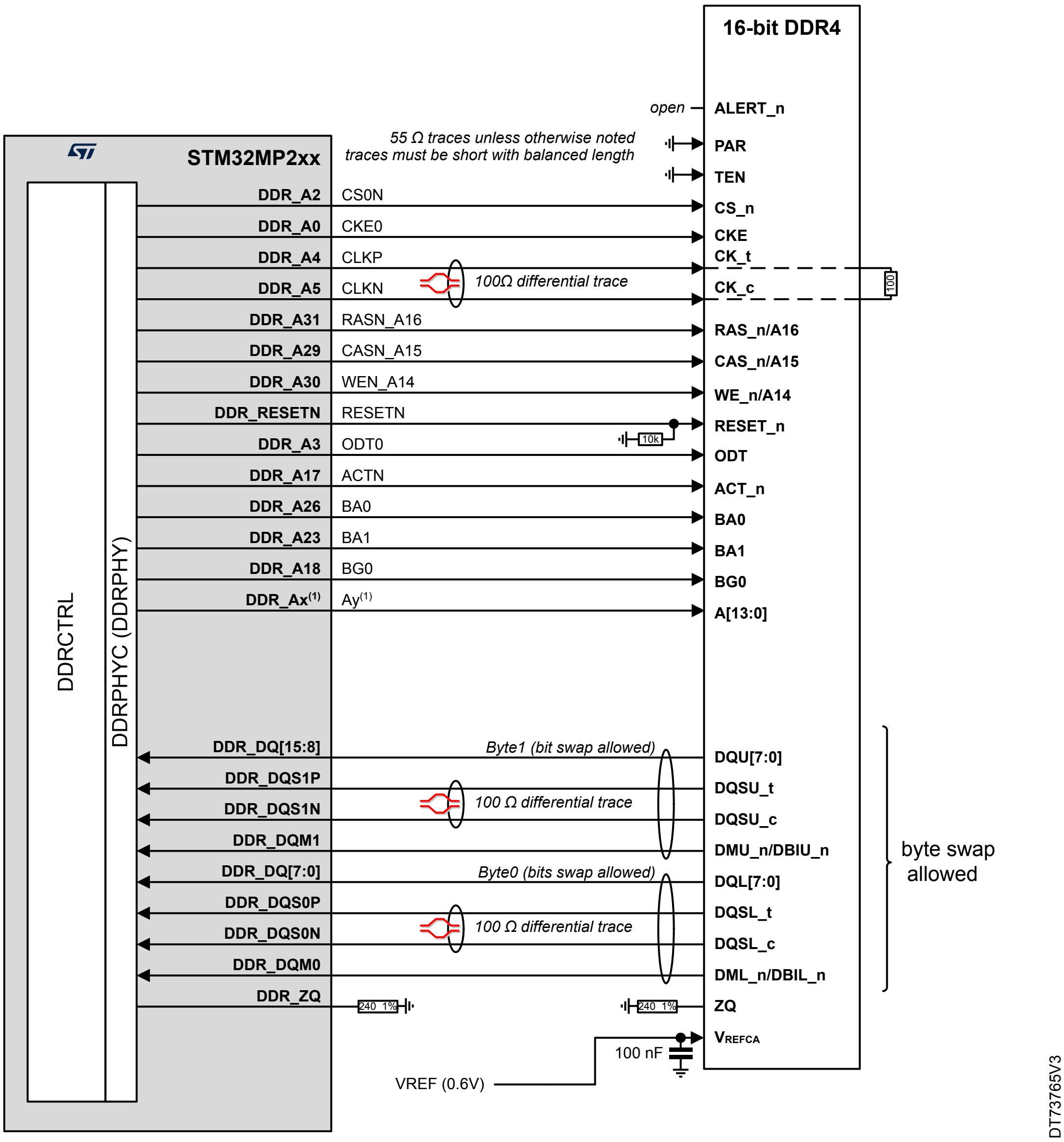
See Table 3. Amount of decoupling recommendation by package.

Note: *On a given I^2C bus, it is not possible to share I^2C devices controlled from both secure and nonsecure software. For example, secure software controls the PMIC in our standard deliveries and that PMIC belongs to a distinct and secured I^2C controller.*

8.6 DDR4 SDRAM

A 240 Ω 1% resistor must be connected between DDR_ZQ and V_{SS}. This resistor must not be shared with the ZQ resistors required on each DDR4 component.

Figure 25. 16-bit DDR4 connection example



Note:
1. *See the table below.*
2. *Alternatively, to ease routing and avoid long V_{REF} lines, V_{REF} can be generated locally by a 1 kΩ 1% resistor divider on V_{DDQ} close to each VREF pin.*
3. *Supplies and decoupling capacitors not shown.*
4. *Detailed routing examples are described in the corresponding application note .*

Table 15. **16-bit DDR4 pin mapping**

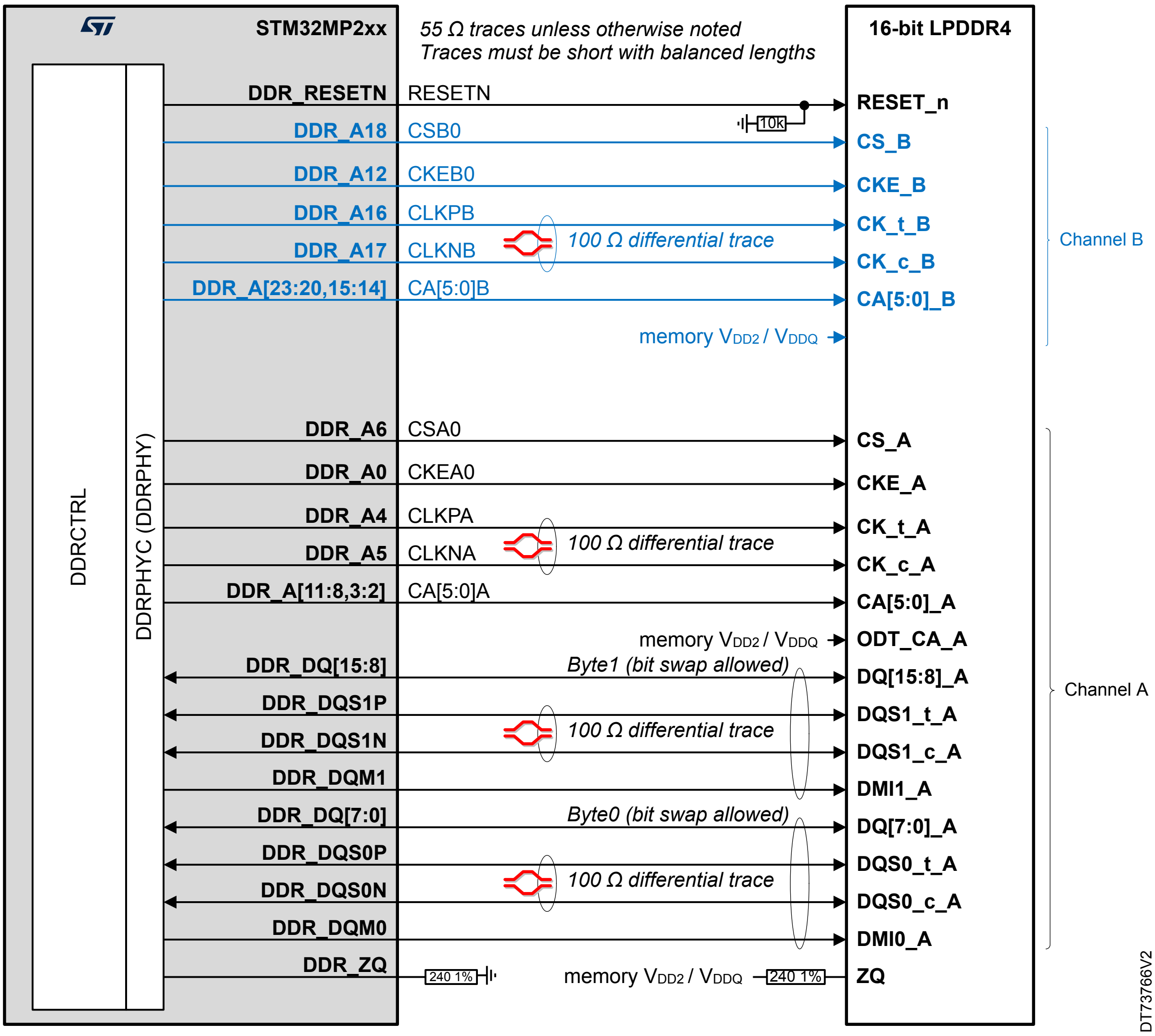
DDRCTRL pin	Signal name	DDR4 ×16	Comments
DDR_RESETN	RESETN	RESET_n	10 kΩ pull-down resistor to memory VSS
DDR_ZQ	-	-	240 Ω 1% to VSS
-	ZQ	-	240 Ω 1% to memory VSS
DDR_VREF	-	-	Not used. Must be left open.
-	VREF	VREFCA	0.6 V reference voltage
-	-	PAR	Not used. Must be connected to memory VSS.
-	-	TEN	
-	-	ALERT_n	Not used. Must be left open.
DDR_A0	CKE0	CKE	-
DDR_A1	CKE1	-	Not used. Must be left open.
DDR_A2	CS0N	CS_n	-
DDR_A3	ODT0	ODT	-
DDR_A4	CLKP	CK_t	-
DDR_A5	CLKN	CK_c	-
DDR_A6	CS1N	-	Not used. Must be left open.
DDR_A7	ODT1	-	Not used. Must be left open.
DDR_A8	A9	A9	-
DDR_A9	A12_BCN	A12/BC_n	-
DDR_A10	A11	A11	-
DDR_A11	A7	A7	-
DDR_A12	A8	A8	-
DDR_A13	A6	A6	-
DDR_A14	A5	A5	-
DDR_A15	A4	A4	-
DDR_A16	not used	-	-
DDR_A17	ACTN	ACT_n	-
DDR_A18	BG0	BG0	-
DDR_A19	not used	-	Not used. Must be left open.
DDR_A20	A3	A3	-
DDR_A21	A2	A2	-
DDR_A22	A1	A1	-
DDR_A23	BA1	BA1	-
DDR_A24	-	-	-
DDR_A25	A13	A13	-
DDR_A26	BA0	BA0	-
DDR_A27	A10_AP	A10/AP	-
DDR_A28	A0	A0	-
DDR_A29	CASN_A15	CAS_n/A15	-
DDR_A30	WEN_A14	WE_n/A14	-
DDR_A31	RASN_A16	RAS_n/A16	-

DDRCTRL pin	Signal name	DDR4 ×16	Comments	
DDR_DQ[16:8]	DQ[15:8]	DQU[7:0]	Data bits could be swapped within a given byte.	Byte1 could be swapped with other bytes.
DDR_DQM1	DQM1	DMU_n/DBIU_n		
DDR_DQS1P	DQS1P	DQSU_t		
DDR_DQS1N	DQS1N	DQSU_c		
DDR_DQ[7:0]	DQ[7:0]	DQL[7:0]	Data bits could be swapped within a same byte.	Byte0 could be swapped with other bytes.
DDR_DQM0	DQM0	DML_n/DBIL_n		
DDR_DQS0P	DQS0P	DQSL_t		
DDR_DQS0N	DQS0N	DQSL_c		

8.7 LPDDR4 SDRAM

A 240 Ω 1% resistor must be connected between DDR_ZQ and V_{SS}. This resistor must not be shared with one or more ZQ resistors required on the LPDDR4 component.

Figure 26. **LPDDR4 connection example**



Note:
1. *Supplies and decoupling capacitors are not shown.*
2. *Detailed routing examples are described in the corresponding application note .*

Table 16. LPDDR4 pin mapping

DDRCTRL pin	Signal name	LPDDR4	Comments
DDR_RESETN	RESETN	RESET_n	10 kΩ pull-down resistor to memory VSS
DDR_ZQ	-	-	240 Ω 1% to VSS
-	-	ZQ	240 Ω 1% to memory VDD2/VDDQ
-	-	ODT_CA_A	Must be connected to memory VDD2/VDDQ (CA terminations enabled by default, could be disabled later inside memory settings).
-	-	ODT_CA_B	
DDR_VREF	-	-	(1)
DDR_A0	CKEA0	CKE_A	-
DDR_A2	CA0A	CA0_A	-
DDR_A3	CA1A	CA1_A	-
DDR_A4	CLKPA	CK_t_A	-
DDR_A5	CLKNA	CK_c_A	-
DDR_A6	CSA0	CS_A	-
DDR_A8	CA2A	CA2_A	-
DDR_A9	CA3A	CA3_A	-
DDR_A10	CA4A	CA4_A	-
DDR_A11	CA5A	CA5_A	-
DDR_A12	CKEB0	CKE_B	-
DDR_A14	CA0B	CA0_B	-
DDR_A15	CA1B	CA1_B	-
DDR_A16	CLKPB	CK_t_B	-
DDR_A17	CLKNB	CK_c_B	-
DDR_A18	CSB0	CS_B	-
DDR_A20	CA2B	CA2_B	-
DDR_A21	CA3B	CA3_B	-
DDR_A22	CA4B	CA4_B	-
DDR_A23	CA5B	CA5_B	-
DDR_A24	-	-	-
DDR_A25	-	-	(1)
DDR_A26	-	-	(1)
DDR_A27	-	-	(1)
DDR_A28	-	-	(1)
DDR_A29	-	-	(1)
DDR_A30	-	-	(1)
DDR_A31	-	-	(1)
DDR_DQ[16:8]	DQ[15:8]	DQ[15:8]_A	Data bits can be swapped within a given byte with an adequate DqLnSel setting inside DDRPHYC. Byte lanes within a channel (0 and 1) can be swapped with adequate programming of derate_byte used for MR4 polling by *DDRCTRL* for T derating polling. Swapping byte lanes between channels is not allowed.
DDR_DQM1	DQM1	DMI1_A	
DDR_DQS1P	DQS1P	DQS1_t_A	
DDR_DQS1N	DQS1N	DQS1_c_A	
DDR_DQ[7:0]	DQ[7:0]	DQ[7:0]_A	
DDR_DQM0	DQM0	DMI0_A	

DDRCTRL pin	Signal name	LPDDR4	Comments
DDR_DQS0P	DQS0P	DQS0_t_A	Data bits can be swapped within a given byte with an adequate DqLnSel setting inside DDRPHYC. Byte lanes within a channel (0 and 1) can be swapped with adequate programming of derate_byte used for MR4 polling by *DDRCTRL* for T derating polling. Swapping byte lanes between channels is not allowed.
DDR_DQS0N	DQS0N	DQS0_c_A	

1. *Must be left open if not used.*

8.8 SD card

Note: *As boot is always done in 'Standard' mode (3 V I/Os), if the card is used by the application in UHS-I, a power cycle on the card supply is required after a Reset mode or Standby mode. NRSTC1MS could be used for that purpose.*

Note that a good signal integrity is dependent on board, *GPIO* strength settings (GPIO_OSPEEDR registers) and V_{DD} voltage.

When using V_{DDIO1} = 1.8 V, setting VDDIOxVRSEL might be required to ensure the adequate speed on pins used on SDMMC1 outputs.

If needed, the impedance matching resistor must be placed as close as possible to the output driver pin. The values in the example below must work in most cases, but could be tailored to I/O drive strengths and *PCB* impedance.

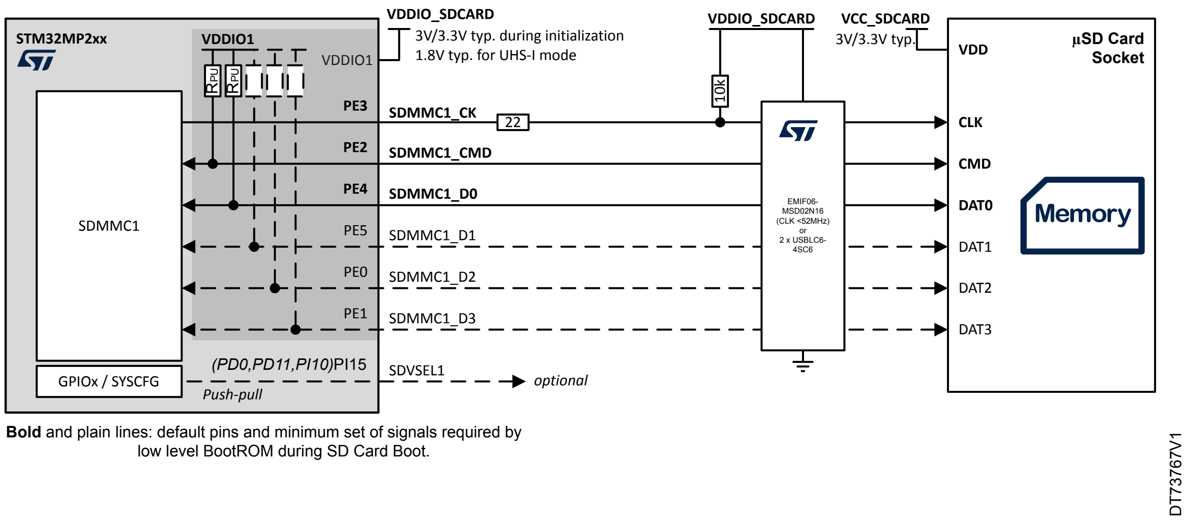
Before the V_{CC_SDCARD} shutdown (for example before a Standby mode), all signals going to the card must be set to 0 or high-Z by the SDMMC1 driver.

The example is independent from MPU I/O voltage V_{DD} and relies on variable VDDIO1 that could be set, either to 3.0 V/3.3 V, or 1.8 V typ. using one of the followings:

- SDVSEL1 ('0' or high-Z = 3 V/3.3 V (default), '1' = 1.8 V) connected to an external regulator or other component managing the V_{DDIO1} voltage.
- A regular *GPIO* output connected to an external regulator or other component managing the V_{DDIO1} voltage.
- An *I²C* bus in case of use with *PMIC*.

If a programmable V_{DDIO_SDCARD} is not available in the platform, V_{DDIO1} could be connected to V_{CC_SDCARD}. In that case, UHS-I is not supported.

Figure 27. SD-Card with embedded level shifter connection



Note: *When switching to UHS-I mode (V_{DDIO1} = 1.8 V), VDDIOxVRSEL must be set only when V_{DDIO1} is within the 1.8 V allowed range. In case of reset of the SD card to the legacy 3 V/3.3 V range, to avoid damage on the I/Os, VDDIOxVRSEL must be cleared before the voltage is outside the 1.8 V allowed range.*

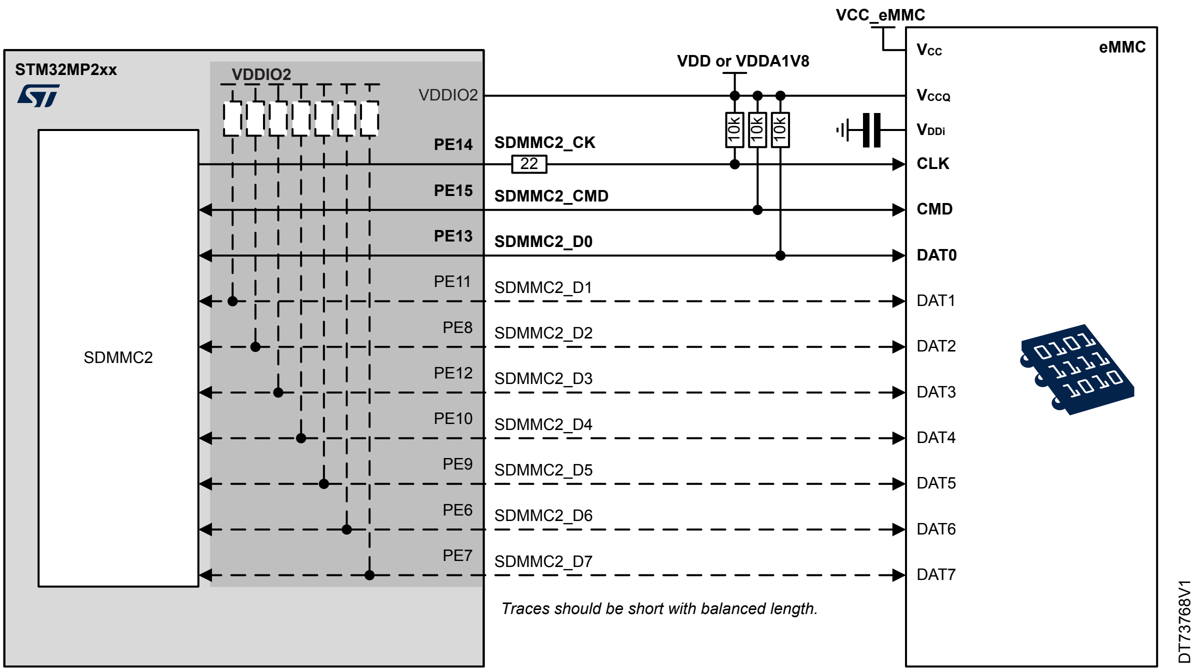
8.9 eMMC flash

Note that a good signal integrity is dependent on board, *GPIO* strength settings (GPIO_OSPEEDR registers), and V_{DDIO2} voltage.

When using V_{DDIO2} = 1.8 V, a setting of VDDIOxVRSEL could be required to ensure the adequate speed on pins used on SDMMC2 outputs.

If needed, the impedance matching resistor should be placed as close as possible of the output driver pin. The values in the example below must work in most cases, but could be tailored to I/O drive strengths and *PCB* impedance.

Figure 28. eMMC™ connection example



Note:
1. *In bold and plain lines, default pins and minimum set of signals required by low level boot ROM during eMMC boot.*
2. *Decoupling capacitors are not shown.*
3. *The VFBGA225 8 × 8 package only supports four bits on SDMMC2 with SDMMC2_CK remapped on PE6 (PE14 is not available).*
4. *The VFBGA225 8 × 8 package DOES NOT support SDMMC2 as a boot source. eMMC boot can be connected to SDMMC1 using either of the two:*
   – *4 bits on the VDDIO1 supply*
   – *8 bits on the VDDIO1 and VDDIO3 supplies*

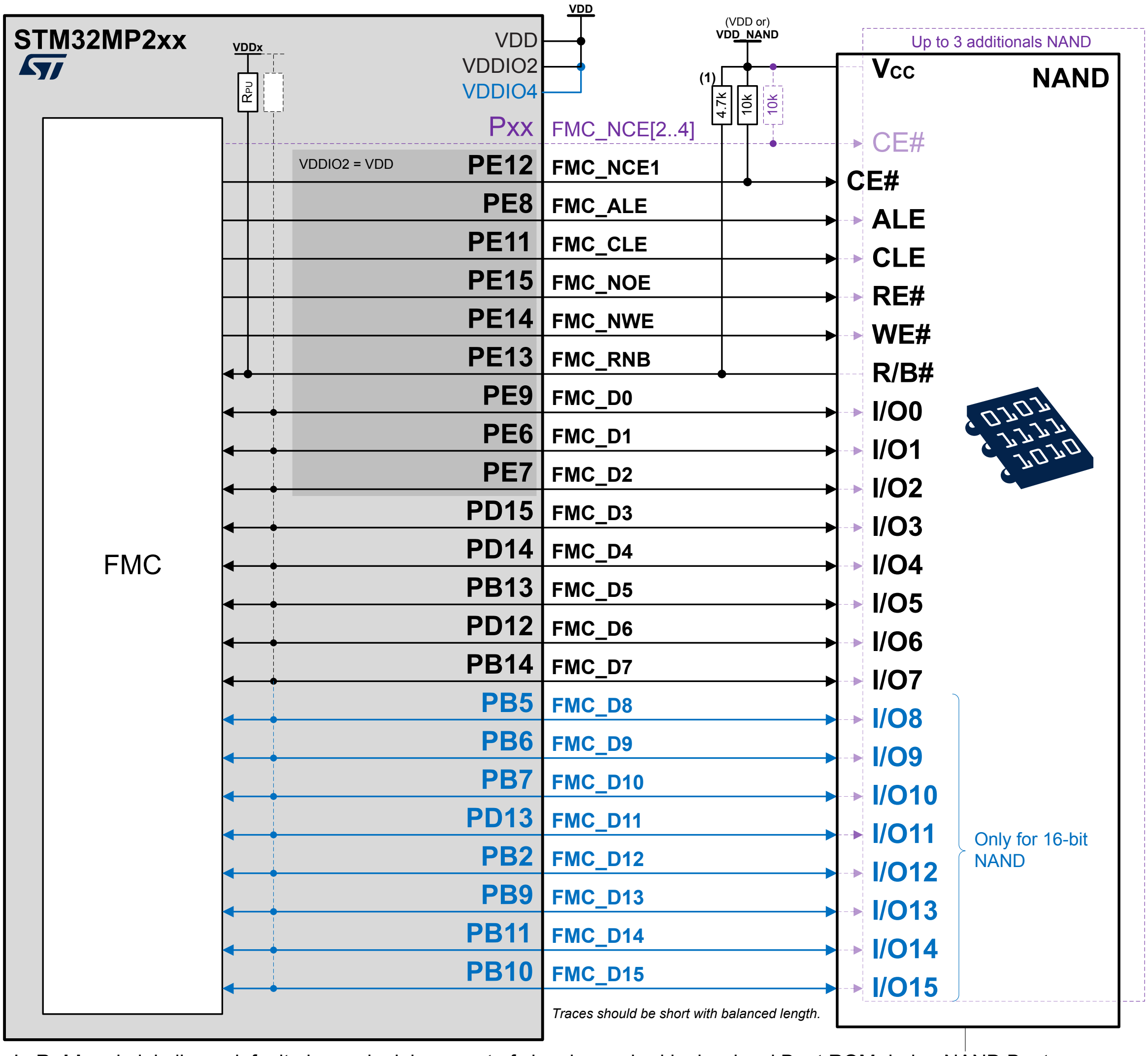
   Hence, using eMMC at 1.8 V is only possible if all I/Os on VDDIO3 are at 1.8 V.

8.10 SLC NAND flash memory

Up to four 8 or 16-bit SLC NAND memory devices (CE# = FMC_NCE1, FMC_NCE2, FMC_NCE3 or FMC_NCE4) are supported.

Note that boot is only done on the SLC NAND memory device connected to FMC_NCE1.

Figure 29. SLC NAND flash memory connection



In **Bold** and plain lines, default pins and minimum set of signals required by low level Boot ROM during NAND Boot.

Note:

1. *Pull-up on FMC_RNB is optional. The 4.7 kΩ value (lower than internal R_{PU}) can give better signal rise time that could reduce the wait time seen by FMC.*
2. *NAND flash memory V_{CC} supply (V_{DD_NAND}) must be cut for >1ms in order to allow reboot (on Reset or Standby mode exit). See NAND flash memory device for details.*
3. *Decoupling capacitors are not shown.*
4. *Only single level cell (SLC) NAND flash memory is supported, with either hamming, BCH4 or BCH8 error correction algorithms.*
5. *VFBGA225 8x8 package only supports 8-bit FMC (PB2, PB5, PB6, PB7, PB9, PB10 not available). FMC_NWE is remapped on PD13 (PE14 is not available).*

8.11 Serial NOR/NAND flash memory

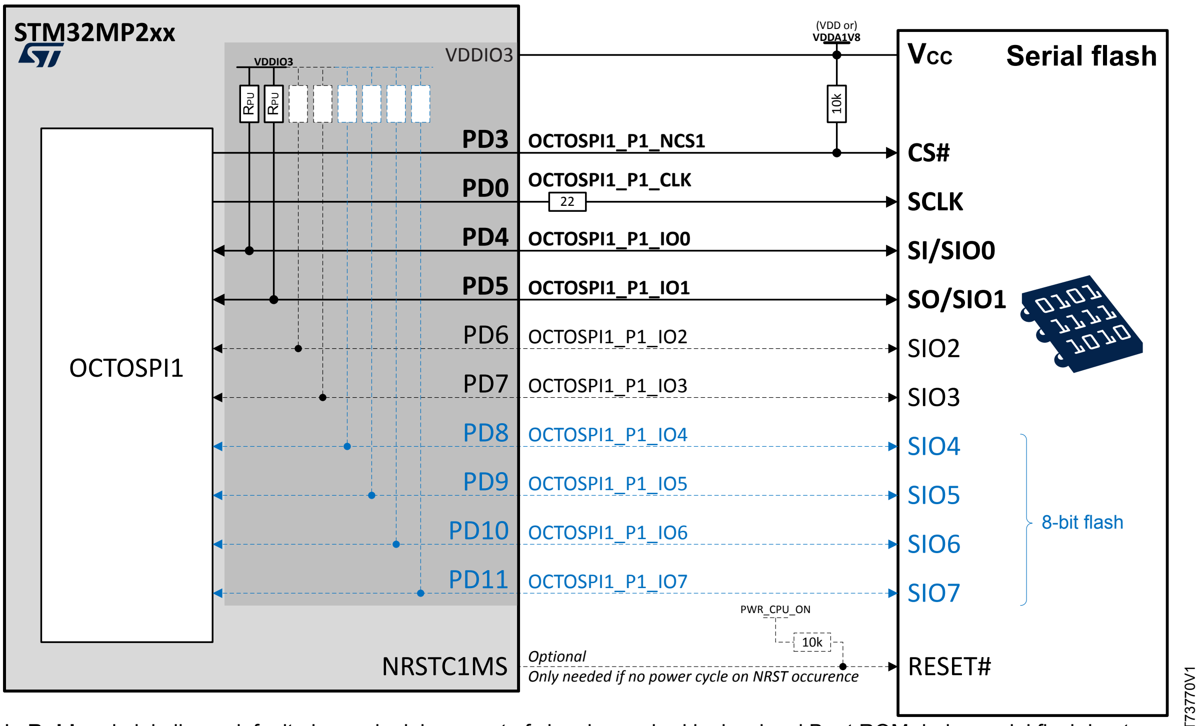
As boot is always done in *SPI* mode, if the serial flash memory is set by the application in multiple data lines, or if the sector addressing has been changed, a power cycle on a serial flash memory supply is required after Reset or Standby mode exit.

Note: A good signal integrity is dependent on the board, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DDIO3} voltage.

When using V_{DDIO3}= 1.8 V, a setting of VDDIOxVRSEL could be required to ensure the adequate speed on pins used on OCTOSPI1 outputs.

If needed, the impedance matching resistor must be placed as close as possible of the output driver pin. The values in the example below work in most cases, but can be tailored to I/O drive strengths and *PCB* impedance.

Figure 30. Serial flash memory connection example



In **Bold** and plain lines, default pins and minimum set of signals required by low level Boot ROM during serial flash boot.

Note:
1. *If RESET# is not connected, the serial flash memory supply (VCC) must be cut for >1 ms to allow reboot (on reset or standby exit). See serial flash memory device documentation for details.*
2. *Decoupling capacitors are not shown.*
3. *During SPI mode boot using SI/SO, some serial memories could use I/O2 and I/O3 pins as an additional feature like HOLD. To make this device boot, it might be necessary to set those pins to an inactive level by adding external pull-ups or by defining an internal pull-up during boot using OTP.*

In case the memory I/O power supply VCC could be shut down independently than VDD, and NRSTC1MS is used for other purposes or other voltages on the platform, NRSTC1MS must not be directly connected to the memory reset pin and the following options could be used:

- Memory reset pin left open (assuming the memory has an internal power on reset and the NRSTC1MS is used to generate a power cycle on the memory)
- Connected through a Schottky diode with the cathode on the NRSTC1MS side

Otherwise, the NRSTC1MS might be pulled low by memory internal protections when memory I/O supply is not present (which could cause some unwanted reset of other platform devices using the NRSTC1MS pin).

Refer to memory documentation to verify the memory reset pin requirements: especially the presence of internal power on reset and/or internal pull-up on the reset pin).

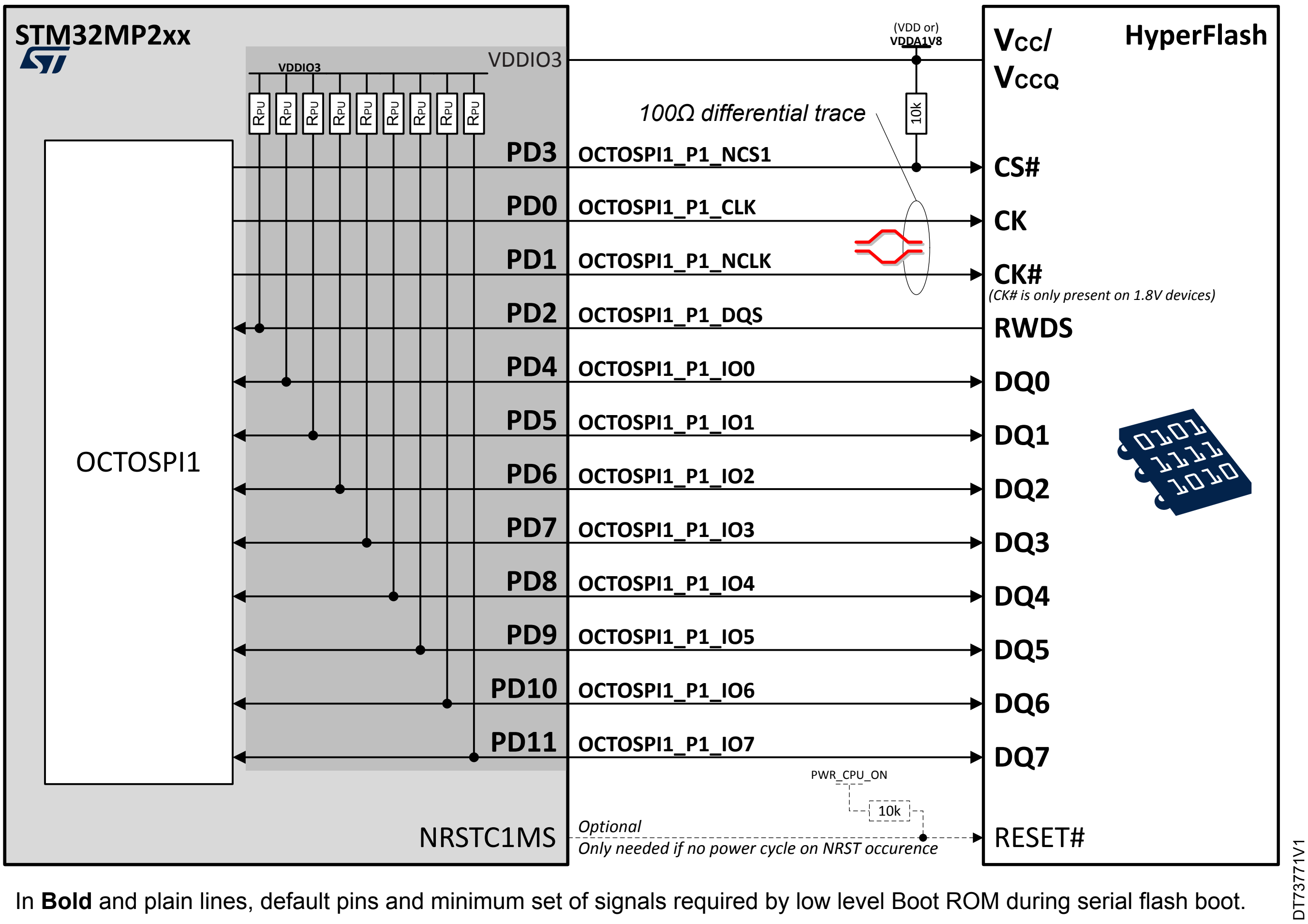
8.12 HyperFlash™

Note: If the serial flash memory mode set by the application is not compatible with the expected mode by the boot ROM, a power cycle on the serial flash memory supply is required after Reset or Standby mode exit. NRSTC1MS could be used for that purpose.

Note that a good signal integrity is dependent on the board, *GPIO* strength settings (GPIO_OSPEEDR registers), and V_{DDIO3} voltage.

When using V_{DDIO3}= 1.8 V, a setting of VDDIOxVRSEL could be required to ensure the adequate speed on pins used on OCTOSPI1 outputs.

Figure 31. HyperFlash™ connection example



In **Bold** and plain lines, default pins and minimum set of signals required by low level Boot ROM during serial flash boot.

Note:
1. *If RESET# is not connected, HyperFlash™ supply (V_{CC}/V_{CCQ}) must be cut for >1 ms to allow reboot (on Reset or Standby mode exit). See HyperFlash™ device documentation for details.*
2. *Decoupling capacitors are not shown.*

8.13 USB

Multiple *USB* options are possible. Examples are listed below:

- 1 × high-speed *USB* device (Figure 32 or Figure 33)
- 1 × high-speed *USB* device (Figure 32 or Figure 33) + 1 × USB high-speed host (Figure 34)
- 1 × SuperSpeed *USB* host (Figure 1), see note below
- 1 × SuperSpeed *USB* dual-role
- 1 × SuperSpeed *USB* dual-role + 1 × USB high-speed host (Figure 34)

The use case of multiple high-speed *USB* hosts using an external USB hub component are not described here.

Note: In case of on-board flash memory programming using the STM32CubeProgrammer, at least one USB with device capabilities is required. This is achieved with Figure 32, Figure 33. See also Figure 34.

Table 17. *USB* high-speed *PCB* routing recommendations

Recommendation	Min	Typ	Max	Unit
Differential impedance	76.5	90	103.5	Ω
Single-ended impedance	38.25	45	51.75	Ω
Length matching within a pair (including package[1])	-50	-	+50	mils
	-1.27	-	+1.27	mm
Max traces length (up to connector or first active component)	-	-	8	inches
	-	-	203	mm
Max number of vias (recommended value)	-	-	2	-
Distance between any differential trace and other signals	S-2S	S-3S or more		[2]
Do no route over power plane split. No stubs (point to point only). No right angles				

1. *See High-speed differential lane PCB track length matching for PCB track length matching details.*
2. *Definition could be found, for instance, in the DDR memory routing guidelines.*

8.13.1 USB high-speed device (OTG)

A 200 Ω 1% resistor must be connected between USB3DR_TXRTUNE and V_{SS}.

- For *GPIO* V_{DD} (or V_{DDIOx}) supply of 3.3 V typical:
  – Ra = 82 kΩ (to GND)
  – Rb = 33 kΩ (to VBUS)
- For *GPIO* V_{DD} (or V_{DDIOx}) supply of 1.8 V typical:
  – Ra = 68 kΩ (to GND)
  – Rb = 82 kΩ (to VBUS)

Refer to the application note for more details on VBUS detection with *GPIO*.

Figure 32. USB high-speed device with Micro-B connector example

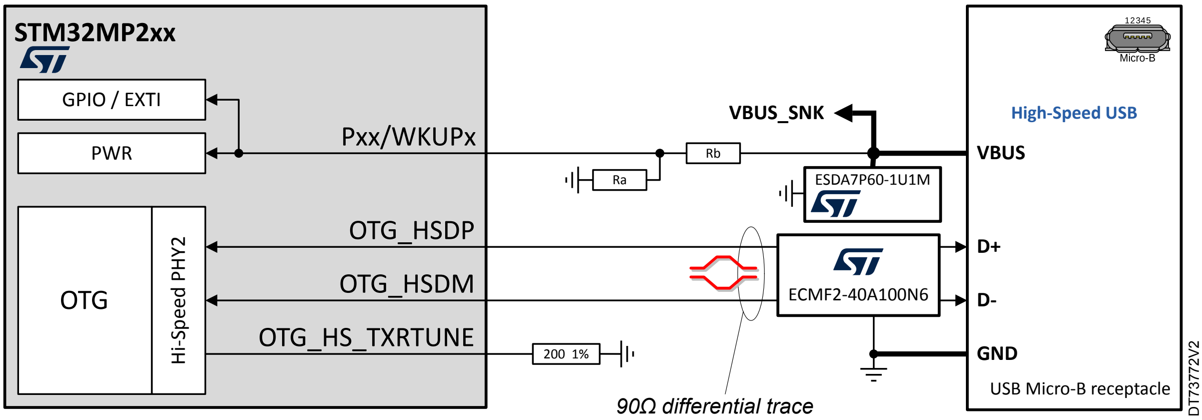
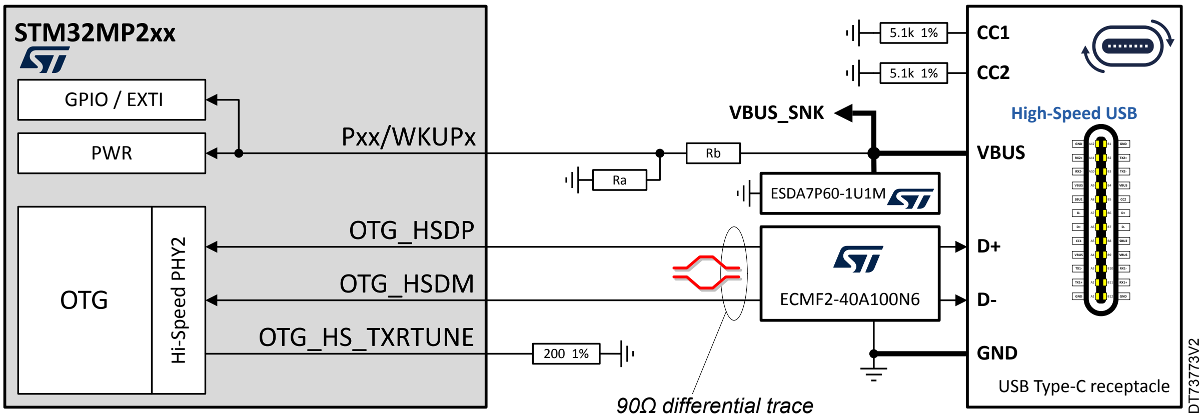


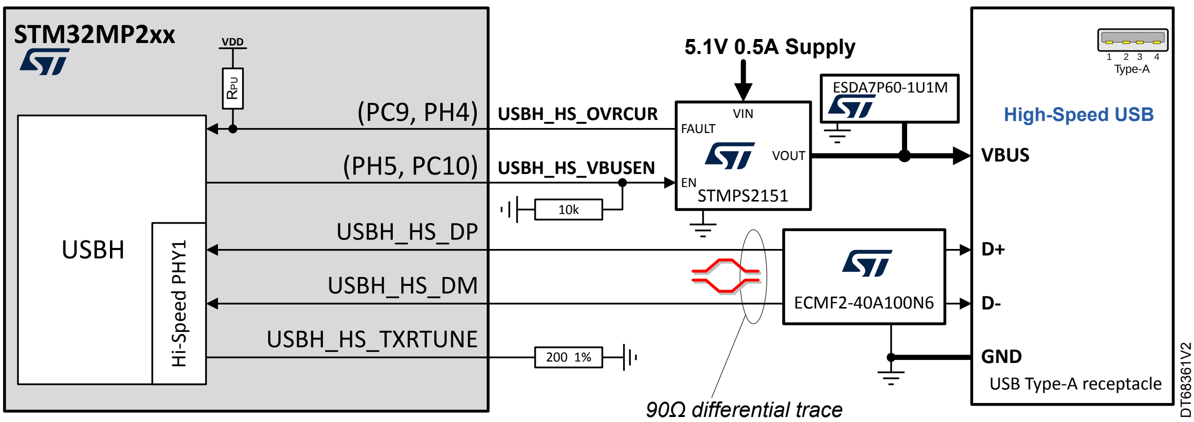
Figure 33. USB high-speed device with Type-C connector example



8.13.2 USB high-speed host with Type-A connector (USBH)

A 200 Ω 1% resistor should be connected between USBH_HS_TXRTUNE and V_{SS}.

Figure 34. USB high-speed host example



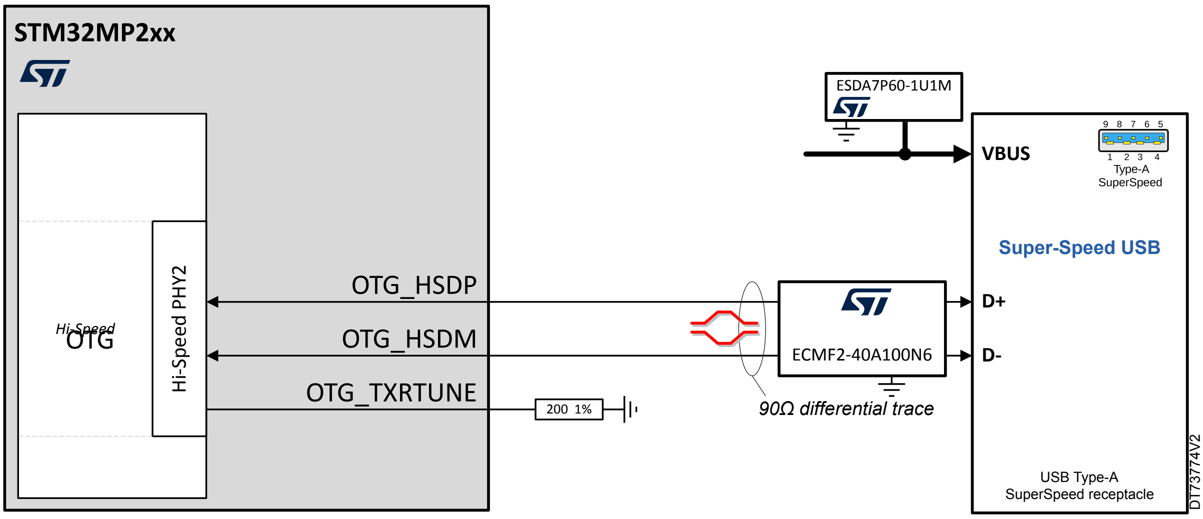
Note: VBUS 1A is also possible using STMPS2171 instead of STMPS2151.

8.13.3 USB high-speed host with Type-A connector (OTG)

A 200 Ω 1% resistor must be connected between OTG_TXRTUNE and V_{SS}.

Note: OTG high-speed device is required by boot ROM when connected to a PC computer running a STM32CubeProgrammer in USB mode, for example, to program board flash memory devices. This is still possible with this USB SuperSpeed host use-case by using a nonstandard Type-A/Type-A USB high-speed cable. It is possible only during STM32CubeProgrammer usage, and might need specific uBoot settings to allow this nonstandard usage.

Figure 35. USB high-speed host connection example



8.14 Ethernet

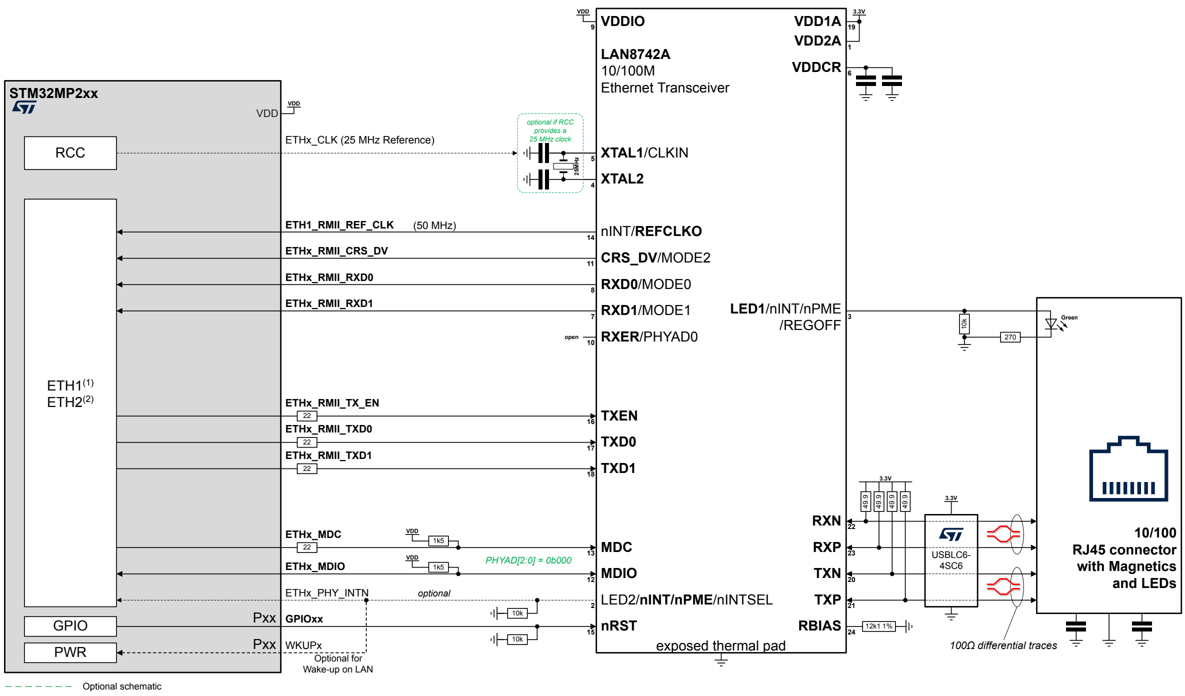
8.14.1 10/100 Mbit/s Ethernet

Note: *A good signal integrity is dependent on the board, the GPIO strength settings (GPIO_OSPEEDR registers), and the V_{DD} voltage.*

When using VDD = 1.8 V, a setting of VDDIOxVRSEL could be required to ensure the adequate speed on the pins used on the ETHx outputs.

If needed, the impedance matching resistors must be placed as close as possible to the output driver pin. Values in the example below work in most cases, but can be tailored to each side I/O drive strength and *PCB* impedance.

Figure 36. 10/100 Mbit/s Ethernet *PHY* connection example



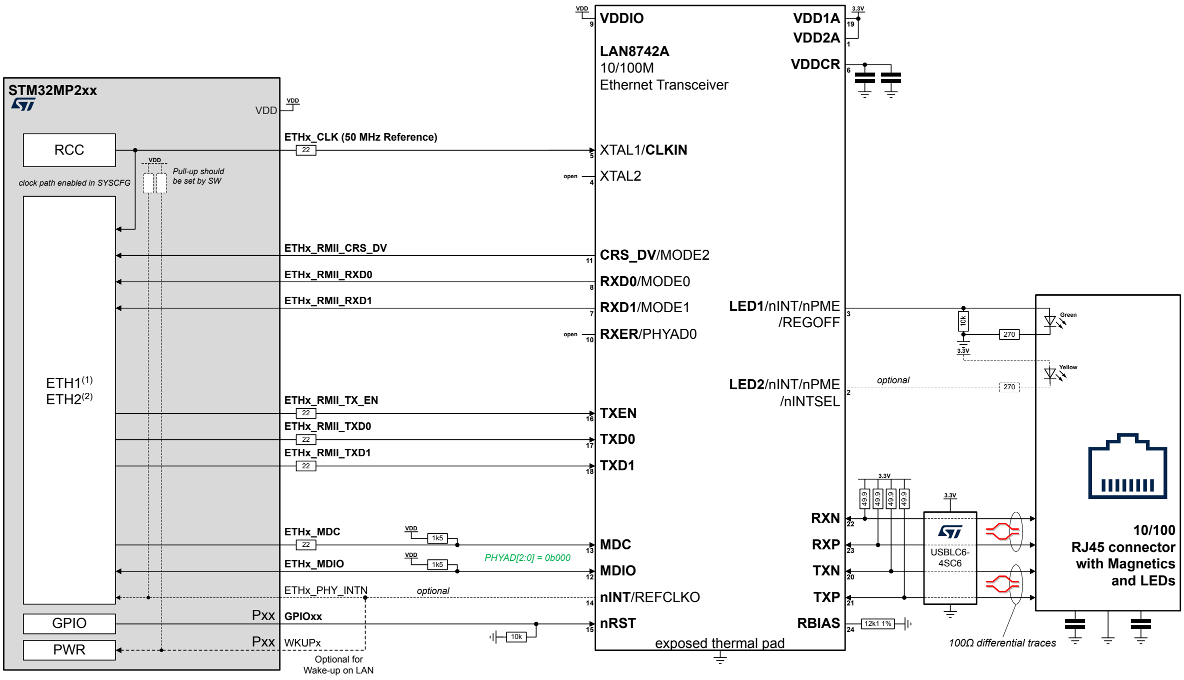
1. *ETH2 is not available on some part numbers.*
2. *Decoupling capacitors not shown.*

Note:

- *As RCC cannot provide the 25 MHz reference clock to the PHY during low-power modes, the dedicated 25 MHz crystal is required on the PHY in the case a wake-up on LAN (WOL) is needed for the platform.*
- *Setting the RCC PLLs to get a 25 MHz output for PHY clocking could constrain other RCC frequencies. In that case, it is more flexible to put a dedicated 25 MHz crystal on the PHY.*

Alternatively, if the *PHY* allows it and if *RCC* can provide a precise 50 MHz clock (to be checked with respect to the *HSE* quartz frequency and other *RCC* peripheral/core clock frequency settings), the STM32MP21x devices can provide a 50 MHz ETH_CLK to the *PHY*. In this case, the REF_CLK is left unconnected on both sides. This saves BOM and area as well as some power on a few *PHY*s.

Figure 37. 10/100 Mbit/s Ethernet *PHY* connection (with REFCLK from *RCC*)



1. *ETH2 is not available on some part numbers.*
2. *Decoupling capacitors are not shown.*

Note:
- *As the RCC cannot provide the 50 MHz reference clock to the PHY during low-power modes, this option is not possible in the case a wake-up on LAN (WOL) is needed for the platform.*
- *Setting the RCC PLLs to get a 50 MHz output for PHY clocking could constrain other RCC frequencies. In that case, this option is not possible.*

Table 18. *ETH* RMII pins

Pin name	(1)	ETH1	ETH2(2)	ETH3	comments
ETHx_CLK	→	PF3, PF5, PF8	PF4, PG3	-(3)	Optional 25 MHz or 50 MHz reference(4)
ETHx_RMII_REF_CLK	←	PA14	PC0, PF6	PA5	Optional if ETHx_CLK provides 50 MHz
ETHx_RMII_CRS_DV	←	PA11	PC3, PF8	PA2	-
ETHx_RMII_RXD0	←	PF1	PG0	PA9	-
ETHx_RMII_RXD1	←	PC2	PC12	PA10	-
ETHx_RMII_TX_EN	→	PA13	PC4	PA3	-
ETHx_RMII_TXD0	→	PA15	PC7	PA6	-
ETHx_RMII_TXD1	→	PC1	PC8	PA7	-
ETHx_MDC	→	PA9, PF0, PF4	PC6, PG4, PH10	-	-
ETHx_MDIO	→ ←	PA10, PF2, PF5	PC5, PF9, PH11	-	-
ETHx_PHY_INTN	←	PA12, PC6, PF5	PF5, PG3	PA1	Optional

1. *Signal direction: → MPU to PHY, ← PHY to MPU*
2. *Not available on some part numbers*
3. *If needed, ETH1_CLK must be used.*
4. *As the RCC cannot provide the reference clock to the PHY during low-power modes, a dedicated 25 MHz crystal is required on the PHY if wake-up on LAN (WOL) is needed for the platform.*

8.14.2 Gigabit Ethernet

Note that a good signal integrity is dependent on board, *GPIO* strength settings (GPIO_OSPEEDR registers), and V_{DD} voltage.

When using V_{DD} = 1.8 V, a setting of VDDIOxRSEL could be required to ensure the adequate speed on pins used on ETHx outputs.

If needed, the impedance matching resistors must be placed as close as possible of the output driver pin. Values in the example below must work in most cases, but could be tailored to each side I/O drive strengths and *PCB* impedance.

Figure 38. Gigabit Ethernet *PHY* connection with VDD = 3.3 V (RTL8211F)

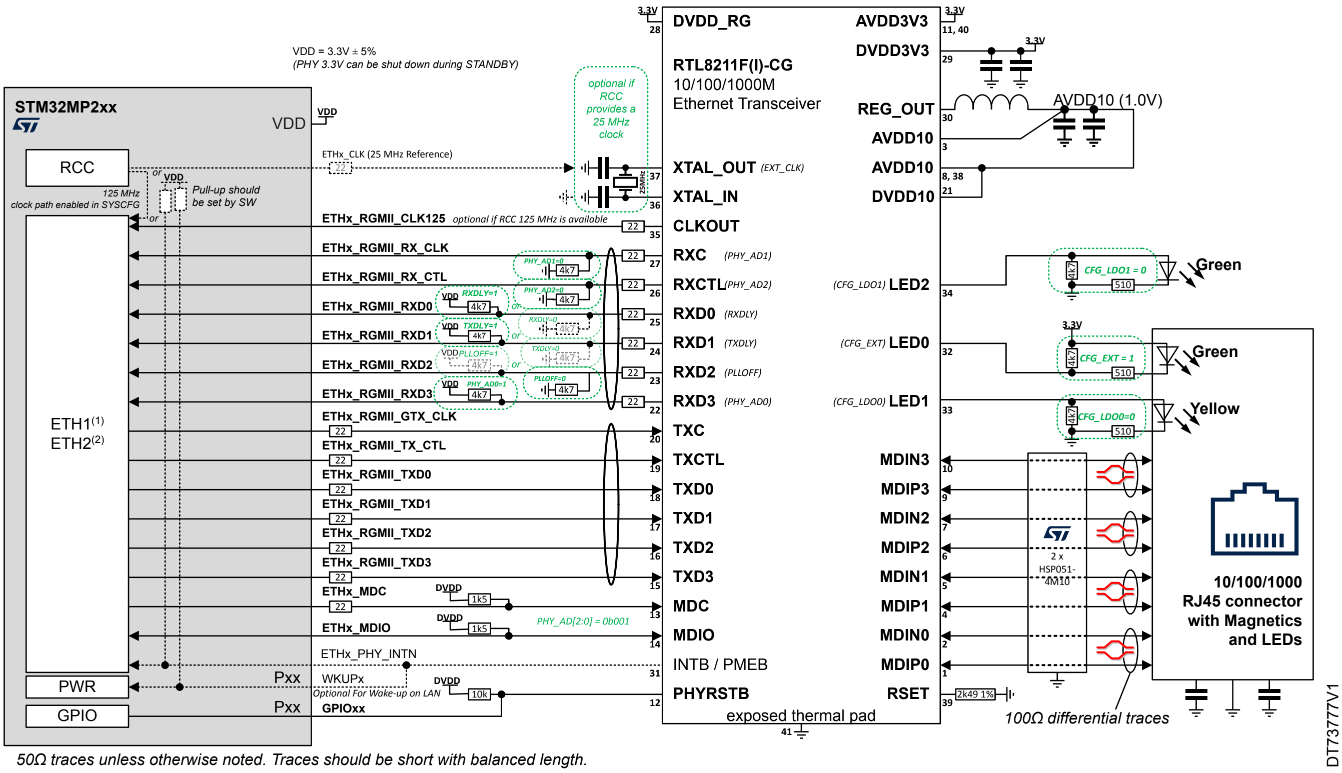
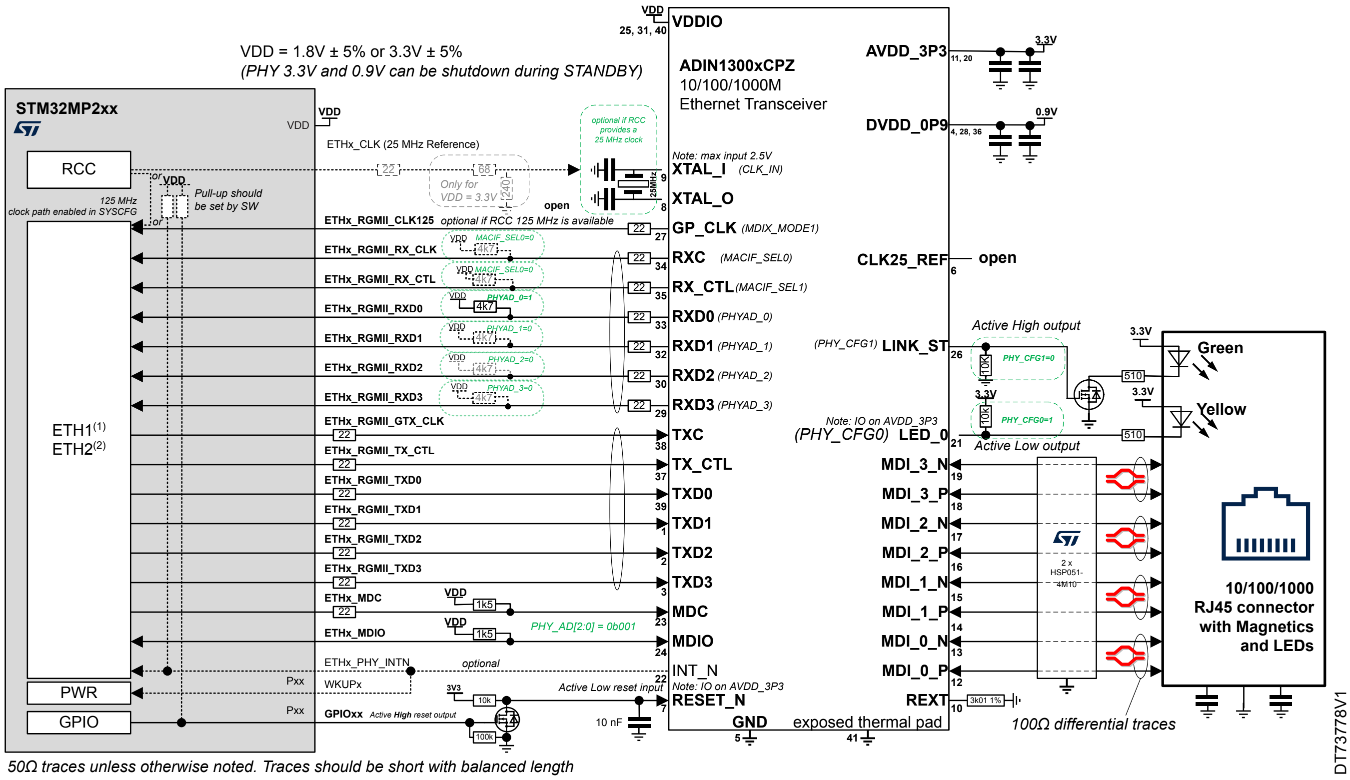


Figure 39. Gigabit Ethernet *PHY* connection (ADIN1300xCPZ)



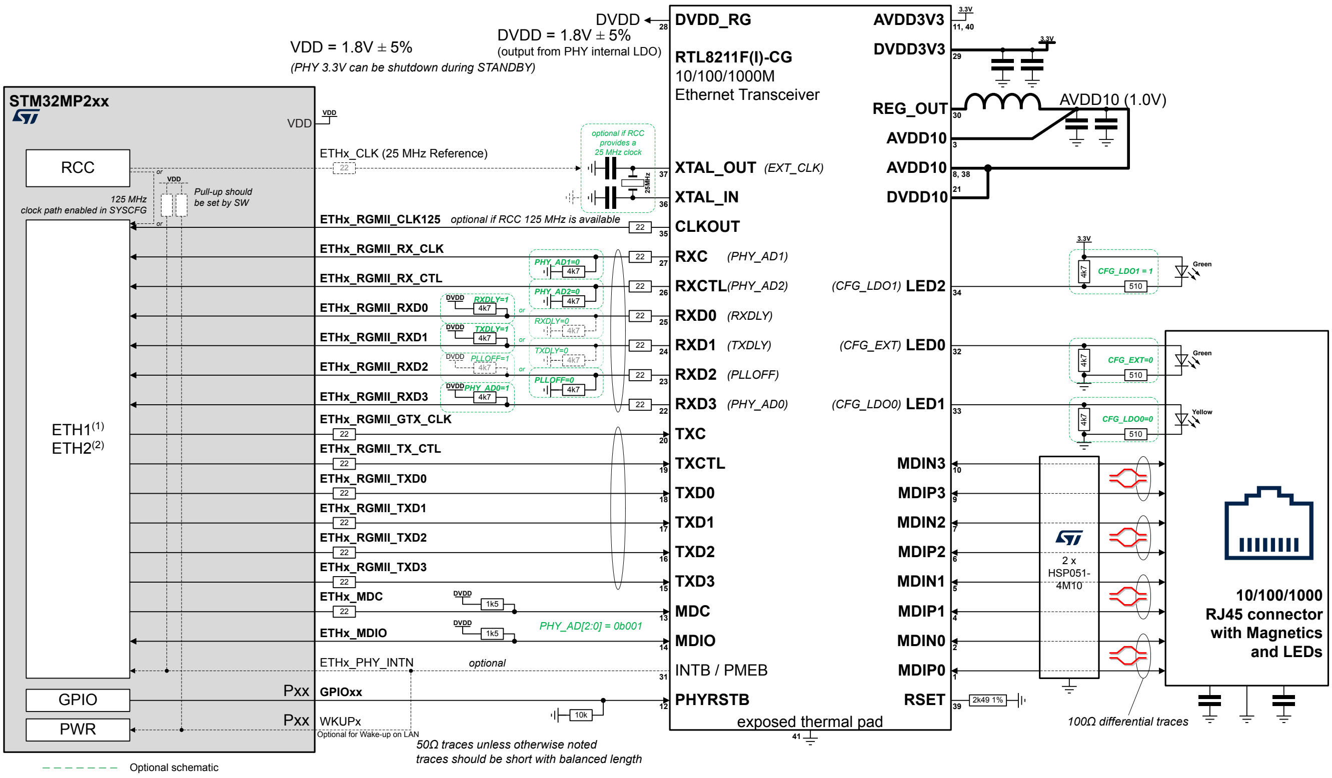
Note: 1. ETH2 is not available on some part numbers.

2. Decoupling capacitors are not shown.

Note:

- *As RCC cannot provide the 25 MHz reference clock to the PHY during low power modes, the dedicated 25 MHz crystal is required on the PHY in case wake-up on LAN (WOL) is needed for the platform.*
- *Setting RCC PLLs to get 25 MHz output for PHY could constrain other RCC frequencies. In that case, it is more flexible to put a dedicated 25 MHz crystal on the PHY.*

Figure 40. **Gigabit Ethernet *PHY* connection with V_{DD} = 1.8 V (RTL8211F)**



Note: 1. *ETH2 is not available on some part numbers.*
2. *Decoupling capacitors are not shown.*

Note:
- *As RCC cannot provide the 25 MHz reference clock to the PHY during low power modes, the dedicated 25 MHz crystal is required on the PHY in case wake-up on LAN (WOL) is needed for the platform.*
- *Setting RCC PLLs to get 25 MHz output for PHY could constrain other RCC frequencies. In that case, it is more flexible to put a dedicated 25 MHz crystal on the PHY.*

Table 19. ETH RGMII pins

Pin name	(1)	ETH1	ETH2(2)	comments
ETHx_CLK	→	PF3, PF5, PF8	PF4, PG3	optional 25 MHz reference(3)
ETHx_RGMII_CLK125	←	PC4, PH9	PF8, PG2	optional if 125 MHz is fed internally from *RCC* to *ETH* function
ETHx_RGMII_RX_CLK	←	PA14	PF6	See also Table 10. *GPIO* advance configuration recommended settings
ETHx_RGMII_RX_CTL	←	PA11	PC3	
ETHx_RGMII_RXD0	←	PF1	PG0	
ETHx_RGMII_RXD1	←	PC2	PC12	
ETHx_RGMII_RXD2	←	PH12	PF9	
ETHx_RGMII_RXD3	←	PH13	PC11	
ETHx_RGMII_GTX_CLK	→	PC0	PF7	
ETHx_RGMII_TX_CTL	→	PA13	PC4	
ETHx_RGMII_TXD0	→	PA15	PC7	
ETHx_RGMII_TXD1	→	PC1	PC8	
ETHx_RGMII_TXD2	→	PH10	PC9	
ETHx_RGMII_TXD3	→	PH11	PC10	
ETHx_MDC	→	PA9, PF0, PF4	PC6, PG4, PH10	-
ETHx_MDIO	→ ←	PA10, PF2, PF5	PC5, PF9, PH11	-
ETHx_PHY_INTN	←	PA12(4), PC6, PF5	PF5, PG3	optional

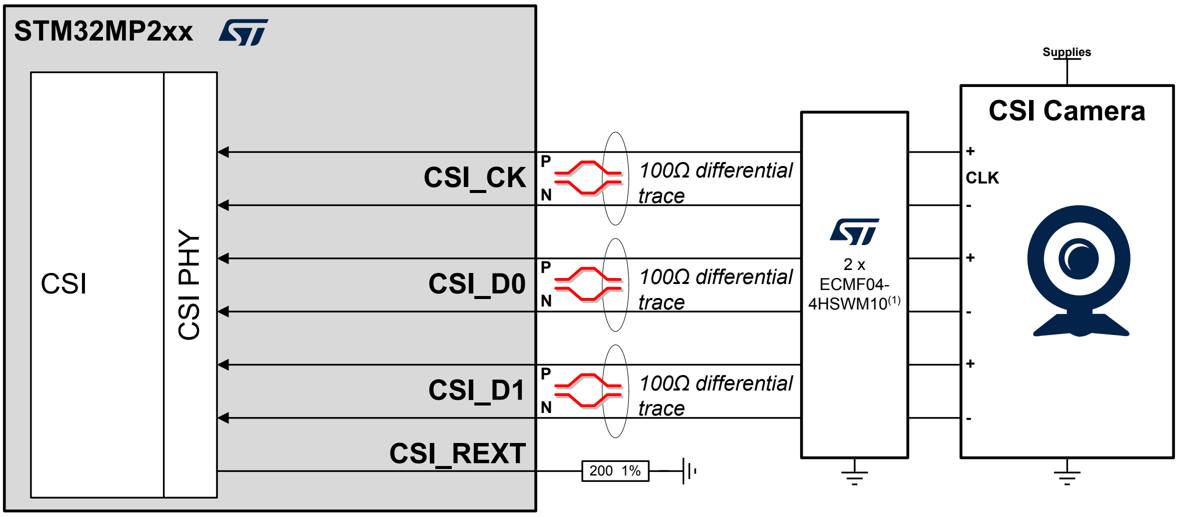
1. *Signal direction: → MPU to PHY, ← PHY to MPU*
2. *Not available on some part numbers*
3. *As RCC cannot provide the reference clock to the PHY during low power modes, a dedicated 25MHz crystal is required on the PHY if wake-up on LAN (WOL) is needed for the platform.*
4. *PA12 is not available on VFBGA225 8x8 package.*

8.15 Camera serial interface (*CSI*)

Note: As the digital camera memory interface pixel processor (DCMIPP) processes the pixel data received by the CSI, the parallel high-resolution sensor interface is not available when the CSI is used. In that case, a second parallel low-performance sensor is still possible using DCMI. See the reference manual for details.

A 200 Ω 1% resistor should be connected between CSI_REXT and V_{SS}.

Figure 41. *CSI* example



Note:
1. *Supplies and decoupling capacitors are not shown.*
2. *Image sensor controls are not shown (I^2C for control, autofocus, and so on.)*

Table 20. *CSI PCB* routing recommendations

Recommendation	Min	Typ	Max	Unit
Differential impedance	90	100	110	Ω
Single-ended impedance	45	50	55	Ω
Length matching within a pair (including package)[(1)]	-5.9	-	+5.9	mils
	-0.150	-	+0.150	mm
Length matching between clock and data pairs	-50	-	+50	mils
	-1.3	-	+1.3	mm
Max link length (including camera module cables)	-	-	8	inches
	-	-	203	mm
Max number of vias (recommended value)	-	-	2	-
Distance between any differential trace and other signals	-	S-3S or more		-[(2)]
Do no route over the power plane split. No stubs (point to point only). No right angles.				

1. *See Section 8.16: High-speed differential lane PCB track length matching for PCB track length matching details.*
2. *Definition could be found, for instance, in the DDR memory routing guidelines [5].*

8.16 High-speed differential lane *PCB* track length matching

Each package has been optimized to provide easier length matching when differential ball pair signals (denoted by xM, xN, and xP) are not directly on adjacent balls. Example: for a package with a 0.8 mm ball pitch, when differential pairs are on two different rows, the package already has around 800 µm of internal length difference to allow the *PCB* track to match the total length with minimum or even no additional routing complexity. The following figure shows (for example, xN minus xP) the length difference (inside the package) at ball level that the *PCB* tool must consider.

Figure 42. Differential *PCB* track for a package with a 0.8 or 0.5 mm ball pitch

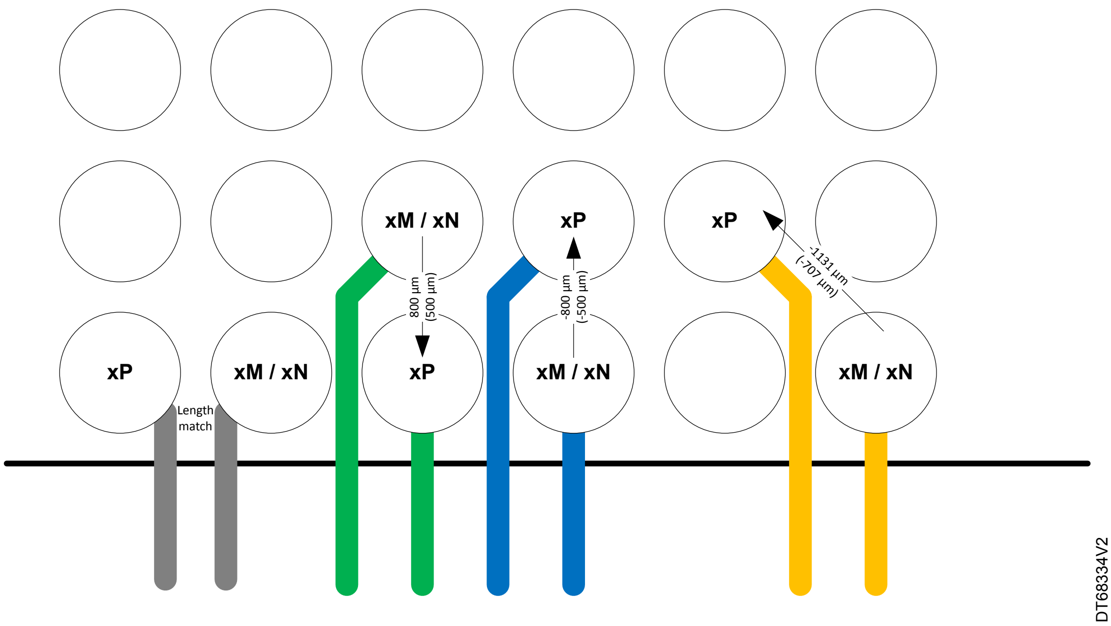


Table 21. Package length matching values

Pin name	VFBGA225 (8 × 8 pitch 0.5 mm)		VFBGA361 (10 × 10 pitch 0.5 mm)		VFBGA273 (11 × 11 pitch 0.5 mm)		TFBGA289 (14 × 14 pitch 0.8 mm)	
	Ball	Δlength (µm)	Ball	Δlength (µm)	Ball	Δlength (µm)	Ball	Δlength (µm)
CSI								
CSI_CKP	-	-	C1	-428	A3	333	A3	378
CSI_CKN	-	-	C2	REF	B3	REF	B3	REF
CSI_D0P	-	-	E2	-379	B1	120	B1	-95
CSI_D0N	-	-	E1	REF	C1	REF	C1	REF
CSI_D1P	-	-	D1	-33	A2	233	A2	291
CSI_D1N	-	-	D2	REF	B2	REF	B2	REF
USB								
USBH_HS_DP	-	-	W11	355	Y19	1	T13	19
USBH_HS_DM	-	-	V11	REF	AA19	REF	U13	REF
OTG_HSDP	P14	256	W12	199	Y20	25	T14	173
OTG_HSDM	R14	REF	V12	REF	Y21	REF	U14	REF

Revision history

Table 22. Document revision history

Date	Revision	Changes
28-Aug-2025	1	Initial release.
23-Sep-2026	2	Added: • Table 1. Applicable products Updated: • Document title • Section 1: General information • Section Introduction • Relocated the glossary to the end of the document • Added footnote reference to Table 13. HSE BOM for oscillator or crystal • Table 19. ETH RGMII pins • Table 21. Package length matching values • Glossary Small text and editorial changes.

Glossary

ADC Analog-to-digital converter

AHB Advanced high-performance bus

BKPSRAM Backup SRAM

BSEC Boot and security controller. OTP interface

CRC Cyclic redundancy check

CSI Camera serial interface

DAP Debug access port

DCMI Parallel digital camera interface

DCMIPP Digital camera memory interface pixel processor

DDR Double data rate

DDRCTRL Double data rate SDRAM controller

ECC Error correction code

eMMC Embedded MultiMediaCard

ETH Ethernet controller

EXTI Extended interrupt and event controller

FDCAN Controller area network with flexible data-rate. Could also support time triggered CAN (TT)

FMC Flexible memory controller

GMAC Gbit/s media access control or controller

GPIO General-purpose input/output

HDP Hidden protection

HSE High-speed external crystal oscillator

HSI high speed internal oscillator.

I^{2}C Inter-integrated circuit

I3C Inter-integrated circuit

IWDG Independent watchdog

I^{2}S Integrated interchip sound

JTAG Joint Test Action Group

JTAG-DP JTAG debug port

LAN Local area network

LCD Liquid crystal display

LDO Low-dropout regulator

LPTIM Low-power timer

LSE Low-speed external crystal oscillator

LSI Low-speed internal oscillator

LTDC LDC TFT display controller

MDIO Management data input/output

MSI Multispeed internal oscillator

NVM Nonvolatile memory - a memory that retains its contents even when powered down, such as flash memory, PCM, OTP memory, or EEPROM

OCTOSPI Octal data serial peripheral interface

OTP One-time programmable

PCB Printed circuit board

PDR Power down reset

PHY Physical layer

PLL Phase-locked loop

PMIC Power management integrated circuit. It is an external circuit that provides various platform power supplies with large controllability through signals and serial interface

POR Power-on reset

PTH Plated through a hole. It is a drilled hole with a conductive wall using, for example, a layer of deposited copper.

PVD Programmable voltage detection

PVM Peripheral voltage monitor

PWR Power control

RC Resistor-capacitor

RCC Reset and clock control

RETRAM Retention SRAM

ROM Read-only memory

RTC Real-time clock

SAI Second application indicator

SCL Serial clock line (I^2C signal)

SD Secure digital

SDA Serial data line (I^2C signal)

SDMMC Secure digital and MultiMediaCard

SLC Single level cell

SMPS Switched-mode power supply

SPI Serial peripheral interface

SRAM Static random-access memory

SWD Serial wire debug

SW-DP Serial wire debug port

SWJ Serial wire and JTAG

SWJ-DP Serial wire/JTAG debug port

SWO Single wire output. A trace port

SYSCFG System configuration

TAMP Tamper detection circuit.

TFT Thin film transistor. An *LCD* technology process

TIM Timer input module

TPIU Parallel TRACE outputs

UART Universal asynchronous receiver/transmitter

USART Universal asynchronous receiver transmitter

USB Universal Serial Bus

USBH USB host controller

USB high speed USB 2.0 at 480 Mbit/s half-duplex

USB-OTG USB on-the-go high-speed

VREFBUF ADC voltage reference buffer

WOL Wake-up on LAN

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