L9908 alternative bootstrap capacitor charging methods

Introduction

The L9908 is a gate driver unit (GDU) capable of controlling 6 N-channel FETs for 3-phase motors in automotive applications.

This document contains a description of a particular working condition that occurs when the phase node voltage rises with a high dV/dt, usually due to sudden inductive current interruption after a LS switch off when the current is flowing into the phase node.

When this happens, the quick rise of CBSn voltage may generate a current from the bootstrap capacitor to VPRE thus causing a voltage drop on the bootstrap capacitor itself.

In some applications the lost bootstrap capacitor charge cannot be fully restored in the next PWM cycles causing a reduction on output HS VGS level. To address this effect, two different applicative countermeasures are described in this application note.

1 Phenomenon description

In the L9908, there is a particular working condition occurring when the phase node voltage rises with a high dV/dt, usually due to sudden inductive current interruption after a LS switch off when the current is flowing into the phase node. When this happens, the quick rise of CBSn voltage may cause a back-feeding current from the bootstrap capacitor to VPRE thus causing a voltage drop on the bootstrap capacitor itself.

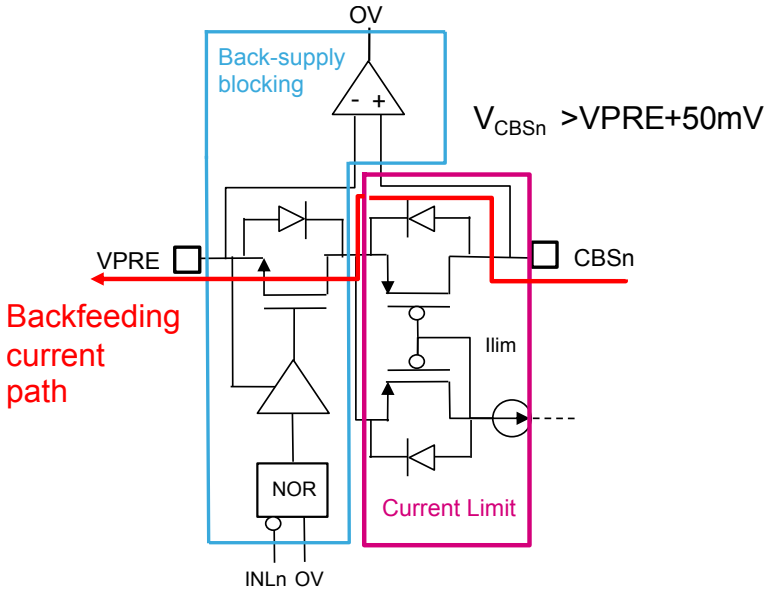
The Bootstrap Limiter 1 (BT1) protects against back-supply when INHn = low and with an overvoltage detector that shut down the back-supply blocking FET when V_{CBSn} > VPRE + 50 mV.

When current is entering the phase node and LS is turned off, the SHS voltage rises quickly according to motor characteristics.

If the SHS voltage rises too fast, the OV comparator delay may allow a back-feeding current pulse from CBSn to VPRE, thus discharging the bootstrap capacitor. The OV comparator delay, and therefore the duration of the current pulse, depends on several parameters (SHS voltage dV/dt, battery voltage level, capacitances, etc.) but the typical duration can be estimated between 300-400 ns.

Usually, the lost charge on bootstrap capacitor can be restored by means of CP2 during HS ON time and during following LS ON time from VPRE. The capacitor charge from VPRE is the most efficient, but if the LS ON time is too small, the BT1 cannot fully restore the missing charge on bootstrap capacitor thus leading to a reduced overdrive to turn on the HS FET. If this condition is repeated multiple times, after a few PWM cycles the bootstrap capacitor voltage will be too low to turn on the external FET correctly and an OND fault may be detected.

Figure 1. BT1 internal circuit



2 Simulations and bench results

In this section, bench analysis and simulation results are reported.
Tests have been performed on ST Eval board and executed on the one pre-driver channel.
The setup is as follows:

- Inductive load connected between phase node and 12 V battery
- C_{BTn} = 390 nF
- PWM pulses on LS
- HS always off

Figure 2. ST Eval board

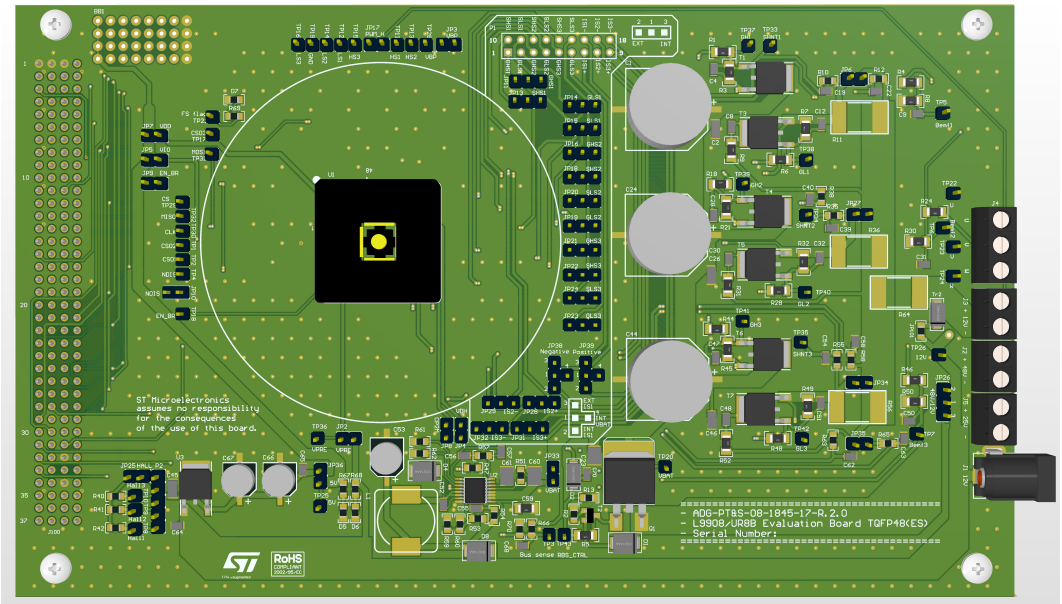
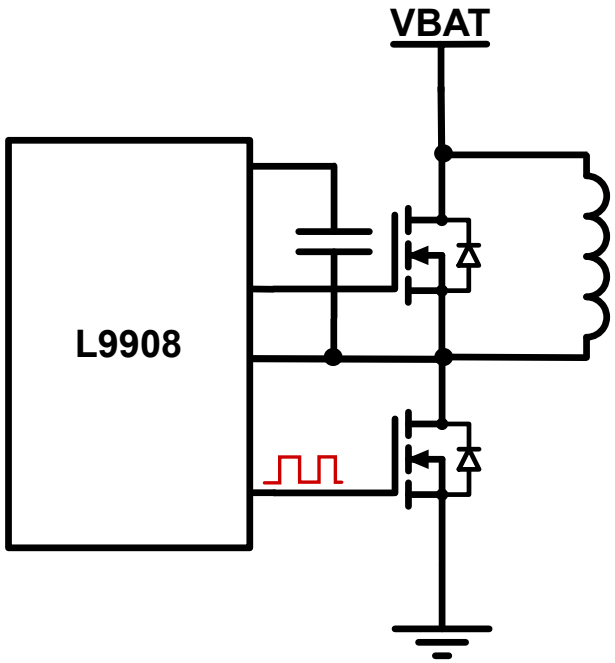


Figure 3. Setup for phenomenon replication



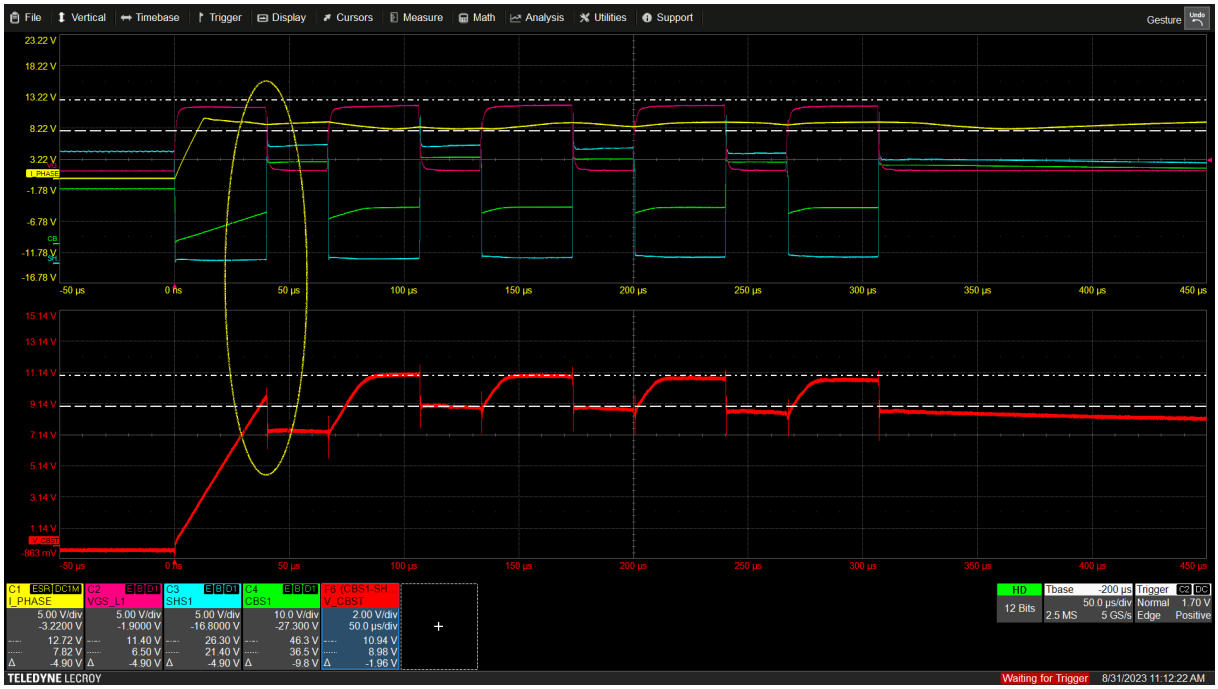
In the Figure 4, phase current, LS1 V_{GS}, V_{SHS1}, V_{CBS1}, V_{CBS1} and V_{SHS1} traces are reported.

It is evident that at LS switch off, a quick ~2 V voltage drop across C_{BT1} is detected, thus causing C_{BT1} discharge over time.

The equivalent current is about 2.5 A, that comes out from

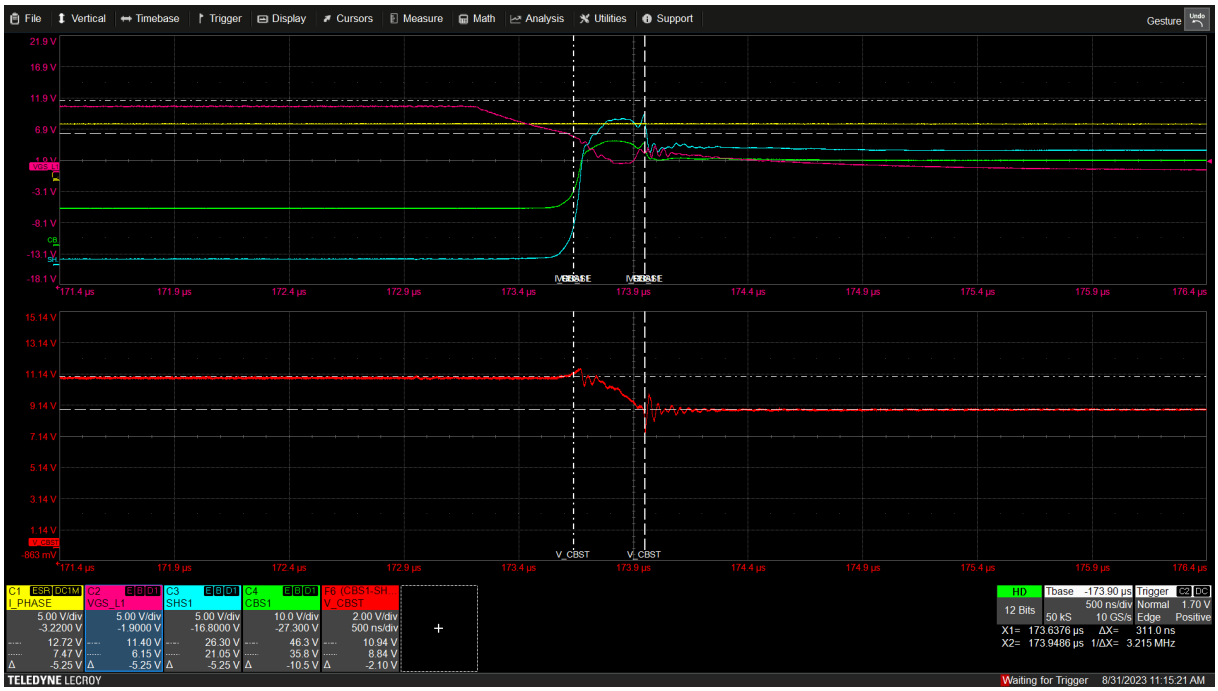
$$I = \frac{\Delta V_{CBSn} \times C_{BTn}}{\Delta t} = \frac{2V \times 390\,nF}{310\,ns} = 2.516\,A \quad (1)$$

Figure 4. Phenomenon replication waveforms



In the figure Figure 5 is shown the detail of the area highlighted in yellow in the Figure 4.

Figure 5. Phenomenon replication waveforms - Detail



This test has been repeated with C_{BTn} = 1 µF instead of 390 nF.

In the Figure 6 is clear that the current level is 2.5 A (the yellow trace is the current flowing into CBSn pin), so the current pulse amplitude can be considered to be independent from the capacitor value.

Figure 6. Phenomenon replication waveforms (C_{BTn} = 1 µF)

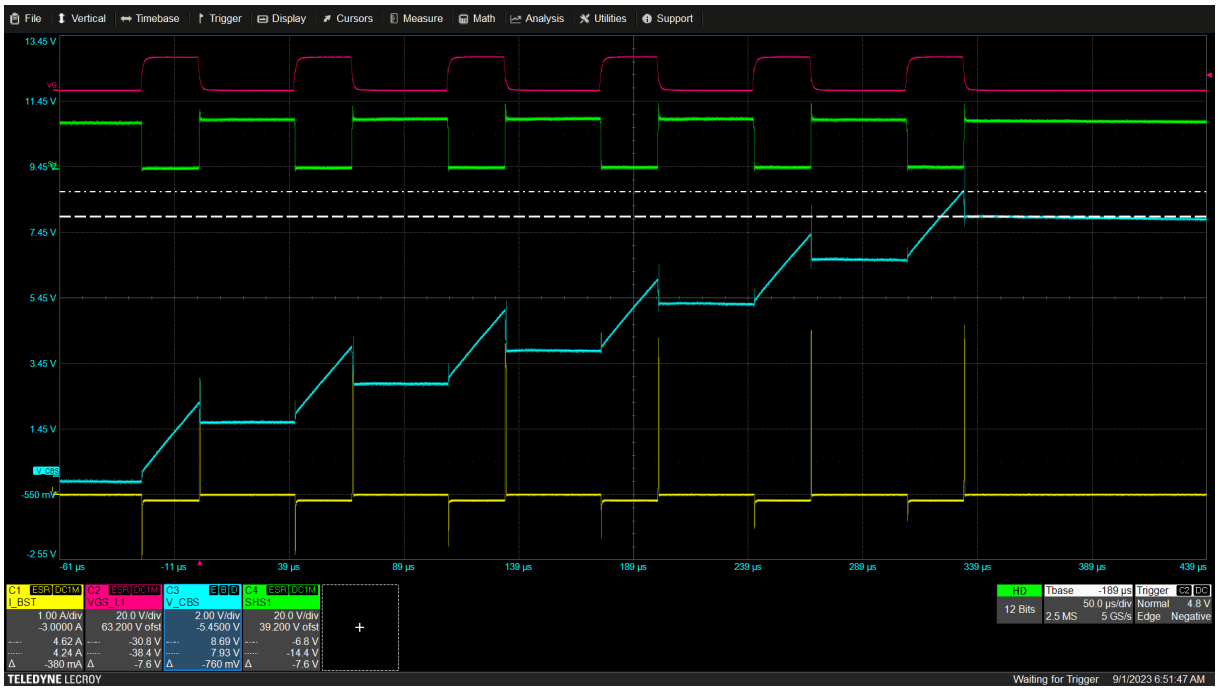
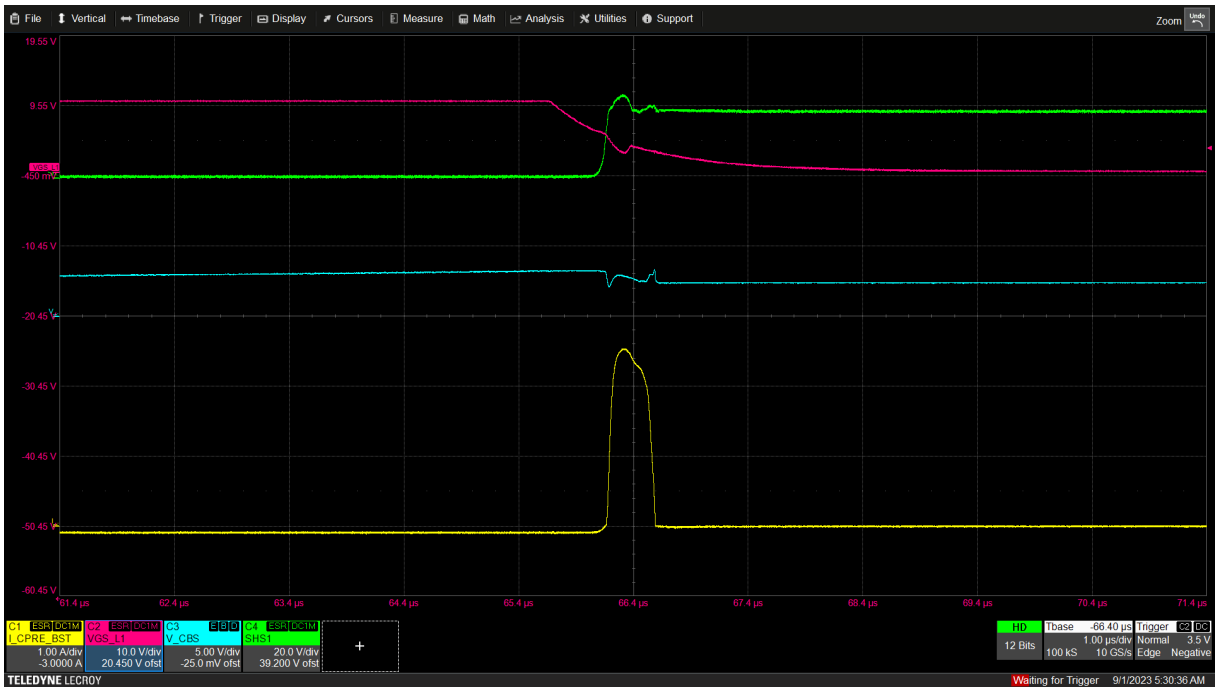


Figure 7. **Phenomenon replication waveforms (C_{BTn} = 1 µF) - Detail**

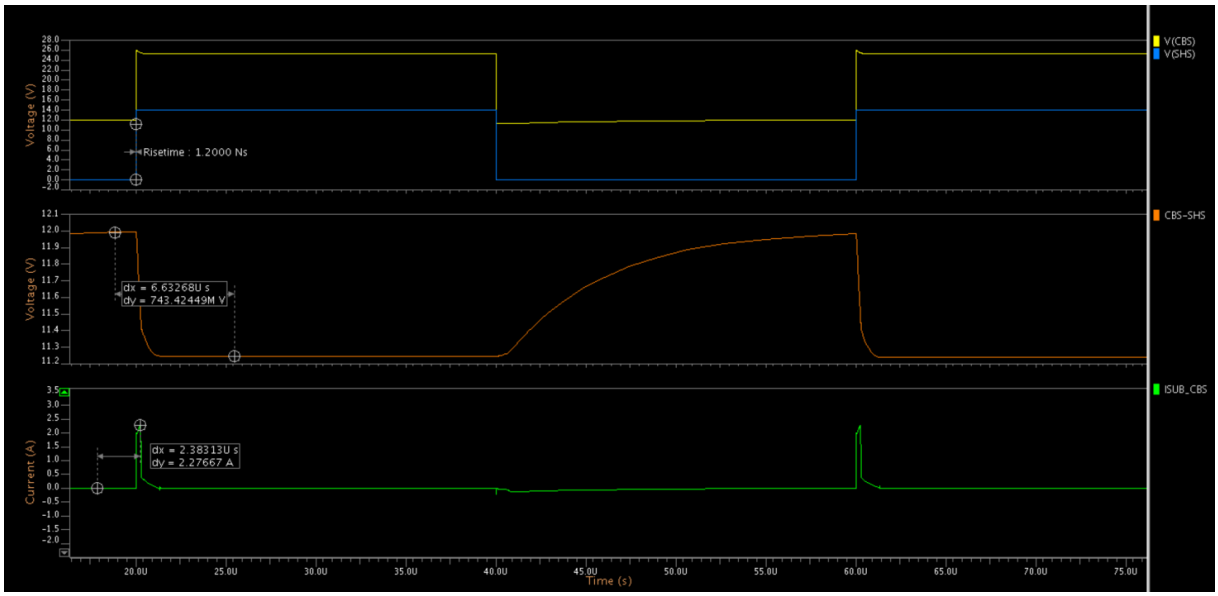


The behavior has also been replicated in a simulation environment.

The bootstrap capacitor C_{BTn} value is 1 µF and the SHS transition has a SR = 140 V/ns.

The result is a voltage drop of 750 mV on C_{BTn} due to a discharge current of 2.4 A (peak value).

Figure 8. **Behavior replication in simulation environment**



As seen in the Figure 8, it is evident once again how the current drained from CBS is back-feeded to the VPRE capacitor during SHS rise.

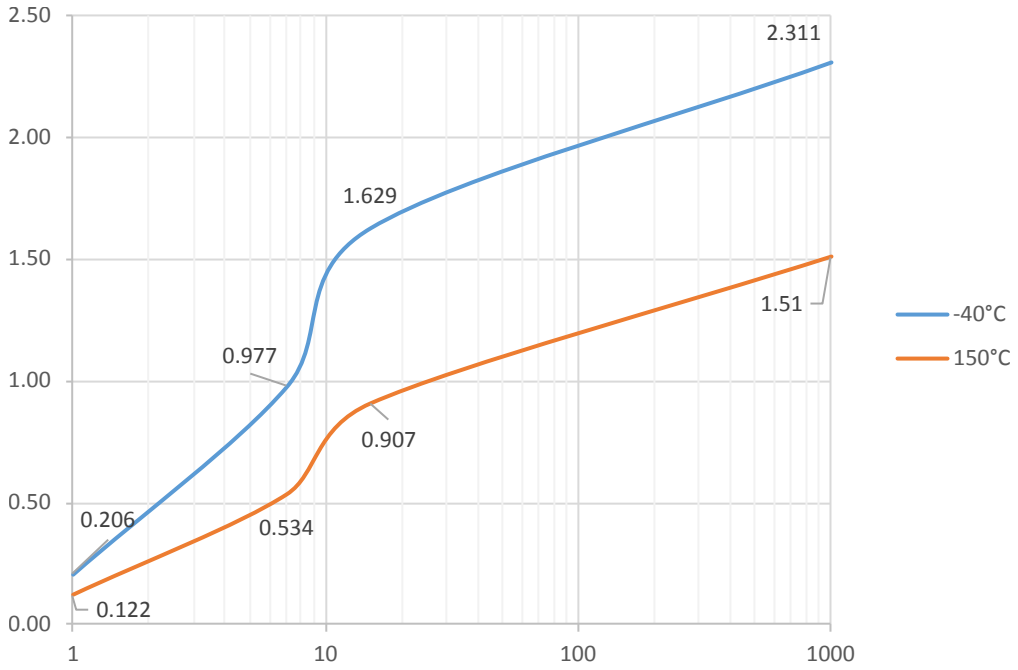
According to these results, the back-feeding current peak on VPRE has been characterized according to different SR on CBSn and temperature considering C_{BTn} = 1 µF.

Results are reported in the Table 1.

Table 1. Back-feeding current value vs SR on CBSn and temperature

SR CBS_n	Min	Typ	Max	Min	Typ	Max	Unit
	Tj = -40 °C			Tj = 150 °C			
14 V/14 ns → 1 V/ns	2.31064	2.311	2.31136	1.50946	1.51	1.51054	A
14 V/1 µs → 14 V/µs	1.5462	1.629	1.7118	0.87478	0.907	0.93922	
14 V/2 µs → 7 V/µs	0.9134	0.977	1.0406	0.5076	0.534	0.5604	
14 V/7 µs → 2 V/µs	0.1916	0.206	0.2204	0.111	0.122	0.136	

Figure 9. VPRE back-feeding current (A_{PK})



Note: The horizontal scale is logarithmic.

It can be noticed that this peak current grows logarithmically with SR increasing and around 10 V/ns has a step variation.

Considering separately these two ranges (before and after the step), the dependance of peak current with SR can be considered as variating linearly with the SR logarithm as depicted in the Figure 10 and Figure 11.

Figure 10. VPRE back-feeding current (A_{PK}) before the step

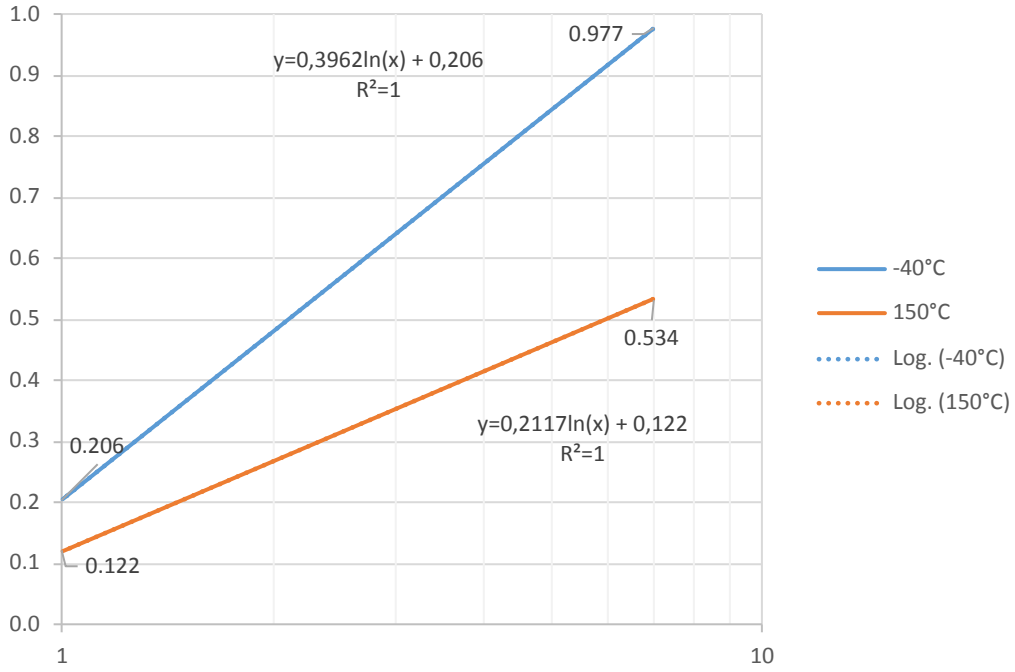
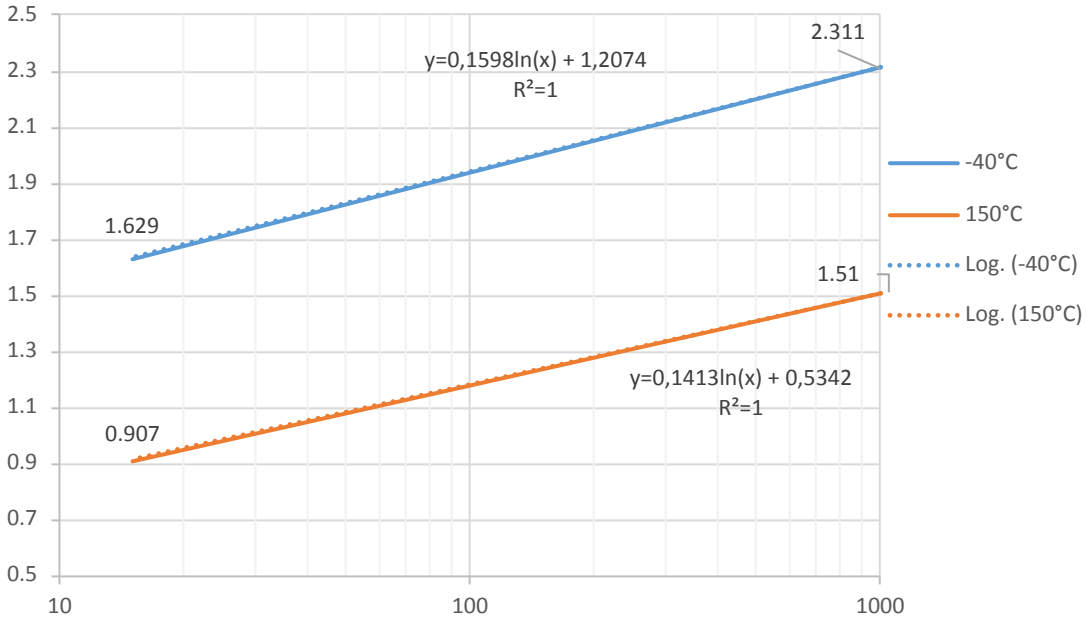


Figure 11. VPRE back-feeding current (A_{PK}) after the step

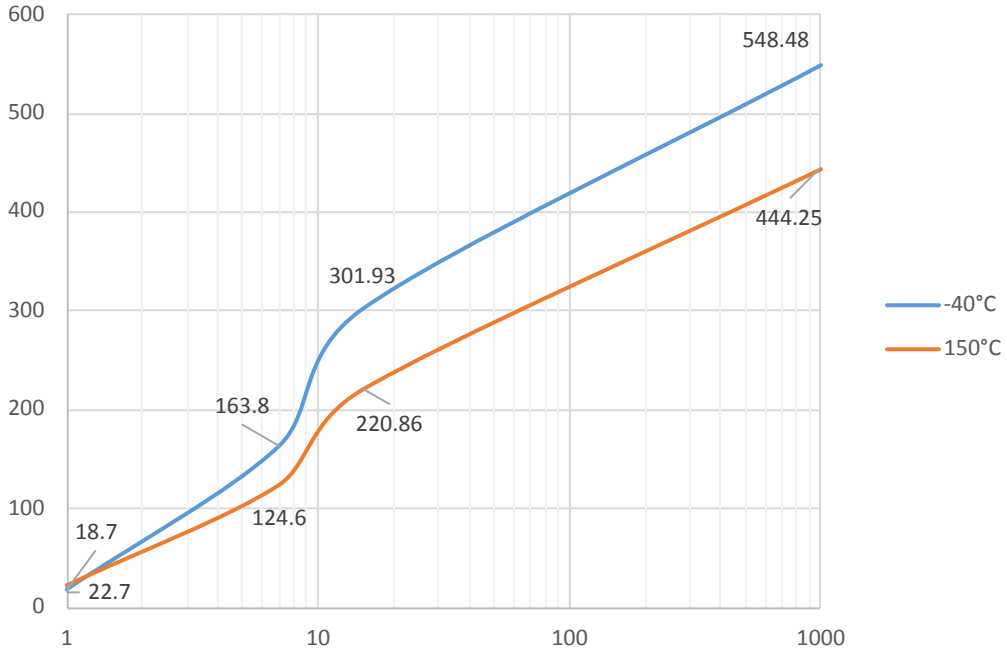


The amount of lost charge has also been estimated.

Table 2. Lost charge vs SR on CBSn and temperature

SR CBS_n	Min	Typ	Max	Min	Typ	Max	Unit
	Tj = -40 °C			Tj = 150 °C			
14 V/14 ns → 1 V/ns	519.62	548.48	577.34	425.47	444.25	463.03	nC
14 V/1 µs → 14 V/µs	247.27	301.93	356.59	199.08	220.86	242.64	
14 V/2 µs → 7 V/µs	134.1	163.8	193.5	110.68	124.6	138.52	
14 V/7 µs → 2 V/µs	10.36	18.7	27.04	18.254	22.7	27.146	

Figure 12. CBSn lost charge (nC)



Note: The horizontal scale is logarithmic.

As well as for the peak current values, the lost charge grows logarithmically with SR increasing and around 10 V/ns has a step variation.

Considering separately these two ranges (before and after the step), the dependance of lost charge with SR can be considered as variating linearly with the SR logarithm as depicted in the Figure 13 and Figure 14.

Figure 13. CBSn lost charge (nC) before the step

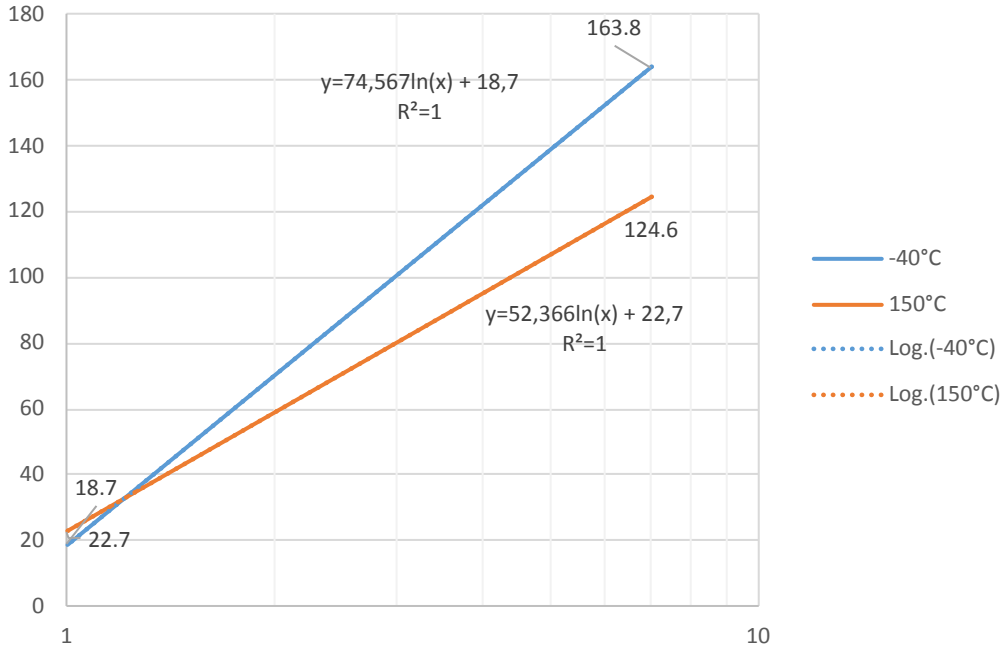
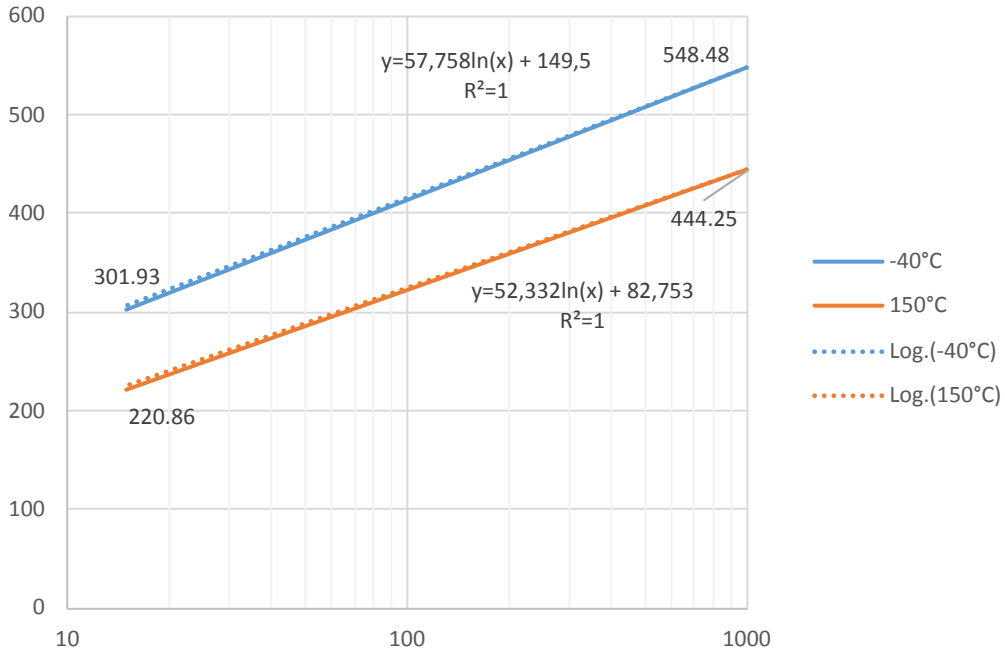


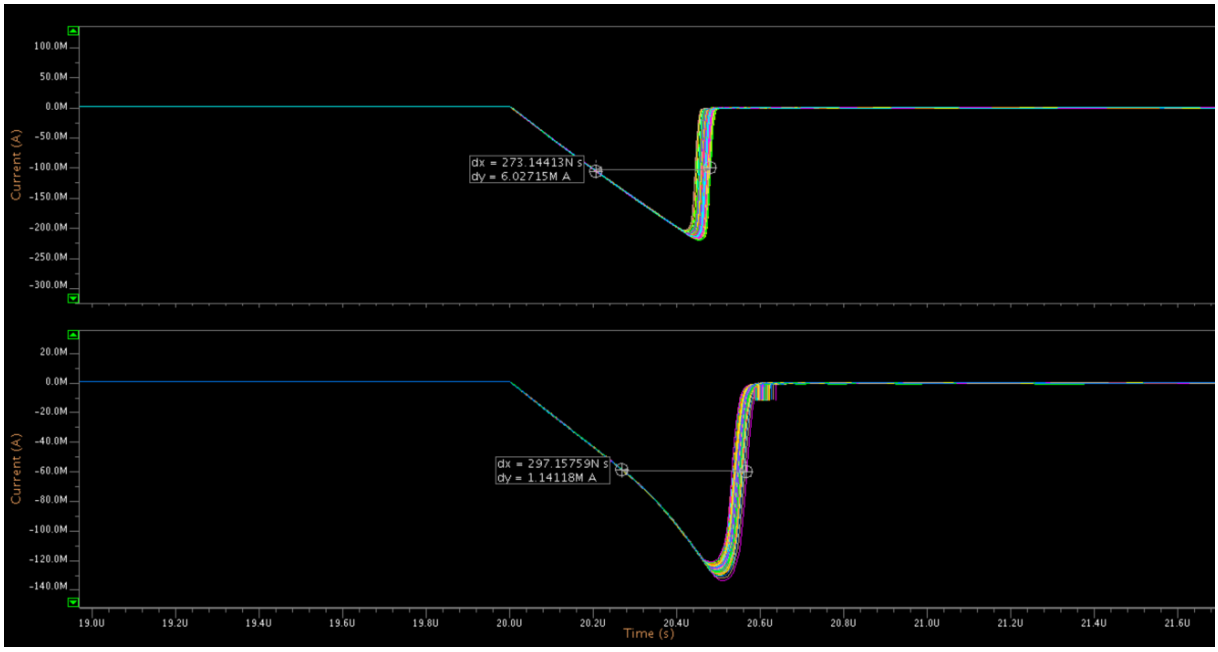
Figure 14. CBSn lost charge (nC) after the step



The current pulses are also extrapolated from the simulations.

A Montecarlo simulation has been made at Thot (Tj = 150 °C) and Tcold (Tj = -40 °C), on 300 runs and for SR = 14 V/7 µs on CBS.

Figure 15. **Back-feeding current pulse at Thot (above) and Tcold (below) for 300 pulses**



It can be noticed that the pulse width depends on the temperature. In the Figure 15 are shown the worst case duration of the pulse for both temperatures.

Following the simulations and bench analysis, it is possible to conclude that the back-feeded current peak on VPRE mainly depends on:

- The temperature: in fact, at Tcold it is higher than at Thot
- The SR on CBS: the dependence is logarithmic, the peak current grows logarithmically with SR

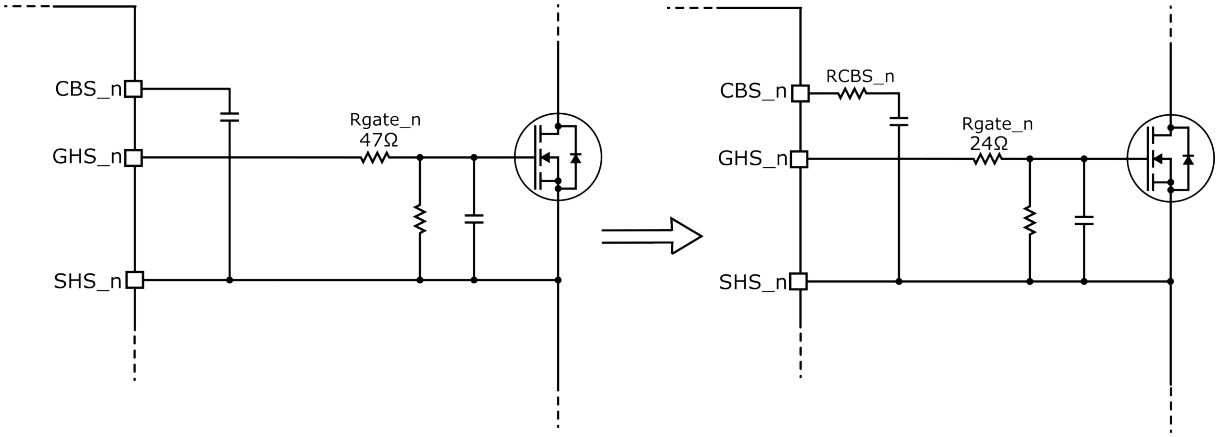
3 Applicative countermeasures

In this section, two different applicative countermeasures have been described to reduce or avoid lost charge on bootstrap capacitor as described above.

3.1 Add a resistance in series to bootstrap capacitor C_{BTn}

The first countermeasure consists of adding a resistance in series to the bootstrap capacitor C_{BTn} on each phase, as depicted in the Figure 16, to reduce the current pulse amplitude and to avoid excessive bootstrap discharge.

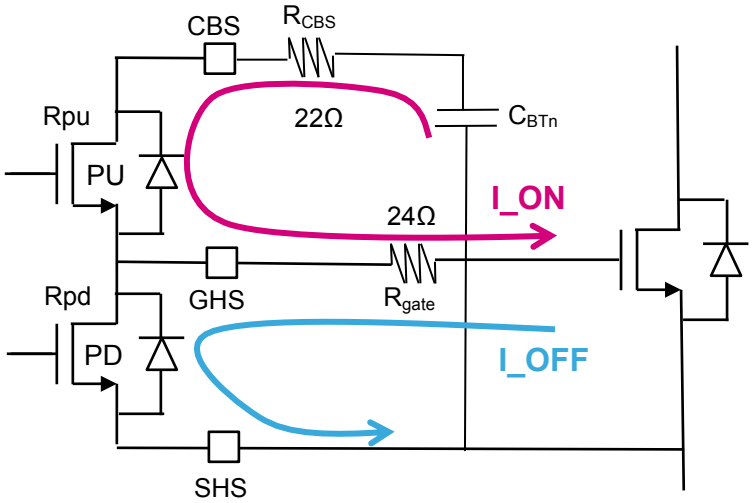
Figure 16. Countermeasure schematic



Putting a resistor in series to bootstrap capacitor is equivalent to adding a resistor in series to the GHS turn-on path, therefore the gate resistance shall be reduced by the same amount to achieve the same turn-on performance. So, for example, if the original value of R_{gate} is 47 Ω and a 22 Ω resistor is added in series to the C_{BTn} capacitor, the R_{gate} shall be reduced accordingly to 47 Ω - 22 Ω = 25 Ω.

With this workaround it is possible to limit the back-feeding current until the OV protection on BT1 is activated, maintaining the turn-on series resistance equals to R_{CBS} + R_{gate}. The turn-off resistance will be equals R_{gate}, thus achieving asymmetry between turn-on and turn-off resistance without the need for unidirectional circuitry (diode) on the gate path.

Figure 17. Equivalent circuit for charge and discharge



Reducing the current pulse, the CP2 current capability may be enough to recover the lost charge on bootstrap capacitor during the HS on time, ensuring the functionality also for low duty cycles on LS PWM.

Here are reported bench tests on the ST Eval board with two setups. The first one with R_{gate} = 47 Ω (as default due to ST Eval board) and R_{CBS} = 1 Ω, while the second with the countermeasure described above.

Both cases are analyzed with load and without load. The load is connected between phase node and battery and consists of an R + L circuit, with R = 11 Ω and L = 350 µH.

Pulses (burst mode in continuous without load and N = 5 cycles with load) on HS1 and LS1 have been sent with an amplitude of 5 V and a frequency of 10 kHz. The duty cycle on LS1 is about 87%, while on HS1 it is about 13% with a delay of 88 µs.

SETUP #1

- R_{gate} = 47 Ω
- R_{CBS} = 1 Ω

In the Figure 18 are reported waveforms in case of load not connected. The blue trace is the current on CBS and its max value is a few hundreds of mA during HS turn-on, and it is the current for the normal HS turn-on.

The Figure 19 reports the waveforms when R + L load is connected. The blue trace is the current on CBS and its max value is 1.16 A recorded during the LS turn-off, which is clearly the back-feeding current.

Figure 18. SETUP #1 waveforms with no load connected

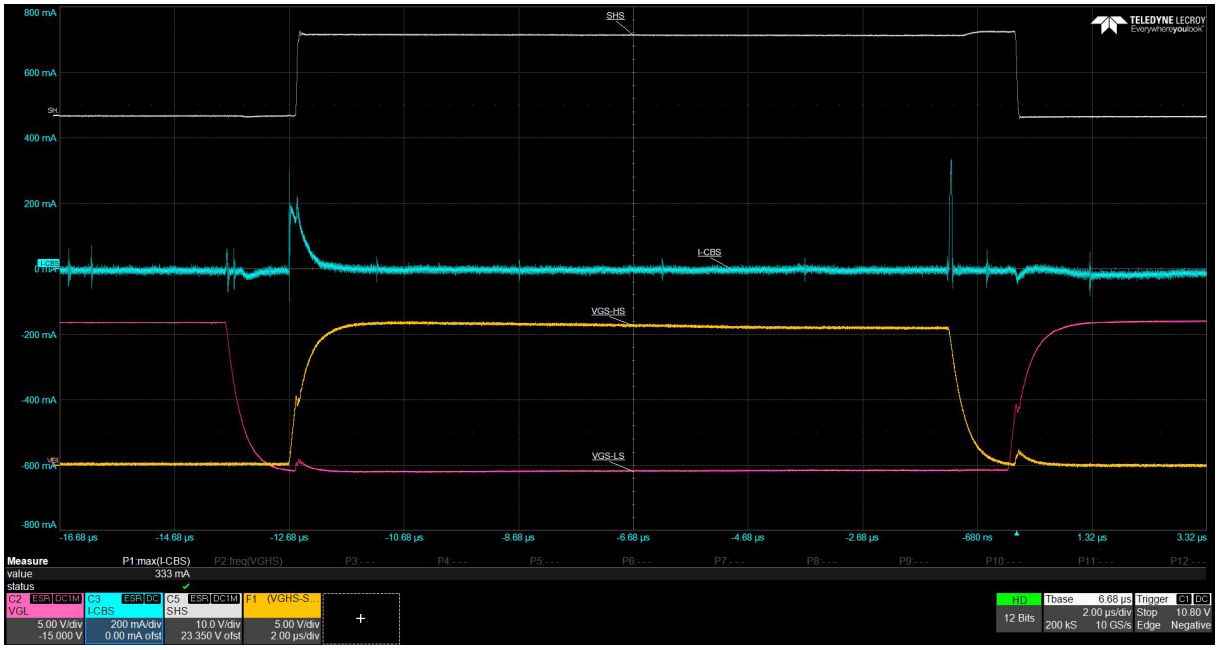
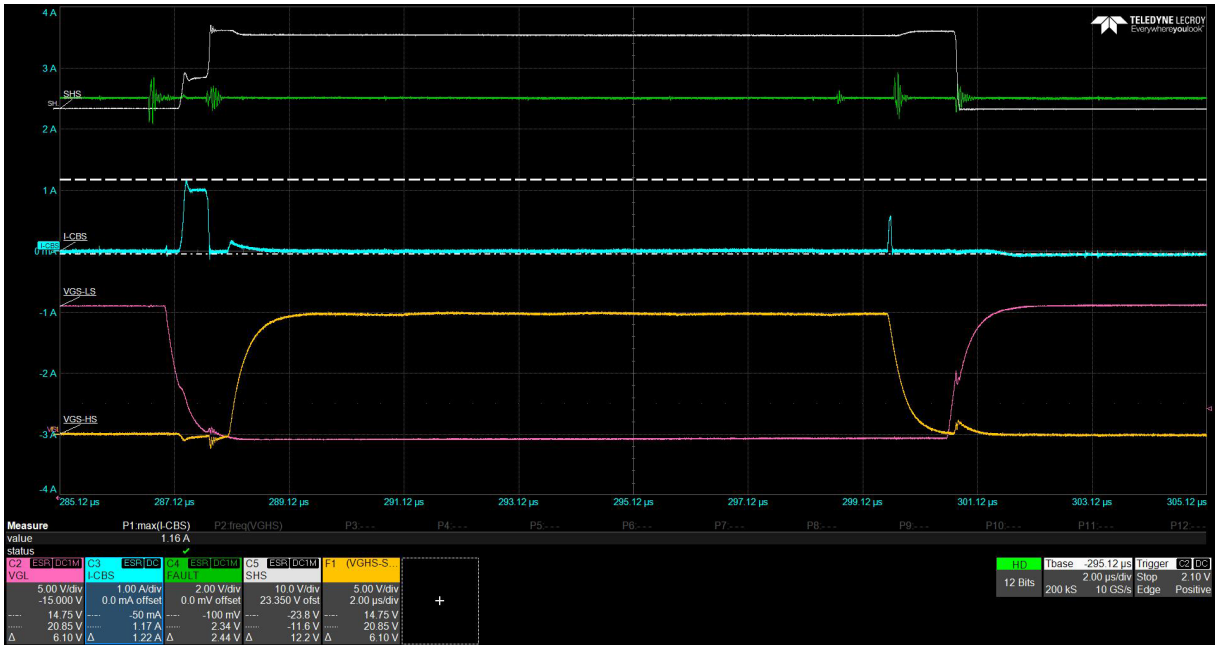


Figure 19. **SETUP #1 waveforms with load connected**



SETUP #2

- R_{gate} = 24 Ω
- R_{CBS} = 22 Ω

In the Figure 20 are reported waveforms in case of load not connected. The blue trace is the current on CBS and its max value is a few hundreds of mA during HS turn-on, and it is the current for the normal HS turn-on.

The Figure 21 reports the waveforms when R + L load is connected. The blue trace is the current on CBS and its max value is 449 mA recorded during the LS turn-off, which is clearly the back-feeding current.

Figure 20. **SETUP #2 waveforms with no load connected**

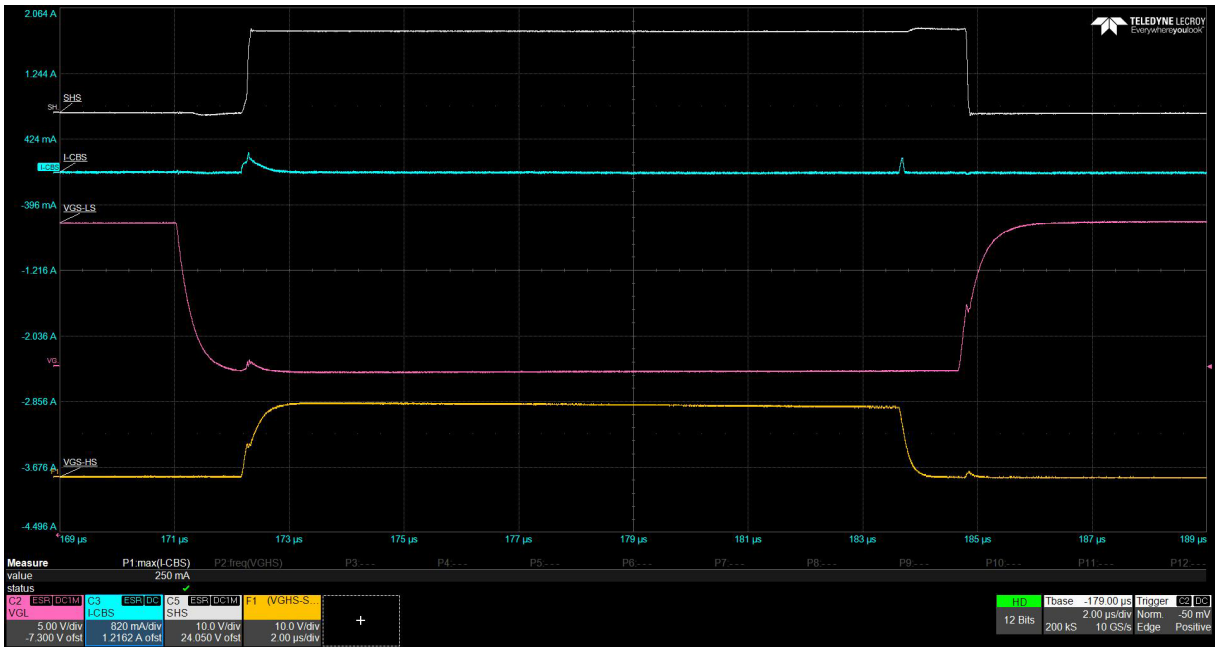
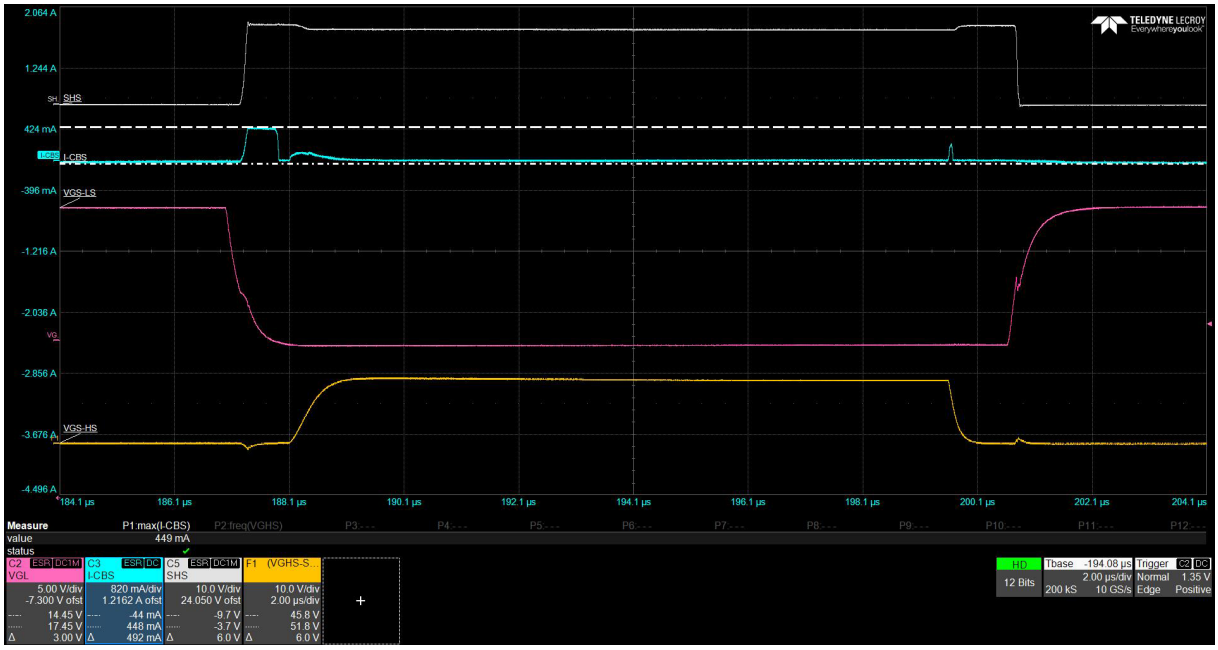


Figure 21. **SETUP #2 waveforms with load connected**



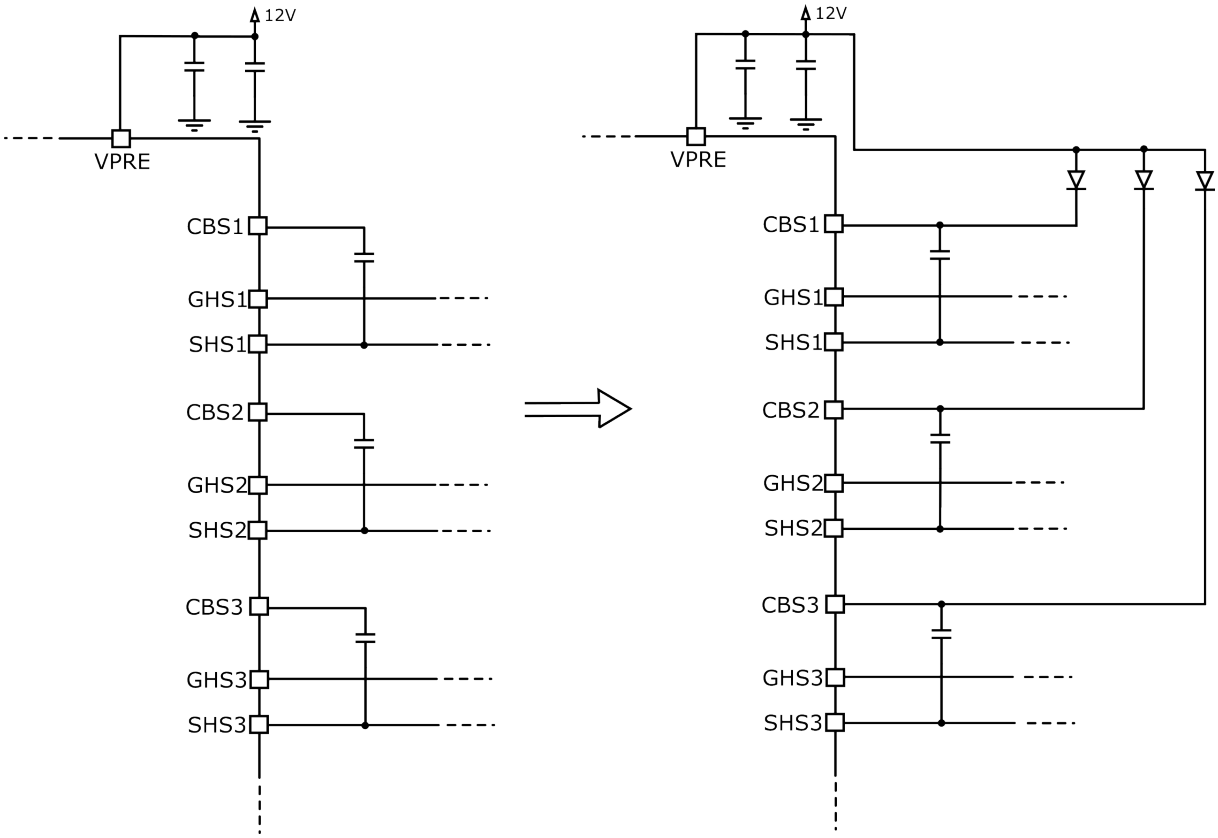
Analyzing the results, it is clear that by increasing the resistance added in series to C_{BTn} from 1 Ω to 24 Ω, the amplitude of the current pulse decreases. These results shall be considered as proof of concepts for the countermeasure, actual resistances value must be selected according to the application.

3.2 Connect VPRE to bootstrap capacitor C_{BTn} through a diode and disable BT1 limiter

The second countermeasure consists of connecting VPRE to bootstrap capacitor C_{BTn} of each phase with a diode and disabling BT1 limiter via SPI. The type of diode to be selected depends on system parameters, but it is suggested anyway to use a Schottky diode to reduce the voltage drop and ensure the maximum overdrive voltage available on CBS.

Maintaining BT1 always disabled will prevent any back-feeding current to flow into VPRE as reported below where bench test results are shown before and after the modification.

Figure 22. Countermeasure schematic



In the Figure 23 are shown waveforms in the following condition:

Circuit has been modified by adding an external path for C_{BTn} charge connecting it to VPRE and enabling BT1 limiter.

The result is a voltage drop on C_{BTn} which subsequently results in a spike current flowing into the CBSn pin. The yellow trace (I_BST) is the current flowing into CBSn pin and its peak is around 2.5 A.

In the Figure 24 are shown waveforms in the followed conditions:

The circuit has been modified by adding an external path for C_{BTn} charge connecting it to VPRE and disabling the BT1 limiter, resulting in no more voltage drop on C_{BTn}, as in the previous case. The yellow trace (I_CPRE_BST) is the current flowing into the external path.

Figure 23. **External diode path and BT1 enabled**

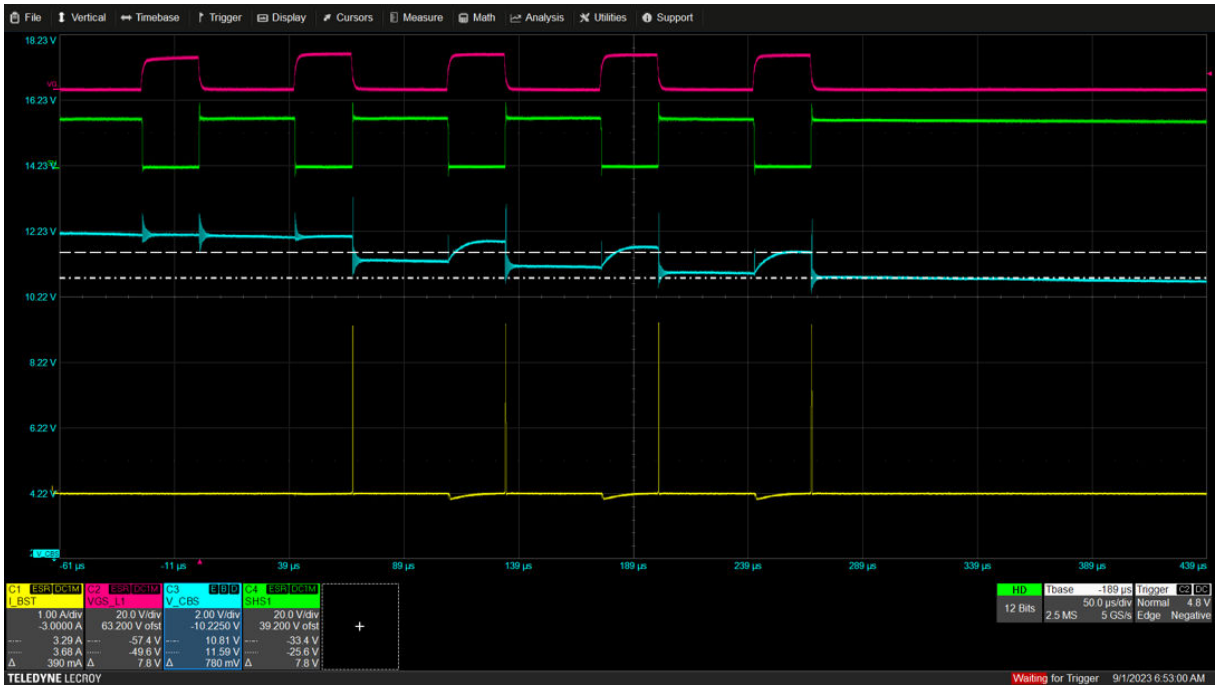


Figure 24. **External diode path and BT1 disabled**

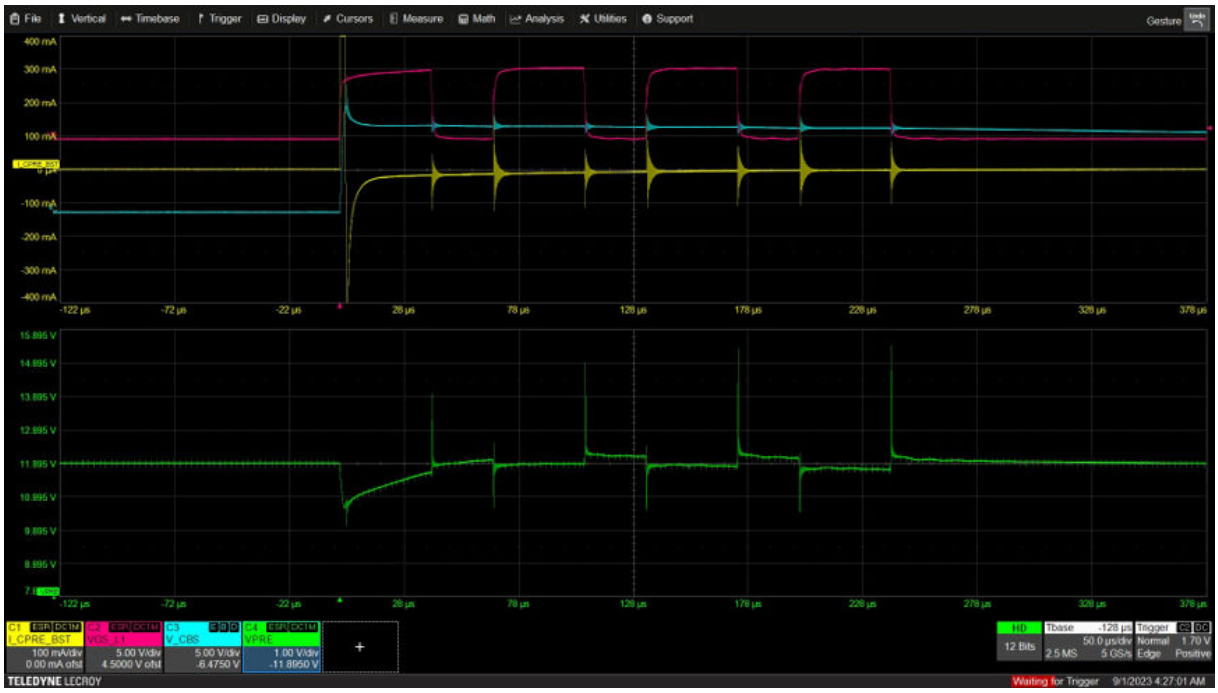
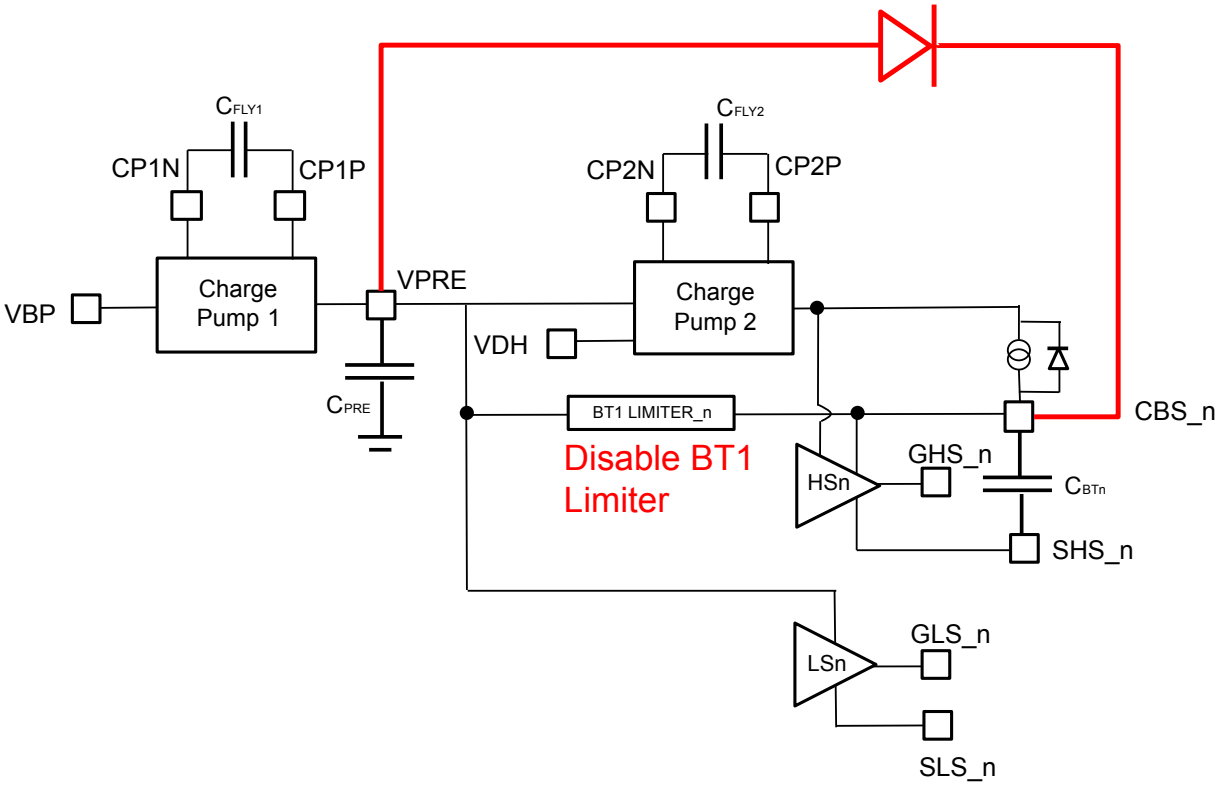
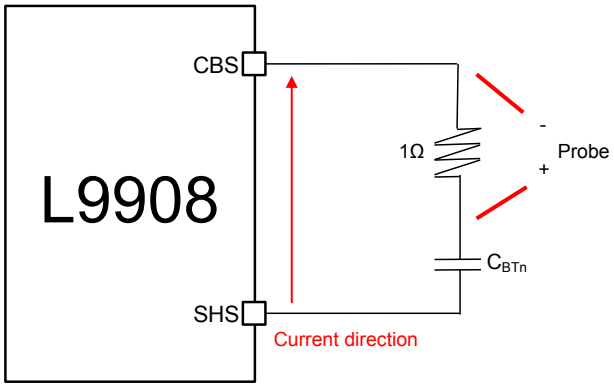


Figure 25. **Schematic of the second countermeasure circuit**



Further evaluation tests have been run driving a 3-phase BLDC. To simplify the measurement setup a 1 Ω resistor has been added in series to the C_{BTn} capacitor allowing to estimate the current by measuring the voltage drop across the resistor as depicted in the Figure 26.

Figure 26. **Block diagram**



In the Figure 27 and Figure 28 the green trace is the phase current and the pink trace is the voltage across the 1 Ω resistor with the external path and BT1 disabled. Comparing these pictures with the snapshots taken in original condition (BT1 limiter enabled and without the diode external path, see the Figure 29 and Figure 30), it is evident that the current pulse generated during LS turn-off is suppressed by the countermeasure.

Figure 27. External diode path and BT1 disabled (#2)

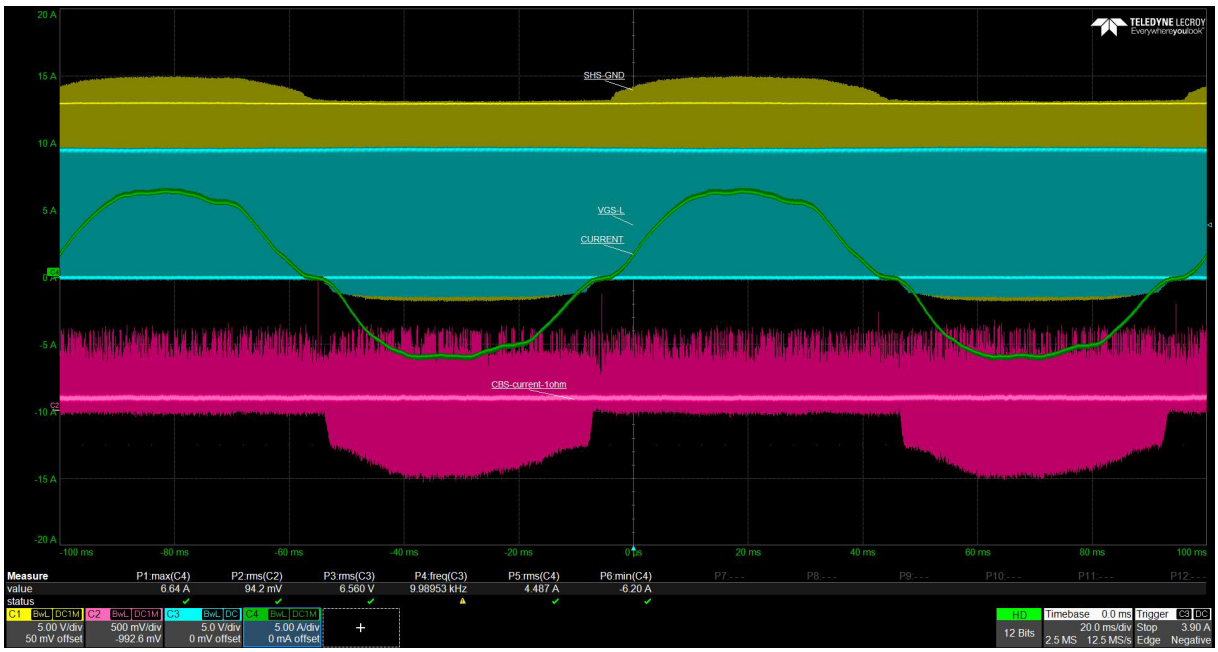


Figure 28. External diode path and BT1 disabled (#2) - Detail

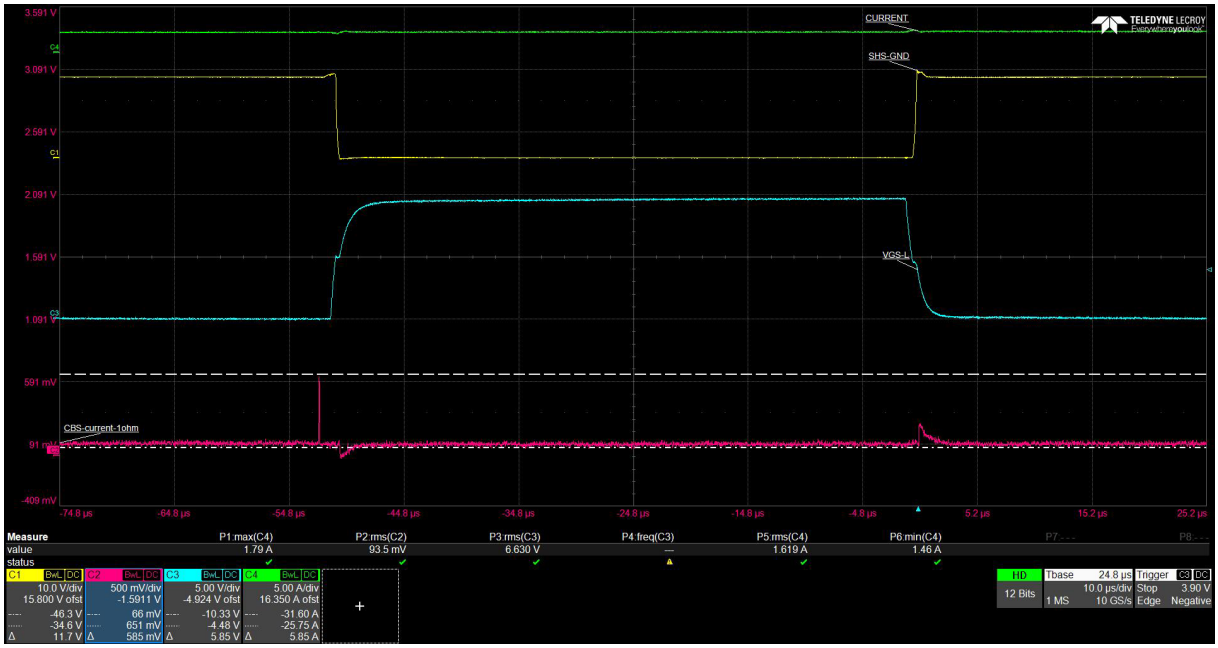


Figure 29. **No external diode path and BT1 enabled**

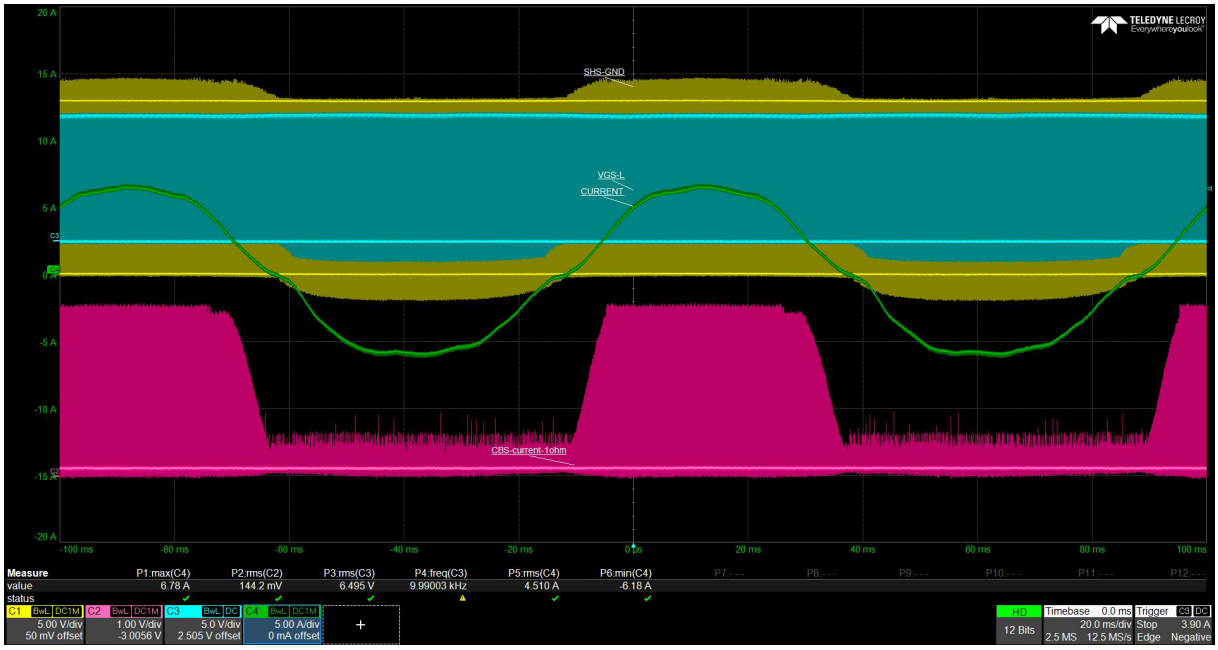
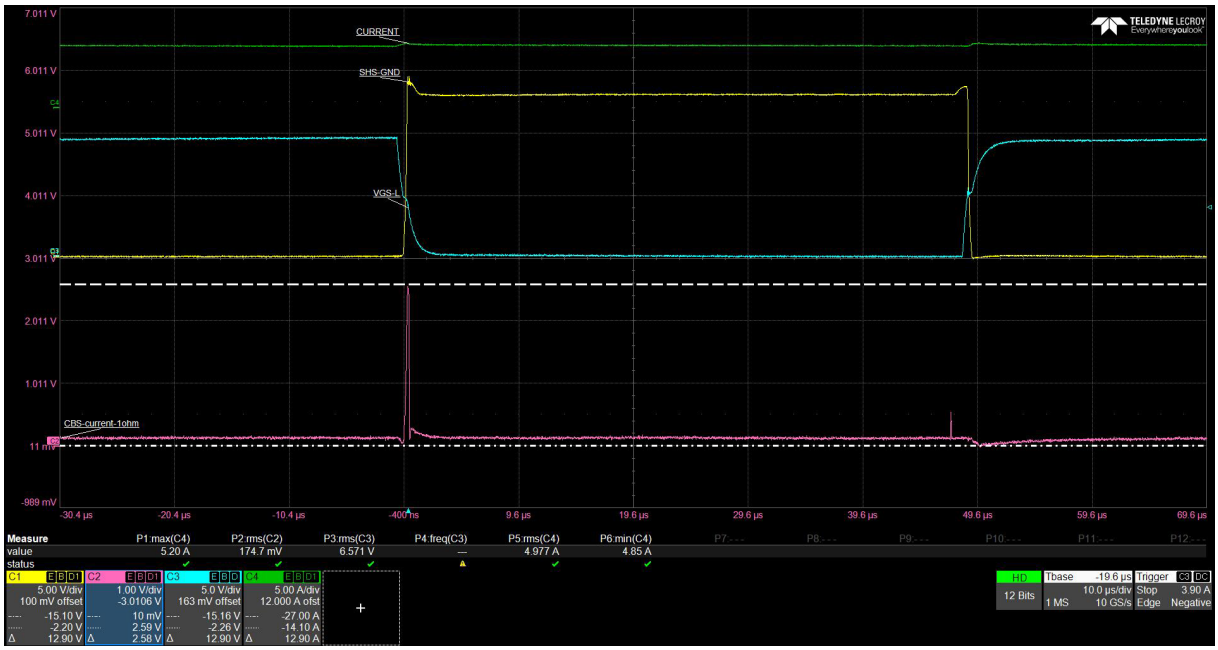


Figure 30. **No external diode path and BT1 enabled - Detail**



Revision history

Table 3. **Document revision history**

Date	Version	Changes
07-Feb-2024	1	Initial release.

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