STEVAL-ISA172V3 2 kW - PSFB DC-DC application note

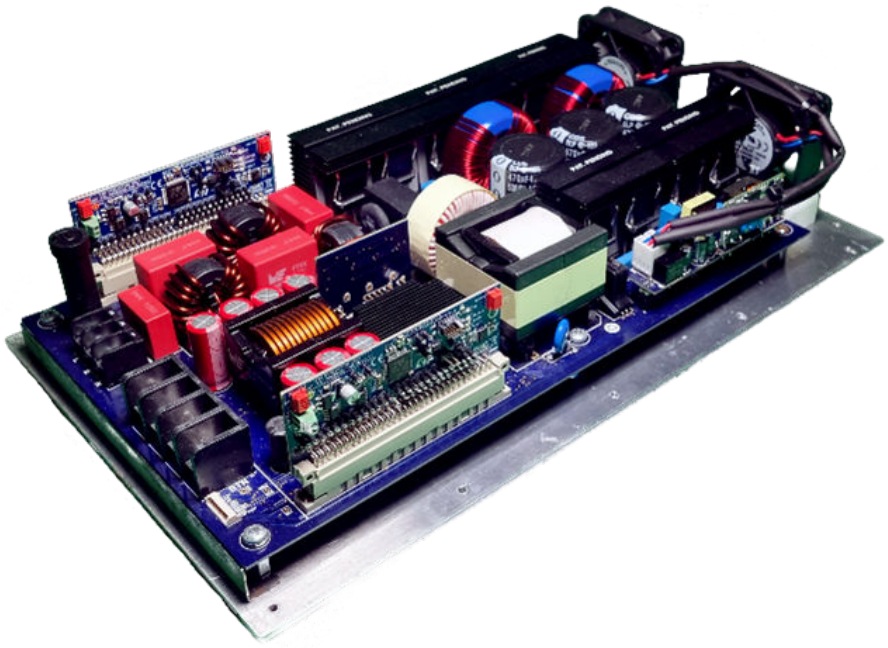
Introduction

The STEVAL-ISA172V3 is a 2kW single-output, fully digital switch mode AC-DC power supply designed for high-performance applications. This evaluation module (EVM) features two main sections: a two-phase interleaved power factor corrector (PFC) and a DC-DC phase-shifted full-bridge converter, each controlled by an STM32G474 microcontroller for precise regulation and efficient operation.

The interleaved PFC is composed of two boost converters operating 180° out of phase, utilizing 600 V MDmesh M6 Power MOSFETs to achieve high efficiency, and interleaved to reduced input current ripple. In the downstream stage, a DC-DC phase-shifted full-bridge converter based on MDmesh DM6 Power MOSFETs steps down the voltage with the help of a high-frequency transformer. The primary-to-secondary turns ratio is selected to maintain optimal efficiency and regulation throughout the entire operating range.

On the primary side of the transformer, zero voltage switching (ZVS) operation of the phase-shifted full-bridge converter minimizes switching losses and improves overall efficiency. On the secondary side, synchronous rectification (SR) is employed to reduce conduction losses. The output voltage waveform is rectified using STripFET Power MOSFETs and then smoothed by the output filter, ensuring a stable and low-noise output voltage for the target application.

Figure 1. STEVAL-ISA172V3 2 kW AC-DC EVM



*Notice: For dedicated assistance, submit a request through our online support portal at **www.st.com/support**.*

1 Disclaimers for safety

Danger: *Use the kit only after applying a fire-resistant protective cover. The protective cover is not included in the kit package.*

There is a danger of serious personal injury, property damage, or death due to electrical shock and burn hazards if the kit or its components are improperly used or installed incorrectly.

Warning: *The kit is not electrically isolated from the high-voltage supply AC-DC input.*

The evaluation kit is directly linked to the mains voltage. No insulation is ensured between the accessible parts and the high voltage. All measurement equipment must be properly isolated from the mains before powering the kit.

When using an oscilloscope with the evaluation kit, the oscilloscope must be isolated from the AC line.This precaution reduces the risk of electric shock when touching a single point in the circuit, but does NOT prevent electric shock when simultaneously touching two or more points in the circuit.

Caution: *During assembly, testing, and operation, the evaluation kit presents several inherent hazards, including but not limited to bare wires, moving or rotating parts and hot surfaces. All operations involving transportation, installation, commissioning, operation, servicing, and maintenance of the kit must be performed exclusively by Skilled Persons, as defined in standard IEC 62368-1, who are trained and experienced in power electronic systems and aware of the associated hazards.*

The board has to be connected directly on the mains. Non-isolated parts at high-voltage levels are present on both sides of the PCB .

Work area safety:

- The work area must be clean and tidy.
- Do not work alone while the kit is powered.
- Protect the work area against unauthorized access by means of suitable barriers and warning signs.
- Any system architecture supplying power to the evaluation kit must include additional control and protective devices in accordance with applicable safety regulations, technical equipment standards, and accident prevention rules.

Electrical safety:

- Remove the power supply from the evaluation kit and electrical loads before performing any electrical measurement.
- Arrange the measurement setup, wiring, and configuration with particular attention to the high voltage section.
- Power the kit only after the setup has been completed and verified.
- Fuse protection is not included with this evaluation kit.

Danger: *Do not touch the evaluation kit when it is powered or immediately after it has been disconnected from the voltage supply as several parts and power terminals containing potentially energized capacitors need time to discharge, and heat-sinks and transformers may still be extremely hot.*

Personal safety:

- Always wear appropriate personal protective equipment (PPE), such as insulating gloves and safety glasses.
- Take adequate precautions to prevent accidental contact with hazardous parts.
- Use suitable protective shields, such as insulating box with interlocks.

2 AC-DC PSU high voltage warning

Operation of the AC-DC PSU involves high voltages. These voltages have the potential to be lethal and users are advised to take adequate safety precautions. Before applying any electrical power, the user is advised to read and familiarize themselves with the use and operation of the AC-DC PSU.

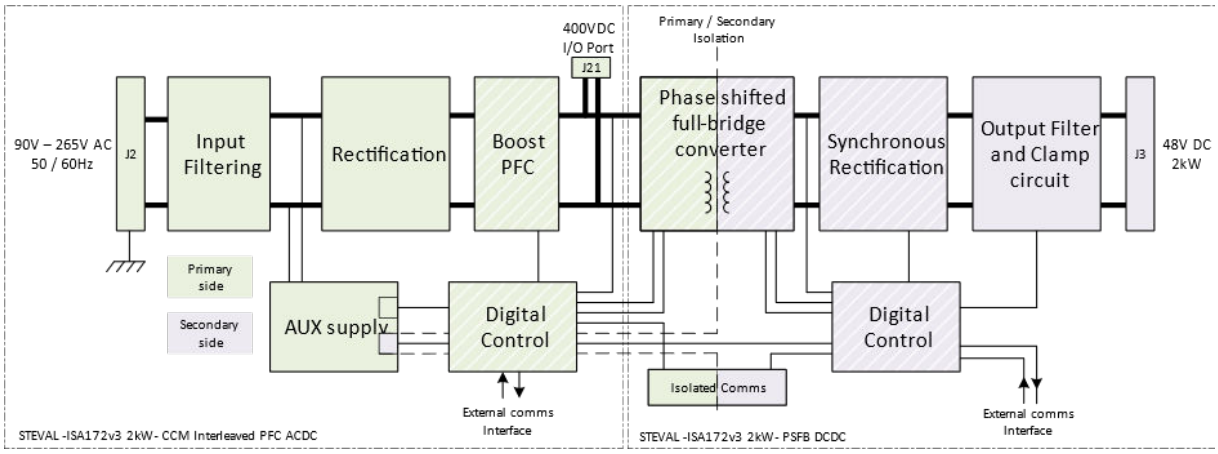
3 Overview of the complete 2 kW AC-DC converter

This overview considers the complete design of the 2kW AC-DC PSU. The design stages are described in greater detail in two separate but related application notes: 'STEVAL-ISA172V3 2 kW - CCM interleaved PFC AC-DC' and 'STEVAL-ISA172V3 2 kW - PSFB DC-DC'.

The first application note, 'STEVAL-ISA172V3 2 kW - CCM interleaved PFC AC-DC', discusses the auxiliary (AUX), primary rectification, boost PFC, and digital control stages. The second application note, 'STEVAL-ISA172V3 2 kW - PSFB DC-DC', covers the phase-shifted full-bridge converter, synchronous rectifier, output filter, and clamp stages.

The 2kW AC-DC PSU is a digitally controlled power supply capable of operating in various modes, configurable through debugging options set via the STLINK programming interface. By default, the AC-DC PSU operates with an AC input voltage range of 90 to 265 Vrms at 50/60 Hz, generating an isolated and regulated 40-54 Vdc output (48 Vdc nominal) up to 2 kW.

Figure 2. 2 kW AC-DC converter block diagram



A bidirectional DC port (J21) is included, allowing users to tap up to 2 kW from the output of the boost PFC stage or input up to 400 V DC to power the downstream DC-DC stage, which consists of the phase-shifted full-bridge converter and synchronous rectifier.

The AC-DC PSU comprises input filtering and rectification, two digitally controlled power stages, output filtering, a low-power AUX supply, and an isolated communication and control interface for configuration and control. Cooling fans and a temperature monitoring function are also integrated into the design.

3.1 Digitally controlled main power stages

The digital control algorithms used on both the STEVAL-ISA172V3 2 kW - CCM interleaved PFC AC-DC and the STEVAL-ISA172V3 2 kW - PSFB DC-DC, are implemented using the STMicroelectronics STM32G474 MCU.

The STM32G474 MCU is a feature-rich 32-bit Arm Cortex®-M4. For this implementation, the microcontrollers are fitted to two identical small ‘daughter’ cards STEVAL-DPSG474M that plug into connectors J4 and J5 of the main power PCB. MCU power is provided by two isolated power rails from the AUX supply. For the STEVAL-ISA172V3 2 kW - CCM interleaved PFC AC-DC, the MCU power supply is referenced to the input ground, GND1, and for the STEVAL-ISA172V3 2 kW - PSFB DC-DC, the supply is referenced to the output ground, GND2.

The voltage and current sensing for both digital controllers is filtered and scaled on the main power PCB and connected to the input pins of the ADC onboard the microcontroller. Similarly, control of the MOSFET is provided by the configurable high-resolution timer (HRTIM) modules onboard the microcontrollers. There are programmable LEDs that can provide visual indication of the operation of functions. Programming and debug access is provided by JTAG interface and can be performed using an STLINK programmer available separately. Reading of the state variables during operation is possible by means of the STLINK and a computer running the STM32CubeIDE and evaluation board project.

The digital control loops manage two primary power switching stages: the boost power factor corrector (PFC) and the phase-shifted full-bridge (PSFB) converter, and synchronous rectifier. The digitally controlled PSFB power stage employs zero-voltage switching (ZVS) and synchronous rectification to maximize efficiency and achieve optimal EMI performance.

3.2 Boost PFC output–external bidirectional port

The boost PFC stage includes an external port (J21) that allows the 400V DC rail to be ‘tapped off’ for use in applications other than the phase shifted full bridge converter stage contained in the AC-DC PSU. It also allows for the phase-shifted full bridge converter stage contained in the AC-DC PSU to be powered by an external DC source. This externally provided source can be in any of two ranges 50 to 60 V DC to allow low voltage testing and 350 V to 400 V DC to provide the full power of the phase shifted full bridge converter stage contained in the AC-DC PSU.

3.3 Simplified operation of the complete AC-DC converter

The AC input voltage is rectified using a simple 4 diode bridge to provide an unregulated DC voltage VIN_PFC (a rectified sinusoid shape). This voltage is connected to the input of a boost PFC stage that boosts the voltage to a regulated 400Vdc (nominal) - VBUS. This boost stage ensures that the input current tracks the AC input voltage waveform and that the input current is in phase with the voltage–this will lead to a near unity power factor and an input current waveform that has little harmonics above the fundamental. This is needed to meet legislative requirements regarding input current harmonics, such as EN-61000-3-2.

A large storage capacitance on the output of the boost stage provides a hold-up, that will maintain operation of the converter in the event of a momentary interruption of the AC input.

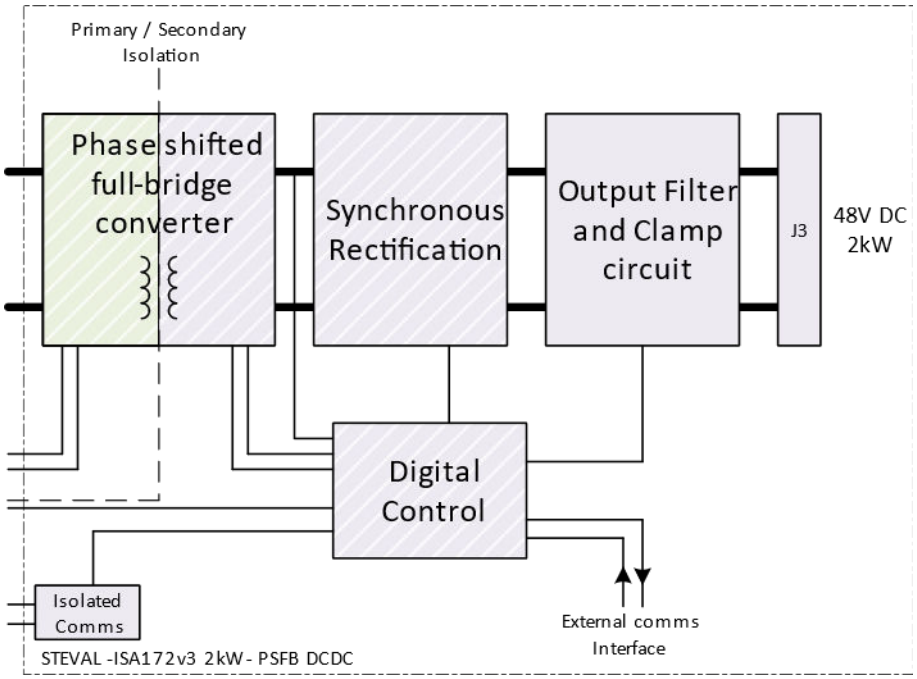
The main power stage of the converter is a phase shifted, full bridge topology, which provides an isolated and regulated 48 V DC (nom.) output voltage. An advantage to this approach is improved efficiency over a conventional full bridge by way of zero voltage switching that reduces component stress and EMI. To further improve the overall efficiency, synchronous rectifiers are used in the output stage. A simple LC output filter provides a low ripple DC output voltage.

An I²C communication interface is provided (referenced to the secondary ground) that allows configuration and control of the power stage. The unit is fan cooled with a temperature monitoring.

The converter can be configured to operate in constant voltage (CV) mode (from 40 V to 55Vdc, with a +/-1% set tolerance) or constant current (CC) mode (0A to 42A, with a +/- 10% set tolerance). It is also possible to power the PSFB converter externally via J21 from a DC input in the range 350 to 400Vdc and also in a low voltage mode (60Vdc in 4.8Vdc out) to aid in test and fault diagnosis.

4 Phase-shifted full-bridge converter operation

Figure 3. **Phase-shifted full-bridge converter block diagram**



4.1 Phase-shifted full-bridge converter

The phase-shifted full-bridge converter is a transformer isolated DC-DC converter that utilizes both the stray inductance of the transformer and an additional primary side resonant inductance in series with the transformer to enable zero voltage switching (ZVS) of the main drive switches (the full-bridge MOSFETs). This technique improves the switching efficiency of the MOSFETs by ensuring that during the turn-on time, at the beginning of each switching cycle, the voltage across the MOSFET is as close to zero as possible. ZVS, as opposed to the standard ‘hard switching’, improves efficiency, significantly reduces electrical / thermal stress and reduces EMI.

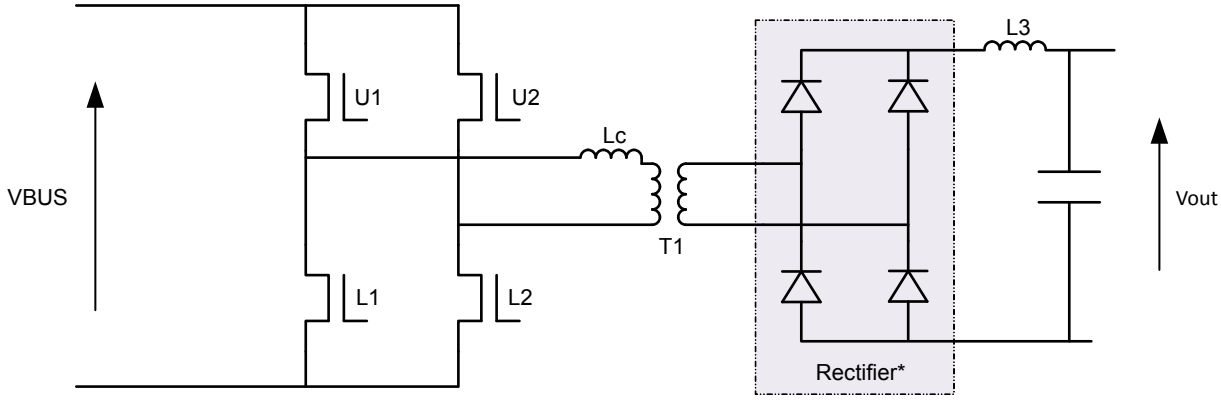
The full Bridge transformer (as opposed to half bridge or forward transformer) provides for the most efficient use of a transformer as it utilizes the full swing of the B-H curve. As such, the size of the transformer is better optimized and is smaller than an equivalent power level non-full bridge. When correctly operated, the design does not require any form of ‘core reset’ as the flux swings fully in both positive and negative directions, resulting in net zero flux.

4.2 How the zero voltage switching (ZVS) technique works

The following is a simplified explanation of the operation of the phase shifted full bridge converter. It is not intended to provide full design considerations of each circuit element; it is a broad overview explaining how the zero voltage switching (ZVS) is achieved.

For this implementation of zero voltage switching (ZVS) a fixed frequency, phase shift technique is implemented by way of the phase-shifted full-bridge converter.

Figure 4. **Phase-shifted full-bridge converter**



Section 4.2 is a simplified diagram of the phase-shifted full-bridge converter. To ease understanding, the synchronous rectifier stage of this design has been replaced with a conventional diode bridge rectifier. Detailed operation of the synchronous rectifier stage is described later in this section.

4.3 Conventional full-bridge converter – Non-ZVS operation

In a conventional full bridge design, the inductor Lc is not present, and is replaced with a direct connection between the MOSFET bridge and the transformer T1. Thus, other than the parasitic elements of the transformer, there is no intended additional inductance. During operation of the conventional full bridge, the diagonally opposing MOSFETs (U1 and L2 or U2 and L1) are turned ON and OFF in turn, applying current to the transformer primary alternately and thus to the output rectifier and filter stage. Importantly the timing of each pair of MOSFETs is fixed such that they turn ON or OFF at the same moment. Modulation of the duty cycle to achieve the correct output voltage and current, is determined by the control algorithm provided by either an analog or digital control strategy.

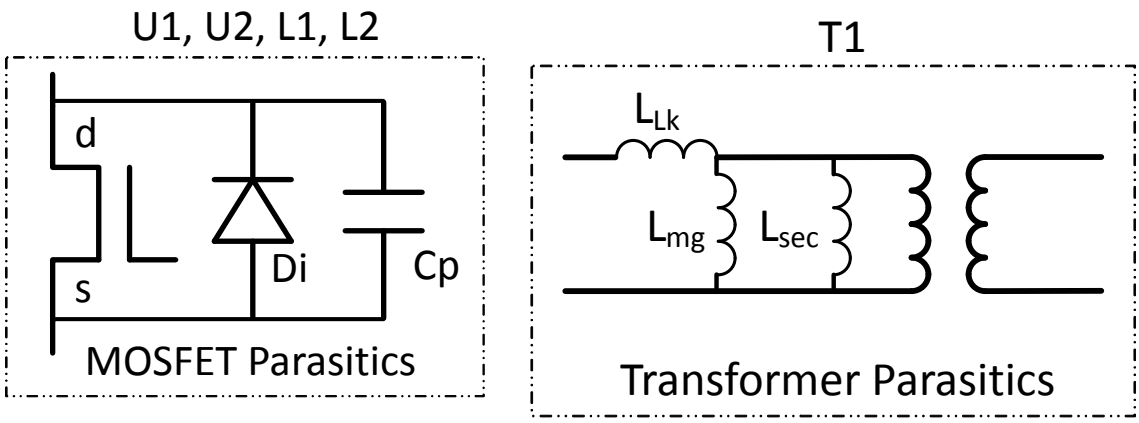
At the point of switching, the MOSFETs will have a large current flowing and need to switch the full supply voltage. This ‘hard’ switching exposes the MOSFETs to both large electrical and thermal stress and, as a result of the very high dv/dt, can cause unwanted resonance with the parasitic inductance and capacitance of the transformer and MOSFETs resulting in problems with EMI.

4.4 Phase-shifted full-bridge converter – ZVS operation

By utilizing both the parasitic elements of the switching bridge (MOSFET capacitance and transformer stray inductance) and additional inductance in series with the transformer (Lc), a semiresonant MOSFET (switch) transition is achieved that ensures that during the MOSFET transitions (OFF to ON and ON to OFF), there is zero-voltage (or very near zero) present across the drain to source, which ensures minimal power loss and reduced EMI.

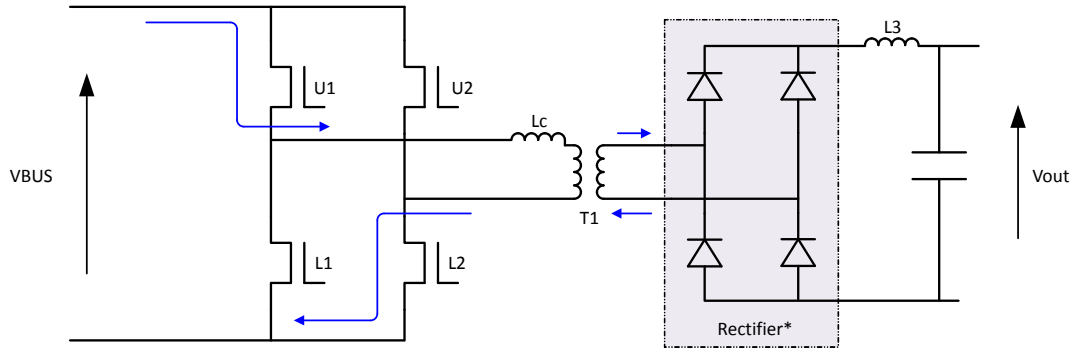
To more fully understand the effect this has, the ideal MOSFET and the transformer need to be considered with their respective parasitic elements (see Section 4.4). The MOSFET has two main parasitic elements, the intrinsic body diode (Di) and the output capacitance (Cp), both of which affect the speed at which the MOSFET can switch are included, and for the transformer it has to be considered as a more complete model including its leakage, magnetizing and a simplified secondary inductance.

Figure 5. MOSFET and transformer with parasitic elements



Section 4.4 shows a simplified representation of the more complete MOSFET and transformer, however for ease of understanding, all other diagrams employ an ideal representation of the MOSFET and the transformer, but when considering the operation, the parasitic elements and their effect need to be understood.

Figure 6. Phase-shifted full bridge before transition



In Section 4.4 diagonal MOSFETs U1 and L2 are ON and current is flowing through the primary of the transformer T1 and the inductor Lc, as indicated by the blue arrows. Current is also flowing in the secondary of the transformer and through the output inductor L3, delivering power to the load. During this time the voltage on the source of MOSFET U2 is very close to 0V (other than the voltage caused by the current and the resistance Rds of MOSFET L2), that is, the Vds of U2 is the full voltage of the bus (VBUS). Similarly, the drain of L1 is close to the full voltage of the bus (VBUS) as well, so the Vds of L1 is the full voltage of the bus (VBUS).

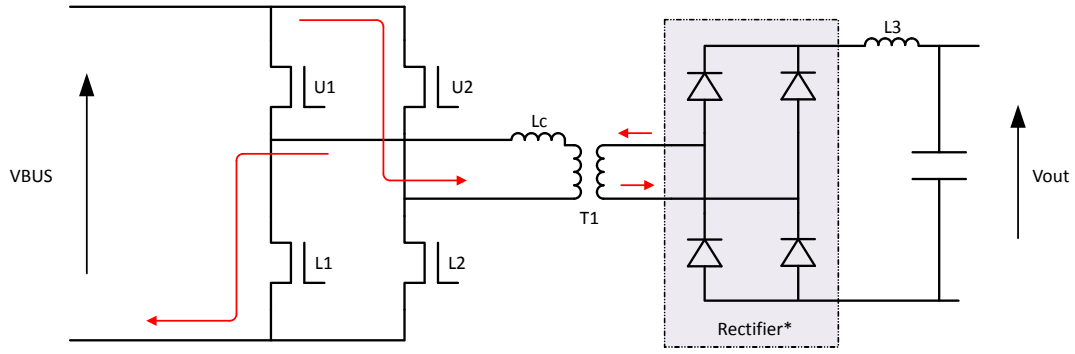
To initiate a transition of the power cycle from primary current flowing in U1 and L2 to flowing in U2 and L1, only L2 is turned OFF by the MCU. Now the primary current that was flowing through the MOSFET conduction channel is maintained by the inductance Lc and Llk, and begins flowing through the parasitic capacitance (Cp) of L2 (see Section 4.4). As a result of this current flow, the voltage on the drain of L2 and the voltage on the source of U2 rise to the supply rail. This voltage rise discharges the parasitic capacitance of U2 and critically, results in near zero voltage condition across the U2, such that it will allow it to switch with extremely low losses – zero voltage switching, ZVS.

Before U2 is turned ON by the controller, the voltage across the transformer will have fallen to zero, and the primary current will now be flowing through the MOSFET U1 (ON) and the intrinsic body diode of U2. At this point, the transformer is no longer providing power to the secondary, so the output inductor L3 maintains the power delivery as it begins to discharge. The only voltage across U2 will be that of its intrinsic body diode and at this point the MOSFET U2 can be switched on.

To transition the power delivery to U2 and L1, U1 is now turned off, resulting in the primary current now flowing through the parasitic capacitance of U1 and resulting in the voltage across the MOSFET rising. This rise in voltage across U1 results in the voltage across L1 falling to virtually zero, limited by the forward bias voltage of the intrinsic body diode. This sets up the condition of MOSFET L1 having virtually zero volts across it, again providing the opportunity for the MOSFET L1 to switch ON with zero volts across it – ZVS.

Synchronized to the frequency of the converter, L1 is turned ON completing the transition of power delivery to U2 and L1 and commencing a power delivery period with current flowing through the transformer and inductor in the opposite direction, as indicated by the red in the figure below.

Figure 7. Phase-shifted full bridge after transition



The rising current flowing in the primary will be a product of the duty cycle of the MOSFETs (the time they are ON), the magnitude of the applied voltage (VBUS), the turns ratio of the transformer (N), the value of the output inductor L3 and the current demand placed on the output. At the end of the switching cycle, determined by the phase shift value, the switches will need to change back to U1 and L2. This is achieved by first turning off MOSFET U2. Much like the previous cycle, the primary current, which is maintained by the resonant condition provided by inductor Lc, Llk and the MOSFET capacitances, will be transferred through U2's capacitance. This results in the voltage across U2 rising as the source voltage falls and at the same time causing the voltage across L2 to fall to virtually zero. The ZVS cycle commences similarly to the previous cycle.

It is this change from switching both U1 and L2 at the same time (or U2 and L1) to switching them at different times, a phase shift, which allows the semiresonant condition and ZVS to occur.

The load current, input voltage, turns ratio and ratio of leakage inductance to magnetizing inductance of the transformer will determine the phase shift and thus the effective duty cycle required to achieve the desired output voltage. Exact calculation of these parameters is beyond the scope of this application note.

4.5 MOSFET gate drive circuitry

Proper MOSFET operation requires the gate pin of the bridge MOSFETs to be driven sufficiently above the source voltage, so as to ensure that the MOSFET is fully on. This means that the gate of the upper MOSFETs (Q3 and Q6) need to be able to drive above the ~400 V of the MOSFET drain voltage (VBUS). To achieve this, galvanically isolated drivers are used (U4, 6, 7, and 9, STGAP2HS) that provide the required offset. Gate control is provided by the PWM outputs of the MCU.

Table 1. Gate drive signals for the phase-shifted full-bridge stage

Signal function	Schematic reference	CubeMX signal name	MCU pin ref.
Bridge MOSFET Q1	GATE_Q1_ON / GATE_Q1_OFF	(SEC) PWM_HS1_GPIO_PIN	PB12
Bridge MOSFET Q2	GATE_Q2_ON / GATE_Q2_OFF	(SEC) PWM_LS1_GPIO_PIN	PB13
Bridge MOSFET Q3	GATE_Q3_ON / GATE_Q3_OFF	(SEC) PWM_HS2_GPIO_PIN	PA10
Bridge MOSFET Q4	GATE_Q4_ON / GATE_Q4_OFF	(SEC) PWM_LS2_GPIO_PIN	PA11

The MOSFET gate drivers are AC coupled and have separate HIGH drive and LOW drive current limits. This allows adjustment of the turn ON and turn OFF characteristics associated with driving high speed MOSFET gates.

4.6 Current and voltage sensing

Primary current sensing is provided by a Hall effect current sensor (U18) connected in series with the transformer primary winding. The output of U18 is filtered and fed to the secondary side MCU. Being a Hall effect sensor, there is no electrical contact with the primary side of the transformer and as such is electrical isolation is maintained between the primary (power input side) and the secondary.

Voltage sensing of the output is achieved with simple resistive potential divider chains and op-amps connected directly to the output rail. The op amp output is filtered and the voltage is read by the ADC of the secondary side MCU.

4.7 Output current monitoring

Output current demand is monitored using a low value (1mΩ) resistor through which the output current flows. The voltage across this resistor, which is directly proportional to the current, is measured by a 'high-side' monitoring op amp (U9) and the resulting voltage connected to the secondary side MCU. This allows for constant current control and voltage foldback when the output current exceeds the preprogrammed limit.

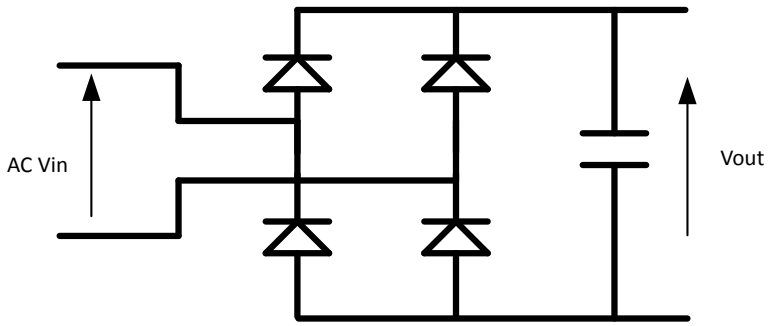
Table 2. Monitor signals for the phase shifted full bridge and synchronous rectifier stage

Signal function	Schematic reference	CubeMX signal name	MCU pin ref.
Output Voltage	VOUT	(SEC) ADCx_VOUT_CHANNEL_PIN	PA0
Output Current	IOUT	(SEC) ADCx_IOUT_CHANNEL_PIN	PA2

4.8 Synchronous rectification stage

The converter utilizes a synchronous rectifier stage on the output of the PSFB converter to rectify the output DC voltage. Synchronous rectification (sometimes referred to as active rectification) is a method where the AC voltage is rectified by active switching elements (usually MOSFETs) as opposed to conventional rectifier diodes.

Figure 8. Conventional diode bridge rectifier stage



In a conventional rectifier shown in Figure 8, the AC voltage is allowed to flow in one direction only, by way of the diodes basic function. This is a simple and reliable method of rectification, but has a downside of conduction loss and subsequent power loss for increasing levels of current.

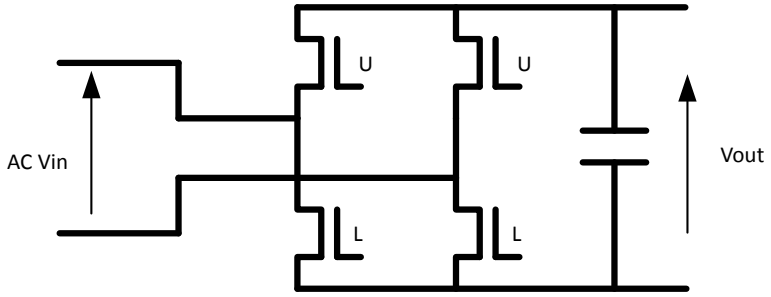
Simply put, power loss = Vf x Iout so for a 10A output and a Vf of 1.2 V, the rectification loss = 12 W.

Replacing the rectifier diode with a controlled or synchronous switch (MOSFET) that turns ON only during the positive half of a wave form, it is possible to reduce the rectification power losses significantly.

Using a MOSFET with Rds of 5mΩ and current of 10A, the losses are reduced to 0.5 W, 4.2% of the loss from using conventional rectifier diodes.

For the synchronous rectifier stage to operate correctly, it is necessary to ensure that the MOSFETs are turned ON and OFF at the correct time. Failure to do so could be catastrophic in a bridge rectifier as it is possible that the output could be shorted directly through the MOSFETs if the upper were on at the same time as the lower. Correct timing of the synchronous rectifier gate drives is achieved as knowledge of the primary side full-bridge MOSFETs switching is also controlled by the same secondary side MCU. Therefore, the switching of the synchronous rectifiers can be accurately controlled by the same MCU.

Figure 9. **Simple synchronous rectifier configuration**



4.9 Synchronous rectifier MOSFET gate drive circuitry

As with the full Bridge MOSFETs, proper MOSFET operation requires the gate pin of the synchronous rectifier MOSFETs to be driven sufficiently above the voltage on the source pin, so as to ensure that the MOSFET is fully on. This means that the gate of the upper synchronous rectifier MOSFETs (Q16, 17, 18, 19, 20, and 21) need to be able to drive above the peak voltage at the output of the main power transformer, i.e., the MOSFET drain voltage. For these synchronous rectifiers, isolation is not needed as the digital controller is already referenced to the secondary side, so only sufficient voltage offset is required. To achieve this, the design uses boot strapped, high current drivers (IC3, 4, 5, 6, 7 and 8, L6498).

Control signals for the synchronous rectifier gate control is provided again by the HRTIM module onboard the MCU.

Table 3. **Gate drive signals for the synchronous rectifier stage**

Signal function	Schematic reference	CubeMX signal name	MCU pin ref.
Synchronous Rectifier Q1	SR_Q1A, SR_Q1B, SR_Q1C	(SEC) PWM_SR1_GPIO_PIN	PB14
Synchronous Rectifier Q2	SR_Q2A, SR_Q2B, SR_Q2C	(SEC) PWM_SR2_GPIO_PIN	PB15
Synchronous Rectifier Q4	SR_Q4A, SR_Q4B, SR_Q4C	(SEC) PWM_SR4_GPIO_PIN	PA9
Synchronous Rectifier Q3	SR_Q3A, SR_Q3B, SR_Q3C	(SEC) PWM_SR3_GPIO_PIN	PA8

4.10 Output filter stage

As with all forward derived topologies, a simple LC filter stage is used on the output of the converter to smooth the high frequency square wave voltage on the secondary side of the transformer to a DC output voltage. This LC filter has a roll-off frequency of approximately 1kHz.

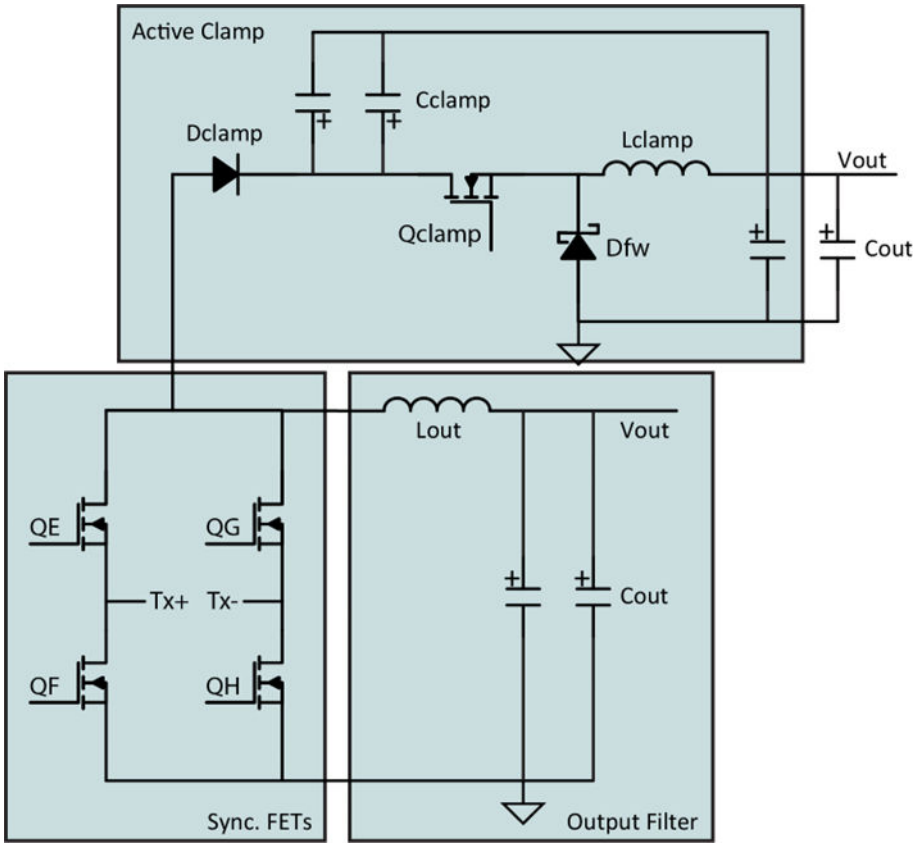
4.11 Active clamp

The leakage inductance, as seen on the secondary side of the transformer, will ring with the parasitic capacitance across the synchronous rectifiers when they are turned off at the end of the power delivery cycle. This ring can cause EMI failures and may also be beyond the gate-source breakdown voltage of the synchronous MOSFETs used.

Therefore, it is necessary to add a clamp circuit to reduce the amplitude of the ringing and also damp the oscillations such that they decay quickly. There are many methods of implementing this type of circuit, however, for this EVM and active clamp circuit used with the aim of recovering the energy stored in the secondary side leakage inductance and transferring to the output capacitors.

This is achieved by means of what is essentially a mini-Buck converter. Section 4.11 shows a simplified circuit of the active clamp. When the synchronous MOSFETs turn off, the energy stored in the leakage inductance on the secondary side of the transformer will start to ring with the parasitic capacitance of the synchronous rectifiers. When the ring voltage increases above the steady state voltage across the clamp capacitors, which are much larger than the Coss of the synchronous rectifiers, the diode Dclamp will become forward biased and the energy stored in the leakage instance will be transferred to the clamp capacitators effectively clamping the voltage across the synchronous rectifiers MOSFETs at the voltage of the clamp capacitors.

Figure 10. **Simplified active clamp circuit**



The clamp capacitors must then be discharged such that this process can be repeated in the subsequent cycles. To recycle this energy usefully the clamp capacitors are discharged into the output capacitors of the PSFB converter. This is achieved by switching Qclamp on for a small period of the cycle. The square wave is then filtered by the LC formed between Lclamp and the output capacitors of the PSFB converter. The snubber capacitors must be sized appropriately such that their voltage does not increase significantly from cycle to cycle for a given discharge period each cycle.

Because the energy is returned to the output stage rather than dissipated in a resistor as in traditional clamp circuits, the efficiency of the output stage is maximized.

Table 4. **Sense signal names**

Signal function	Schematic reference	CubeMX signal name	MCU pin ref.
Input Voltage sense (L & N)	Vin_P + Vin_P	(PRI) ADCx_MAIN_VOLTAGE_CHANNEL_PIN	n/a
Boost Phase 1 Current	*N/A*	(PRI) ADCx_CT_CURRENT1_CHANNEL_PIN	n/a
Rectified Input Voltage	VIN_PFC	(PRI) ADCx_RECT_VOLTAGE_CHANNEL_PIN	n/a
Boost Voltage	VBUS	(PRI) ADCy_VBUS_CHANNEL_PIN	n/a
Boost Phase 2 Current	N/A	(PRI) ADCz_CT_CURRENT2_CHANNEL_PIN	n/a
Bridge Current	*N/A*	(SEC) ADCx_IIN_CHANNEL_PIN	PC1 + PA3
Output Voltage	VOUT	(SEC) ADCx_VOUT_CHANNEL_PIN	PA0
Output Current	IOUT	(SEC) ADCx_IOUT_CHANNEL_PIN	PA2

Table 5. **Control signal names and their digital controller signal name**

Signal function	Schematic reference	CubeMX signal name	MCU pin ref.
Synchronous Rectifier Q1	SR_Q1A, SR_Q1B, SR_Q1C	(SEC) PWM_SR1_GPIO_PIN	PB14

Signal function	Schematic reference	CubeMX signal name	MCU pin ref.
Synchronous Rectifier Q2	SR_Q2A, SR_Q2B, SR_Q2C	(SEC) PWM_SR2_GPIO_PIN	PB15
Active Clamp Switch	CLAMP_GATE	(SEC) PWM_SR_CLAMP1	PC8
Synchronous Rectifier Q4	SR_Q4A, SR_Q4B, SR_Q4C	(SEC) PWM_SR4_GPIO_PIN	PA9
Synchronous Rectifier Q3	SR_Q3A, SR_Q3B, SR_Q3C	(SEC) PWM_SR3_GPIO_PIN	PA8
Bridge MOSFET Q1	GATE_Q1_ON / GATE_Q1_OFF	(SEC) PWM_HS1_GPIO_PIN	PB12
Bridge MOSFET Q2	GATE_Q2_ON / GATE_Q2_OFF	(SEC) PWM_LS1_GPIO_PIN	PB13
Bridge MOSFET Q3	GATE_Q3_ON / GATE_Q3_OFF	(SEC) PWM_HS2_GPIO_PIN	PA10
Bridge MOSFET Q4	GATE_Q4_ON / GATE_Q4_OFF	(SEC) PWM_LS2_GPIO_PIN	PA11

5 Voltage mode control explained

5.1 Advantages and disadvantages

Voltage mode control is one of the most popular control methods due to its simplicity and effectiveness in regulating an output voltage given any changes in load. Under voltage mode control, the output voltage is measured and compared with the desired set point or reference. The difference between the actual output voltage and the desired output voltage is used as an input to a controller and the output of the controller determines the new value of the duty cycle to close the control loop.

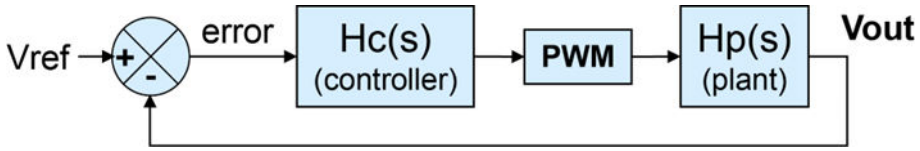
Therefore, unlike other methods of control such as peak current mode, the voltage mode controller only needs information about the output voltage to close the control loop and provide a regulated and stable output voltage. Typically, some current information is required to provide an overall power limit and prevent transformer saturation in transformer-isolated topologies.

Further advantages of voltage-mode control include the ability to step down the voltage by a significant amount and maintain proper regulation for small and no loads and provide good constant-voltage regulation for varying output voltage setpoints.

As discussed so far, voltage mode control has good load regulation – it compensates for any changes in load to maintain a set output voltage. However, in its standard implementation, voltage mode control has poor line regulation – there is a delay between the line voltage increasing or decreasing and the duty cycle adjusting to compensate for the subsequent change in output voltage. Therefore, it is common to add a “feedforward” term to the control loop, which is a measure of the input voltage. However, in the case of this AC-DC PSU, the input voltage is derived from the PFC bus and is relatively constant due to the action of the voltage loop within the PFC stage. Therefore, no feedforward term is implemented in this converter.

5.2 Step-by-step control loop

Figure 11. step-down converter control loop



The simplified control loop of a voltage mode converter is shown in Section 5.2. For this initial analysis, let us assume that the converter is a simple step-down converter operating under voltage mode control. Here, the power stage containing the switching MOSFETs, output filter inductor and output filter capacitor are all shown within the block Hp(s). This is referred to as the plant transfer function. The controller, which will be designed to compensate this control loop, is shown as the block Hc(s). This is referred to as the controller transfer function. The PWM block is usually included as part of the plant, Hp(s) block, however, it has been separated so that the effects of this block can be analyzed independently.

For the purposes of this discussion, we are currently working in the continuous-time domain, also known as the s-domain, and this is why the plant and controller are a function of the Laplace operator, s. The translation from the continuous-time domain to the discrete-time domain will be discussed later in this application note.

At steady state, the plant power stage will provide a fixed output voltage given the fixed input voltage and duty cycle. In Section 5.2 the output voltage of the power stage is fed back and compared with a reference, Vref. This is the desired output voltage and therefore if there is any deviation from the reference there will be a nonzero error term.

The error term is used as an input to the controller, Hc(s). The controller will manipulate the error term in some way depending on the type of controller that is designed. The output of the controller will be the duty cycle that is used as an input to the power stage and modulates the MOSFET switches.

This closed-loop control process can be easily visualized by means of a numerical example. For now, let us assume that the controller Hc(s) is a simple proportional controller with unity gain and the reference is set to the desired output voltage, for now assume this is 3.3 V.

If the output voltage dropped down to 3.2 V due to an increase in output load, then the error term would be calculated as follows:

$$V_{ERROR} = V_{REF} - V_{OUT}$$

$$V_{ERROR} = 3.3V - 3.2V$$

$$V_{ERROR} = 0.1V$$

As the proportional controller has unity gain, the output of the controller can be calculated as follows:

$$H_C(s) = \frac{Y(s)}{X(s)}$$

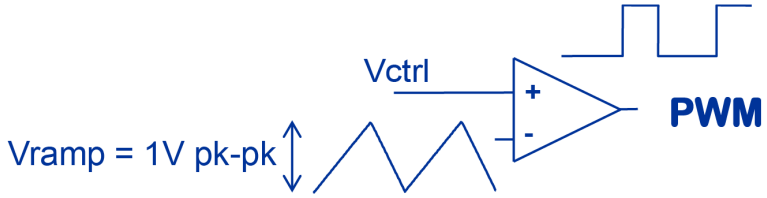
$$Y(s) = H_C(s) \times X(s)$$

$$Y(s) = 1 \times 0.1V$$

$$Y(s) = 0.1V$$

The output of the controller is then used as an input for the PWM block. The PWM block will take the controller output and convert this to an effective duty cycle. There are several different methods for achieving this, however for this analysis of the analog step-down converter, this is typically achieved using a PWM comparator and an RC ramp as shown in the following figure.

Figure 12. PWM comparator comparing RC ramp to control voltage



Within the PWM block the control voltage, $Vctrl$, which is the output of the previous controller block, is compared with an RC ramp using a comparator. The output of the comparator will be high when the control voltage is larger than the RC ramp voltage. Therefore, to achieve a 100% duty cycle the control voltage would need to be equal to the maximum RC ramp height. This is typically internal to many analog ICs and the implementation differs in digital, which will be discussed later in this application note. If, for now, we assume that the maximum ramp height is 1V, then the duty cycle can be calculated as follows:

$$Duty = X(s) \times PWM_{COMP}$$

$$Duty = 0.1V \times \left(\frac{100\%}{1V}\right)$$

$$Duty = 10\%$$

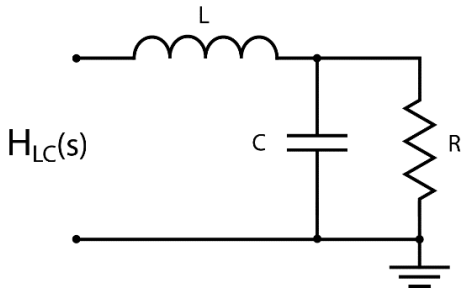
This is then used as an input to the plant block, which contains the buck power stage and thus subsequently determines the output voltage and the loop is now closed. This simplified analysis helps to explain the different blocks within the closed-loop system. However, in reality, the analysis performed is small-signal analysis with the purpose of determining the s-domain transfer functions for the different blocks within the system. In the case of this application note, the power stage is a PSFB converter and the modulation method differs slightly as it is the phase shift between the gate drive signals that provides an effective duty cycle.

The small-signal analysis aims to describe the behavior and therefore the output of the system given small changes in the input. The stability of the system can then be determined using this analysis. We will use the modeled behavior of our system, through means of s-domain transfer functions, to characterize the plant and then analytically design a compensator to stabilize the control loop.

5.3 Forward-type plant transfer function

The derivation of the forward-type power stage transfer function is straightforward under voltage-mode control. The output filter inductor resonates with the output filter capacitor forming a double pole in the plant transfer function. Consider the output LC filter of all forward converters shown in the following figure.

Figure 13. LC output filter of the step-down converter power stage



The transfer function of the LC filter can be determined using Laplace and by analyzing the impedances in series and parallel.

$$Z_1 = sL$$

$$Z_2 = \frac{1}{sC} // R$$

$$Z_2 = \frac{R \cdot \frac{1}{sC}}{R + \frac{1}{sC}}$$

$$Z_2 = \frac{R}{sCR + 1}$$

$$H_{LC}\left(s\right) = \frac{Z_2}{Z_1 + Z_2}$$

$$H_{LC}\left(s\right) = \frac{\frac{R}{sCR+1}}{sL + \frac{R}{sCR+1}}$$

$$H_{LC}(s) = \frac{R}{sL(sCR + 1) + R}$$

$$H_{LC}\left(s\right) = \frac{R}{s^2LCR + sL + R}$$

$$H_{LC}\left(s\right) = \frac{1}{s^2LC + s\frac{L}{R} + 1}$$

Putting this in the standard form for a second-order polynomial:

$$H_{LC}\left(s\right) = \frac{1}{\frac{s^2}{{\omega_{LC}}^2} + s\frac{1}{Q\omega_{LC}} + 1}$$

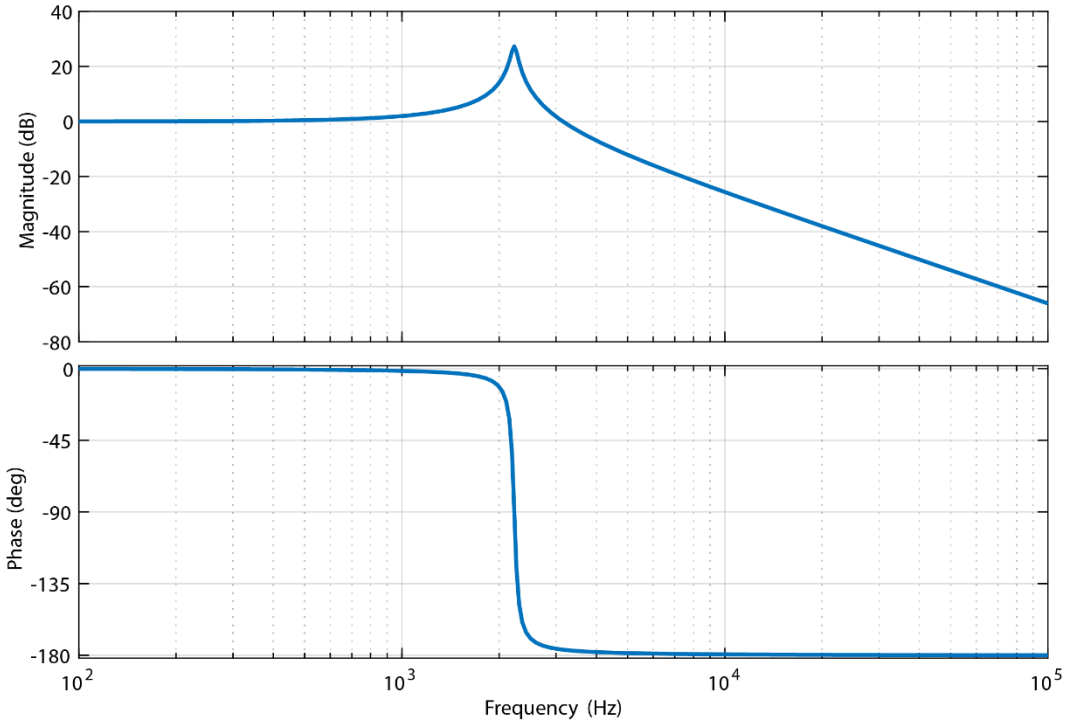
Therefore:

$$\omega_{LC} = \frac{1}{\sqrt{LC}}$$

$$Q = \frac{1}{2\zeta} = R\sqrt{\frac{C}{L}}$$

From this analysis, we can see that the double pole will have an undamped natural frequency, ω_n , and a resonant peak depending on the Q . The typical Bode plot of this double pole output filter is shown in Section 5.3. In the case of the phase-shifted full-bridge converter, the resonant inductance and effective duty cycle also impact the location and damping of this double pole. A full and detailed analysis is available in a paper titled “An enhanced model for small-signal analysis of the phase-shifted full-bridge converter”.

Figure 14. Bode plot of the LC filter transfer function

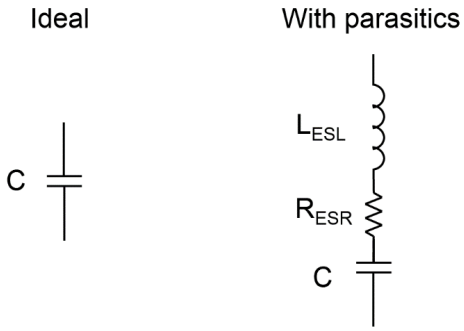


In the Bode plot shown in Section 5.3, the low-frequency gain is 0dB. This is because the LC filter will have no effect at low frequencies. However, in reality, there will be some low-frequency gain introduced by the modulation method being used, be it standard PWM or phase-shift modulation. For now, let us assume that this low frequency gain has a value G_{PWM} .

5.4 Capacitor ESR zero

The model discussed so far does not include the parasitic elements of the output filter capacitor. The parasitic elements of the capacitor are shown in Figure 15.

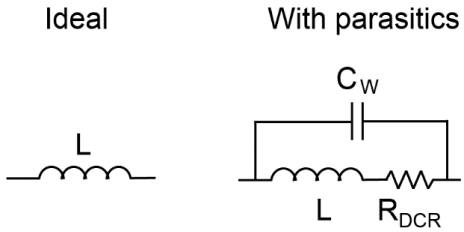
Figure 15. Ideal capacitor and capacitor with parasitic elements



The parasitic equivalent series resistance (ESR) has a significant impact on the plant transfer function for the Forward type converter. The parasitic equivalent series inductance of the capacitor is usually only dominant at much higher frequencies and therefore it can be ignored in this transfer function.

Likewise, the inductor will have the parasitic elements as shown in Figure 16. Typically, only the DC resistance (DCR) of the inductor windings is considered as the interwinding capacitance is only an issue at high frequencies that are above that of the control loop.

Figure 16. Ideal inductor and inductor with parasitic elements



The effect of the capacitor ESR is that the zero is formed in the power stage transfer function. The zero is shown in the numerator of the plant transfer function in Equation 1.

$$H_P(s) = \frac{\left(1 + \frac{s}{\omega_{ESR}}\right)}{\frac{s^2}{\omega_{LC}{}^2} + s\frac{1}{Q\omega_{LC}} + 1} \quad (1)$$

The location of the zero is given in Equation 2 and is dependent on the capacitance and the ESR value.

$$\omega_{ESR} = \frac{1}{C \cdot R_{ESR}} \quad (2)$$

The addition of the capacitor ESR and inductor DCR will also affect the damping of the double pole and the natural frequency. The updated equation for the Q and natural frequency of the double pole is given in Equation 3 and Equation 4.

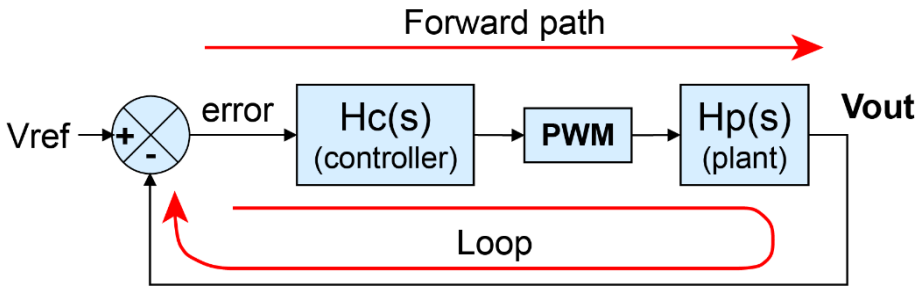
$$\omega_{LC} = \frac{1}{\sqrt{LC\left(1 + \frac{R_{ESR}}{R}\right)}} \quad (3)$$

$$Q = \frac{1}{\omega_{LC}\left(\frac{L}{R} + C\left(R_{ESR} + \left(1 + \frac{R_{ESR}}{R}\right)R_{DCR}\right)\right)} \quad (4)$$

6 Voltage mode compensator design

6.1 Loop stability criteria

Figure 17. **Closed-loop and open-loop transfer functions**



Consider the control loop of the converter shown in . In this Figure, the “Forward” and “Loop” paths of the control loop have been identified. The transfer function for the closed-loop system is given in Equation 5.

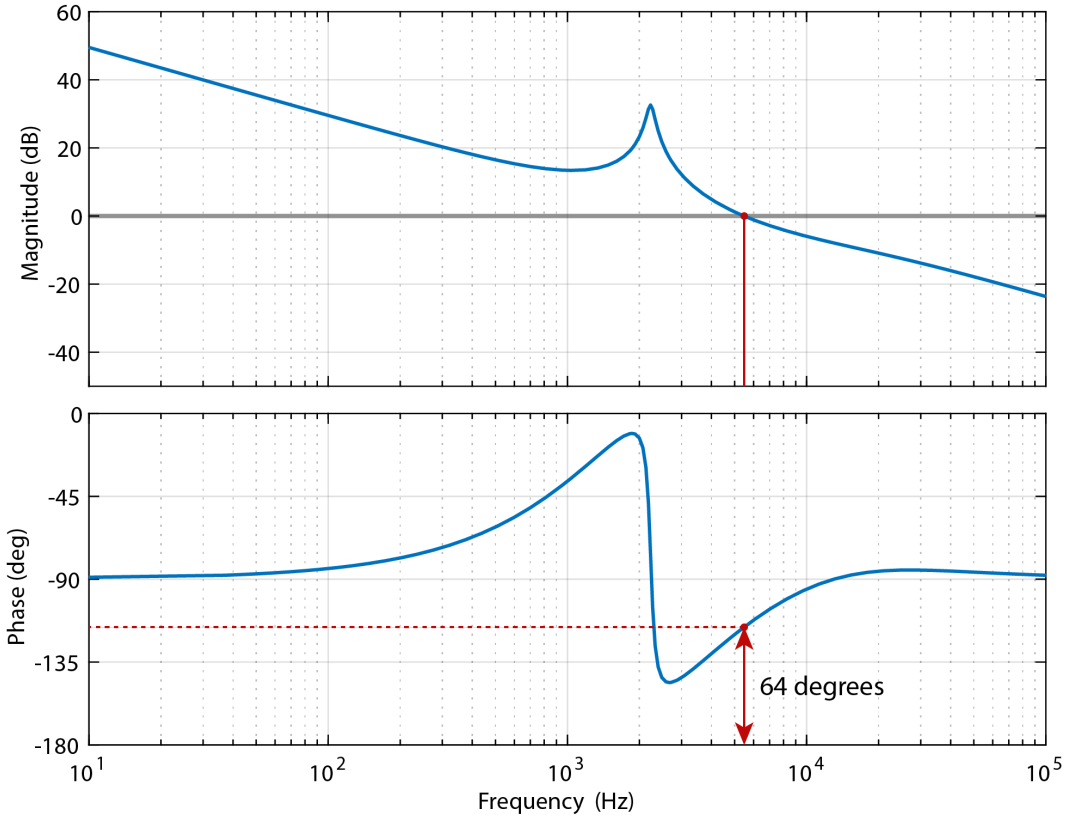
$$TF = \frac{Forward}{1 - Loop} \tag{5}$$

The closed-loop transfer function can be derived by applying this to Figure 17:

$$H_{CL}(s) = \frac{Foward}{1 - (-Loop)} \tag{6}$$

The loop response, which is also called the “open-loop”, is the compensator transfer function Hc(s) combined with the plant or power stage transfer function Hp(s) and also includes the modulator gain – the PWM block. The Bode plot of a typical loop response is shown in Figure 18.

Figure 18. **Open-loop Bode plot of step-down converter: plant, PWM, and compensator**



Several terms can be defined from this Bode plot. The first is the crossover frequency. This is the frequency at which the gain plot crosses the 0dB axis. If the gain plot is falling at a rate of 20dB/decade around the crossover frequency, then below the crossover frequency (i.e. at a lower frequency – going left on the frequency X-axis) the gain plot will have positive gain – i.e. it will have a gain that is greater than 1.

At the crossover frequency, the value of the phase in the open-loop will determine the stability of the closed-loop system. If the phase is -180 or less with a gain greater than or equal to 1 then the closed-loop system will become unstable. This can be seen from the denominator of Equation 6.

Therefore, to ensure stability, the phase of the open-loop system must be greater than -180 at the crossover frequency. This term is defined as the phase margin and is the amount by which the phase is above the -180° at the crossover frequency. Typically, the compensator will be designed such that the phase margin is 45° or more at the crossover frequency. A phase margin of 45° would equate to a loop phase of -135°. Therefore, the loop phase is 45° above the -180° point of instability. In Figure 18, the phase margin is shown as 64 degrees.

6.2 Crossover and phase margin specification

The choice of crossover frequency and phase margin will determine how well the converter responds to line and load transients. Typically, the higher the crossover frequency is the faster the response and recovery in the time domain. However, there are certain limitations that prevent the choice of a crossover frequency that is too high. In a standard analog voltage-mode controlled Forward converter, the plant phase will roll-off due to the double pole. The capacitor ESR zero will add phase to the loop however it cannot be relied upon to achieve stability. Furthermore, the op amp internal to analog control ICs will have introduce a phase roll-off as the frequency approaches the bandwidth.

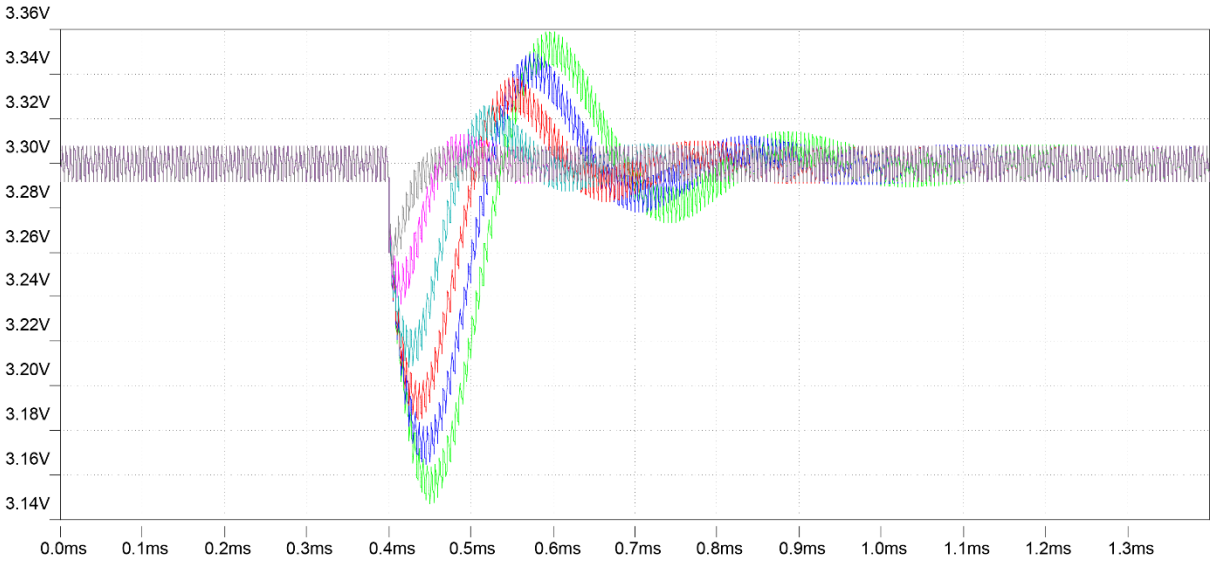
With a digital compensator, there is no analog op amp bandwidth to consider. However, the delays within the digital system will introduce a phase loss. As the frequencies approach the sampling frequency this phase loss becomes significant. A method for calculating the anticipated phase loss will be covered later in this application note. Therefore, a recommended starting point for the crossover frequency between 1/10th and 1/20th of the sampling frequency. This is assuming that the sampling frequency is the same as the switching frequency.

Crossover speciation: 1/10th to 1/20th of the sampling/switching frequency.

As discussed earlier, the phase margin is an indicator of the stability of the system. With 0° of phase margin, the system would become unstable. For <30° of phase margin, the system would likely have multiple oscillations in the time domain when subjected to the line and load transients. For 45° of phase margin, the system would likely have one ring in the time domain after recovery from a transient. Therefore, 45° of phase margin is typically the minimum allowable.

Conversely, a larger phase margin would result in a slower response to line and load transients. For example, a phase margin of 60° may result in zero overshoot, no ringing, and a slower recovery. Therefore, there must be a balance between the choice of crossover frequency and the amount of phase margin that the combined system has. In Figure 19, the step response for a system with decreasing crossover frequency and phase margin is shown (from gray to green). The response becomes slower and more oscillatory as the crossover and phase margin are both decreased.

Figure 19. Step response for a system with decreasing crossover and phase margin (gray to green)



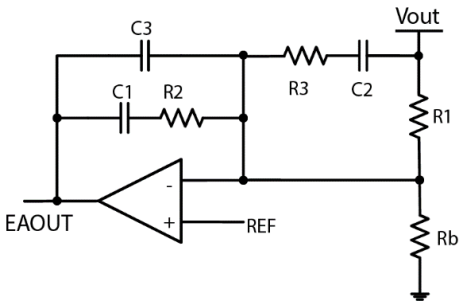
Phase margin specification: a minimum of 45° of phase margin at the crossover frequency. Ideally between 50° and 60°.

6.3 Types of Compensator

A compensator needs to be designed and added into the loop to shape the loop response to meet the desired crossover frequency and phase margin specifications. In the analog domain, a compensator usually consists of an inverting op amp with a compensation network of capacitors and resistors around the negative feedback path. The combinations of capacitors and resistors determine the location of the poles and zeros of the compensator.

There are typically two types of compensators that are used for stabilizing power supplies. These are universally referred to as the Type II and Type III compensators. For voltage mode control, the Type III compensator is required. This is because Type II does not provide enough zeros to compensate for the phase lag due to the double pole of the voltage mode Forward plant transfer function. The circuit for a Type III compensator is shown in the following figure.

Figure 20. Type III compensator implemented in analog using op amp



The transfer function for this circuit can be derived in the same manner as that of the forward-type power stage. For brevity, the full transfer function has been included without derivation in Equation 7.

(7)

$$H_C\left(s\right) = \left(\frac{\omega_{CP0}}{s}\right)\frac{\left(\frac{s}{\omega_{CZ1}}+1\right)\left(\frac{s}{\omega_{CZ2}}+1\right)}{\left(\frac{s}{\omega_{CP1}}+1\right)\left(\frac{s}{\omega_{CP2}}+1\right)}$$

The transfer function in Equation 7 has two zeros, two poles and a pole at the origin. The locations of these zeros and poles are determined by the capacitors and resistors in the compensation network according to Equation 8 through Equation 12.

$$\omega_{CZ1} = \frac{1}{R_2 C_1} \quad (8)$$

$$\omega_{CZ2} = \frac{1}{C_2(R_1 + R_3)} \quad (9)$$

$$\omega_{CP0} = \frac{1}{R_1(C_1 + C_3)} \quad (10)$$

$$\omega_{CP1} = \frac{(C_1 + C_3)}{R_2 C_1 C_3} \quad (11)$$

$$\omega_{CP2} = \frac{1}{R_3 C_2} \quad (12)$$

In digital, this compensator will be implemented on the MCU and the translation from analog to digital will be discussed in the next chapter.

6.4 Compensator pole/zero placement

The locations of the poles and zeros of the compensator need to be selected such that, when the compensator is combined with the plant power stage, the open-loop frequency response meets the stability criteria of:

- Desired crossover frequency
- Desired phase margin at the crossover
- A shallow slope of -20dB/decade around the crossover

There are several different methods that can be applied to achieve this. In this application note, the straightforward and intuitive method of pole/zero cancellation will be applied. Consider the plant transfer function discussed earlier:

- The plant has a double pole due to the resonance between the output filter inductor and capacitor
- The plant has a single zero due to the ESR of the output filter capacitor
- The plant has a DC/low frequency gain

The effects of the plant double pole can be partially canceled out by placing the two compensator zeros at the natural frequency of the double pole. It is of course not possible to completely cancel out the complex conjugate double pole of the plant with two real zeros in the compensator, however, it will lessen the effect of the double pole and provide 180° of phase boost at around one decade above this frequency.

$$\{\omega_{CZ1}, \omega_{CZ2}\} = \omega_n = \frac{1}{\sqrt{LC}} \quad (13)$$

Now that the compensator's two zeros have been placed, the compensator's two poles and the pole at origin still remain. One of the compensator's poles can be used to cancel out the parasitic ESR zero of the power stage. This will effectively eliminate the gain and phase contribution from the parasitic ESR zero. However, this is reliant on the accurate determination of the actual ESR value for the capacitor or capacitors used.

$$\omega_{CP1} = \omega_{ESR} = \frac{1}{C \,.\, R_{ESR}} \quad (14)$$

The second compensator pole can be placed at half the switching frequency and in doing so the high-frequency gain will be attenuated while not having a significant impact on the phase at around the crossover frequency.

$$\omega_{CP2} = \pi F_S \quad (15)$$

The final term of the compensator to calculate is the pole at the origin. As the name implies, this compensator pole is at the origin and therefore setting the position of the pole at the origin is, in fact, changing the gain and not moving the pole. This can be used to adjust the crossover frequency of the loop. Adding the pole at the origin to the compensator will introduce the constant -20dB/decade gain roll-off, which is desirable around the crossover frequency. The pole at the origin will also provide a very high low-frequency gain, which will remove steady-state errors and reject and low-frequency perturbations of the control loop.

The gain contributions from all of the other poles and zeros in the system must be taken into account to determine the exact gain required by the compensator to achieve the desired crossover frequency. The equality given in Equation 16 must be solved for the compensator pole at the origin:

$$20log_{10}|H_P(j\omega)| + 20log_{10}|H_C(j\omega)| = 0dB \quad (16)$$

Given that the plant transfer function and compensator transfer functions are both known, this can be solved for the unknown term ω_{CP0} . Evaluating this equation will determine the amount of gaigain, whicheds to be added by the compensator in tohieve the specified crossover frequency.

The method discussed so far gives the user control over the crossover frequency but not the phase margin. Typically, it would result in a large phase margin, however, in a digital system the phase loss due to the digitization delays may result in a significant amount of phase margin erosion. Therefore, it is possible to derive an equation that analytically calculates the precise location of one of the compensator zeros to achieve the specified phase margin. This is achieved by solving the equality shown in Equation 17 for the compensator zero ω_{CZ1} .

$$\angle(H_P(j\omega) \,.\, H_C(j\omega)) = -\pi + \theta_M \quad (17)$$

Equation 17 states that the phase of the plant combined with the compensator must be equal to -180° plus the desired phase margin at the crossover frequency.

This equation requires the calculation of the inverse tangent of complex numbers necessitating the use of a mathematical package to evaluate. For this application note, the software tool Biricha ST WDS will be used to perform the calculations and is available for download free of charge from the Biricha website: www.biricha.com/st-wds. This tool will be discussed in detail through means of a complete design example later in this application note.

7 Discrete-time controller

7.1 Bilinear transform

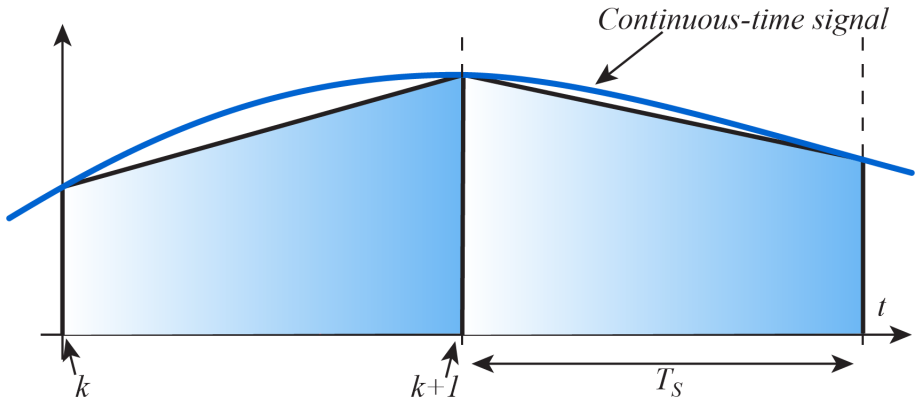
With the poles and zeros of the compensator placed in the continuous-time domain, the s-domain, they must be converted into the discrete-time domain to implement the controller on the MCU. To implement the discrete-time controller, the continuous-time Type III compensator, which was discussed in the previous section, will be converted into its discrete-time equivalent.

There is a direct mapping between the continuous-time domain, the s-domain, and the discrete-time domain, the z-domain. The relationship is shown in Equation 18.

$$z = e^{sT} \tag{18}$$

There are several different methods that can be used to covert an s-domain transfer function into the discrete-time z-domain. A commonly used method is the bilinear transform (also called the Tustin or trapezoidal transform). This transform approximates the continuous-time signal based on a trapezoid from k to k+1. An example of this is shown in the fiure below.

Figure 21. Continuous time signal sampled in discrete time using a trapezoidal approximation

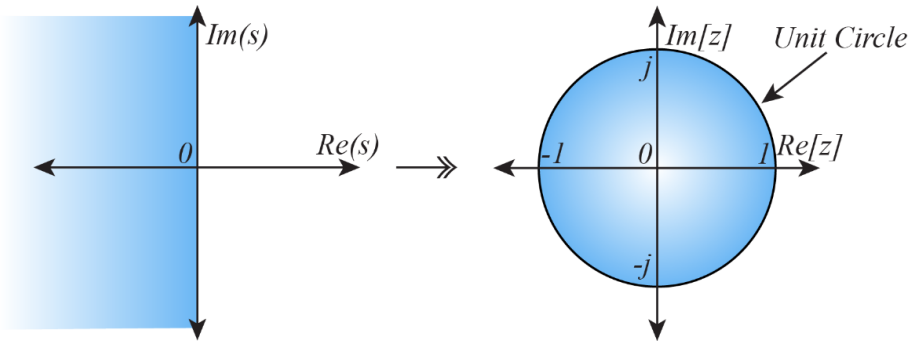


This trapezoidal approximation gives rise to the transform given in Equation 19.

$$s \leftarrow \frac{2}{T_S}\frac{1 - z^{-1}}{1 + z^{-1}} \tag{19}$$

This transform has the advantage that a system with stable (i.e. left-hand plane) poles and zeros will transform into a system with stable z-domain poles and zeros. The stable region in the z-domain is the area on or inside the unit circle. Therefore, the mapping is shown in the figure below.

Figure 22. Trapezoidal approximation mapping from s to z-domain



There will inevitably be some distortion with the mapping given that the entirety of the left-hand s-plane is mapped to the unit circle in the z-domain. However, this distortion is only significant as the frequency approaches the sampling frequency. For this power supply application, most of the compensator poles and zeros are significantly below the sampling frequency. Furthermore, the crossover frequency has been specified as between 1/10th to 1/20th of the sampling frequency and there will be no significant distortion from the mapping around this frequency.

However, this transform does not include the effects of the pure time delays in the discrete-time system and there will be an additional phase roll-off that is not considered here. This will manifest itself as a phase erosion at the crossover frequency and this must be taken into account when the compensator is being designed.

7.2 3p3z controller

The bilinear transform is applied to the s-domain Type III compensator by replacing every instant of ‘s’ in the s-domain transfer function with the bilinear mapping. The initial substitution is given in Equation 20 and the simplified result is given in Equation 21.

$$H_C\left[\right]z = \left(\frac{\omega_{CP0}}{\frac{2}{T_S}\frac{1-z^{-1}}{1+z^{-1}}}\right)\frac{\left(\frac{\frac{2}{T_S}\frac{1-z^{-1}}{1+z^{-1}}}{\omega_{CZ1}}+1\right)\left(\frac{\frac{2}{T_S}\frac{1-z^{-1}}{1+z^{-1}}}{\omega_{CZ2}}+1\right)}{\left(\frac{\frac{2}{T_S}\frac{1-z^{-1}}{1+z^{-1}}}{\omega_{CP1}}+1\right)\left(\frac{\frac{2}{T_S}\frac{1-z^{-1}}{1+z^{-1}}}{\omega_{CP2}}+1\right)} \tag{20}$$

$$H_C[z] = \frac{B_3\ z^{-3} + B_2\ z^{-2} + B_1\ z^{-1} + B_0}{-A_3\ z^{-3} - A_2\ z^{-2} - A_1\ z^{-1} + 1} \tag{21}$$

In the discrete-time z-domain, the transfer function now has three z-domain poles and three z-domain zeros. Therefore, this controller is now referred to as a three-pole three-zero controller or 3p3z for short.

The numerator of the transfer function has been grouped into like terms consisting of ‘B’ coefficients and likewise, the denominator has been grouped into like terms consisting of ‘A’ coefficients. These coefficients are given in Equation 22 to Equation 28.

$$B_3 = \frac{T_S \times \omega_{CP0} \times \omega_{CP1} \times \omega_{CP2} \times (-2 + T_S \times \omega_{CZ1}) \times (-2 + T_S \times \omega_{CZ2})}{(2 \times (2 + T_S \times \omega_{CP1}) \times (2 + T_S \times \omega_{CP2}) \times \omega_{CZ1} \times \omega_{CZ2})} \tag{22}$$

$$B_2 = \frac{T_S \times \omega_{CP0} \times \omega_{CP1} \times \omega_{CP2} \times \left(-4 + 3 \times {T_S}^2 \times \omega_{CZ1} \times \omega_{CZ2} - 2 \times T_S \times (\omega_{CZ1} + \omega_{CZ2})\right)}{(2 \times (2 + T_S \times \omega_{CP1}) \times (2 + T_S \times \omega_{CP2}) \times \omega_{CZ1} \times \omega_{CZ2})} \tag{23}$$

$$B_1 = \frac{T_S \times \omega_{CP0} \times \omega_{CP1} \times \omega_{CP2} \times \left(-4 + 3 \times {T_S}^2 \times \omega_{CZ1} \times \omega_{CZ2} + 2 \times T_S \times (\omega_{CZ1} + \omega_{CZ2})\right)}{(2 \times (2 + T_S \times \omega_{CP1}) \times (2 + T_S \times \omega_{CP2}) \times \omega_{CZ1} \times \omega_{CZ2})} \tag{24}$$

(25)

$$A_3 = \frac{(-2 + T_S \times \omega_{CP1}) \times (-2 + T_S \times \omega_{CP2})}{(2 + T_S \times \omega_{CP1}) \times (2 + T_S \times \omega_{CP2})} \tag{26}$$

$$A_2 = -\frac{\left(12 - {T_S}^2 \times \omega_{CP1} \times \omega_{CP2} - 2 \times T_S \times (\omega_{CP1} + \omega_{CP2})\right)}{(2 + T_S \times \omega_{CP1}) \times (2 + T_S \times \omega_{CP2})} \tag{27}$$

$$A_1 = -\frac{\left(-12 + {T_S}^2 \times \omega_{CP1} \times \omega_{CP2} - 2 \times T_S \times (\omega_{CP1} + \omega_{CP2})\right)}{(2 + T_S \times \omega_{CP1}) \times (2 + T_S \times \omega_{CP2})} \quad (28)$$

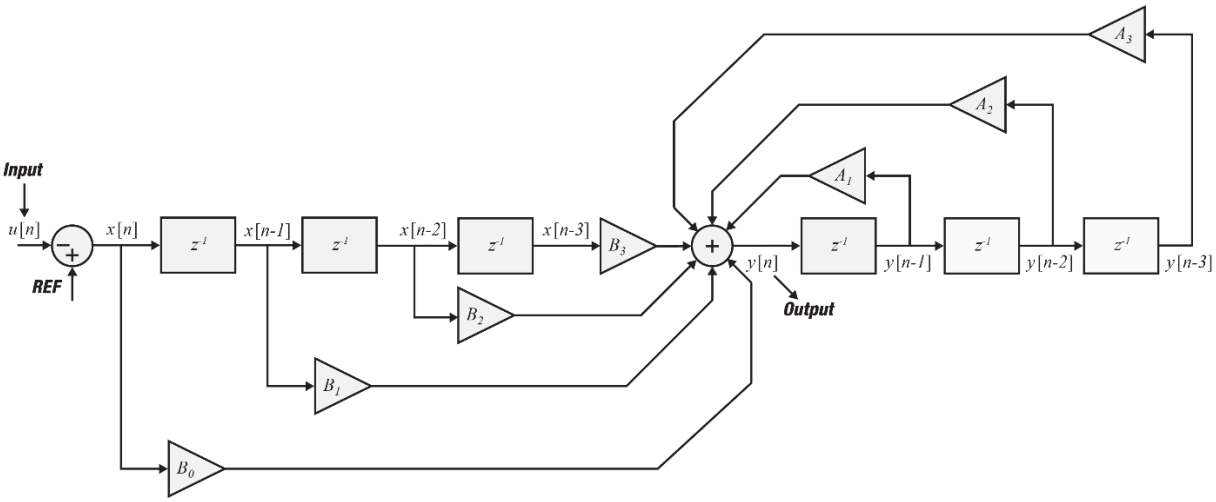
There is no need to calculate these controller coefficients by hand as the software tool Biricha ST WDS available from www.biricha.com/st-wds will perform these calculations for you.

Finally, now that the controller is in the discrete-time 3p3z form, it can be converted into a linear differential equation that can be easily implemented on the MCU. This takes advantage of the shifting property of the z-domain transfer function and converts from z-domain to discrete sample in Equation 29.

$$y[n] = A_1 y[n-1] + A_2 y[n-2] + A_3 y[n-3] + B_0 x[n] + B_1 x[n-1] + B_2 x[n-2] + B_3 x[n-3] \quad (29)$$

Where y[n] is the output for the current sampling interval. The structure of this controller is depicted in the following figure.

Figure 23. 3p3z controller structure



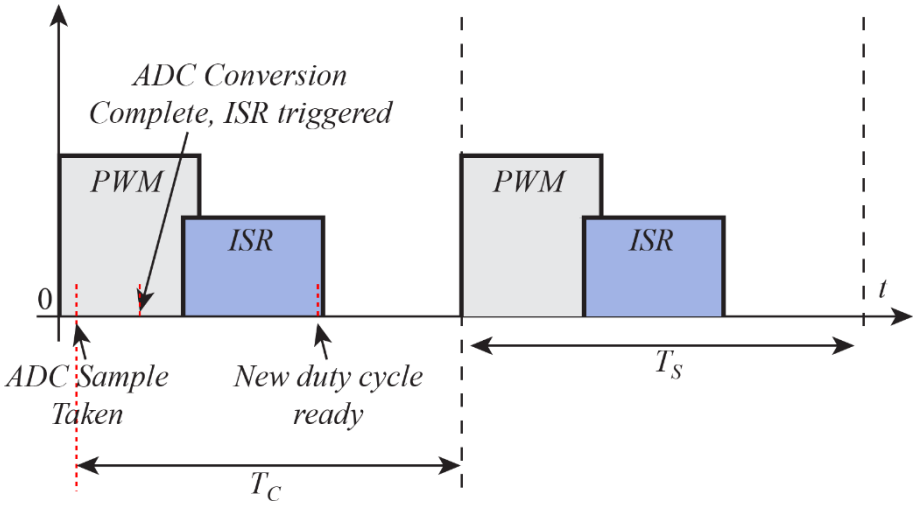
For this voltage mode converter, the current output of the controller would be the new value of phase shift, which will be used in the following switching period. Therefore, there is now an equation that can implement the analytically designed controller and will be calculated by the MCU at every sampling interval when there is a new sample available.

7.3 Pure time delays

In this discrete-time digital system, there are additional time delays that are not present in the equivalent analog continuous-time system. A pure time delay in the discrete-time system will result in a phase delay that is proportional to the frequency and time delay.

There are two sources of time delay in the digital system. The first is the time from which the output voltage sample was taken, to the time at which it was used. This is referred to as the calculation delay. In effect the older the sample the more phase delay will be associated with the sample. For example, a convenient time to trigger the ADC and sample the output voltage may be at the beginning of the switching period. In this case, the output voltage will be sampled, converted, and used in the controller to provide the new value of the duty cycle. This sampling and calculation time may take several hundred nanoseconds and the new value of the duty cycle will be ready to use towards the end of that switching period. This situation is described in the following figure.

Figure 24. **Sources of delay within the discrete-time system**



However, as the new duty cycle will not be used until the following switching cycle, the total time delay for this calculation time is considered to be one complete switching period. Of course, if you are able to delay the trigger for the ADC until later in the switching period then it is possible to reduce this time delay.

The second contribution to the time delay is that of the zero-order-hold introduced by this sampled data system. The ADC is triggered once per switching cycle, this sampled data is used to calculate the new value of duty cycle and that duty cycle is held constant for the remainder of the next switching period. Therefore, there is one zero-order-hold in this system. The frequency response of a ZOH is given in Equation 30.

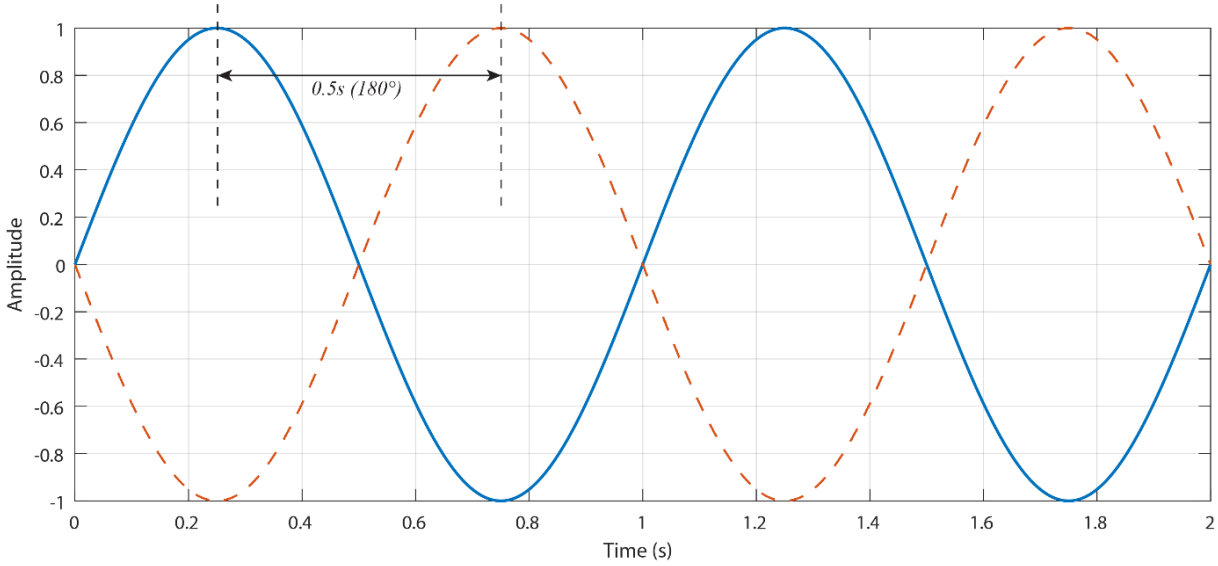
$$F_{ZOH}(j\omega) = \frac{1 - e^{-j\omega T_S}}{j\omega} \tag{30}$$

This can be shown to be a complex number expressed in polar form, and therefore the phase angle is given in Equation 31.

$$\angle F_{ZOH}(j\omega) = -\omega\frac{T_S}{2} \tag{31}$$

To understand how this phase angle can relate to a time delay, consider as an example the 1Hz sine wave shown in Figure 23. If this sine wave were delayed by 0.5 seconds, the result would be the sine wave shown as a dashed line in Figure 25.

Figure 25. **Time delay relationship to phase delay**



It is clear from this that the time-delayed sine wave now has a phase delay of 180°. Therefore, the equation to calculate the phase delay of a sine wave given the pure time delay T_D is given in Equation 32.

$$p.d. = -2\pi f T_D \tag{32}$$

This indicates that there will be some phase delay across all frequencies, however, when $T_D \ll 1/f$ the phase delay will be negligible. This will be true for very low frequencies assuming that the phase delays in the digital system can be kept to a minimum.

The frequency at which this phase delay could become a concern would be the crossover frequency of the open-loop system as this is where the phase margin is defined. Earlier in this application note, it was specified that the phase margin has a minimum value of 45° to ensure a transient response that is not oscillatory in the time domain. Therefore, the amount of phase loss at the crossover frequency can be calculated given the known time delays in the digital system.

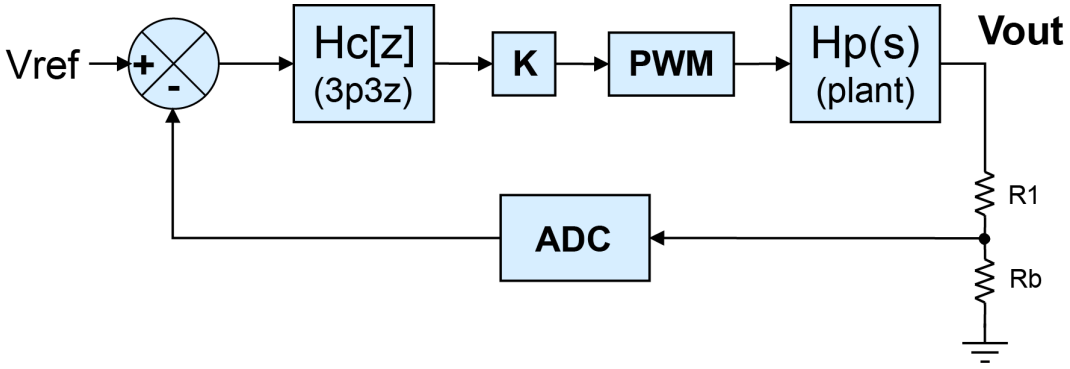
$$p.e. = -2\pi f_X T_D \tag{33}$$

The expected phase erosion at the crossover frequency can be added to the desired phase margin such that this phase loss is compensated for at design time. This can be achieved by adding the expected phase erosion to the desired phase margin. This will adjust the location of the compensator zero to add the require phase boost and compensate for this phase loss such that the resulting overall phase margin meets the specification.

7.4 Digital gains

The output of the 3p3z controller in Figure 26 is scaled by a factor, K. This scaling factor is responsible for negating all of the additional gains introduced by the digital system. The compensator poles and zeros have been analytically calculated to achieve the specified crossover frequency and phase margin. If the additional gains within the digital system are not accounted for then the overall loop gain, and thus phase margin, will be incorrect.

Figure 26. **Additional gains within the digital system**



Consider the block diagram of the digital control loop shown in Figure 26. The output voltage, Vout, will need to be scaled down to a voltage suitable for sampling by the ADC onboard the MCU. This is the purpose of the potential divider formed by R1 and Rb. This will also determine the setpoint value that the controller must regulate to. The gain of the pre-ADC scaling potential divider can be calculated in Equation 34.

$$G_{PD} = \frac{R_b}{R_1 + R_b} \tag{34}$$

Then the ADC on the MCU will convert the voltage, which is between 0V and 3.3 V, and provide a 12-bit output, a number between 0 and 4095. Therefore, the gain of the ADC can be calculated using Equation 35.

$$G_{ADC} = \frac{2^{12} - 1}{3.3V} \tag{35}$$

The output of the controller will be used to update the duty cycle register and therefore this must be in the correct scaling The PWM is implemented using the HRTIM module onboard the MCU and the timer compare register is used to control the effective duty cycle. The HRTIM module will output a duty cycle of 100% when the timer compare register is set to the period value. Therefore, the gain of the PWM module can be calculated using Equation 36. This is similar to the RC ramp and analog comparator gain seen earlier in the analog voltage-mode example.

$$G_{PWM} = \frac{100\%}{period} \tag{36}$$

In order to achieve the correct loop gain, the controller must negate these additional gains. That is achieved using the scaling factor K, which can be calculated in Equation 37.

$$K = \frac{1}{G_{PD} G_{ADC} G_{PWM}} \tag{37}$$

Finally, the ADC output is compared with the digital reference set point. This digital reference must be in the same scaling as the ADC output and take into account the divider on the input of the ADC. Therefore, the reference can be calculated using Equation 38.

$$REF = V_{OUT} G_{PD} G_{ADC} \tag{38}$$

8 Software implementation

8.1 Targeted application

The following configuration sets up the STM32G474 MCU to operate the PSFB converter using the onboard peripherals, including the ADC, DMA, and HRTIM. The example software project to accompany this application note is called “STEVAL-ISA172V3-secondary” and is available from www.biricha.com/steval-isa172V3.

8.2 Peripheral configuration using STM32CubeMX

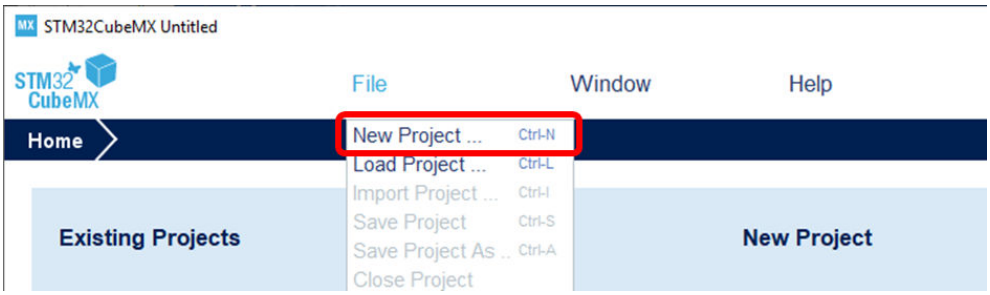
The following section contains step-by-step instructions for recreating the STM32CubeMX project for the PSFB converter under voltage mode control on the STEVAL-ISA172V3 kit. This complete project can be downloaded by following the links provided within this application note appendix. However, the full configuration is included here for completeness.

Step 1. Open STM32CubeMX by clicking on the [**MX**] icon.

We now create a new STM32CubeMX "Project". This project configures the MCU peripherals and also generates an IAR project. IAR is used to compile and link the code as well as for programming and debugging the MCU.

Step 2. Within the STM32CubeMX window click on [**File**]>[**New Project**].

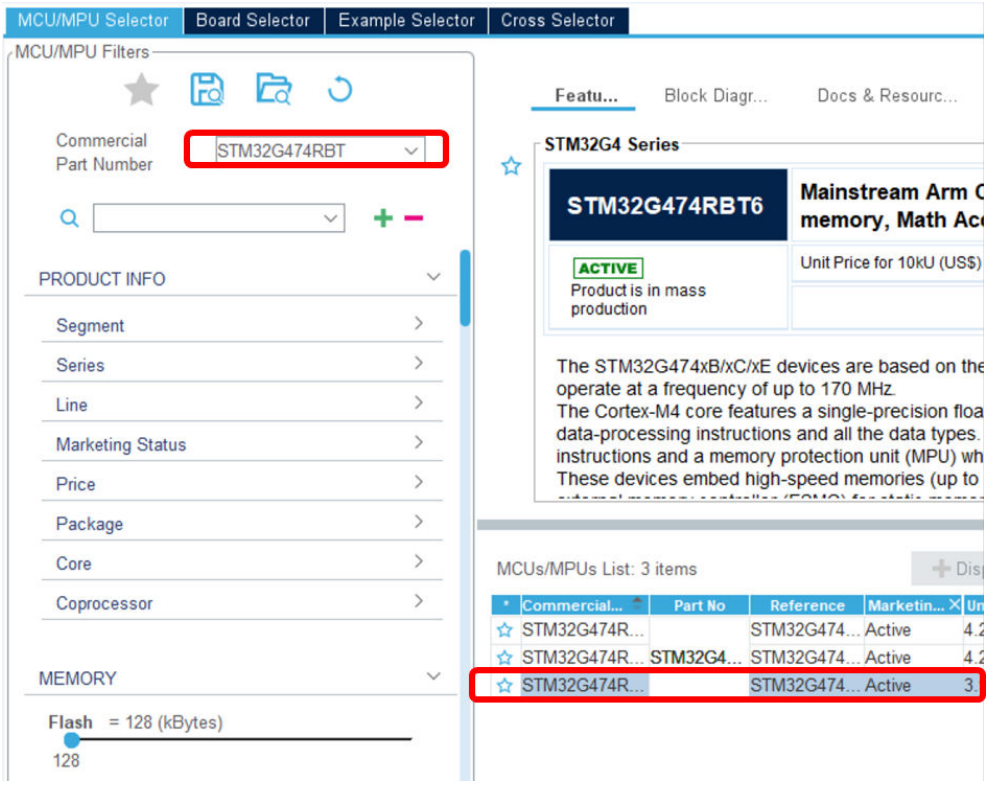
Figure 27. STM32CubeMX new project selection



The new project device selector window now opens.

Step 3. Within this window, click on the [**MCU/MPU selector**] tab and filter the MCUs by entering *STM32G474RBT* in the [**Commercial Part Number box**].

Figure 28. STM32CubeMX MCU/MPU selection

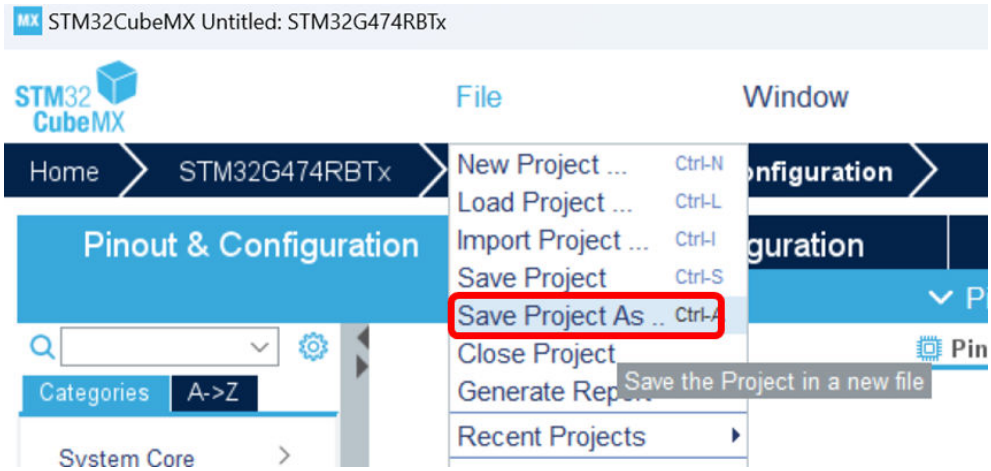


This should filter down the available MCUs on the right-hand side of this window to include the STM32G464RBT6 option.

Step 4. Double-click on this MCU within the table.

Step 5. Before making any changes to the project, save the project by going to [**File**], [**Save project As..**].

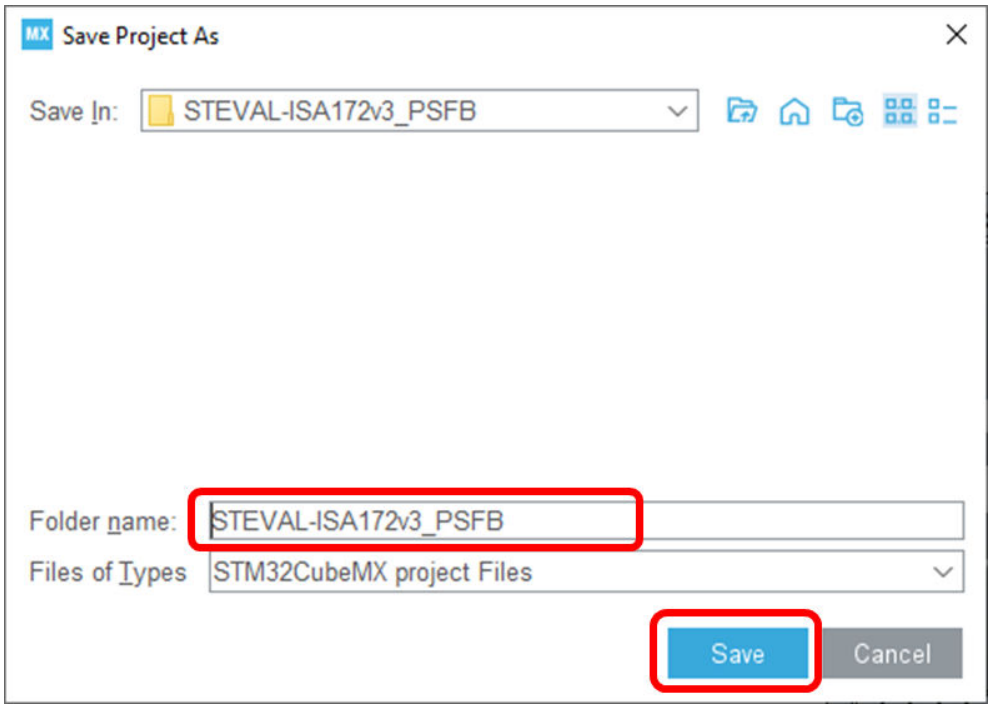
Figure 29. STM32CubeMX MCU/MPU save project



The name which you give to the folder, *Folder name*, is also the name of the project. If this folder does not exist it is created for you.

Step 6. Click [**Save**] when done.

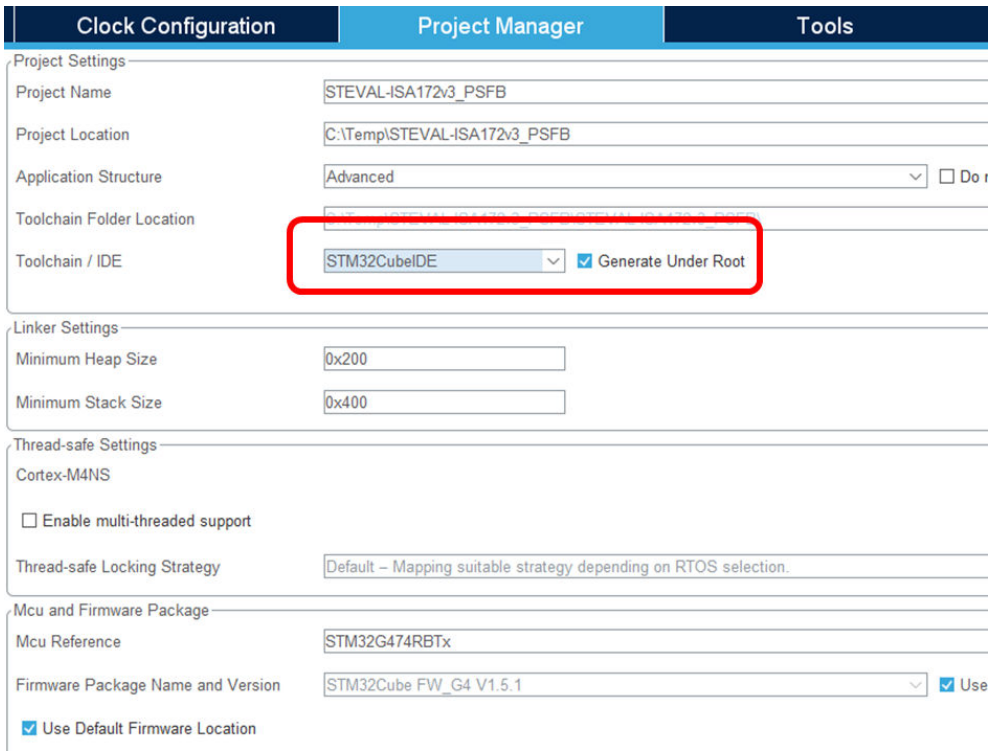
Figure 30. STM32CubeMX MCU/MPU folder name



Step 7. On the right-hand side of the main window, click [**Project Manager**] and select your preferred toolchain and version from the dropdown list as shown below.

This application note is using the STM32CubeIDE tool.

Figure 31. STM32CubeMX project manager configuration



8.2.1 Clock Configuration

Before configuring the clock, the MCU pins for the high-speed external oscillator must be configured.

Step 1. Select the [**Pinout & Configuration**] tab along the top of the main STM32CubeMX window.

Step 2. Locate the pin *PF0-OSC_IN* and left click on it.
A menu will pop up with the configuration options for this pin.

Step 3. Select [**RCC_OSC_IN**] from the list.

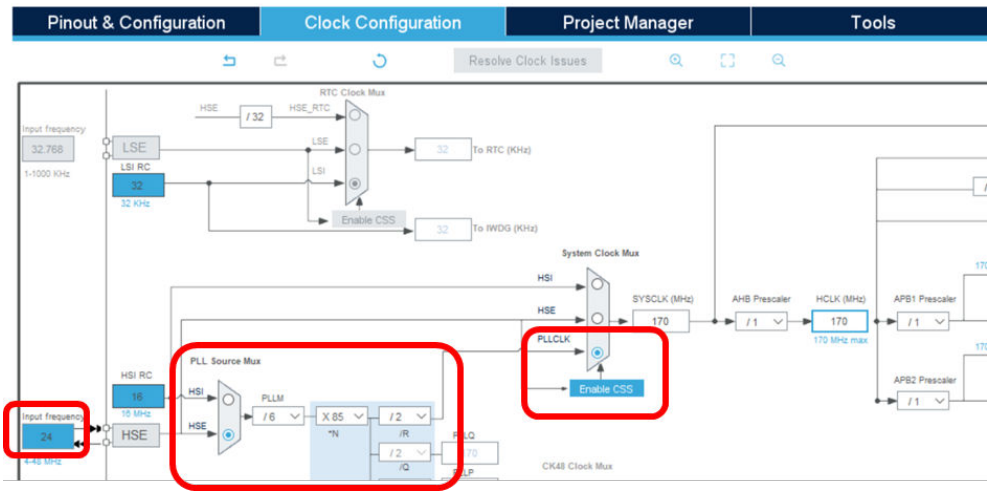
Step 4. Repeat this for *PF1-OSC_OUT* and select [**RCC_OSC_OUT**].
Both of these pins should now be highlighted green.

Step 5. Select the [**Clock Configuration**] tab along the top of the main STM32CubeMX window.

Step 6. Locate the following settings and change as described below.
These settings are highlighted in the image below.

- Input Frequency: 24 MHz
- PLL Source Mux: HSE
- PLLM: /6
- *N X85
- System Clock Mux: PLLCLK

Figure 32. STM32CubeMX clock configuration



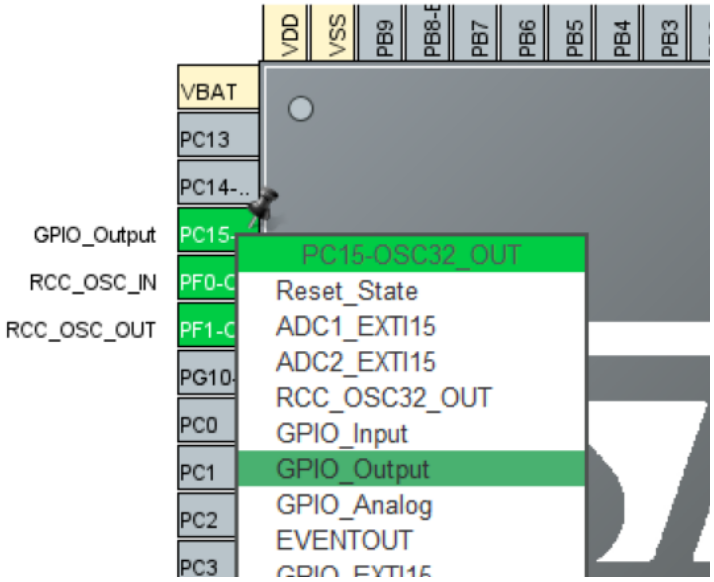
8.2.2 GPIO Peripheral configuration

For this application note, a digital pin will be configured to allow timing measurements to be performed.

Step 1. On the [**Pinout & Configuration**] tab, locate the pin PB9 towards the top left of the microcontroller.

Step 2. Left click on the pin PC15 and select [**GPIO_Output**] as shown below.

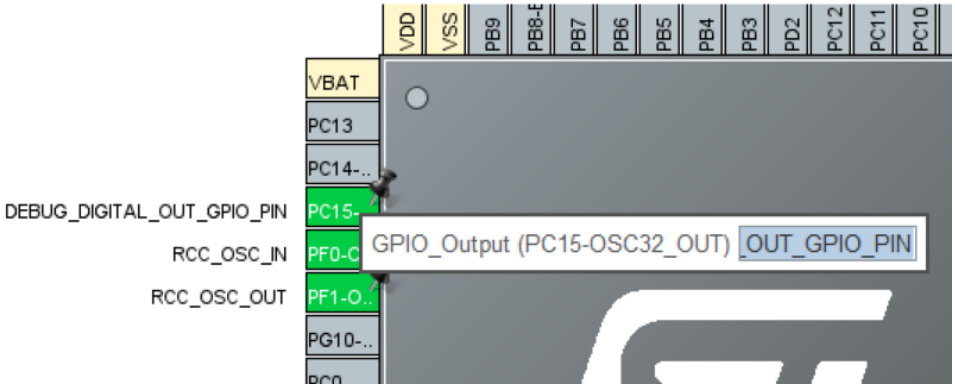
Figure 33. STM32CubeMX GPIO output pin section



Step 3. Then, right click on PC15 and select [**Enter User Label**].
This allows us to change the name of the pin so that it can be easily referenced within our code.

Step 4. This pin will be called [**DEBUG_DIGITAL_OUT_GPIO_PIN**]. Enter this in the popup box as per the image below.

Figure 34. STM32CubeMX GPIO output pin renaming



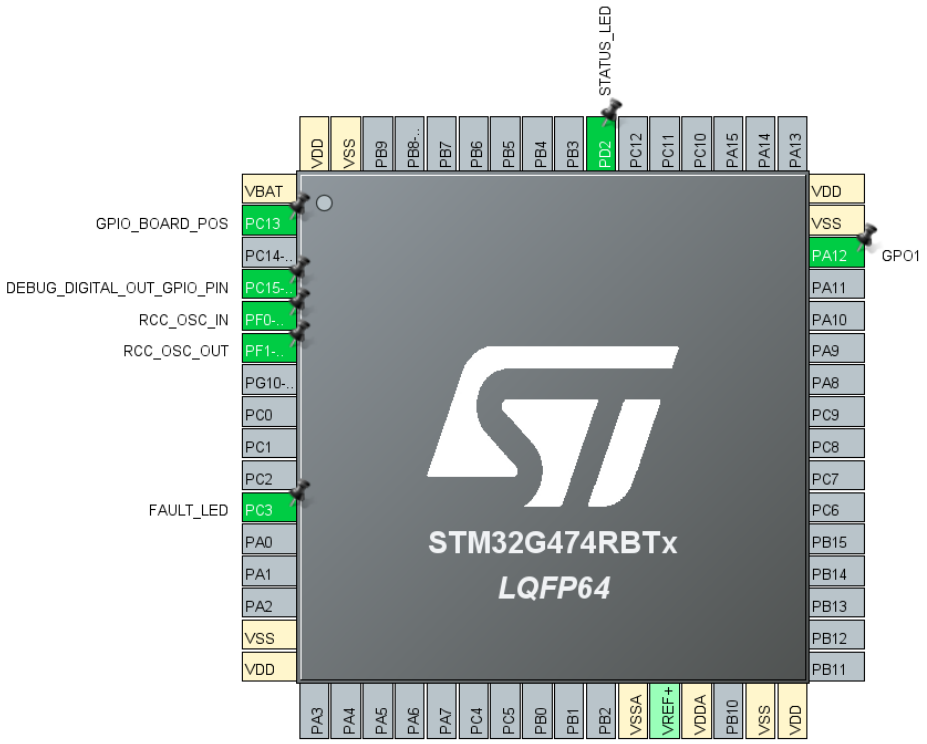
Step 5. Repeat this configuration process for the pins in the following table.
The peripheral pins will be configured later.

Table 6. STM32CubeMX remaining pin configurations

Pin	Input or output	Name
PA12	Output	GPO1
PC3	Output	FAULT_LED
PD2	Output	STATUS_LED
PC13	Input	GPIO_BOARD_POS

The pins should then be configured as per the image below.

Figure 35. STM32CubeMX complete GPIO pin configuration



The GPIO configuration is now complete.

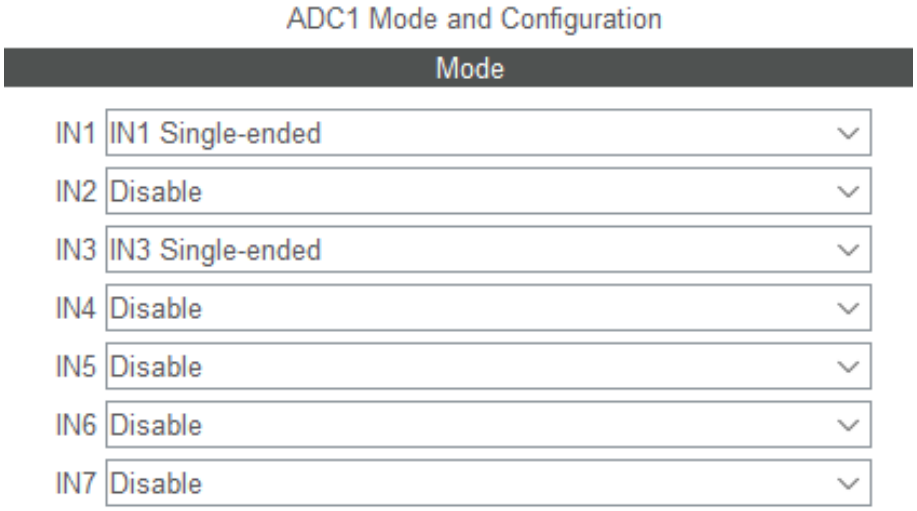
8.2.3 ADC peripheral configuration

The peripherals can now be configured.

Step 1. On the top menu, select [**Pinout & Configuration**] and then on the left-hand pane, expand the [**Analog**] list and select [**ADC1**].

Step 2. Set ADC inputs IN1 and IN3 as [**single-ended**] using the drop-down box as per the image below. These will be used to sample the input currents and voltages.

Figure 36. STM32CubeMX ADC1 peripheral configuration



Step 3. On the pin-out view on the right-hand side, rename these pins to reflect the signal that is being sampled as per the table below.

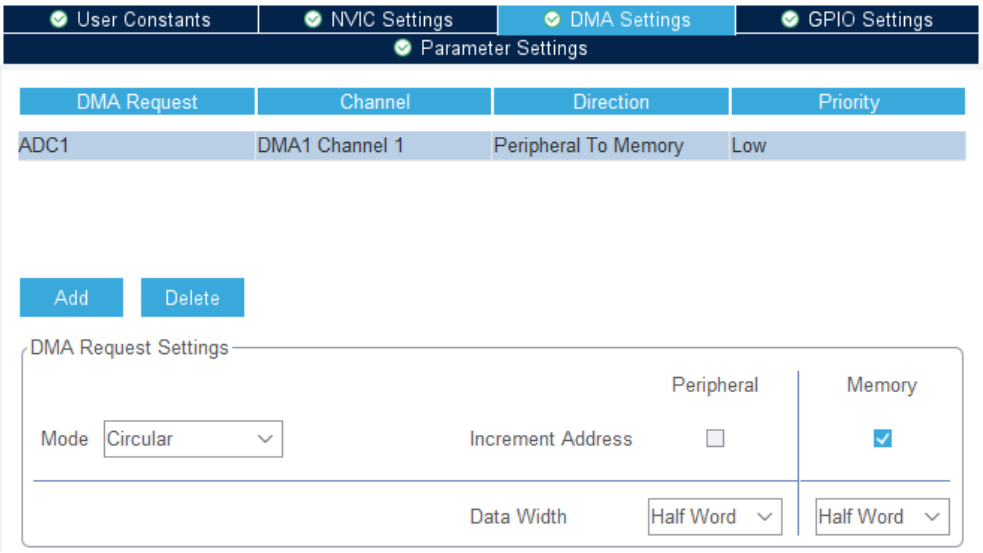
Table 7. STM32CubeMX ADC1 pin renaming

Pin	ADC Channel	Name
PA0	ADC1 IN1	ADCx_VOUT_CHANNEL_PIN
PA2	ADC1 IN3	ADCx_IOUT_CHANNEL_PIN

Step 4. In the ADC1 configuration pane, go to the [**DMA Settings**] and click the [**Add**] button to configure a DMA request as follows:

– Mode: Circular
– Increment address: Memory only
– Data width: Half word for both peripheral and memory

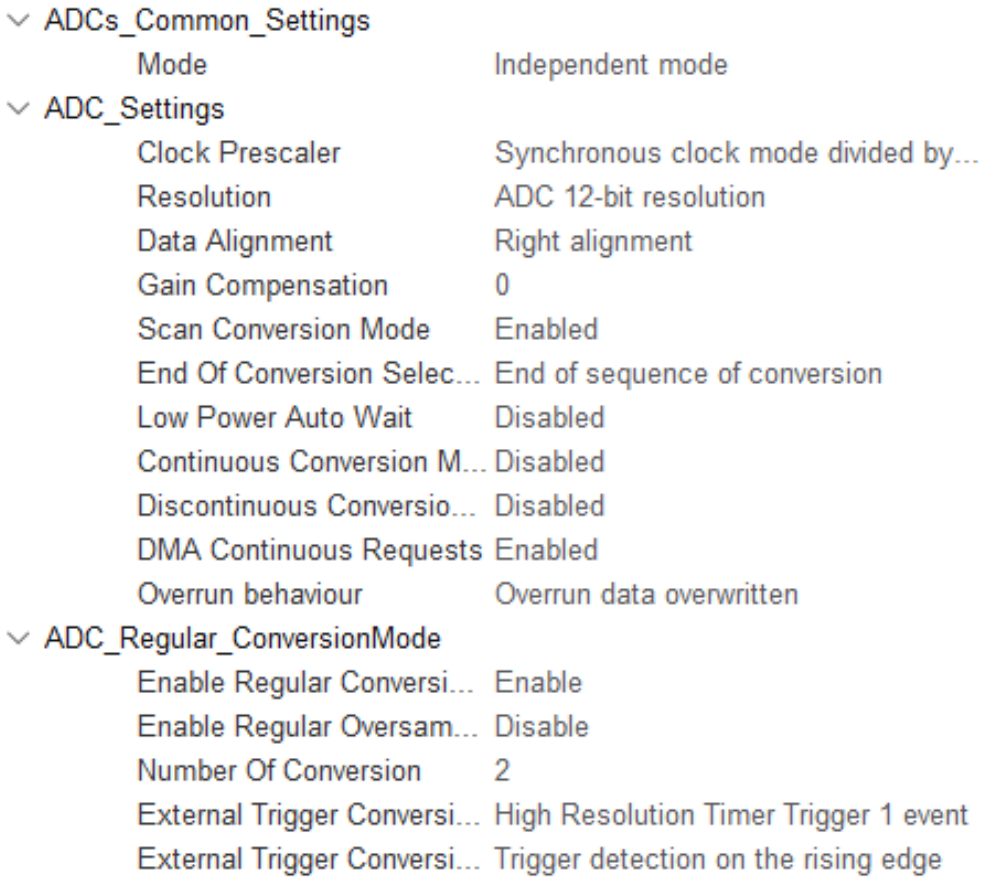
Figure 37. STM32CubeMX ADC1 DMA configuration



Step 5. Also, in the ADC1 configuration pane, click [**Parameter Settings**] and apply the following settings:

- Scan conversion mode: Enabled (need to add the number of conversions first)
- End of conversion selection: End of conversion sequence
- DMA continuous requests: Enabled (need to configure the DMA first)
- Overrun behavior: Overrun data overwritten
- Enable regular conversions: Enable
- Number of conversions: 2
- External trigger source: High-resolution timer Trigger 1 event
- External trigger conversion edge: Trigger detection on rising edge
- Enable injection conversions: Disabled

Figure 38. STM32CubeMX ADC1 settings



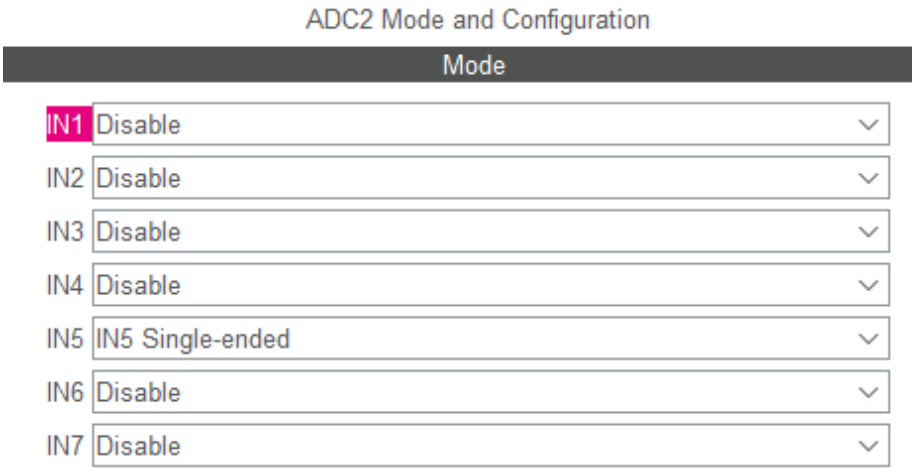
The conversion ranks are now entered. This is the order in which the ADC inputs will be sampled:

- Rank 1:
  - Channel: Channel 1
  - Sampling time: 12.5 cycles
  - Offset number: No offset
- Rank 2:
  - Channel: Channel 3
  - Sampling time: 12.5 cycles
  - Offset number: No offset

This completes the configuration of ADC1.

Step 6. Next, select [**ADC2**] from the left-hand pane and enable IN5 as *single-ended* using the drop-down box as per the image below.

Figure 39. STM32CubeMX ADC2 peripheral configuration



Step 7. On the pinout view on the right-hand side, rename this ADC pin to reflect the signal that is being sampled as per the table below.

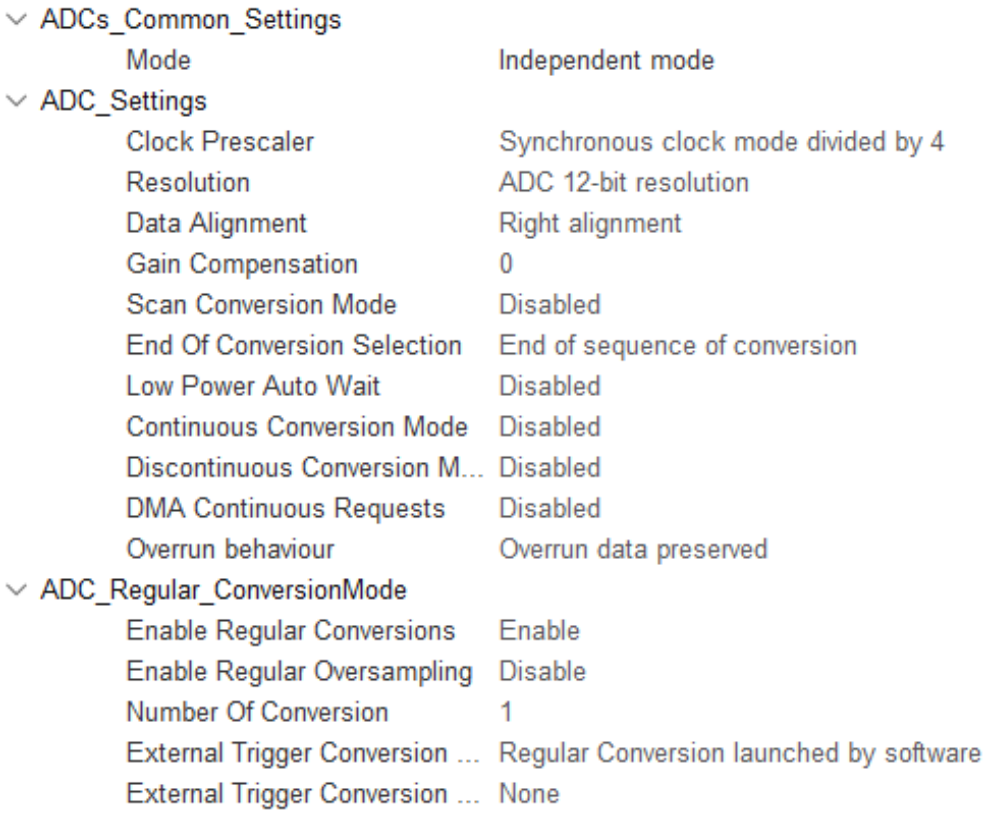
Table 8. STM32CubeMX ADC2 pin renaming

Pin	ADC Channel	Name
PC4	ADC2 IN5	ADCy_TEMP_CHANNEL1

Step 8. In the ADC2 configuration pane, apply the following settings:

- Scan conversion mode: Enabled (need to add the number of conversions first)
- End of conversion selection: End of sequence of conversion
- Overrun behavior: Overrun data overwritten
- Enable regular conversions: Enabled
- Number of conversions: 1
- External trigger source: Regular conversion launched by software
- External trigger conversion edge: None
- Enable injection conversions: Disabled

Figure 40. STM32CubeMX ADC2 settings



The conversion ranks are now entered. This is the order in which the ADC inputs will be sampled:

- Rank 1:
- Channel: Channel 5
- Sampling time: 2.5 cycles
- Offset number: No offset

The ADC2 configuration is now complete.

8.2.4 Comparator and DAC configuration

The remaining analog peripherals can now be configured.

Step 1. First, from the left-hand side analog peripheral list, select [**DAC1**].

Step 2. Enable this by configuring the [**OUT2 mode**] to *OUT2 Connected to on chip-peripherals only*.
This will route the output of the DAC to the comparator module which we will use to detect on overcurrent condition of the primary side MOSFETs. There are no settings that require change from default in the DAC configuration.

Step 3. Repeat this for [**DAC3**] on the left hand-side. This time, select *OUT1 Connected to on chip-peripherals only*.

The DAC1 and DAC3 configurations should now match the following images.

Figure 41. STM32CubeMX DAC1 peripheral configuration

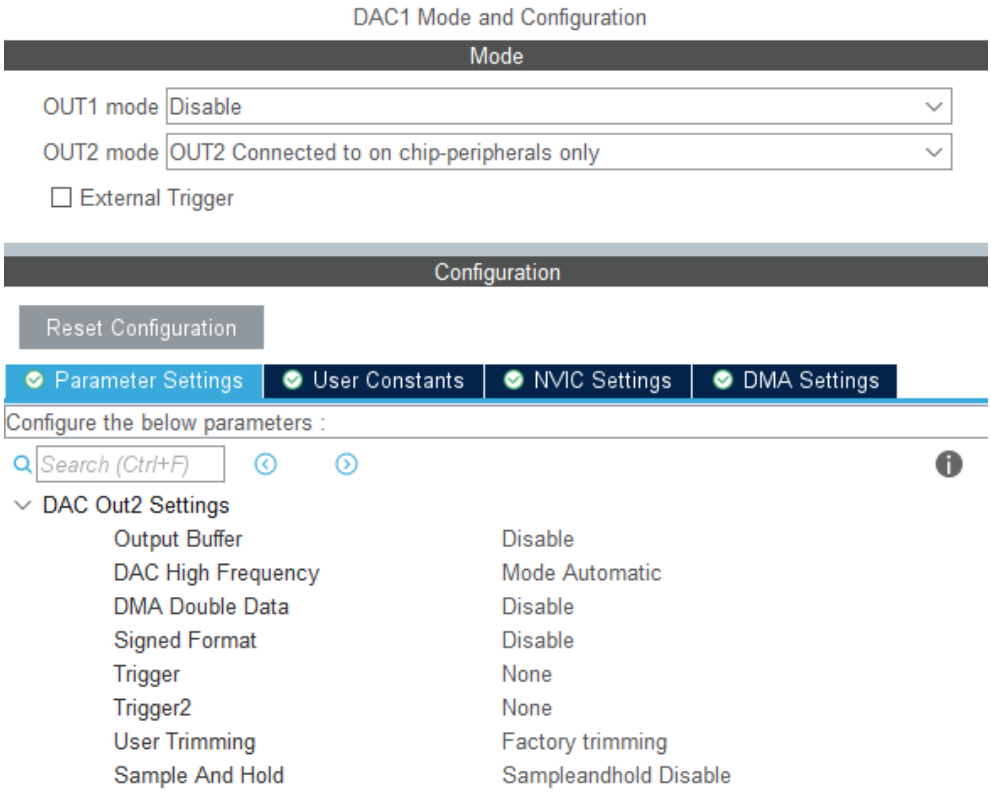
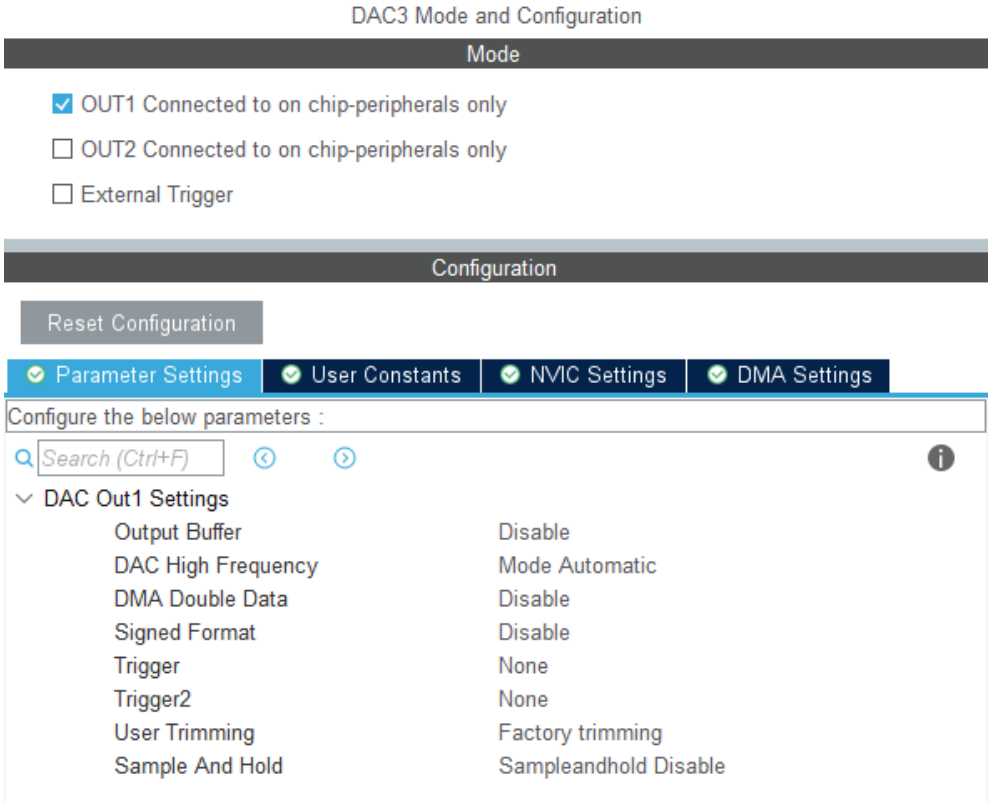


Figure 42. **STM32CubeMX DAC3 peripheral configuration**



Step 4. Now, the comparators can be configured. Enable comparator module 2, COMP2, by ticking the [**Input [+]**] box and select [**Input [-]**] as *DAC1 OUT2*.

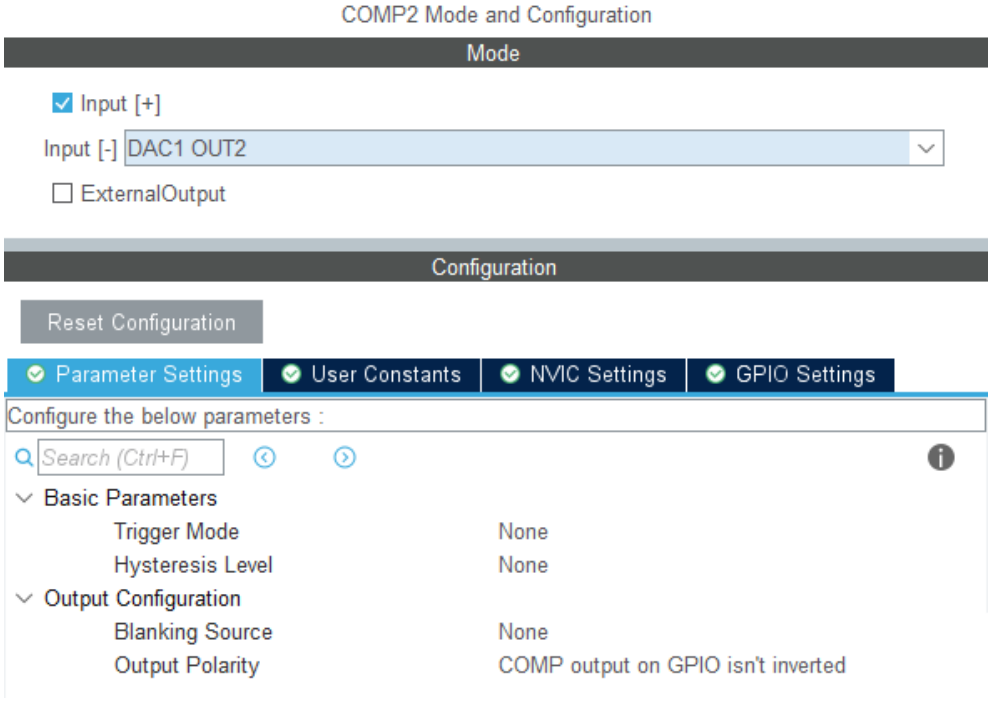
Step 5. The COMP2 noninverting input pin can be renamed on the pinout configuration diagram to match the signal that is being routed to it. In this case, the current transducer for the full bridge FETs.

Table 9. STM32CubeMX COMP2 pin renaming

Pin	Comp input	Name
PA3	COMP2 input [+]	IIN_COMP2_INP

There are no options that require changing form default under the configuration options. The configuration should now match the following image.

Figure 43. STM32CubeMX COMP3 peripheral configuration



Step 6. Repeat this process for COMP3 by ticking the [**Input [+]**] box and select [**Input [-]**] as *DAC3 OUT1*.

Step 7. Under the [**Parameter Settings**] of the configuration pane, change the [**Output Polarity**] to *COMP output on GPIO is inverted*.

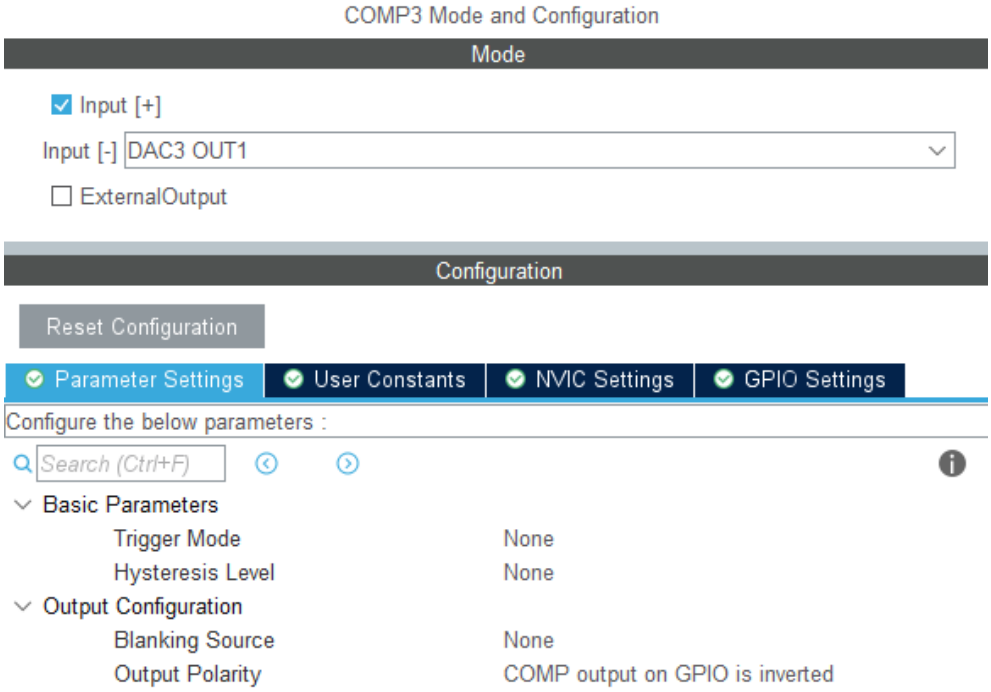
Step 8. The pin can also be renamed for the noninverting input accordingly.

Table 10. STM32CubeMX COMP3 pin renaming

Pin	Comp input	Name
PC1	COMP3 input [+]	IIN_COMP3_INP

The configuration for COMP3 should now look as follows:

Figure 44. STM32CubeMX COMP3 peripheral configuration



8.2.5 HRTIM configuration

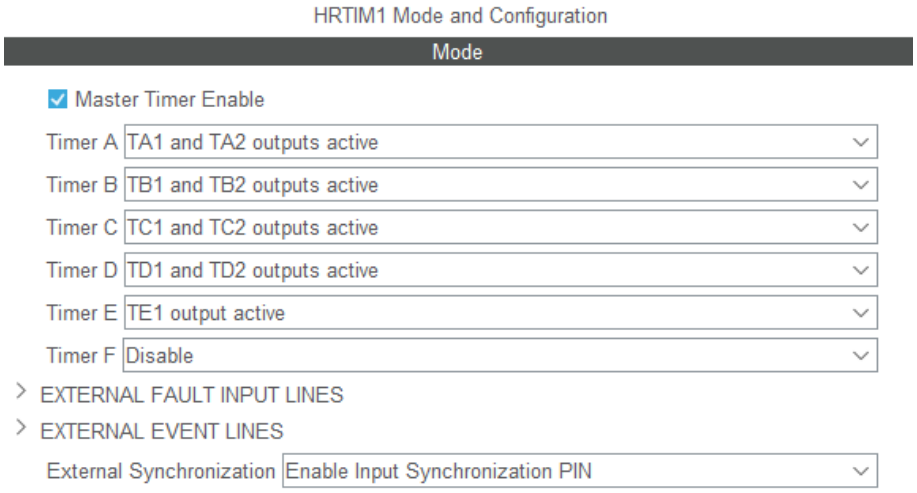
Next, the hi-resolution timer module will be configured to generate the PWM.

Step 1. On the left-hand side peripherals pane, expand the [**Timers**] category and click on [**HRTIM1**].

The PSFB converter requires multiple timers to be configured for the input bridge FETs, synchronous rectification FETs and the active clamp FET.

Step 2. On the [**MRTIM1 mode and Configuration**] window, enable the [**Master Timer**] and [**Timers A through D**] with *Tx1* and Tx2 outputs active, and [**Timer E**] with *TE1* output active. The window should now look like the following:

Figure 45. STM32CubeMX HRTIM1 peripheral configuration



Step 3. On the pinout view, rename the HRTIM1 pins to reflect their usage:

Table 11. STM32CubeMX HRTIM1 pin renaming

Pin	HRTIM1 output	Name
PA8	HRTIM1_CHA1	PWM_SR3_GPIO_PIN
PA9	HRTIM1_CHA2	PWM_SR4_GPIO_PIN
PA10	HRTIM1_CHB1	PWM_HS2_GPIO_PIN
PA11	HRTIM1_CHB2	PWM_LS2_GPIO_PIN
PB12	HRTIM1_CHC1	PWM_HS1_GPIO_PIN
PB13	HRTIM1_CHC2	PWM_LS1_GPIO_PIN
PB14	HRTIM1_CHD1	PWM_SR1_GPIO_PIN
PB15	HRTIM1_CHD2	PWM_SR2_GPIO_PIN
PC8	HRTIM1_CHE1	PWM_SR_CLAMP1

Step 4. First, the [**Master Timer**] is configured. Under the configuration pane, click on the [**Master Timer**] configuration tab.

Step 5. The time base settings must be configured initially. Set the period value to *54400* – the tool should automatically switch from hex to decimal when you press [**Enter**].

The resulting PWM period should now be calculated as 100000Hz.

Step 6. Also under time base settings, set the [**Repetition Counter**] to *HRTIM_REP_RATE,* which will be defined in the header files.

Step 7. In order for this to be accepted by the tool, click the cog icon on the right-hand side of the text box and select [**No check**].

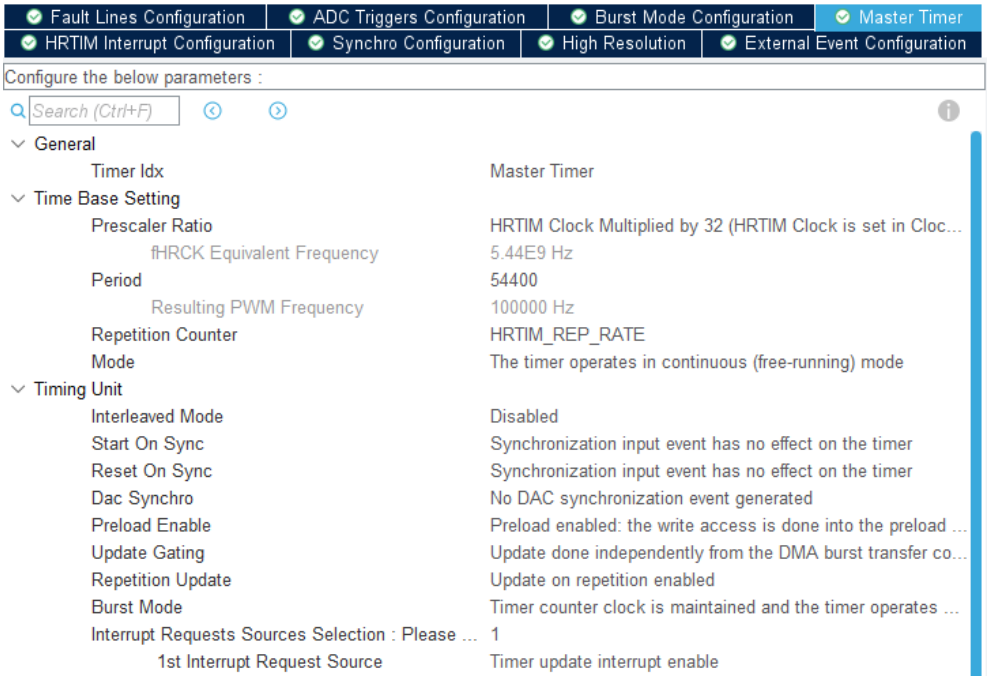
Step 8. Under the [**Timing Unit**] settings, set [**Preload Enable**] to *Preload enabled*.

Step 9. Set [**Repetition Update**] to *Update on repetition enabled*.

Step 10. Finally, under [**Interrupt Requests Sources selection**] set this to *1* and add the [**1st Interrupt Request Source**] as *Timer update interrupt enable*.

The master timer settings should then be as follows:

Figure 46. STM32CubeMX Master Timer configuration

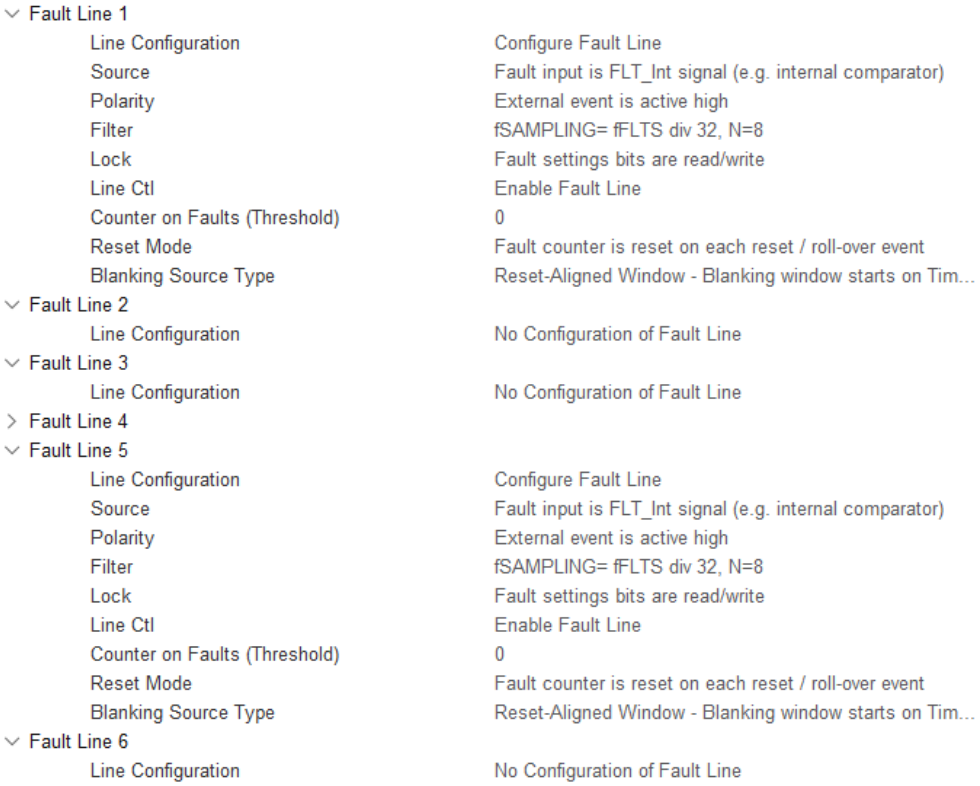


Step 11. First the fault lines must be configured as these will be used within the individual timer modules. Click on the [**Fault Lines Configuration**] tab and enable [**Fault line 1**] by selecting [**Configure Fault Line**] under [**Line Configuration**].

Step 12. For the [**Fault Line 1**] configuration settings, the only setting that needs to be changed from default is the [**Filter**]. Set the [**Filter**] to the maximum *fSAMPLING = fFLTS div 32 N=8*.

Step 13. Repeat this for [**Fault Line 5**].
The fault lines configuration window should now looks as follows:

Figure 47. STM32CubeMX Fault Line settings



Step 14. For the individual timer configurations, let us begin with *Timer C*, which is the timer that controls the lagging switches in the full-bridge on the primary side of the PSFB converter. Click on the [**Timer C**] tab within the configuration pane and configure the following settings.

Table 12. STM32CubeMX Timer C settings

Time Base setting	Period	54400
Timing Unit	Preload Enable	Preload enabled
	Repetition Update	Update on repetition enabled
	Number of Faults to enable	2
	1st Fault Source	Fault 1 enabled
	2nd Fault Source	Fault 5 enabled
	Dead time Insertion	Deadtime is inserted between output 1 and output 2
	Reset Trigger Sources selection	1
	1st Reset Trigger Source	The timer counter is reset upon master timer period event
Compare Unit 1	Compare Unit 1 Configuration	Enable
	Compare Value	27200
Compare Unit 4	Compare Unit 4 Configuration	Enable
	Compare Value	27200
Dead time	Prescaler	fDTG = fHRTIM
	Rising Value	DEAD_TIME_LAGGING_RISING_DT_TICK
	Falling Value	DEAD_TIME_LAGGING_FALLING_DT_TICK
Output 1 Configuration	Set Source selection	1
	1st Set Source	Timer period event forces the output to its active state
	Reset Source selection	1
	1st Reset Source	Timer compare 1 event forces the output to its inactive state
	Fault Level	Output at inactive level when in FAULT state
Output 2 Configuration	Fault Level	Output at inactive level when in FAULT state

Step 15. Moving on to *Timer B*, which controls the leading switches in the full-bridge on the primary side of the PSFB converter. Click on the [**Timer B**] tab within the configuration pane and configure the following settings.

Table 13. STM32CubeMX Timer B settings

Time Base setting	Period	54400
Timing Unit	Preload Enable	Preload enabled
	Repetition Update	Update on repetition enabled
	Number of Faults to enable	2
	1st Fault Source	Fault 1 enabled
	2nd Fault Source	Fault 5 enabled
	Dead time Insertion	Deadtime is inserted between output 1 and output 2
	Reset Trigger Sources selection	1
	1st Reset Trigger Source	The timer counter is reset upon master timer period event
Compare Unit 1	Compare Unit 1 Configuration	Enable
	Compare Value	PHASE_SHIFT_MIN
Compare Unit 2	Compare Unit 2 Configuration	Enable
	Compare Value	PHASE_SHIFT_MIN + HALF_HRTIM_PWM_PERIOD
Compare Unit 3	Compare Unit 3 Configuration	Enable
	Compare Value	3000
Dead time	Prescaler	fDTG = fHRTIM
	Rising Value	DEAD_TIME_RISING_DT_TICK
	Falling Value	DEAD_TIME_FALLING_DT_TICK
Output 1 Configuration	Set Source selection	1
	1st Set Source	Timer compare 1 event forces the output to its active state
	Reset Source selection	1
	1st Reset Source	Timer compare 2 event forces the output to its inactive state
	Fault Level	Output at inactive level when in FAULT state
Output 2 Configuration	Fault Level	Output at inactive level when in FAULT state

Step 16. Moving on to *Timer A*, which controls the lagging switches in the full-bridge synchronous rectifier on the secondary side of the PSFB converter. Click on the [**Timer A**] tab within the configuration pane and configure the following settings.

Table 14. STM32CubeMX Timer A settings

Time Base setting	Period	54400
Timing Unit	Preload Enable	Preload enabled
	Repetition Update	Update on repetition enabled
	Number of Faults to enable	2
	1st Fault Source	Fault 1 enabled
	2nd Fault Source	Fault 5 enabled
	Dead time Insertion	Deadtime is inserted between output 1 and output 2
	Reset Trigger Sources selection	1
	1st Reset Trigger Source	The timer counter is reset upon master timer period event
Compare Unit 1	Compare Unit 1 Configuration	Enable
	Compare Value	HRTIM_PWM_PERIOD - DEAD_TIME_RISING_HR_TICK
Compare Unit 2	Compare Unit 2 Configuration	Enable
	Compare Value	PHASE_SHIFT_MIN + DEAD_TIME_FALLING_HR_TICK
Dead time	Prescaler	fDTG = fHRTIM
	Rising Value	DEAD_TIME_RISING_DT_TICK
	Falling Value	DEAD_TIME_FALLING_DT_TICK
Output 1 Configuration	Set Source selection	1
	1st Set Source	Timer compare 1 event forces the output to its active state
	Reset Source selection	1
	1st Reset Source	Timer compare 2 event forces the output to its inactive state
	Fault Level	Output at inactive level when in FAULT state
Output 2 Configuration	Fault Level	Output at inactive level when in FAULT state

Step 17. Moving on to [**Timer D**], which controls the leading switches in the full-bridge synchronous rectifier on the secondary side of the PSFB converter. Click on the [**Timer D**] tab within the configuration pane and configure the following settings.

Table 15. STM32CubeMX Timer D settings

Time Base setting	Period	54400
Timing Unit	Preload Enable	Preload enabled
	Repetition Update	Update on repetition enabled
	Number of Faults to enable	2
	1st Fault Source	Fault 1 enabled
	2nd Fault Source	Fault 5 enabled
	Dead time Insertion	Deadtime is inserted between output 1 and output 2
	Reset Trigger Sources selection	1
	1st Reset Trigger Source	The timer counter is reset upon master timer period event
Compare Unit 1	Compare Unit 1 Configuration	Enable
	Compare Value	HALF_HRTIM_PWM_PERIOD - DEAD_TIME_RISING_HR_TICK
Compare Unit 2	Compare Unit 2 Configuration	Enable
	Compare Value	PHASE_SHIFT_MIN + HALF_HRTIM_PWM_PERIOD + DEAD_TIME_FALLING_HR_TICK
Dead time	Prescaler	fDTG = fHRTIM
	Rising Value	DEAD_TIME_RISING_DT_TICK
	Falling Value	DEAD_TIME_FALLING_DT_TICK
Output 1 Configuration	Set Source selection	1
	1st Set Source	Timer compare 1 event forces the output to its active state
	Reset Source selection	1
	1st Reset Source	Timer compare 2 event forces the output to its inactive state
	Fault Level	Output at inactive level when in FAULT state
Output 2 Configuration	Fault Level	Output at inactive level when in FAULT state

Step 18. Finally, on to *Timer E*, which controls the active clamp PWM to clamp the leakage ringing/spike across the synchronous rectifier on the secondary side of the PSFB converter. Click on the [**Timer E**] tab within the configuration pane and configure the following settings.

Table 16. STM32CubeMX Timer E settings

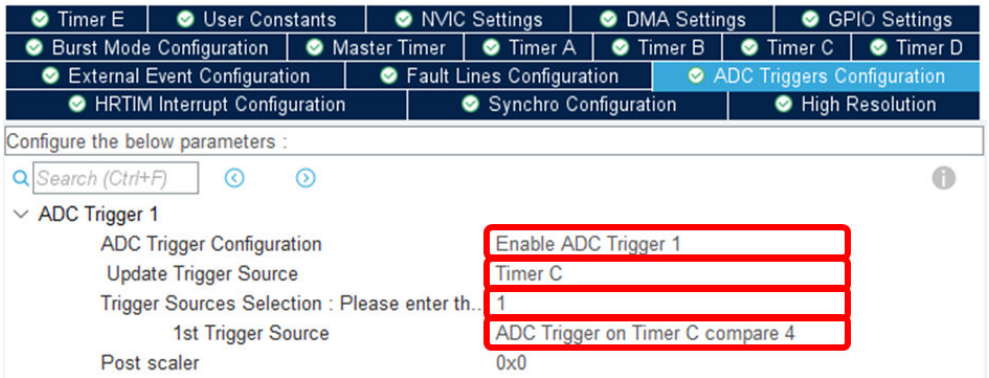
Time Base setting	Period	27200
Timing Unit	Preload Enable	Preload enabled
	Repetition Update	Update on repetition enabled
	Number of Faults to enable	2
	1st Fault Source	Fault 1 enabled
	2nd Fault Source	Fault 5 enabled
	Reset Trigger Sources selection	1
	1st Reset Trigger Source	The timer counter is reset upon master timer period event
Compare Unit 1	Compare Unit 1 Configuration	Enable
	Compare Value	1000
Compare Unit 2	Compare Unit 2 Configuration	Enable
	Compare Value	1000 + ACTIVE_CLAMP_PULSE_DURATION_HR_TICK
Output 1 Configuration	Polarity	Output is active LOW
	Set Source selection	1
	1st Set Source	Timer compare 1 event forces the output to its active state
	Reset Source selection	1
	1st Reset Source	Timer compare 2 event forces the output to its inactive state
	Fault Level	Output at inactive level when in FAULT state

Step 19. The ADC trigger must be configured for the HRTIM1 module. Under [**HRTIM1**] select the [**ADC Triggers Configuration**] tab.

Step 20. Enable the [**ADC Trigger 1**] and set the [**Update Trigger Source**] to *Timer C*, enter the number of [**Trigger Sources selection**] to *1*.

Step 21. From the [**1st Trigger Source**] drop down box select *ADC Trigger on Timer C compare 4*. This is the event, which will trigger the ADC.

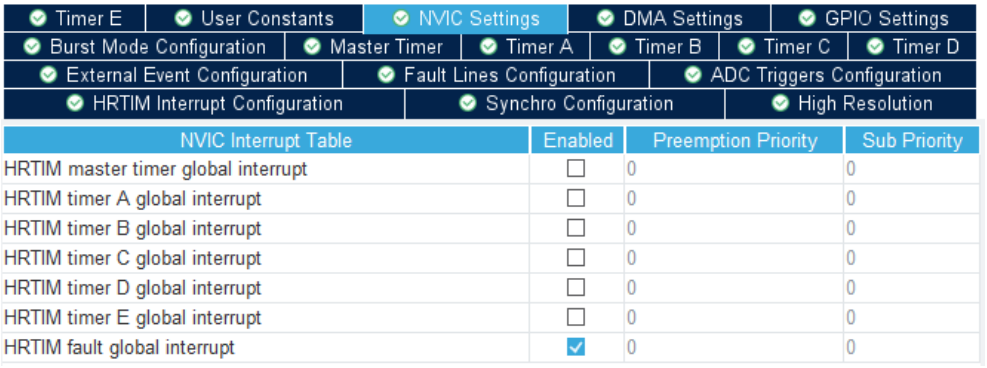
Figure 48. STM32CubeMX ADC Triggers configuration



Step 22. Then, select the [**NVIC**] configuration option along the row of [**HRTIM configuration tabs**]. This allows the interrupts to be for each timer.

Step 23. From the table, enable [**HRTIM fault global interrupt**].
The interrupt table should match the image below.

Figure 49. STM32CubeMX NVIC configuration



Step 24. Furthermore, under the [**HRTIM Interrupt Configuration**] tab, set the [**1st Interrupt Source**] as the *Fault 1 Interrupt*.

8.2.6 USART configuration

The USART module is used to provide communication between the primary and secondary side MCUs on the evaluation board. This allows the primary MCU to inform the secondary that the PFC bus is at the nominal voltage and the output can be started for example.

Step 1. To enable the USART, scroll down on the left-hand side peripherals list to [**Connectivity**] and expand this heading. Select [**USART1**] and change the [**mode**] to *Asynchronous*.

Step 2. Pins PB7 and PB6 are physically connected to the USART transceiver on the daughter card for this evaluation board. Therefore, you will need to manually move the USART RX pin from PC5 to PB7. To do this, simply left click on [**PB7**] and scroll down to the [**USART1_RX**] option and select it.
The pin should turn green and PC5 should go back to gray.

Step 3. Under the [**Parameter Settings**] on the configuration pane, set both the [**TX pin Active Level Inversion**] and the [**RX pin Active Level Inversion**] to *Enable*. All of the other settings can be left as default.

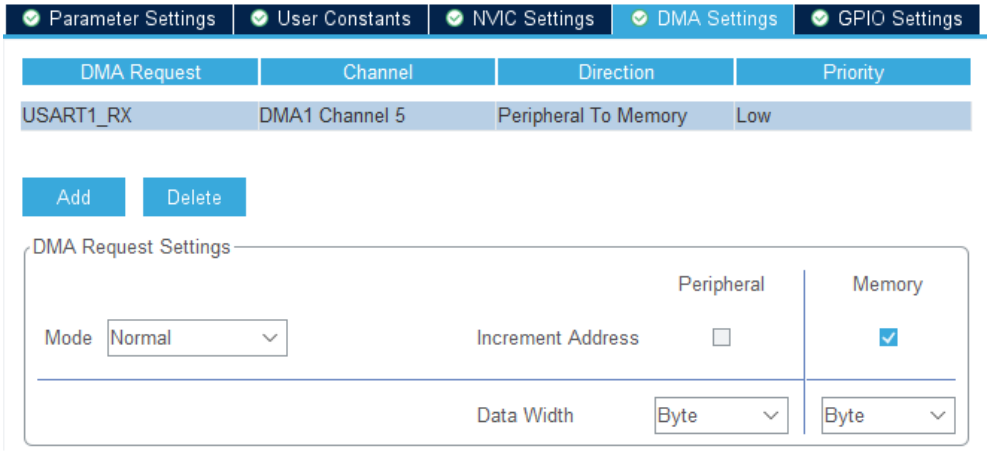
Step 4. Under the [**DMA Settings**] on the configuration pane of the USART1, add a DMA request by clicking [**Add**] towards the bottom of the window.

Step 5. From the drop-down box, select [**USART1_RX**] and set the channel to *DMA1 Channel 5*.

Step 6. Highlight the DMA request by clicking on it and the request settings should appear at the bottom of the configuration window. Change the [**mode**] to *Circular*.

The settings should look as follows:

Figure 50. STM32CubeMX DMA configuration



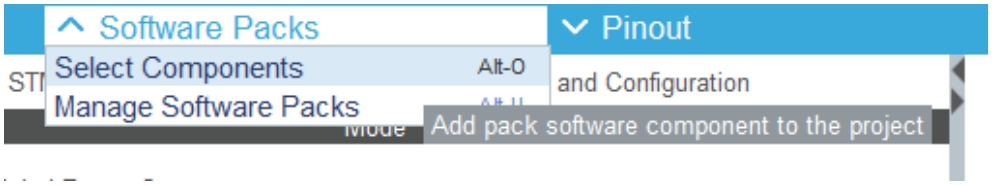
8.2.7 Debug Pins

Step 1. Finally, again under [**System Core**], click on the [**SYS**] peripheral and set the [**Debug**] mode to *Serial*.

8.3 Digital Power Pack Configuration using STM32CubeMX

With the X-CUBE-DPower pack installed, the option to configure the pack will be available from the [**Software Packs**]>[**Select Components**] menu option in STM32CubeMX.

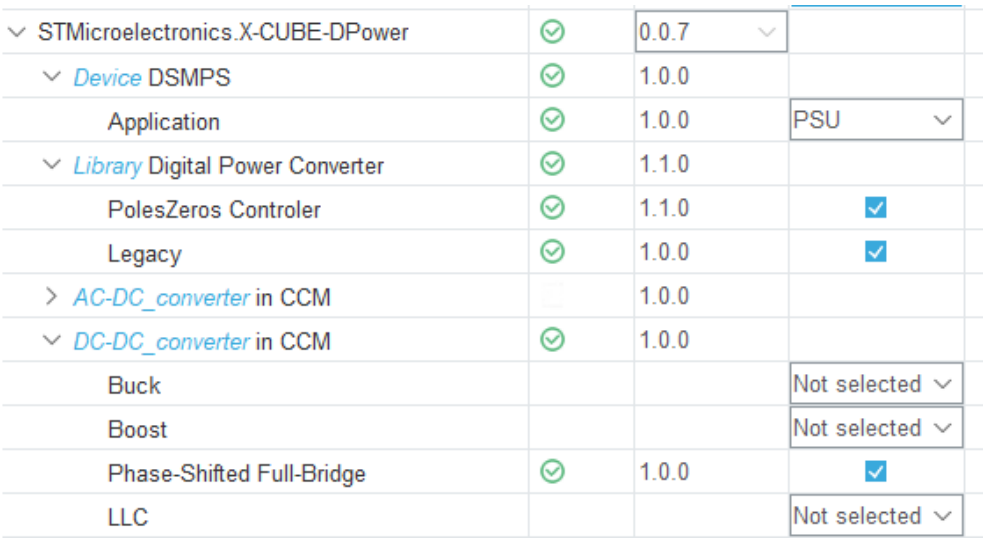
Figure 51. STM32CubeMX select software components menu



Step 1. To configure the X-CUBE-DPower pack for controlling the PSFB converter, the options shown in the following Figure are selected. First, set [**Application**] to *PSU* under the [**Device**] options.

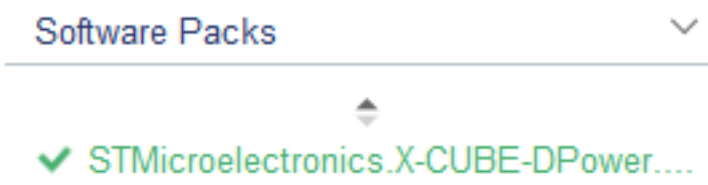
Step 2. Both [**PolesZeros**] [**controller**] and [**Legacy**] options are ticked under the [**Library**] options and in the [**DC-**] [**DC_converter**] options the [**phase-shifted Full-Bridge**] converter is selected.

Figure 52. X-CUBE-DPower software pack configuration



With these options selected, the X-CUBE-DPower pack will now be available under the [**Software Packs**] section of the [**Categories**] toolbar on the left-hand pane of STM32CubeMX.

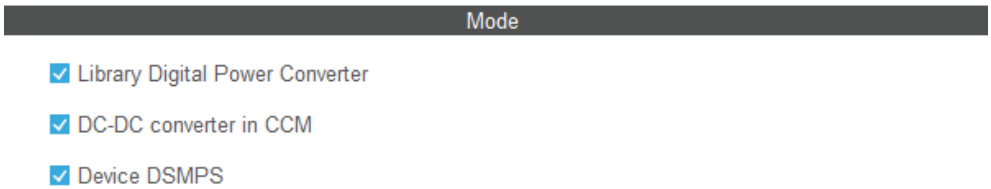
Figure 53. X-CUBE-DPower software pack visibility in STM32CubeMX



8.3.1 Project settings

Step 1. With the X-CUBE-DPower pack enabled and pack options configured for the PSFB converter, the following [**mode**] options should be selected.

Figure 54. X-CUBE-DPower mode options



Step 2. The user must then configure the parameters according to their specific application. The parameters populated by default are those required for the STEVAL-ISA172V3 board.

Figure 55. X-CUBE-DPower parameter settings - 1

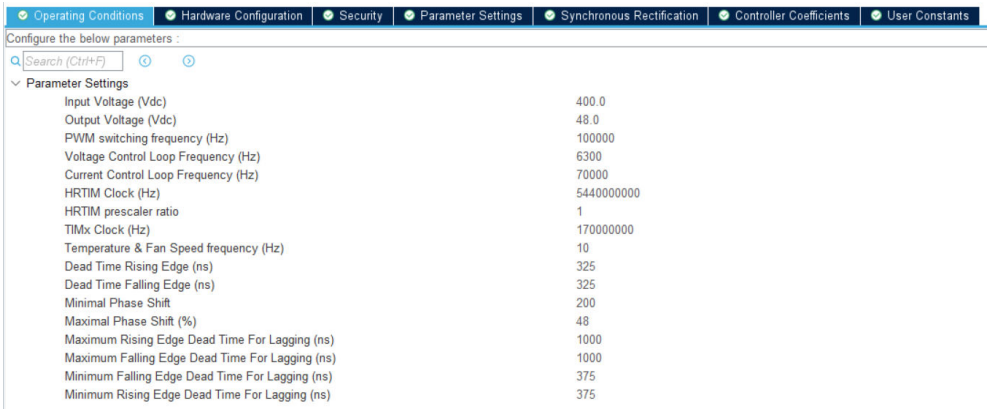


Table 17. X-CUBE-DPower parameter descriptions - 1

Parameter	Description
Vin	Nominal input voltage (V)
Vout	Desired output voltage (V)
SWITCHING_FREQ_HZ	PWM signals frequency (Hz)
VOLTAGE_CONTROL_LOOP_FREQ	Execution frequency of Vout control loop (Hz) (choose a submultiple of PWM frequency) For example, it is 5000 for the MB1971 LLC board For example, it is 6300 for the PFC part and 50000 for the PSU part of the STEVAL-ISA172V3 board
CURRENT_CONTROL_LOOP_FREQ	Execution frequency of Iout control loop (Hz) (choose a submultiple of PWM frequency) For example, it is 70000 for the STEVAL-ISA172V3 board
HRTIM_CLK_HZ	Clock frequency of the HRTimer (Hz)
HRTIM_PRESC_RATIO	Prescaler ratio of the HRTimer It is known as CKPSC[2:0] inside the RM document : from 0b000 (=0d1) to 0b111 (=0d128)
TIMx_CLK_HZ	Clock frequency of the TIMx used for COMP blanking window (OCP) (Hz)
TEMPERATURE_FAN_CTRL_FREQ	Frequency of the temperature acquisition and also fan speed control routine (Hz)
DT_RISING_EDGE	Dead Time of rising edge for main power switches (ns)
DT_FALLING_EDGE	Dead Time of falling edge for main power switches (ns)
PS_MIN	Minimal phase shift (HRTIM ticks) This value must be at least 32 (Cf. RM)
PS_MAX	Maximal phase shift (%) This value must be lower than 50% of PWM period
MAX_LAGGING_DT_RISING_EDGE	Maximum Dead Time of rising edge for lagging half of the bridge (ns)
MAX_LAGGING_DT_FALLING_EDGE	Maximum Dead Time of falling edge for lagging half of the bridge (ns)
MIN_LAGGING_DT_FALLING_EDGE	Minimum Dead Time of falling edge for lagging half of the bridge (ns)
MIN_LAGGING_DT_RISING_EDGE	Minimum Dead Time of rising edge for lagging half of the bridge (ns)

Figure 56. **X-CUBE-DPower parameter settings - 2**

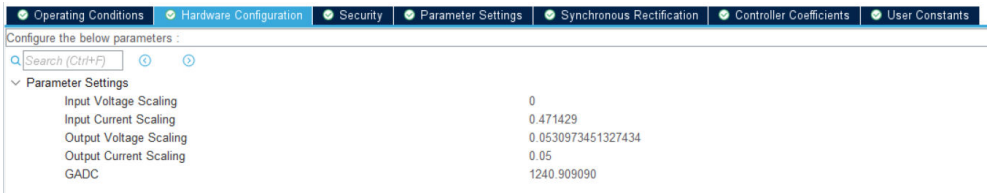


Table 18. **X-CUBE-DPower parameter descriptions - 2**

Parameter	Description
Vin_Scaling	Scaling of the input voltage, Vin: For example, it is computed as this [6.8k / (6.8k + 27k)] for the PSU part, based on B-G474E-DPOW1 board For example, it is computed as this (3.6f / ((180.0f * 3.0f) + (3.6f))) * (1.0f + (3.3f / 10.0f)) for the PFC part, based on STEVAL-ISA172V3 board
Iin_Scaling	Scaling of the input current, Iin: For example, with the current sense transformer method used, it is computed as this [(1/70) * (200*18)/(200+18))] based on STEVAL-ISA172V3 board
Vout_Scaling	Scaling of the output voltage, Vout: For example, it is computed as this [22k / (22k + 360k)] based on STEVAL-ISA172V3 board
Iout_Scaling	Scaling of the output current, Iout
GADC	Scaling ADC gain : It is computed as (12-bit ADC / ADC Vref) = (4095.0f/3.3f)

Figure 57. **X-CUBE-DPower parameter settings - 2**

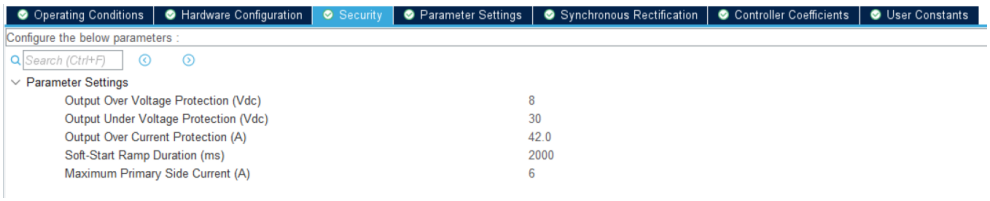


Table 19. **X-CUBE-DPower parameter descriptions - 2**

Parameter	Description
Vout_OVP	Overvoltage protection level for the output (V)
Vout_UVP	Minimum output voltage level for short circuit detection and protection (V)
Vout_OCP	Overcurrent protection level for the output current (A)
SOFT_START_MS	Soft-start period (ms). This is the duration of the ramp-up from starting voltage (peak of rectified input) to steady state output voltage.
MAX_TRANSFO_CURRENT	Maximum primary side current (A). It is used to determine the point at which the primary switches are shut off in the case of over-current.

Figure 58. **X-CUBE-DPower parameter settings - 3**

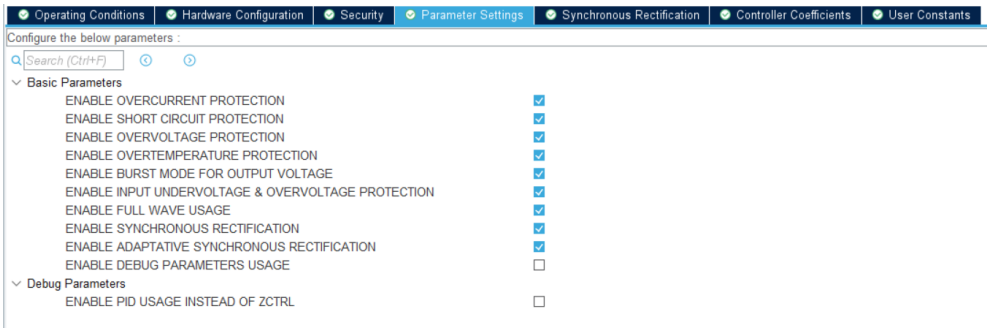


Table 20. **X-CUBE-DPower parameter descriptions - 3**

Parameter	Description
OVERCURRENT_PROTECTION	When defined, enable the overcurrent protection mechanism to disable the output when the primary current is above the user's threshold
SHORT_CIRCUIT_PROTECTION	When defined, enable the short-circuit protection check that disabled the output when the load current is above the user's defined threshold
OVERVOLTAGE_PROTECTION	When defined, enable the overvoltage protection mechanism to disable the output when the input voltage is above the threshold.
OVERTEMPERATURE_PROTECTION	When defined, enable the overtemperature Protection mechanism to disable the output when the temperature is above the threshold
OUT_VOLTAGE_BURST_MODE	When defined, enable the burst mode usage to control output voltage
IN_OVER_UNDER_VOLTAGE_PROTECTION	When defined, Enable the UVP & OVP mechanism (→ DC/DC is disabled) when the input voltage is outside the threshold It is useful for resonant converters
FULL_WAVE	When enabled, the active clamp and the synchronous rectification features operate in full wave mode. Otherwise, these features operate in center tapped mode.
SYNCH_RECTIFICATION	When defined, the synchronous rectification is enabled to reduce conduction losses
ADAPTATIVE_SYNCH_RECTIFICATION	When defined, the synchronous rectification on the secondary side is enabled, using an adaptive algorithm to reduce conduction losses
DEBUG_MODE	When defined, provide debug mode access as a set of debugging parameters useful during compilation time
CHANGE_CTRL_TO_PID	When defined, enable the PID controller instead of 2p2z/3p3z controller usage

Figure 59. **X-CUBE-DPower parameter settings - 4**

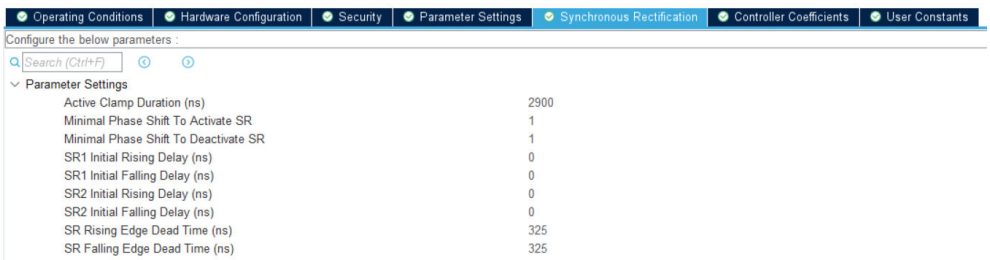


Table 21. **X-CUBE-DPower parameter descriptions - 4**

Parameter	Description
ACTIVE_CLAMP_DURATION	This is the on-time for the active clamp pulse used to clamp the synchronous rectification voltage of the converter (ns)
PS_MIN_SR_ACTIVATION	Minimal phase shift to activate synchronous rectification (HRTIM ticks)
PS_MIN_SR_DEACTIVATION	Minimal phase shift to turn off synchronous rectification (HRTIM ticks)
SR1_RISING_DELAY	Initial rising delay for synchronous rectification switches SR1 (ns)
SR1_FALLING_DELAY	Initial falling delay for synchronous rectification switches SR1 (ns)
SR2_RISING_DELAY	Initial rising delay for synchronous rectification switches SR2 (ns)
SR2_FALLING_DELAY	Initial falling delay for synchronous rectification switches SR2 (ns)
SR_DT_RISING_EDGE	Dead time of the rising edge for synchronous rectification switches (ns)
SR_DT_FALLING_EDGE	Dead time of the falling edge for synchronous rectification switches (ns)

Figure 60. **X-CUBE-DPower parameter settings - 5**

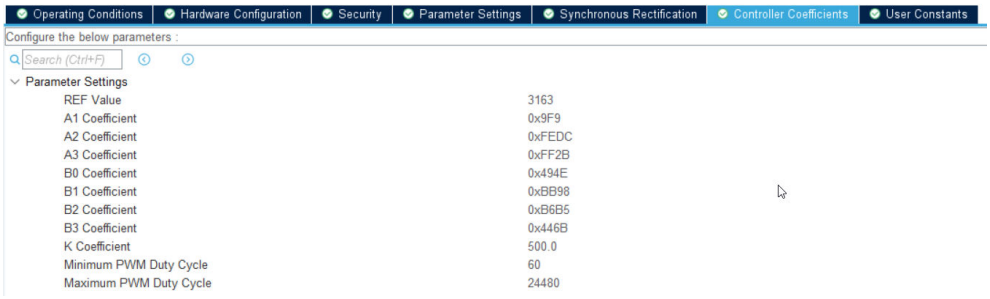


Table 22. **X-CUBE-DPower parameter descriptions - 5**

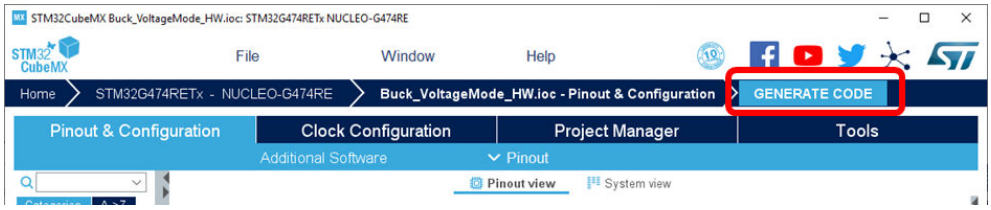
Parameter	Description
REF	Output voltage reference value. It is expressed as an ADC value.
A1	Poles and zeros controller coefficient: A1
A2	Poles and zeros controller coefficient: A2
A3	Poles and zeros controller coefficient: A3
B0	Poles and zeros controller coefficient: B0
B1	Poles and zeros controller coefficient: B1
B2	Poles and zeros controller coefficient: B2
B3	Poles and zeros controller coefficient: B3
K	Poles and zeros controller coefficient: K
DUTY_TICKS_MIN	Minimum PWM for the duty cycle control (HRTIM ticks)
DUTY_TICKS_MAX	Maximum PWM for the duty cycle control (HRTIM ticks)

8.4 Code Generation Configuration using STM32CubeMX

Step 1. Finally, generate the project by clicking the [**GENERATE CODE**] button.

This will create the necessary project files for the selected IDE and include Digital Power functions within the auto-generated .c/.h files. In this example STM32CubeIDE from STMicroelectronics is used.

Figure 61. STM32CubeMX generate code button



Step 2. A prompt will appear once the project files have been created which asks if you would like to open the project.Click [**Open project**] to load the project into the selected IDE.

Step 3. The main.c file contains the code for this project, open the main.c file and read the comments.

8.4.1 Project Implementation

The generated project structure consists of multiple layers:

- Standard project files:
  - main.c/.h
  - stm32g4xx_hal_msp.c/.h
  - stm32g4xx_it.c/.h
  - system_stm32g4xx.c/.h
- Application specific files:
  - app_dpower.c/.h
  - DCDC_Control_Layer.c/.h
  - DCDC_IRQ_Handlers.c
  - DCDC_Lib_Conf.h
- Common board support files:
  - DPC_Communication.c/.h
  - DPC_Miscellaneous.c/.h
  - DPC_STM32_Interface.c/.h
  - DCDC_PWMnCurrVoltFdbk.c/.h
  - DCDC_Fault_Processing.c/.h

Having set up the parameters for the PSU in STM32CubeMX, the user need only modify the main.c/.h and stm32g4xx_it.c/.h files to add their own application specific code.

In this section, the digital Power implementation in the source files is described by identifying its specific functions.

8.5 Program flow description

The main.c file contains the majority of the code for setting up and initializing the peripherals. Some of the code within this file has been automatically generated by the STM32CubeMX tool as per the configuration process in the previous step of this application note

Within these code files, there are comments similar to *USER CODE BEGINS HERE* and *USER CODE ENDS HERE*. It is essential that any additional code added to the project is kept between these two comments. This is because, outside of these comments, the code is automatically generated by the STM32CubeMX tool.

If any changes are made to the project configuration within the tool, and the code is regenerated by clicking [**GENERATE CODE**], the additional changes made outside of these comment bounds will be lost.

Keeping user code within these comment bounds ensure that the code persists after the next time the code is regenerated using the STM32CubeMX tool.

The figure below shows examples of the user code locations highlighted in red.

Figure 62. **Example of user code locations within main.c**

```
/**
  * @brief  The application entry point.
  * @retval int
  */
int main(void)
{
  /* USER CODE BEGIN 1 */

  /* USER CODE END 1 */


  /* MCU Configuration--------------------------------------------------------*/

  /* Reset of all peripherals, Initializes the Flash interface and the Systick. */
  HAL_Init();

  /* USER CODE BEGIN Init */

  /* USER CODE END Init */

  /* Configure the system clock */
  SystemClock_Config();

  /* USER CODE BEGIN SysInit */

  /* USER CODE END SysInit */

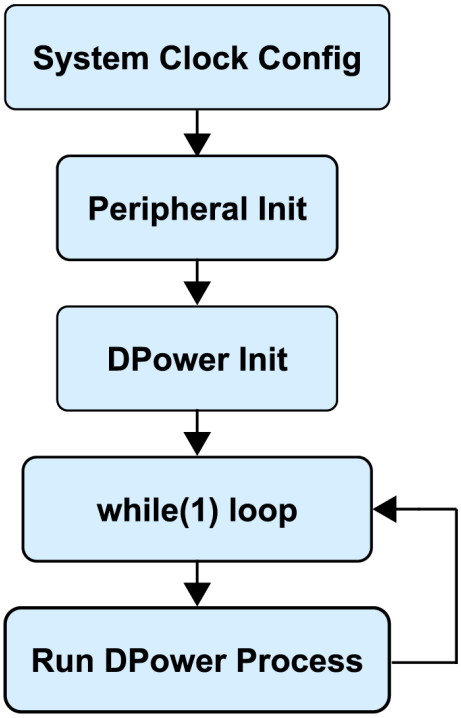
  /* Initialize all configured peripherals */
  MX_GPIO_Init();
  MX_DMA_Init();
  MX_RTC_Init();
  MX_ADC1_Init();
  MX_HRTIM1_Init();
  MX_FMAC_Init();
  /* USER CODE BEGIN 2 */

    /*## Configure the FMAC peripheral ##########################################*/
  sFmacConfig.InputBaseAddress  = INPUT_BUFFER_BASE;
  sFmacConfig.InputBufferSize   = INPUT_BUFFER_SIZE;
  sFmacConfig.InputThreshold    = INPUT_THRESHOLD;
  sFmacConfig.CoeffBaseAddress  = COEFFICIENT_BUFFER_BASE;
```

The structure of the main function within main.c is represented in Figure 63. This is the function that the MCU will jump to after power-on; the entry point within the code. Therefore, this function contains calls to all of the initialization functions to set up the peripherals onboard the MCU. After this, the controller for the PSFB converter is set up and initialized with the calculated coefficients.

Finally, the ADC is started and begins sampling the output voltage and the PWM outputs are enabled to drive the main power switches.

Figure 63. **Function flow of main() within main.c**



8.5.1 MX_DPower_Init();

The MX_DPower_Init() function is responsible for initializing the peripherals required for controlling the PSU stage, in this case the PSFB converter.

The init function starts by configuring the DC-DC converter's controller structure using the DCDC_config() function from the Biricha digital Power Library. This function sets up the controller with the specified topology, modulation method and control mode.

Next, the function initializes the 3p3z converter used to close the outer voltage loop. This is done using either the FMAC (filter math accelerator) peripheral or with a 3p3z (3-pole, 3-zero) controller running on the main core, depending on the definition of the 'USE_FMAC' user modality. The __3p3zInitFmacInt16() and __StartFmacInt16() functions are used to set up and start the FMAC peripheral, while the CNTRL_3p3zInit() function is used to set up the 3p3z converter without using the FMAC.

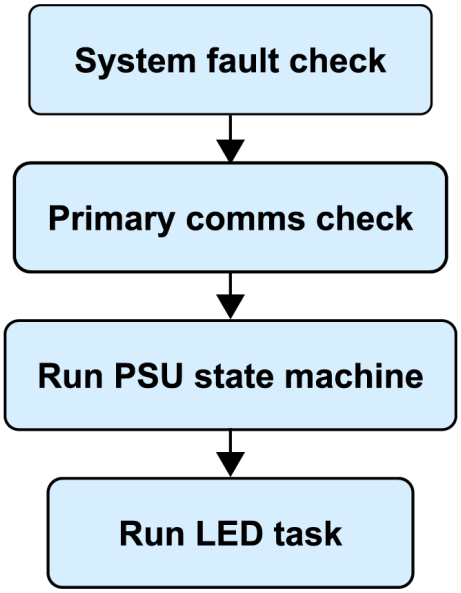
The function then initializes the soft start ramp using the CNTRL_RampFloatConfig() function, again from the Biricha digital Power Library. This is used to smoothly ramp up the output voltage of the converter at startup.

The Digital Power init function also initializes the ADC peripherals. These are used to measure the output voltage, output current and operating temperature of the converter. The HAL_ADCEx_Calibration_Start() calibrates the ADC for single-ended conversion. The ADC measuring the output voltage and current, ADCx, is started in DMA mode using HAL_ADC_Start_DMA(). This means that the ADC results will be copied automatically to the measurement data structured by the DMA when the ADC conversion is complete.

Furthermore, ADC end of sequence interrupts are enabled for ADCx. The ADC interrupt will be used to run the 3p3z control loop routine.

Finally, the function sets up and starts the TIM2 timer to provide blanking for the overcurrent comparator and enables the HRTIM counter for the main PWM, synchronous rectifier PWM, and active clamp PWM outputs.

Figure 64. **Function flow conclusion of main() within main.c**



8.5.2 MX_DPower_Process();

The MX_DPower_Process() function is called repeatedly to monitor, control, and transition between operating states for the selected DC-DC converter topology. The function achieves this by use of a finite state machine.

The function first checks if a fault has occurred on the DC-DC converter or if a fault has been communicated by the PFC (power factor correction) stage via the isolated communication bus using UART. This is achieved by calling the DCDC_FaultCheck() and DCDC_PrimaryStatusCheck() functions.

Next, the function enters a switch statement that contains a case for each state in the finite state machine. The current state of the machine is indicated by the myDcdc.m_DCDC_State variable within the DC-DC converter structure, which can take on the following values:

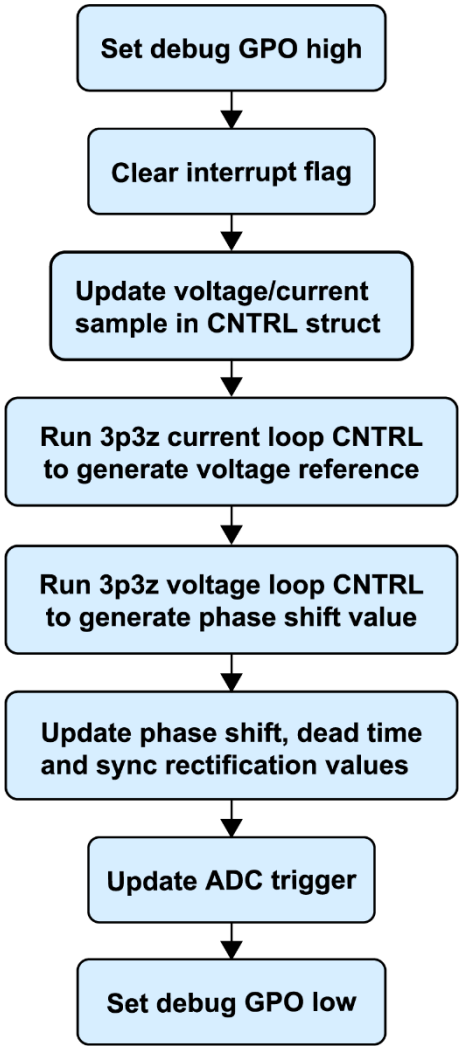
- DCDC_IDLE: This state is used to wait for the input voltage and frequency conditions to be satisfied before starting up the DC-DC converter. The conditions are communicated via the isolated communication interface between primary and secondary MCUs. The LED is set to blink until the startup conditions are satisfied.
- DCDC_INIT: This state is used to reinitialize the control variables and enable the PWM outputs of the converter. A delay timer is set for the ramp-up duration – this is used to detect if the converter failed to reach the voltage set point in the allowed time, indicating a problem at the output of the converter. The LED is set to blink quickly until the ramp-up is complete.
- DCDC_START: This state is used to ramp up the output voltage of the DC-DC converter. The power-up flag is set, and the undervoltage and overtemperature checks are enabled after the startup time has elapsed. If the converter is using synchronous rectification, these outputs are also enabled. If the DC-DC output reaches the specified set point within the target time, the LED blink frequency is changed and the next state is set to DCDC_RUN.
- DCDC_RUN: This state is used to run the DC-DC converter in normal operation. The LED is set to blink slowly, and the voltage and current control loops are run to regulate the output of the converter in the ADC ISR. Undervoltage and overtemperature checks are enabled.
- DCDC_STOP: This state is used to disable the converter. The main PWM, active clamp, and synchronous rectifier outputs are disabled. Any system fault is stored in the ‘m_DCDC_Last_System_Fault’ element of the DC-DC structure, undervoltage and overtemperature checks are disabled and the ‘DCDC_START_UP_OK’ flag is cleared. The next state is set to ‘DCDC_FAULT’.
- DCDC_ERROR: This state is used to filter out temporary errors of the converter. The following state is WAIT until all expected trials are over. Then, depending on error condition, the next state is either FAULT or either IDLE.
- DCDC_FAULT: This is a persistent state that can only be exited when there is ‘DCDC_NO_ERROR’ present in the ‘m_DCDC_System_Fault’ fault flags. When all errors are cleared, a delay timer is initialized and the next state is set to DCDC_WAIT.
- DCDC_WAIT: This state waits for the delay timer to expire before setting the next state to DCDC_IDLE.

8.6 Interrupt Service Routine

In this example, the PSU is controlled using two 3p3z controller both running on the main core. The control loops are executed within the ADC interrupt service routine. It is also possible to run one of the control loops using the FMAC by adding the “USE_FMAC” define directive as discussed later in this application note.

The X-CUBE-DPower pack automatically generates the ADC ISR and includes the functions necessary to run the controllers responsible for stabilizing the PSU.

Figure 65. Software flow of the ADC ISR



The ADC1_2_IRQHandler() function is the interrupt service routine for the ADC1 and ADC2 peripherals. When the ADC1 or ADC2 peripherals generate an interrupt, this function is executed to handle the interrupt.

The function begins by setting a GPIO pin high and then clearing the interrupt flags for the ADC1 and ADC2 peripherals, using the __HAL_ADC_CLEAR_FLAG() function. This is necessary to capture future interrupt requests by the peripheral. This function is provided by the STM32 HAL (hardware abstraction layer), and is used to clear the specified interrupt flags in the ADC1 or ADC2 peripherals.

Next, the function stores the feedback values sampled by the ADC for the voltage and current of the power supply in the myDcdc.vLoop.m_Fdbk and myDcdc.iLoop.m_Fdbk variables respectively. These values are read from the DCDC_MeasureStruct structure, which holds the measured values for the voltage and current. The values in this structure are automatically copied from the ADC results registers using the DMA.

Next, if the voltage loop is running on the FMAC this will be triggered by writing to the WDATA register of the FMAC peripheral. In this example, the FMAC is not used therefore this is excluded by the compiler.

The function then executes the CNTRL_3p3z() function for the current loop. The output of the current loop is the demand reference value for the voltage loop. Effectively, if the output current is too high, the output voltage will be reduced to reduce the output current.

If the voltage loop is running on the main core, the 3p3z controller for the voltage loop is executed. The output of this controller will be the new phase shift value computed in this sampling interval.

The function then updates the phase shift value for the main PWM switches and, if enabled, updates the dead-time between switching for these main power switches. The dead time is calculated based on an application-specific algorithm. Therefore, these values may need to be adjusted for your application.

If synchronous rectification is enabled, these PWM outputs are also updated based on the new phase shift value. Finally, the ADC trigger point is updated to ensure that the ADC sample is taken in the middle of the switch on-time to ensure that a clean sample is achieved.

At the end of the ISR function, the GPIO pin is set to low to allow the duration of the ISR to be measured using an oscilloscope.

8.7 3p3z controller coefficients

The 3p3z controller coefficients are defined in the header file, app_dpower.h. This can be easily accessed by locating the #include "app_dpower.h" towards the top of the main.c file, right-clicking on “app_dpower.h” and selecting “Open “app_dpower.h” from the menu. Within this header file, there are several defines for specific to this application, which have been automatically generated by STM32CubeMX.

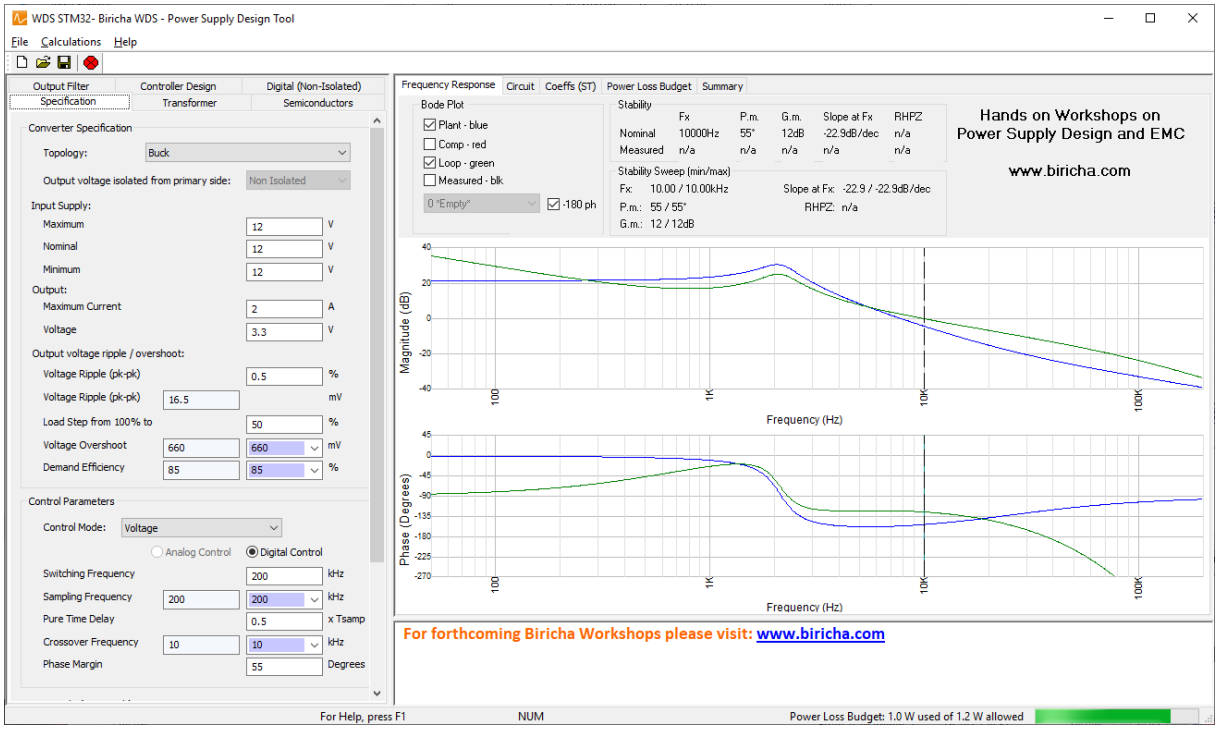
Further down this file, there is a section where the definitions for the HW/FMAC and SW/CPU based controller configurations begin. The coefficients (B0, B1, B2, B3, A1, A2, A3) for use on the FMAC are given in a fixed-point hexadecimal form and the coefficients for use on the CPU are given in floating-point form. Earlier in this application note, it was shown how the compensator poles and zeros, in the continuous-time domain, are converted into discrete-time controller coefficients. These coefficients have been obtained from ST-WDS. Designing this compensator in WDS is discussed in the next section.

8.8 ST WDS configuration

The power-supply design tool ST WDS from Biricha will be used to generate the fixed-point or floating-point controller coefficients for the controller. ST WDS is free-to-use and can be downloaded for free from the Biricha website. Visit www.biricha.com/st-wds for more information.

The .wds file associated with this application note is included in the project downloads in the appendix of this application note. However, the process for recreating the WDS project settings is included here for completeness.

Figure 66. **Biricha ST WDS**



The initial screen of ST WDS is shown in Figure 66. The left-hand pane is used for entering the specification of the power supply along with the other pertinent design parameters. The right-hand pane displays the control loop Bode plots, schematic, and outputs the required digital controller coefficients.

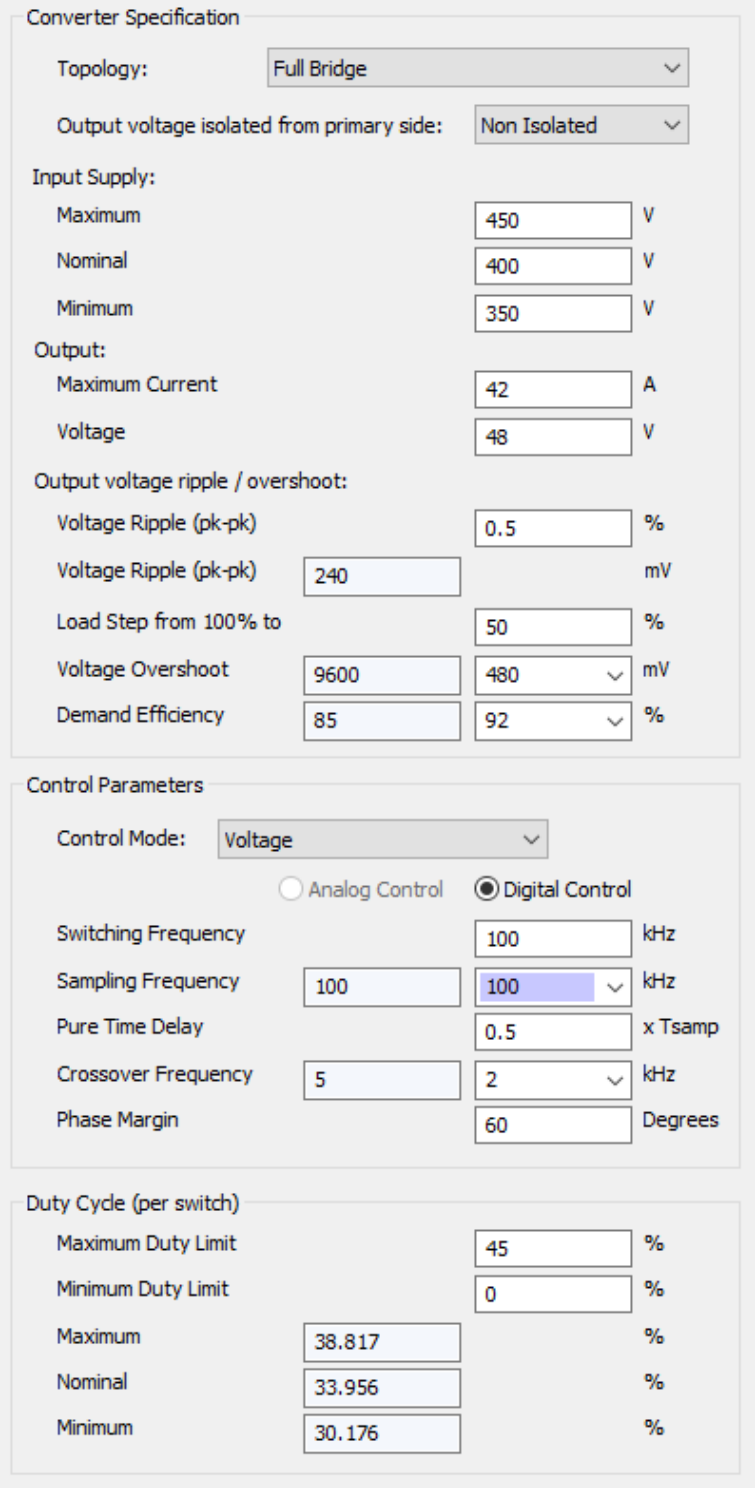
Step 1. To calculate the digital controller coefficients the power supply specification must first be entered. On the [**Specification**] tab, enter the specification shown in the following table.

Table 23. PSFB Specification

Specification tab parameter	Value
Topology	Full-bridge
Input supply max	450 V
Input supply nom	400 V
Input supply min	380 V
Output maximum current	42 A
Output voltage	48 V
Voltage Ripple (pk-pk)	0.5%
Load step 100% to…	50%
Voltage overshoot	480 mV
Demand efficiency	92%
Control mode	Voltage, digital Control
Switching frequency	100 kHz
Pure time delay	0.5
Crossover frequency	2 kHz
Phase margin	60 degrees
Maximum duty limit	45%
Minimum duty limit	0%

The [**Specification**] tab should now look like the screenshot shown below.

Figure 67. **ST WDS Specification tab**



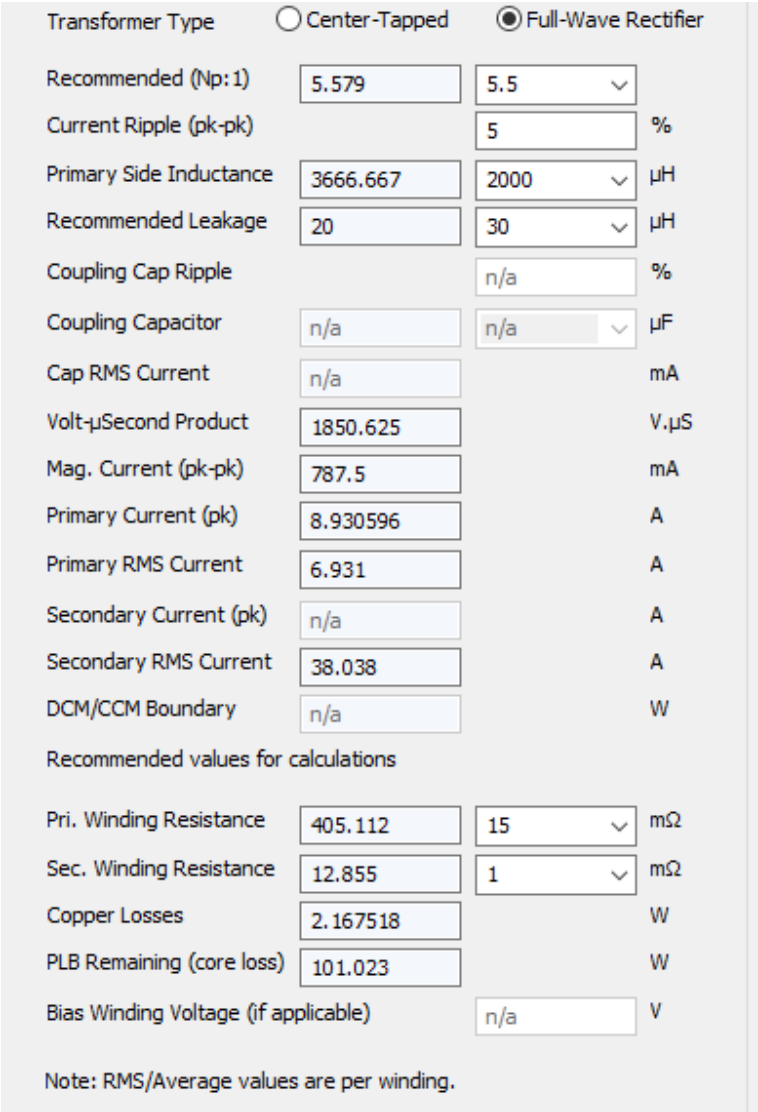
Step 2. The [**Transformer**] tab recommends the turns ratio for the main power transformer based on the information entered on the specification tab. This can then be used as a starting point for selecting an off-the-shelf transformer or designing a custom transformer. In this case, a custom transformer was used. Enter the details provided in the table below in to the transformer tab.

Table 24. Transformer parameters

Semiconductors tab parameter	Value
Transformer Type	Full-wave
Turns ratio (Np:1)	5.5
Primary side inductance	2000µH
Recommended leakage	30µH
Pri. winding resistance	15 mΩ
Sec. winding resistance	1mΩ

The [**Transformer**] tab should now look like the screenshot shown below.

Figure 68. ST WDS Transformer tab



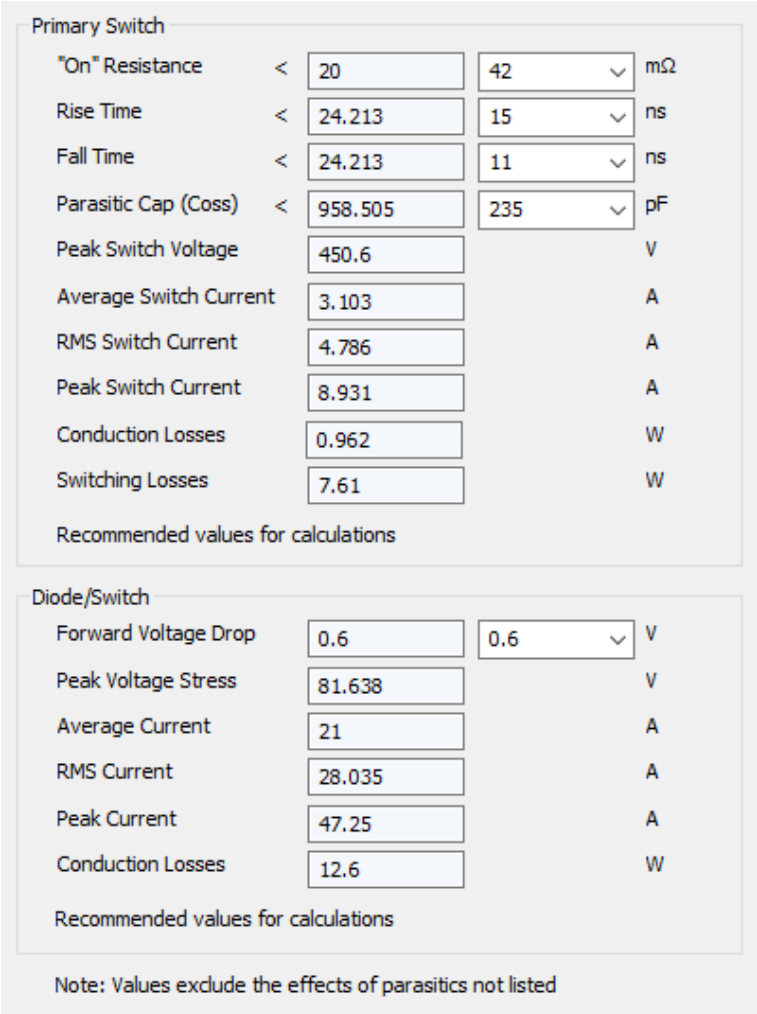
Step 3. Next, click on the [**Semiconductors**] tab and enter the specification shown in the table below.

Table 25. Semiconductor parameters

Semiconductors tab parameter	Value
“On” resistance	42mΩ
Rise time	15 ns
Fall time	11 ns
Parasitic cap (Coss)	235 pF
Forward voltage drop	0.6 V

The [**Semiconductors**] tab should now look like the screenshot shown in the figure below.

Figure 69. ST WDS Semiconductor tab



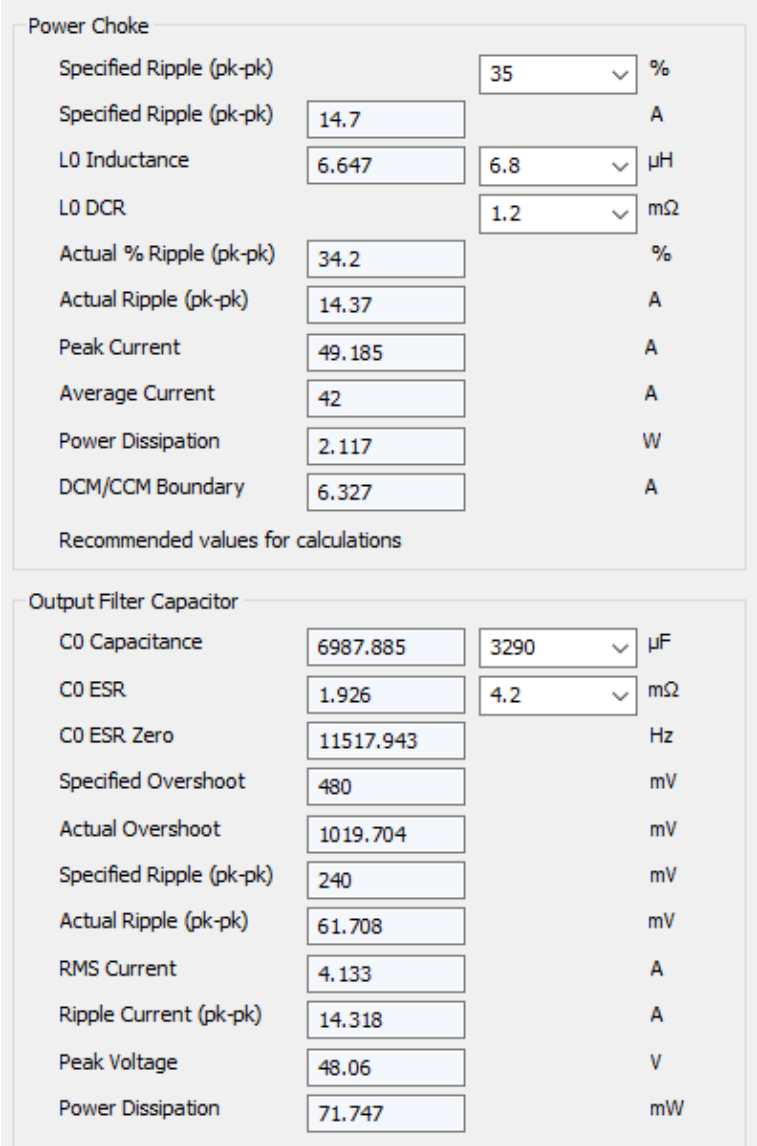
Step 4. The [**output Filter**] tab is next and has the specification shown below.

Table 26. Output Filter parameters

Output Filter tab parameter	Value
Specified Ripple (pk-pk)	35%
L0 inductance	6.8µH
L0 DCR	1.2mΩ
C0 capacitance	3290 µF
C0 ESR	4.2 mΩ

The [**Output Filter**] tab should now look like the screenshot shown in the figure below.

Figure 70. ST WDS Output FIlter tab

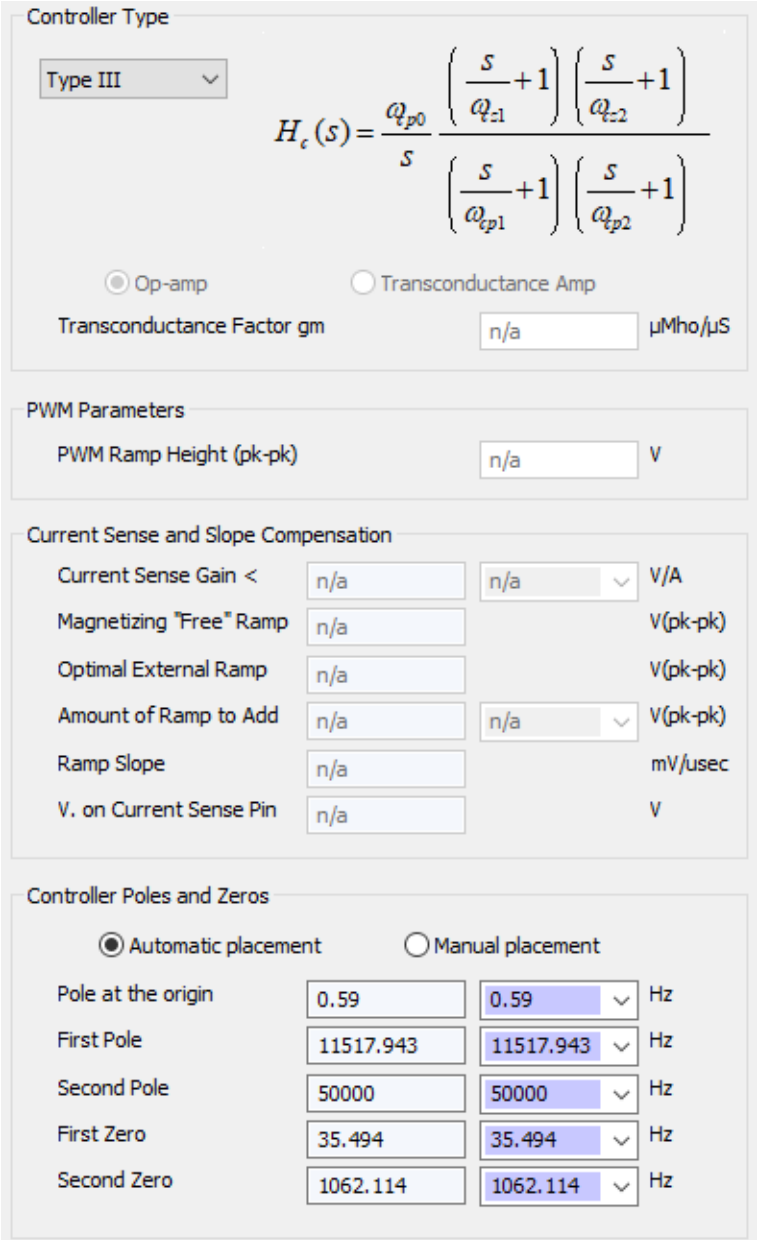


Step 5. On the next tab, [**Controller Design**], a Type III compensator will be automatically designed by WDS by placing the compensator poles and zeros so as to achieve the desired crossover frequency and phase margin. There is no need to enter any parameters into this tab as the poles and zeros will have already been calculated and should match those given below.

Table 27. Controller Design parameters

Controller Design tab parameter	Value
Pole at the origin	0.59 Hz
First Pole	11517.943 Hz
Second Pole	50,000 Hz
First zero	35.494 Hz
Second zero	1062.114 Hz

Figure 71. ST WDS Controller Design Tab

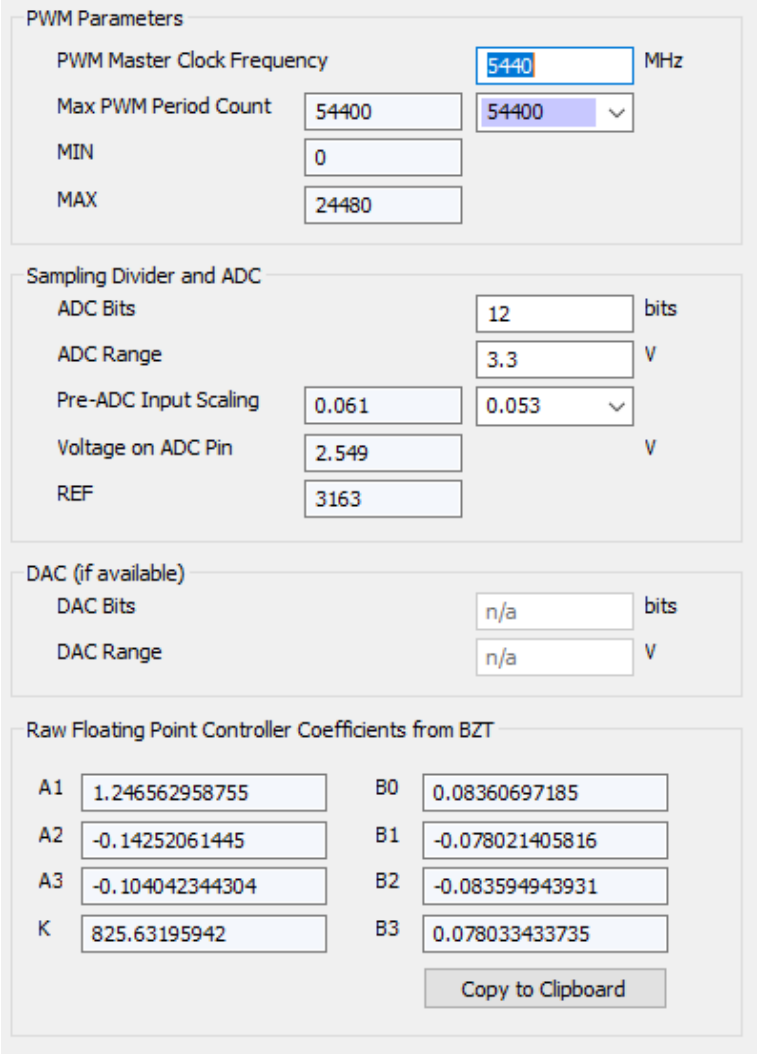


Step 6. The last configuration tab is [**digital (Non-Isolated)**]. Enter the specification given below.

Table 28. Digital (Nonisolated) Parameters

Digital (Non-Isolated) Tab parameter	Value
PWM master clock frequency	5440 MHz
Max PWM period count	54400
ADC bits	12
ADC Range	3.3 V
Pre-ADC input scaling	0.053

Figure 72. ST WDS digital (Nonisolated) Tab



Step 7. Now that the controller coefficients have been calculated, these can be copied to the clipboard by clicking the [**Copy to Clipboard**] button such that they can be pasted into the code.

The coefficients within the code are located in the “app_dpower.h” file. The following coefficients should now be on your clipboard:

```
#define B0 (+0.083606971850)
#define B1 (-0.078021405816)
#define B2 (-0.083594943931)
#define B3 (+0.078033433735)
#define A1 (+1.246562958755)
#define A2 (-0.142520614450)
#define A3 (-0.104042344304)
#define K (+825.631959418423)
#define REF (3163)
#define DUTY_TICKS_MIN (0)
#define DUTY_TICKS_MAX (24480)
```

These are the voltage loop coefficients that are used within the example application.

9 Getting started

9.1 2 kW AC-DC PSU modes of operation.

Operational modes for the AC-DC PSU are as described in the following section. Selection of modes other than the default (Mode 1) requires the explicit selection of the mode required by changing defines in the code (e.g. #define LOW_VOLTAGE), recompiling and reflashing the MCU. To reconfigure into a different mode, the AC-DC PSU needs to be powered OFF, the MCU reflashed, and then powered ON.

9.1.1 Operational mode 1 – Boost PFC operation, AC input 48 V DC output.

Boost PFC stage derives its power from the 90 to 265 Vrms, 50 / 60Hz AC input, boosting to 410 V DC (nom) and operating the phase shifted full bridge converter and synchronous rectifier stage to deliver 48 V DC (nom) at up to 2 kW from J2.

This is the default mode of operation.

9.1.2 Operational mode 2 – Boost PFC operation, AC input, 400V DC ‘tap-off’ no 48V DC output.

Boost PFC stage derives its power from the 90 to 265 Vrms, 50 / 60Hz AC input, boosting to 410 V DC (nom) and allowing the power to be drawn from the bidirectional port J21.

In this mode the phase shifted full bridge converter and synchronous rectifier stage is not operating and there is no power available on the output connector J2.

9.1.3 Operational mode 3 – Boost PFC operation, AC or DC input, ‘tap-off’ of a reduced power DC output.

Boost PFC stage derives its power from a reduced input in the range of 35 to 40Vac or 50-55Vdc, to power the boost PFC stage. The boost PFC stage output is at a reduced level of 60 V DC and this can be ‘tapped off’ from J21.

In this mode the phase shifted full bridge converter and synchronous rectifier stage is not operating and there is no power available on the output connector J2.

9.1.4 Operational mode 4 – NO Boost PFC operation, External DC input full power 48 V DC output.

AC-DC PSU derives its power from the external bidirectional port J21 and operates the phase shifted full bridge converter and synchronous rectifier stage to deliver 48 V DC (nom) at up to 2 kW from J2.

In this mode, the boost PFC stage is disabled.

9.1.5 Operational mode 5 – NO Boost PFC operation, External DC input reduced power 60 V DC output.

AC-DC PSU derives reduced power (50-60Vdc) from the external port (J21) and operates the phase shifted full bridge converter and synchronous rectifier stage to deliver 4.8 V DC at up to 100 W from J2.

In this mode, the boost PFC stage is disabled.

9.1.6 Undocumented operational modes

Any attempted operation of the AC-DC PSU outside of the above-described modes will result in indeterminate operation and shall be avoided.

9.1.7 User modified firmware modes of operation

It is possible for the user to alter the firmware to set up modes of operation different to those described herein. Any such modifications will need to be carefully considered and are at the user’s risk.

9.2 AC-DC PSU test operation – general configuration

For purposes of the test, the AC-DC PSU will be considered as a single complete design encompassing both the STEVAL-ISA172V3 2 kW - CCM interleaved PFC AC-DC and STEVAL-ISA172V3 2 kW - PSFB DC-DC application notes.

As well as the high voltage, high power AC input mode (up to 2 kW), the AC-DC PSU can operate in low power, low voltage mode, either from an AC source or DC source. By utilizing the AC input [J2] or bidirectional port [J21], and configuring an appropriate test mode, it is possible to test each stage separately.

Table 29. Configurable AC-DC operation modes

Mode	Input voltage J2	Input voltage J21	AC or DC input?	Output voltage J21	Output voltage J3	Power Level
1	90-265cVac ⚠	N/A	AC	N/A(1) ⚠	48 V DC	Up to 2 kW
2	90-265cVac ⚠	N/A	AC	400 V DC ⚠	N/A	Up to 2 kW
3	35 – 40cVac 50-55cVdc	N/A	AC or DC	N/A(1) ⚠	4.8 V DC	Up to 100 W
4	N/A	400cVdc ⚠	DC	N/A	48 V DC	Up to 2 kW
5	N/A	50 – 60cVdc	DC	N/A	5 V DC	Up to 100 W

1. *Voltage is present but not intended for use.*

9.2.1 AC-DC PSU test operation – prerequisites

It is assumed that the operator is competent in the use of electrical / electronic test equipment and is familiar with relevant safe operating procedures in relation to use of voltages up to and including 450 V DC.

It is recommended that the user fully familiarize themselves with the contents of both application notes [STEVAL-ISA172V3 2 kW - CCM interleaved PFC AC-DC and STEVAL-ISA172V3 2 kW - PSFB DC-DC].

Operation of the AC-DC PSU shall only be permitted in a dry lab environment and that all electrical connections be made using insulated connectors with no exposed conductors.

Use of current limited power sources with suitable RCD protection is recommended.

Prior to connecting the AC-DC PSU to any electrical connection, ensure that all the screws and fittings are secure and that there are no loose parts or FOD in the unit.

Ensure that a risk assessment has been performed, documented, and reviewed. It is recommended that no solo-working is permitted when working on voltages above SELV.

Connections between the laptop and the digital controllers should use the isolated USB in circuit debugger, ST-LINK/V2-ISOL shown in Figure 73.

Ensure the laptop that connects to the digital controller board (STEVAL-DPSG474M) and is configured with the correct IDE and firmware versions for the controllers (see EVM website for latest firmware revision information).

Figure 73. ST-LINK/V2 isolated USB in circuit debugger



9.2.2 Initial low power operation – Mode 3, Low Voltage DC input and Low Voltage DC output

Initial testing of the AC-DC PSU will be at a reduced power level – Mode 3, and uses a low voltage DC input. In this mode, the output voltage of the PSU will be 4.8 V DC and during operation,

9.2.3 Initial connection checks

Refer to the general test configuration in Figure 74.

Step 1. Connect the AC-DC PSU to a 55V DC, current limited supply – max 2A (do NOT turn on at this point).

Step 2. Connect a 10 W (2.5 Ω) load to J21 and the output of the AC-DC PSU. These loads can be fixed resistors or electronic loads, but must have sufficient power capacity to safely dissipate the electrical power / heat.

Step 3. Connect a digital voltmeter (or DMM configured appropriately) across J21 and the DC output J2.

Step 4. Connect the laptop to the digital Controllers using the isolated USB in circuit debugger ST-LINK/V2.

Figure 74. AC-DC PSU general test configuration – DC input test mode

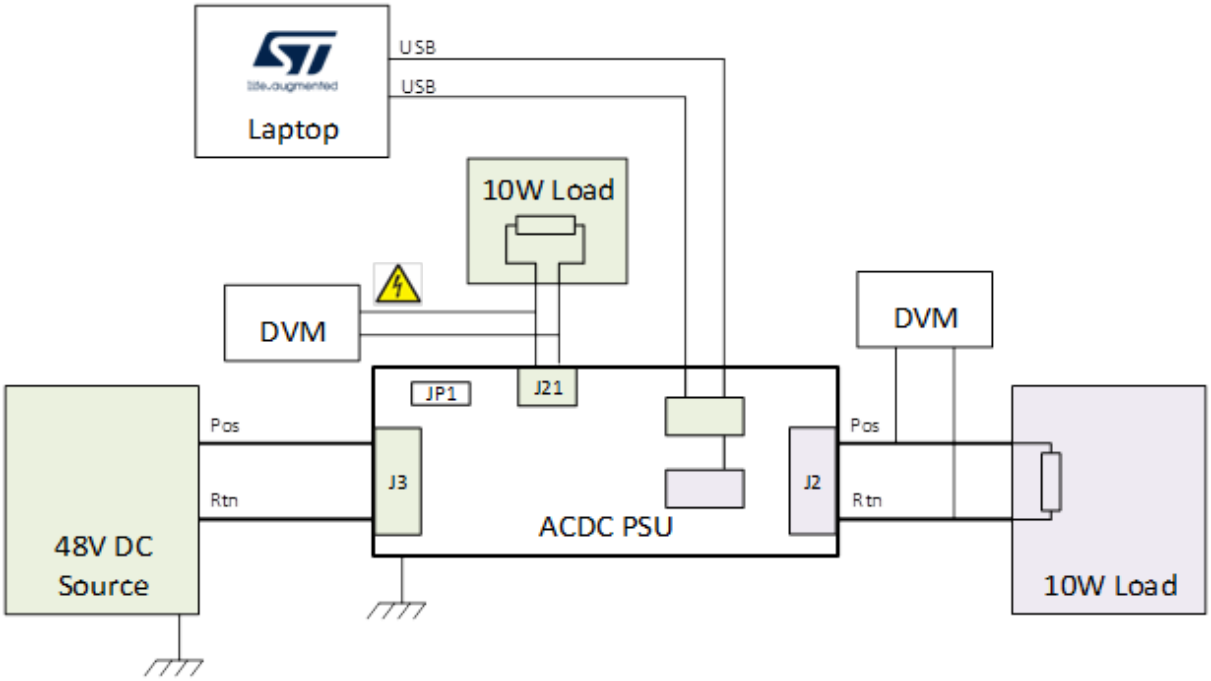


Table 30. AC-DC PSU test configuration electrical connections

Connection	Signal	Schematic signal name	Notes
J3 pin 1	55 V DC positive	LIVE*	AC or DC input (mode dependent)
J3 pin 3	55 V DC return	NEUTRAL*	AC or DC input (mode dependent)
J2 pin 1, 2	5 V DC output	VOUT_SENSE	DC output
J2 pin 3, 4	5 V DC return	GND2	DC output

9.2.4 Initial power up – Boost PFC stage, 60 V DC output

Step 1. With the connections as described above, enable the 55V DC electrical power source.

Step 2. Confirm the current demand is no greater than 500 mA.
The boost PFC stage will begin to operate.

Step 3. Confirm the DVM connected to J21 displays 60 V DC.

Step 4. Ensure that the current drawn from the DC source does not exceed 1A. If the current drawn is higher, switch OFF the 55V DC source and check the test configuration.

9.2.5 Measuring Boost PFC stage, 60 V DC output

Step 1. Observe the DVM indicating ~60 V DC present on the AC-DC PSU output.
If an electronic load with a current meter is used, a figure of ≈500 mA should be displayed.

Step 2. Increase the load on the PFC stage of the PSU by reducing resistance of the load at J21– up to a maximum of 60 W (1A) and confirm that the output stays within limits.

9.2.6 Noise and ripple measurement of the Boost PFC output

Configuring an oscilloscope to display the AC content of the output will allow the noise and ripple to be measured.
Recommended method: 100 MHz oscilloscope

Step 1. Select AC coupled on measuring channel.

Step 2. Reduce amplitude of channel to 100 mV / division (adjust as necessary during measurement).

Step 3. Set time base of channel to 100 µs / division (adjust as necessary during measurement).

Step 4. Connect oscilloscope probe center to positive output (J21 pin 1) as close to output as possible; probe negative to return (J21 pin 2).

Step 5. Measure and confirm the level of noise and ripple on the 60V DC output.

Note: It may be necessary to increase the time base (20 0µs, 500 µs, 1 ms) to display any voltage ripple as the frequency of the ripple is likely to be lower than the noise content.

9.2.7 Initial power up – Phase Shift Full bridge converter stage, 4.8 V DC output

With the boost PFC stage operating (as described above), perform the following:

Step 1. Set power demand on the J21 (60 V DC) output to 10 W.

Step 2. Confirm the current demand is no greater than 500 mA.
The phase shift full bridge stage will begin to operate.

Step 3. Confirm the DVM connected to J3 displays 4.8 V DC.

Step 4. Ensure that the current drawn from the DC source does not exceed 1 A.
If the current drawn is higher, switch OFF the 55 V DC source and check the test configuration.

9.2.8 Measuring DC output

Step 1. Observe the DVM indicating ~4.8 V DC present on the AC-DC PSU output.
The lengths of the connections between the output of the AC-DC PSU and the load / DVM will affect the voltage reading.

Step 2. Increase the load on the AC-DC PSU up to a maximum of 48 W by reducing resistance of the load on the main 4.8 V output J2, and confirm that the output voltage remains within limits.

9.2.9 Noise and ripple measurement of the Phase Shift Full bridge output

Configuring an oscilloscope to display the AC content of the output will allow the noise and ripple to be measured.
Recommended method: 100 MHz oscilloscope,

Step 1. Select AC coupled on measuring channel.

Step 2. Reduce amplitude of channel to 100 mV / division (adjust as necessary during measurement).

Step 3. Set time base of channel to 100 µs / division (adjust as necessary during measurement).

Step 4. Connect oscilloscope probe center to positive output (J2 pin 1) as close to output as possible; probe negative to return (J2 pin 3).

Step 5. Measure and confirm the level of noise and ripple on the PSFB PSU output.

Note: It may be necessary to increase the time base (200 µs, 500 µs, 1 ms) to display any voltage ripple as the frequency of the ripple is likely to be lower than the noise content.

9.2.10 Turn-off and reconfiguration

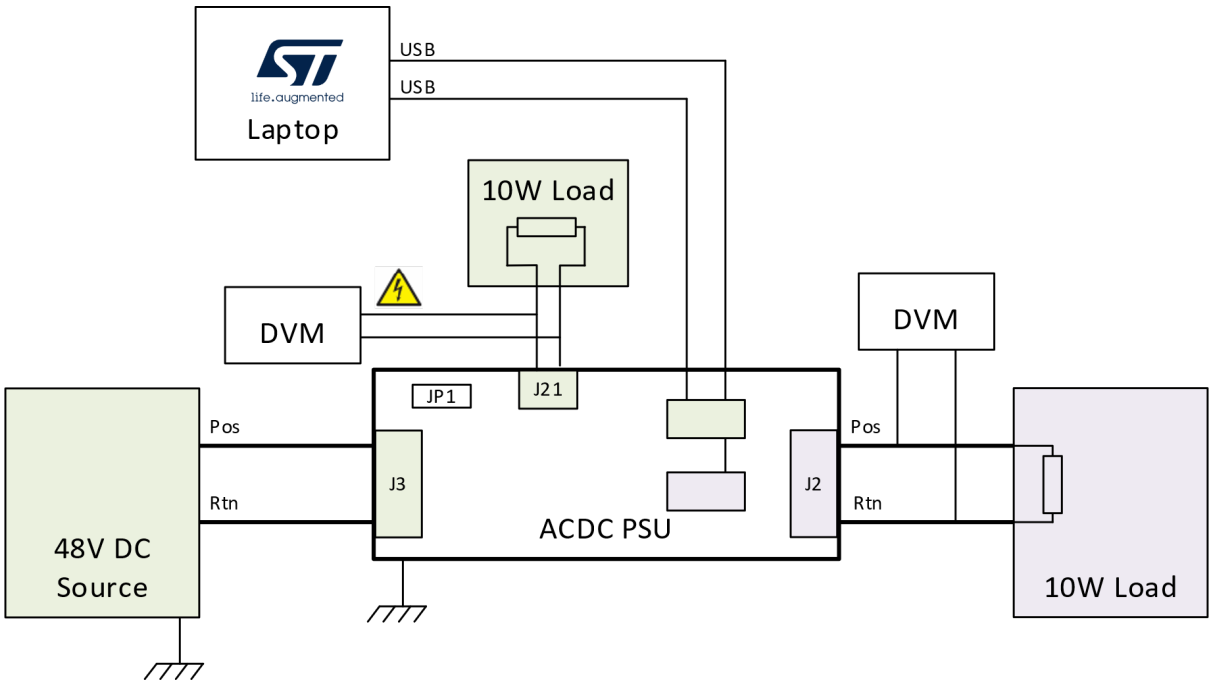
Step 1. Disable the DC source and reconfigure the test environment as necessary.

Operation of the AC-DC PSU in other modes will require the hardware and firmware to be reconfigured, refer to the previous section for the different modes of operation.

9.3 Operation of the AC-DC PSU in Mode 1 – default, 230Vac input, 48 V DC output up to 2 kW

General configuration of the AC-DC PSU operating in mode 1 – default.

Figure 75. AC-DC PSU general test configuration – AC input mode 1



9.3.1 Initial connection checks

Step 1. Connect the AC-DC PSU to a 90-265 V AC current limited supply – max 10 A for 230 Vac input (do not turn ON at this point).

Step 2. Connect a variable load, initially set to 48 W (or 1 A), to the output of the AC-DC PSU. Ensure that the load has sufficient power capacity to safely dissipate the electrical power/heat.

Step 3. Connect a volt meter (or DMM configured appropriately) across the DC output.

Table 31. AC-DC PSU test configuration electrical connections

Connection	Signal	Schematic signal name	Notes
J3 pin 1	90-265 V AC live	LIVE*	AC input (mode dependent)
J3 pin 3	90-265 V AC neutral	NEUTRAL*	AC input (mode dependent)
J2 pin 1, 2	48 V DC output	VOUT_SENSE	DC output
J2 pin 3, 4	48 V DC return	GND2	DC output
J21 pin 1	400 V DC output	VBUS	PFC boost output (400 V DC)
J21 pin 2	400 V DC return	GND1	PFC boost output (400 V DC)

9.3.2 Power up of Boost PFC stage, 90-265 V AC input, 400 V DC output

Step 1. With the connections as described above, enable the 90-265 V AC power source.

Step 2. After the PFC bulk caps have charged, confirm that the current demand is no greater than 500 mA.

Step 3. Confirm the DVM connected to J21 displays 400 V DC .

9.3.3 Power up of Phase Shift Full bridge converter stage, 90-265 V AC input, 48 V DC output

Step 1. With the boost PFC stage operating (as described above), confirm the DVM connected to J3 displays 48 V DC.

Step 2. Ensure that the current drawn from the AC source does not exceed 0.5A. If the current drawn is higher, switch OFF the 90-265V AC input and check the test configuration.

9.3.4 Measuring 48 V DC output

Step 1. Observe the DVM indicating ~48 V DC present on the AC-DC PSU output. The lengths of the connections between the output of the AC-DC PSU and the load / DVM will affect the voltage reading.

Step 2. Increase the load on the AC-DC PSU by reducing resistance of the load – up to a maximum of 2 kW and confirm that the output voltage stays within limits.

9.3.5 Noise and ripple of the Phase Shift full bridge PSU output

Configuring an oscilloscope to display the AC content of the output will allow the noise and ripple to be measured.

Step 1. Recommended method: 100 MHz oscilloscope

Step 2. Select AC coupled on measuring channel,

Step 3. Reduce amplitude of channel to 100 mV / division (adjust as necessary during measurement),

Step 4. Set time base of channel to 100 µs / division (adjust as necessary during measurement),

Step 5. Connect oscilloscope probe center to positive output – as close to output as possible, probe negative to return

Step 6. Measure and confirm the level of noise and ripple on the AC-DC PSU output.

Note: It may be necessary to increase the time base (200 µs, 500 µs, 1 ms) to display any voltage ripple as the frequency of the ripple is likely to be lower than the noise content.

9.3.6 Load regulation of the AC-DC PSU

The AC-DC PSU does not use remote voltage sensing, so the voltage measured across the load as it increases will drop proportionately. This effect can be minimized by connecting the DVM as close to the output of the AC-DC PSU as practical, ideally directly to the pins of J2.

9.4 Runtime configuration

When the project has been generated using STM32CubeMX, there should be minimal configuration required by the user within the IDE. Any changes made manually to autogenerated functions will be overwritten the next time the user regenerates the code within STM32CubeMX.

Only code located within `/*USER CODE … BEGIN */` and `/*USER CODE … END */` tags, or in custom user added files, will persist.

9.4.1 User modalities

The app_dpower.h file contains a set of defined user modalities. These modalities determine the operation of the converter and can be used to help debug or verify correct operation. The following table details the list of user modalities along with a brief description of their function.

Although these settings can be added in or commented out manually for debugging purposes, the persistent behavior should be configured by modifying the parameters using the X-CUBE-DPower pack via STM32CubeMX.

Table 32. User modalities

User modality	Description
START_WITHOUT_COMMAND	DCDC_State initialized at DCDC_INIT so the converter can start without waiting for a command. Primary communication is still checked and could override.
START_WITHOUT_PRIMARY_COMMUNICATION	Primary communication is checked but does not prevent the DCDC from starting up (e.g., in the case of low PFC bus voltage).
SYNCH_RECTIFICATION	Enables PWM output and PWM duty update for the synchronous rectifiers. Comment out if synchronous rectifiers are not used.
FULL_WAVE	Enables 4 PWM outputs for full-wave synchronous rectification. With this mode commented out, the synchronous rectification will have two outputs (i.e., assuming a current-doubler configuration).
ADAPTIVE_DEADTIME	Enables calculation and update of the dead time for the primary side PWM outputs to ensure ZVS across the widest possible load range. The calculation of the dead time may require adapting for your application. Comment out if not used.
ACTIVE_CLAMP	Enables the active clamp output. Active clamp is implemented to reduce voltage overshoot/ringing across secondary side rectifiers. Comment out if an active clamp is not used.
PWM_ACTIVE_CLAMP_TYPEII	Enables the Type II version of the active clamp. Type II is used with full-wave synchronous rectification and where there is only one clamp PWM output. With this commented out, there will be two active clamp outputs.
FAN_USAGE	Enables the fan output.
FAN_PWM_DRIVING	Enables speed control of the fan output.
OUT_VOLTAGE_BURST_MODE	Enables burst mode for light loads (i.e. PWM shuts down for periods providing pulse skipping).
OVERCURRENT_PROTECTION	With overcurrent protection enabled, the primary side PWM outputs will shut down in the event that the overcurrent threshold is passed.
OVERVOLTAGE_PROTECTION	With overvoltage protection enabled, the primary side PWM outputs will shut down in the event that the overvoltage threshold is passed.
SHORT_CIRCUIT_PROTECTION	With short circuit protection enabled, the primary side PWM outputs will shut down in the event that the minimum output voltage is not reached within a defined period of time.
OVERTEMPERATURE_PROTECTION	With overtemperature protection enabled, the primary side PWM outputs will shut down in the event that the overtemperature threshold is passed.
LOW_VOLTAGE	In low voltage mode, all inputs and outputs are divided by a factor of 10. This allows the PSU to be tested at low voltages in a safe manner to confirm correct operation.

User modality	Description
DEBUG_MODE	In debug mode, the 3p3z voltage and current loop controllers are not executed. The phase shift value must be set manually using the debugger.
DEBUG_COMP_OUT	This option enables the output of comparator 2 for debugging purposes.
DEBUG_BLANKING_WINDOW_OUT	This option enables the output of the blanking window used to ignore a portion of the current sense measurement during the primary side PWM period.
RUN_OPEN_LOOP	This option disables the controllers and forces the system to run in open loop mode.
PLOT_WAVEFORM	This option stores the selected waveform to an array for display in the IDE (plot view supported in IAR only).
USE_FMAC	This option uses the FMAC onboard the STM32G474 device to execute the 3p3z voltage loop controller.

9.5 Overall usage

The STM32 MCU control cards installed on the evaluation kit come preflashed with the example software. This example software implements the full functionality as described in this application note and the accompanying application note for the PFC stage. To reprogram the MCU card that controls the PSFB stage, the user must first compile the project associated with this application note.

The following dependencies are required to do this:

- PC with Windows 7 or later
  STM32 compatible IDE, such as STM32CubeIDE or IAR Embedded Workbench or Keil µVision
- STM32CubeMX (from v6.5.0) together with STM32Cube FW library for G4 (from v1.5.1) installed

To get started:

Step 1. Ensure that the any mains input is disconnected. There must be no voltage present on the board, all capacitors must have fully discharged. Check this with a DMM before connecting anything to the board.

Step 2. Connect the ST-LINK/V2 ISO debugger to the JTAG header on the PSFB control card.

Step 3. Apply 3.3 V to power the MCU via test pins TP46 (+3.3 V) and J7 (GND).

9.6 Loading the project

The PSFB example project for this EVM, as well as the associated ST WDS design files, are available within the digital Power pack, X-CUBE-DPOWER, for STM32CuebMX.

See https://www.st.com/content/st_com/en/ecosystems/stm32-digital-power.html for more information on this pack.

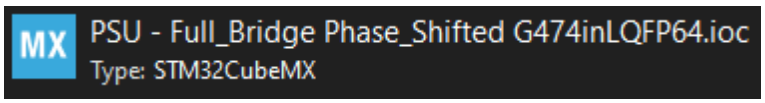
Step 1. With the pack installed, locate the example .ioc file from the pack's file references directory.

The directory is typically located in:
C:\Users\<user>\STM32Cube\Repository\Packs\STMicroelectronics\X-CUBE-DPower\<version>\CubeMX Files References

Step 2. Open STM32CubeMX by clicking on the [**steval-isa172v2-primary-cube-ide-g4-64pin.ico**] as shown below.

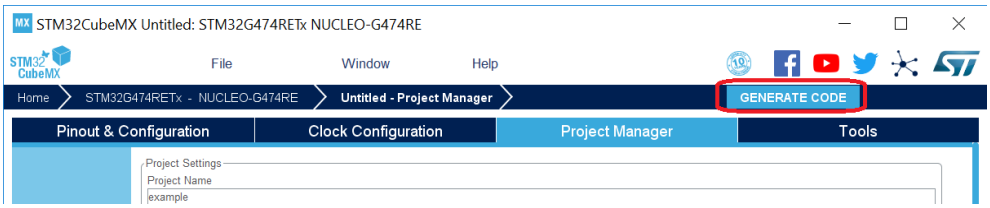
Note: The icon and the path may be different

Figure 76. PSFB example icon



Step 3. Generate the project by clicking the [**GENERATE CODE**] button in STM32CubeMX.

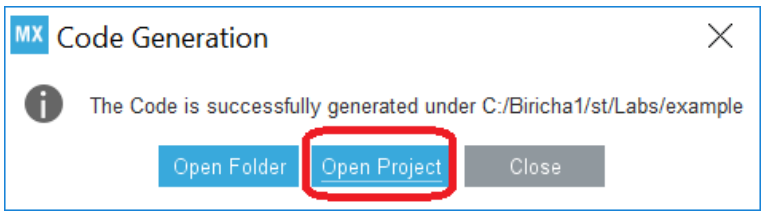
Figure 77. PSFB example code generation



This will generate the project for your selected IDE. In this case, it will be an STM32CubeIDE project.

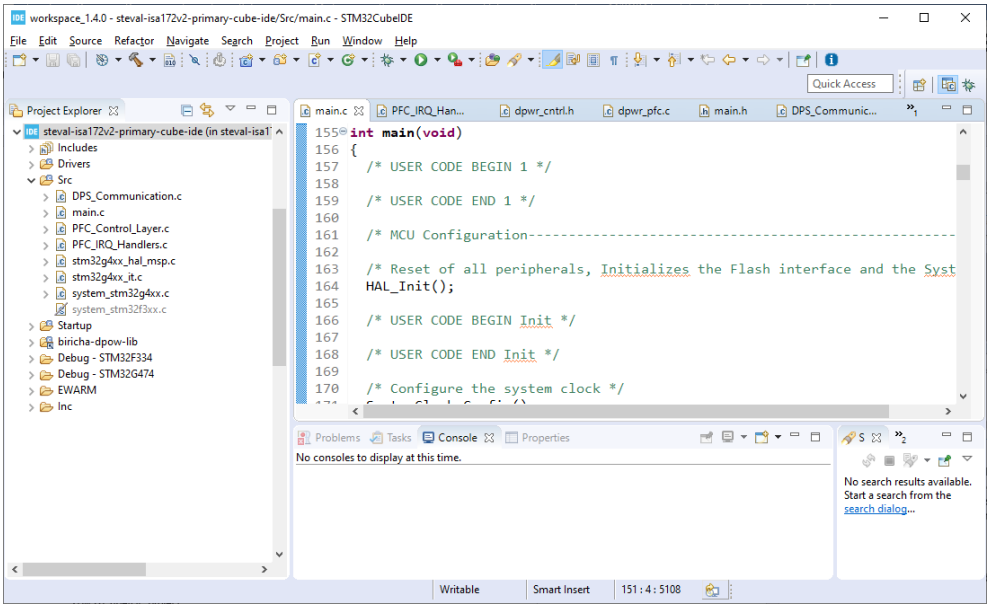
Step 4. When prompted with the dialog box, open the project by clicking [**Open project**].

Figure 78. PSFB example Open Project



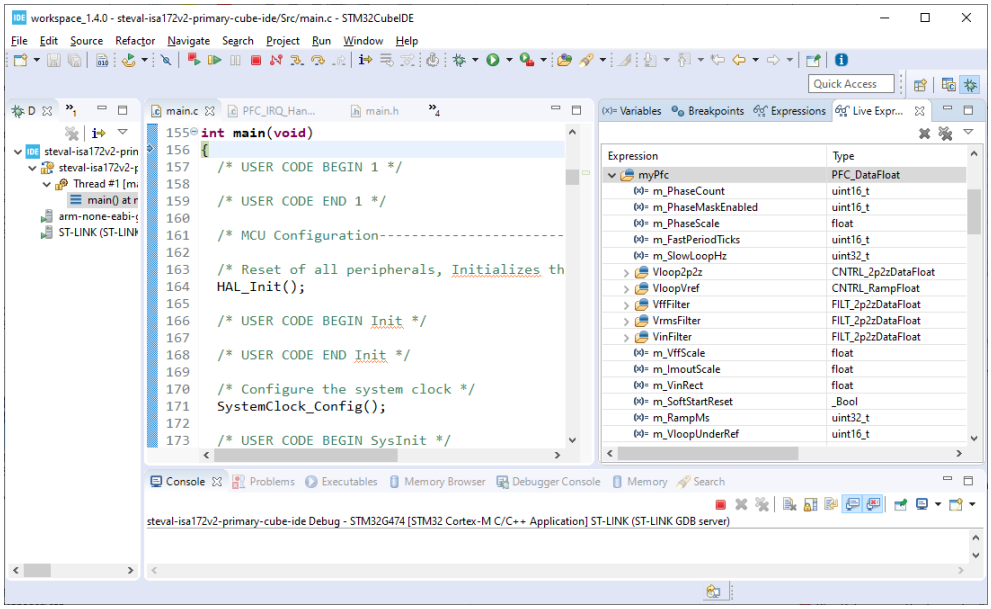
This will open STM32CubeIDE, or the IDE that you have selected under the [**Project Manager**] tab.

Figure 79. PSFB example open in IDE



Step 5. Inside the IDE, click the [**Debug**] icon that  will compile and download your code to the MCU. The code is now ready to run. The IDE will move the program counter to your *int main(void)* function.

Figure 80. PSFB example int main(void) function



Step 6. The buttons along the top menu bar have the functions described below. Click the [**Go**] button to run the code.

-  Resume – This runs the code
-  Suspend – This halts the code
-  Terminate – This terminates the debug session
-  Reset - This resets the MCU and sets the code start back to the beginning

Step 7. Click [**Terminate**]  to end the debug session.

The firmware has now been downloaded into the microcontroller flash and as such, the IDE can now be closed if the debugging features are not being used. The same program will restart each time power is applied to the MCU as it is running from the MCU flash.

Step 8. Close the IDE.

9.7 Low voltage operation

Before exercising the PSFB converter with a 400Vdc input from the PFC stage, it is prudent to check the switching waveforms and dead-time are correctly functioning. This check can be performed under low voltage operation. This means that an external 60 Vdc input is applied across the PFC bulk capacitance (the input to the PSFB converter) and the PSFB converter regulates a 4.8 Vdc output.

The example software has been written such that when the “LOW_VOLTAGE” compiler directive is defined the control loop will regulate to 4.8 Vdc and the converter will start operating without any primary side communications, as the PFC stage will not be running.

Note: IMPORTANT: Do not run the converter under “LOW_VOLAGE” operation when powered from the AC line or from a high voltage DC source. This should only be used when there is ≤60Vdc voltage present at the input of the PSFB stage to verify operation of the switches.

To run the PSFB converter under low voltage mode, locate and uncomment the line of code `#define RUN_OPEN_LOOP` in *app_dpower.h*.

10 Measured results

In this section the results of various tests that have been performed on the EVM hardware are presented. The tests are intended to verify the capabilities of the hardware and functionality of the software. The tests are by no means exhaustive, for example, a significant amount of environmental testing has been omitted, however the tests presented here cover some of the key tests that are typically performed when designing an AC-DC power supply.

The tests performed are as follows:

- Line and load regulation
- Efficiency
- Output voltage ripple/noise
- Output voltage transient response
- Output voltage loop response
- Over-voltage protection
- Thermals
- ADC ISR Timing durations

During these tests the PSU is operating under closed-loop control and, as there is an integrator within the control loop, there should be good load regulation. This means that the converter should respond to any changes in load and regulate such that the output voltage remains constant.

This can be tested by measuring the output voltage on the oscilloscope and varying the load using an electronic load. This process can then be repeated for the entire input voltage range of the AC-DC PSU. This allows the converters line regulation to be tested, meaning how the output voltage varies with changes in the line. In this case, as there is a PFC stage on the input boosting the input voltage to around 400Vdc, the output voltage should not change for different line voltages.

10.1 Line and load regulation

The line and load regulation, as well as power factor and efficiency are recorded across the entire output voltage and current range.

Table 33. Line and load regulation @ 230Vac, 48 V output

Test ID	Input voltage (source)	Input voltage (conn)	Input current (A)	Input Freq (Hz)	Input (Real) Power (W)	Input PF	Output voltage (V)	Output current (A)	Output Power (W)	Efficiency	Status
0	230	230.4	0.825	50	9.7	0.12	48.183	0	0	0.00%	PASSED
1	230	230.3	1.013	50	115.28	0.55	48.177	2.082	100.329	78.10%	PASSED
2	230	230.1	1.324	50	219.7	0.76	48.172	4.169	200.816	86.30%	PASSED
3	230	230.1	1.692	50	321.73	0.86	48.171	6.247	300.915	89.90%	PASSED
4	230	229.9	2.085	50	423.62	0.91	48.168	8.333	401.386	92.00%	PASSED
5	230	229.8	2.521	50	526.51	0.93	48.16	10.419	501.786	93.00%	PASSED
6	230	229.6	2.952	50	630.15	0.95	48.163	12.497	601.912	93.80%	PASSED
7	230	229.5	3.375	50	738.25	0.97	48.165	14.584	702.419	93.70%	PASSED
8	230	229.5	3.815	50	843.18	0.98	48.163	16.67	802.859	94.00%	PASSED
9	230	229.4	4.264	50	947.96	0.98	48.153	18.748	902.767	94.20%	PASSED
10	230	229.3	4.713	50	1053.26	0.98	48.156	20.834	1003.29	94.30%	PASSED
11	230	229.2	5.204	50	1163.64	0.98	48.153	22.92	1103.676	94.10%	PASSED
12	230	229.1	5.652	50	1269.26	0.99	48.15	24.998	1203.666	94.30%	PASSED
13	230	229.1	6.105	50	1375.85	0.99	48.15	27.084	1304.105	94.30%	PASSED
14	230	229	6.567	50	1485.09	0.99	48.148	29.171	1404.525	94.20%	PASSED
15	230	228.9	7.028	50	1592.13	0.99	48.146	31.249	1504.492	94.20%	PASSED
16	230	228.8	7.49	50	1699.2	0.99	48.137	33.337	1604.743	94.20%	PASSED
17	230	228.7	7.955	50	1807.08	0.99	48.13	35.415	1704.518	94.20%	PASSED
18	230	228.6	8.43	50	1915.97	0.99	48.127	37.501	1804.81	94.10%	PASSED
19	230	228.5	8.9	50	2024.47	0.99	48.118	39.587	1904.859	94.10%	PASSED
20	230	228.4	9.374	50	2133.11	1	48.11	41.666	2004.549	94.00%	PASSED

Table 34. **Line and load regulation @ 230Vac, 40 V output**

Test ID	Input voltage (source)	Input voltage (conn)	Input current (A)	Input Freq (Hz)	Input (Real) Power (W)	Input PF	Output voltage (V)	Output current (A)	Output Power (W)	Efficiency	Status
22	230	230.4	0.825	50	10.25	0.12	40.289	0	0	0.00%	PASSED
23	230	230.4	0.966	50	96.66	0.49	40.221	2.099	84.416	76.80%	PASSED
24	230	230.2	1.218	50	185.83	0.71	40.211	4.201	168.936	84.80%	PASSED
25	230	230.1	1.517	50	273.18	0.82	40.206	6.304	253.453	88.50%	PASSED
26	230	230.1	1.833	50	358.59	0.88	40.197	8.398	337.584	90.70%	PASSED
27	230	230	2.17	50	445.34	0.92	40.196	10.501	422.082	92.10%	PASSED
28	230	229.9	2.551	50	533.36	0.93	40.197	12.603	506.606	92.80%	PASSED
29	230	229.8	2.914	50	621.33	0.95	40.191	14.698	590.71	93.10%	PASSED
30	230	229.7	3.277	50	709.87	0.96	40.195	16.8	675.275	93.60%	PASSED
31	230	229.6	3.644	50	802.09	0.97	40.184	18.903	759.592	93.40%	PASSED
32	230	229.5	4.016	50	890.45	0.98	40.178	20.997	843.613	93.70%	PASSED
33	230	229.5	4.396	50	979.43	0.98	40.167	23.099	927.849	93.80%	PASSED
34	230	229.4	4.785	50	1069.32	0.98	40.169	25.202	1012.339	93.80%	PASSED
35	230	229.3	5.208	50	1164.14	0.98	40.166	27.296	1096.379	93.40%	PASSED
36	230	229.2	5.593	50	1254.73	0.99	40.159	29.399	1180.625	93.40%	PASSED
37	230	229.1	5.977	50	1345.26	0.99	40.157	31.501	1265.017	93.50%	PASSED
38	230	229.1	6.366	50	1437.69	0.99	40.145	33.606	1349.123	93.40%	PASSED
39	230	229	6.755	50	1528.47	0.99	40.141	35.698	1432.951	93.40%	PASSED
40	230	228.9	7.152	50	1620.62	0.99	40.144	37.803	1517.548	93.30%	PASSED
41	230	228.8	7.549	50	1712.81	0.99	40.137	39.905	1601.687	93.30%	PASSED
42	230	228.8	7.943	50	1804.12	0.99	40.136	42	1685.708	93.20%	PASSED

Table 35. **Line and load regulation @ 230Vac, 55 V output**

Test ID	Input voltage (source)	Input voltage (conn)	Input current (A)	Input Freq (Hz)	Input (Real) Power (W)	Input PF	Output voltage (V)	Output current (A)	Output Power (W)	Efficiency	Status
43	230	230.4	0.825	50	9.2	0.12	55.227	0	0	0.00%	PASSED
44	230	230.3	1.004	50	111.69	0.54	55.213	1.822	100.581	80.60%	PASSED
45	230	230.2	1.329	50	220	0.76	55.215	3.639	200.925	86.20%	PASSED
46	230	230.1	1.7	50	323.34	0.86	55.213	5.458	301.371	89.60%	PASSED
47	230	230	2.081	50	423.13	0.91	55.215	7.276	401.724	92.10%	PASSED
48	230	229.9	2.516	50	526.04	0.93	55.199	9.093	501.915	93.20%	PASSED
49	230	229.8	2.944	50	628.55	0.95	55.2	10.91	602.244	93.90%	PASSED
50	230	229.7	3.367	50	731.79	0.96	55.198	12.727	702.534	94.40%	PASSED
51	230	229.7	3.798	50	839.02	0.97	55.192	14.545	802.754	94.40%	PASSED
52	230	229.5	4.243	50	943.46	0.98	55.2	16.362	903.183	94.60%	PASSED
53	230	229.5	4.695	50	1048.9	0.98	55.198	18.188	1003.91	94.80%	PASSED
54	230	229.4	5.182	50	1158.29	0.98	55.189	20.005	1104.037	94.50%	PASSED
55	230	229.3	5.627	50	1263.23	0.99	55.184	21.822	1204.239	94.70%	PASSED
56	230	229.2	6.075	50	1368.73	0.99	55.188	23.637	1304.5	94.70%	PASSED
57	230	229.1	6.533	50	1476.22	0.99	55.181	25.457	1404.726	94.70%	PASSED
58	230	228.9	6.99	50	1582.74	0.99	55.181	27.272	1504.877	94.70%	PASSED
59	230	228.9	7.447	50	1689.6	0.99	55.177	29.091	1605.174	94.70%	PASSED
60	230	228.7	7.913	50	1796.48	0.99	55.179	30.909	1705.516	94.80%	PASSED
61	230	228.6	8.374	50	1903.66	0.99	55.18	32.726	1805.819	94.80%	PASSED
62	230	228.5	8.84	50	2011.05	1	55.167	34.551	1906.078	94.70%	PASSED
63	230	228.5	9.31	50	2118.65	1	55.166	36.369	2006.325	94.70%	PASSED

Table 36. **Line and load regulation @ 120Vac, 48 V output**

Test ID	Input voltage (source)	Input voltage (conn)	Input current (A)	Input Freq (Hz)	Input (Real) Power (W)	Input PF	Output voltage (V)	Output current (A)	Output Power (W)	Efficiency	Status
64	120	120.9	0.551	60	9.35	0.34	48.202	0	0	0.00%	PASSED
65	120	120.7	1.209	60	117.66	0.9	48.197	2.082	100.369	76.30%	PASSED
66	120	120.5	2.098	60	224.2	0.94	48.186	4.169	200.873	84.30%	PASSED
67	120	120.3	2.897	60	327.52	0.98	48.188	6.247	301.016	88.10%	PASSED
68	120	120.2	3.734	60	431.11	0.99	48.187	8.333	401.54	90.30%	PASSED
69	120	120	4.619	60	539.41	1	48.178	10.419	501.971	90.80%	PASSED
70	120	119.8	5.503	60	646.34	1	48.179	12.499	602.206	91.40%	PASSED
71	120	119.6	6.409	60	754.86	1	48.175	14.585	702.661	91.80%	PASSED
72	120	119.4	7.34	60	866.88	1	48.169	16.67	802.969	91.70%	PASSED
73	120	119.2	8.242	60	975.45	1	48.171	18.748	903.106	91.90%	PASSED
74	120	119	9.169	60	1086.79	1	48.167	20.836	1003.612	92.00%	PASSED
75	120	118.8	10.092	60	1197.24	1	48.167	22.92	1104.009	92.00%	PASSED
76	120	118.7	11.014	60	1307.33	1	48.161	25	1204.049	92.20%	PASSED
77	120	118.6	11.954	60	1419.86	1	48.164	27.084	1304.495	92.10%	PASSED
78	120	118.4	12.903	60	1532.97	1	48.155	29.173	1404.817	92.10%	PASSED
79	120	118.3	13.851	60	1646.02	1	48.157	31.249	1504.842	92.00%	PASSED

Table 37. **Line and load regulation @ 120Vac, 40 V output**

Test ID	Input voltage (source)	Input voltage (conn)	Input current (A)	Input Freq (Hz)	Input (Real) Power (W)	Input PF	Output voltage (V)	Output current (A)	Output Power (W)	Efficiency	Status
80	120	120.9	0.551	60	10	0.35	40.306	0	0	0.00%	PASSED
81	120	120.8	1.042	60	97.75	0.89	40.248	2.082	83.815	75.30%	PASSED
82	120	120.6	1.829	60	188.43	0.92	40.233	4.169	167.721	82.80%	PASSED
83	120	120.5	2.491	60	275.9	0.96	40.228	6.247	251.297	86.80%	PASSED
84	120	120.3	3.174	60	362.25	0.98	40.224	8.333	335.187	89.10%	PASSED
85	120	120.2	3.888	60	450.11	0.99	40.215	10.419	419.003	90.30%	PASSED
86	120	120	4.64	60	541.89	1	40.209	12.497	502.508	90.50%	PASSED
87	120	119.9	5.388	60	632.16	1	40.231	14.584	586.712	91.00%	PASSED
88	120	119.7	6.144	60	723.26	1	40.218	16.67	670.424	91.20%	PASSED
89	120	119.6	6.909	60	814.59	1	40.21	18.748	753.845	91.40%	PASSED
90	120	119.5	7.686	60	908.28	1	40.211	20.834	837.746	91.30%	PASSED
91	120	119.3	8.442	60	999.66	1	40.19	22.92	921.158	91.50%	PASSED
92	120	119.1	9.224	60	1093.46	1	40.194	25	1004.87	91.40%	PASSED
93	120	118.9	10.006	60	1187.01	1	40.178	27.084	1088.204	91.50%	PASSED
94	120	118.8	10.792	60	1280.94	1	40.174	29.173	1171.981	91.50%	PASSED
95	120	118.7	11.583	60	1375.3	1	40.165	31.249	1255.114	91.40%	PASSED

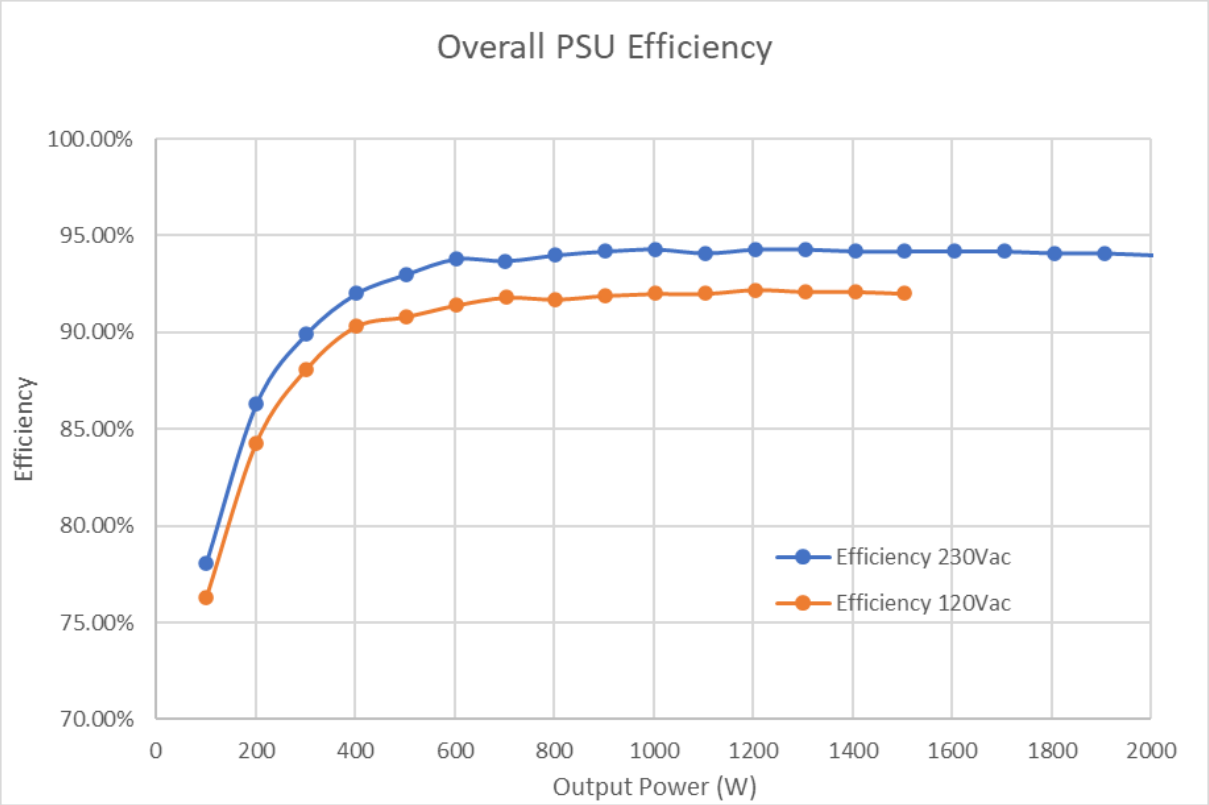
Table 38. **Line and load regulation @ 120Vac, 55 V output**

Test ID	Input voltage (source)	Input voltage (conn)	Input current (A)	Input Freq (Hz)	Input (Real) Power (W)	Input PF	Output voltage (V)	Output current (A)	Output Power (W)	Efficiency	Status
96	120	120.9	0.547	60	8.99	0.34	55.229	0	0	0.00%	PASSED
97	120	120.8	1.175	60	113.79	0.9	55.229	1.822	100.61	78.90%	PASSED
98	120	120.6	2.102	60	224.57	0.94	55.236	3.639	201.001	84.10%	PASSED
99	120	120.4	2.91	60	329.02	0.98	55.222	5.458	301.422	87.80%	PASSED
100	120	120.3	3.726	60	430.49	0.99	55.222	7.276	401.778	90.40%	PASSED
101	120	120.1	4.606	60	538.03	1	55.22	9.093	502.111	91.10%	PASSED
102	120	119.9	5.482	60	643.71	1	55.209	10.908	602.229	91.80%	PASSED
103	120	119.7	6.375	60	750.94	1	55.211	12.727	702.701	92.20%	PASSED
104	120	119.6	7.302	60	861.94	1	55.204	14.545	802.934	92.10%	PASSED
105	120	119.4	8.199	60	970.12	1	55.204	16.362	903.252	92.40%	PASSED
106	120	119.2	9.122	60	1081.16	1	55.202	18.188	1003.983	92.40%	PASSED
107	120	119	10.036	60	1190.62	1	55.192	20.005	1104.097	92.50%	PASSED
108	120	118.9	10.959	60	1300.49	1	55.195	21.822	1204.462	92.60%	PASSED
109	120	118.6	11.886	60	1411.5	1	55.184	23.639	1304.507	92.60%	PASSED
110	120	118.5	12.826	60	1523.17	1	55.189	25.457	1404.932	92.60%	PASSED
111	120	118.3	13.766	60	1635.9	1	55.182	27.272	1504.926	92.60%	PASSED

10.2 Efficiency

Peak efficiency at nominal output voltage is measured as 93.4% with a 1000 W load.
The highest overall efficiency is measured as 94.8% at 55 V output and a 1000 W load.
Note that the external fans are excluded during the efficiency test.

Figure 81. Overall PSU efficiency measured with 48 V output (nominal)



10.3 Output voltage ripple/noise

The output voltage ripple is measured using a standard oscilloscope probe across the output connector of the PSFB converter. Using a ripple and noise probe may reduce the measured noise further.

Table 39. Ripple/noise measurements

Load	Ripple/noise
1 kW	0.42% ripple/noise pk-pk
2 kW	0.52% ripple/noise pk-pk

Figure 82. **Ripple/noise measured at 1 kW (0.42% ripple/noise pk-pk)**

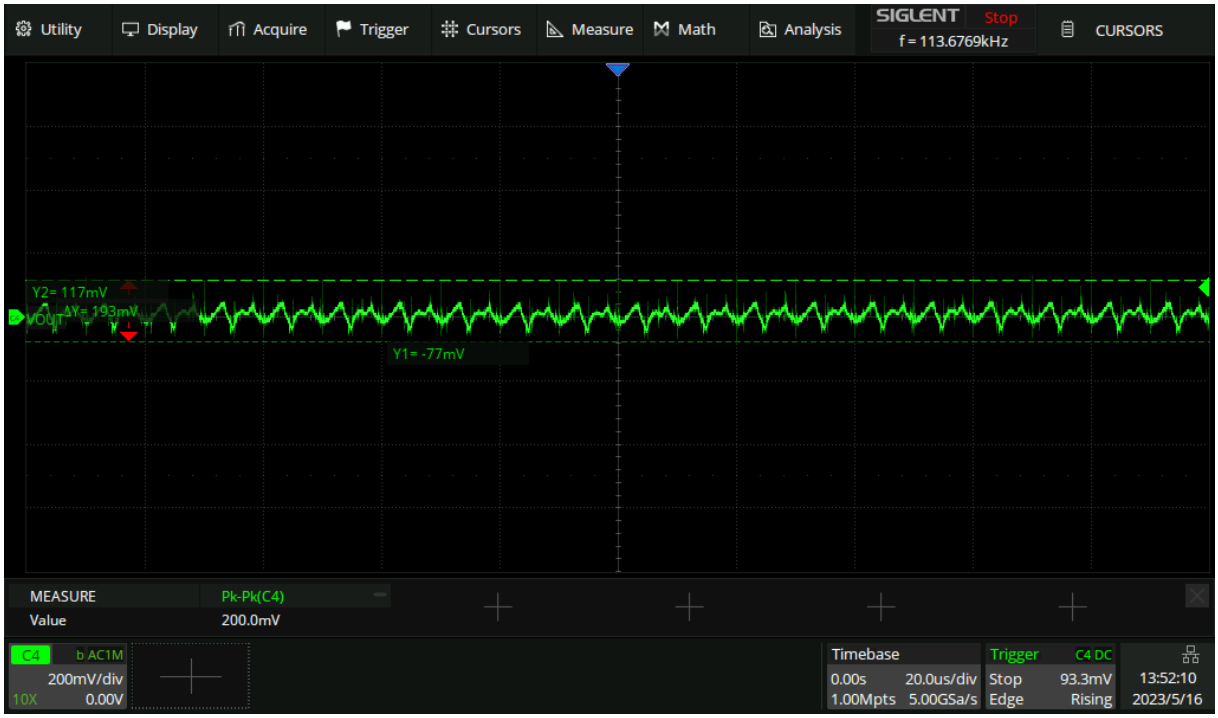
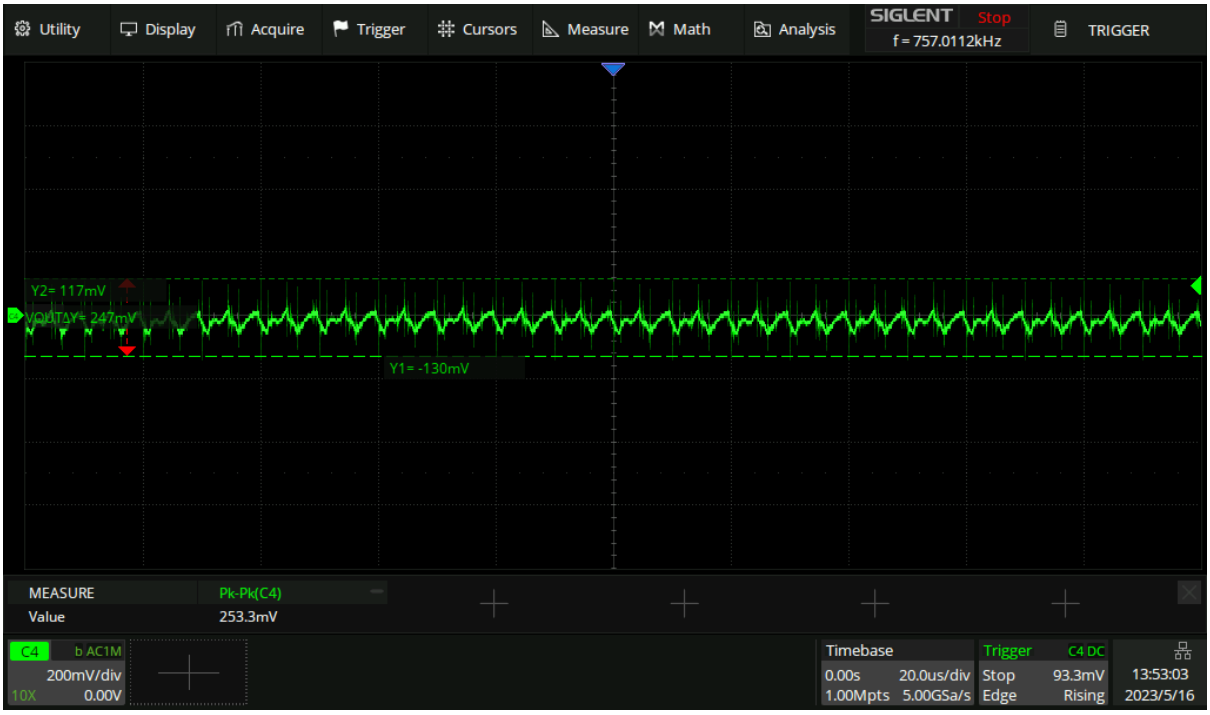


Figure 83. **Ripple/noise measured at 2 kW (0.52% ripple/noise pk-pk)**



10.4 Output voltage transient

The output voltage transient response is measured by applying a step load. The voltage drop and recovery time indicate the PSUs ability to recover from this transient. As discussed earlier in the application note, the transient response can provide useful information about the stability of the closed-loop system. The transient response of the PSFB converter can be measured by placing one oscilloscope channel on the output voltage and using another oscilloscope channel to measure the output current. The output voltage channel is AC coupled to see the deviation from the setpoint at the moment of the load transient.

Section 10.4: Output voltage transient shows the transient response for a step-change in load from 10% to 50%. The output voltage on Channel 4 deviates from the steady-state by <200 mV and recovers back to steady-state within 1 ms. Importantly, there is no ringing in the recovery. This is an indication that there is a sufficient phase margin in the loop to ensure stability.

It is prudent to check the transient response across a range of load conditions. In Figure 85. Transient response: 25% -> 75% (10.5A -> 31.5A), the transient response is shown for a step-change in load from 25% to 75%. This load step crosses the boundary over which the second phase of the interleaved CCM boost converter is enabled. Nonetheless, the output voltage only deviates <1.5% from the set point. A summary of the transient response tests is given in Section 10.4.

The transient response can provide some information about the stability of the system and how the system responds to a large signal disturbance. However, it does not provide all of the information necessary to quantify the stability of the system. This information can be obtained by measuring the frequency response of the converter. The frequency response measurement is presented in the next section.

Figure 84. Transient response: 10% -> 50% (4.2A -> 21A)

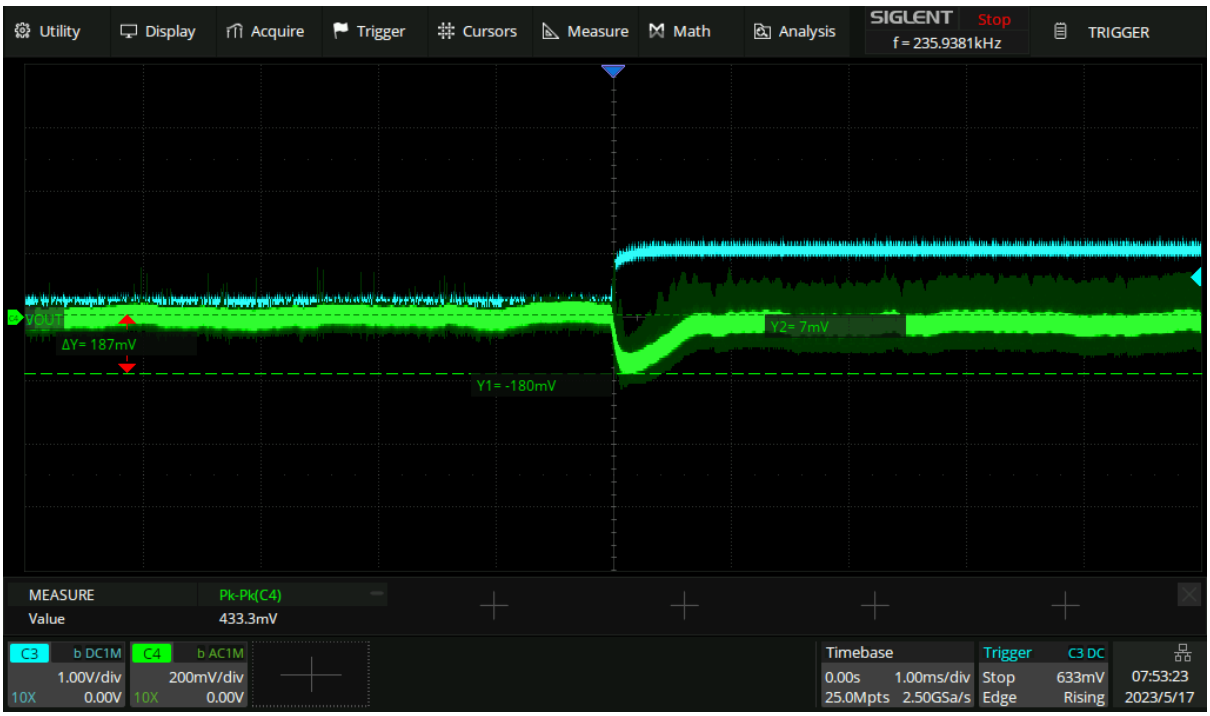


Figure 85. **Transient response: 25% -> 75% (10.5A -> 31.5A)**

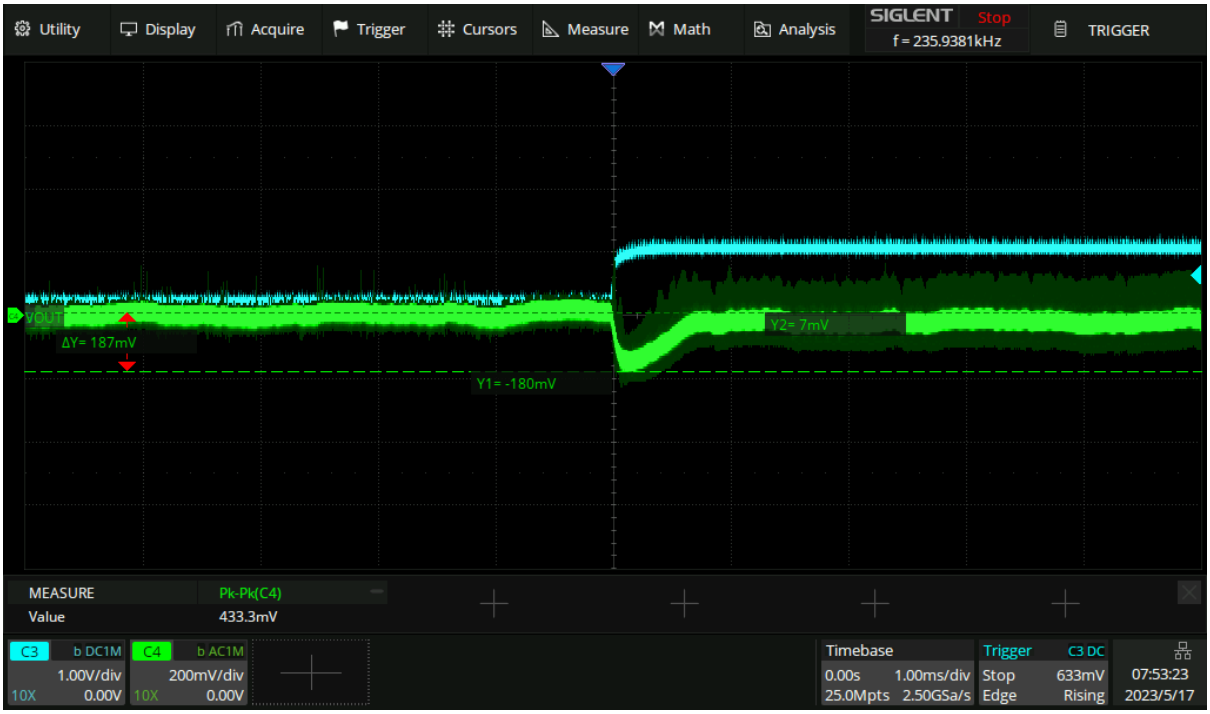
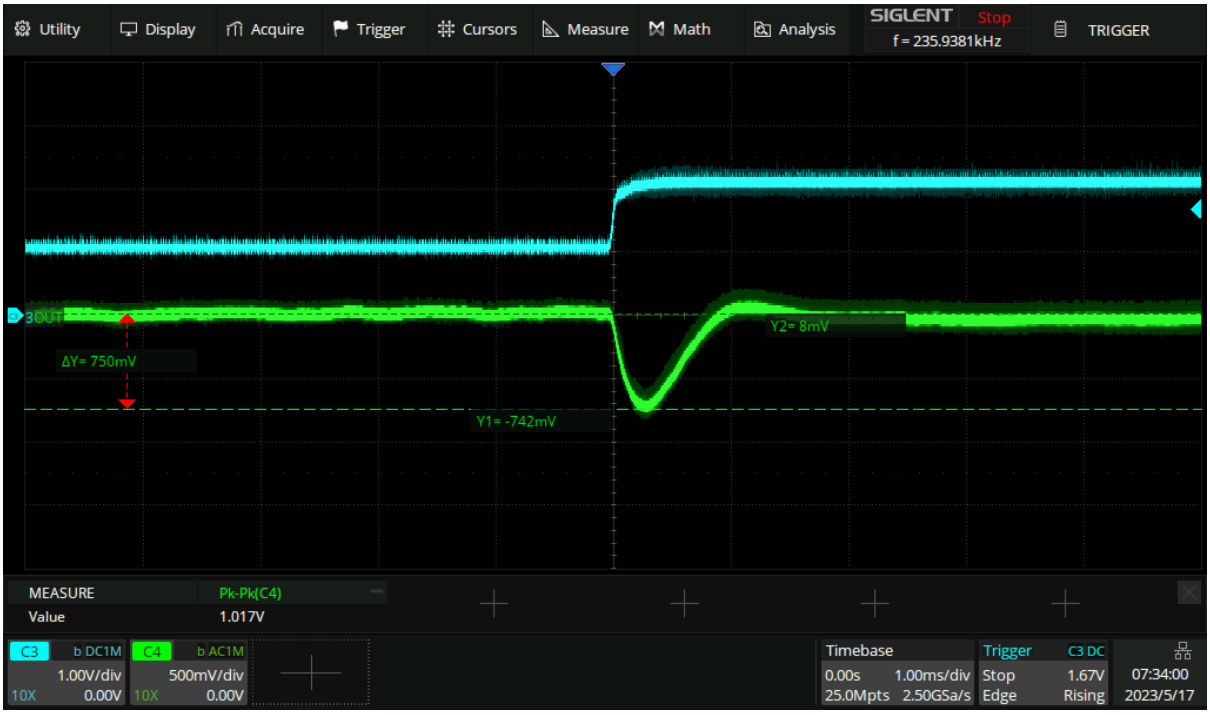


Figure 86. **Transient response: 50% -> 100% (21A -> 42A)**



The transient response summary is provided in the following table.

Table 40. **Transient response summary, 48 V output**

Load step	Undershoot	Settling time
10% -> 50%	0.38% (180 mV)	1 ms

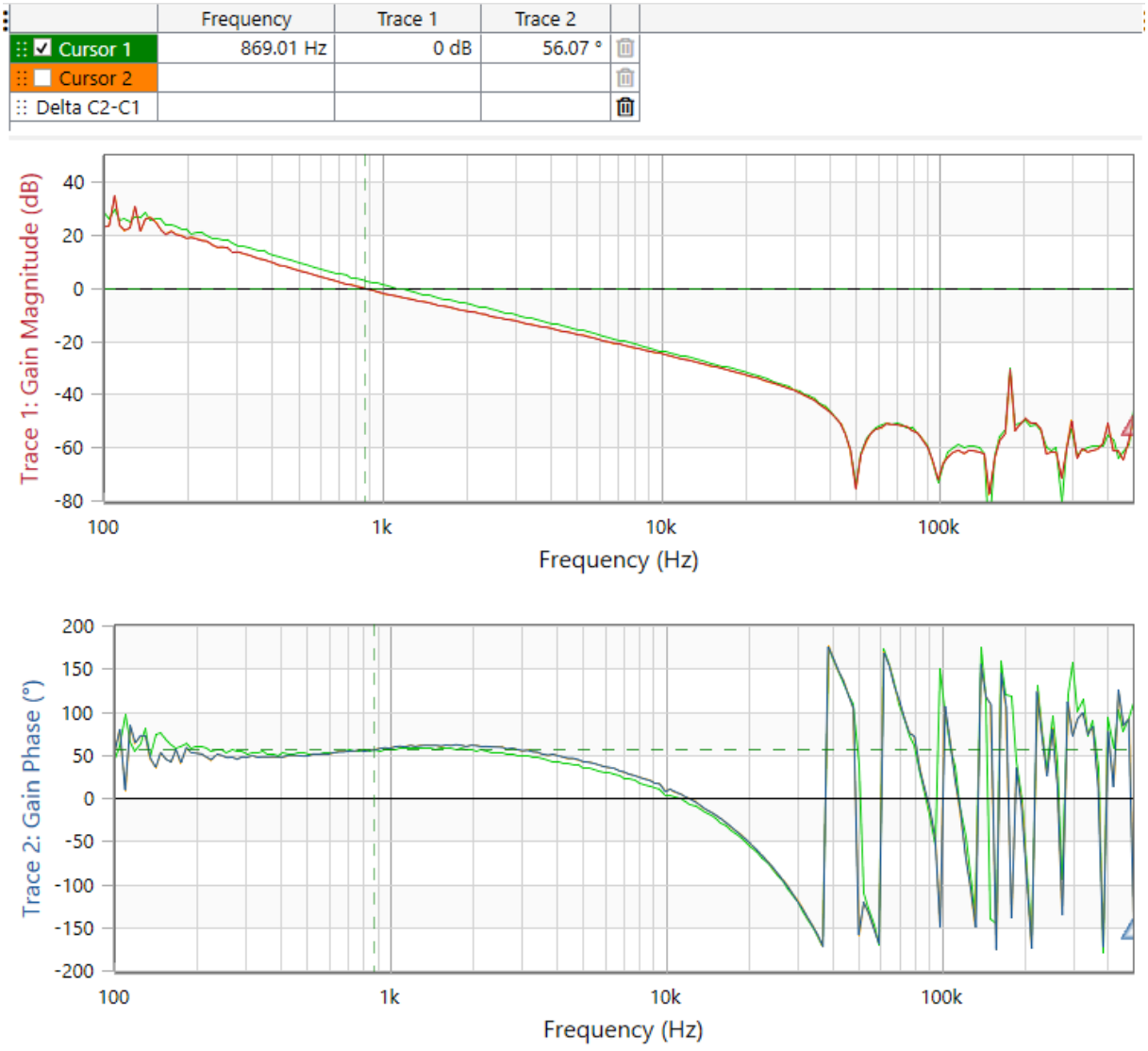
Load step	Undershoot	Settling time
25% -> 75%	1.4% (653 mV)	1.5 ms
50% -> 100%	1.55% (742 mV)	1.5 ms

10.5 Output voltage loop

Section 10.5 shows the measured control-to-output loop response of the PSFB converter at 100% load. A crossover frequency of 869Hz is measured which is close to the desired crossover frequency of 1kHz. A phase margin of 56° is achieved in the real measurement.

In Figure 88 the loop response of the PSFB converter at 50% load is measured. As expected, the overall loop response is very similar to that of the system at 100% load however there will be some changes as they dynamics of the system change as the load changes. Therefore, the crossover frequency and phase margin change slightly, and the system is still stable.

Figure 87. Loop response measured at 2 kW



break

Figure 88. **Loop response measured at 1 kW**

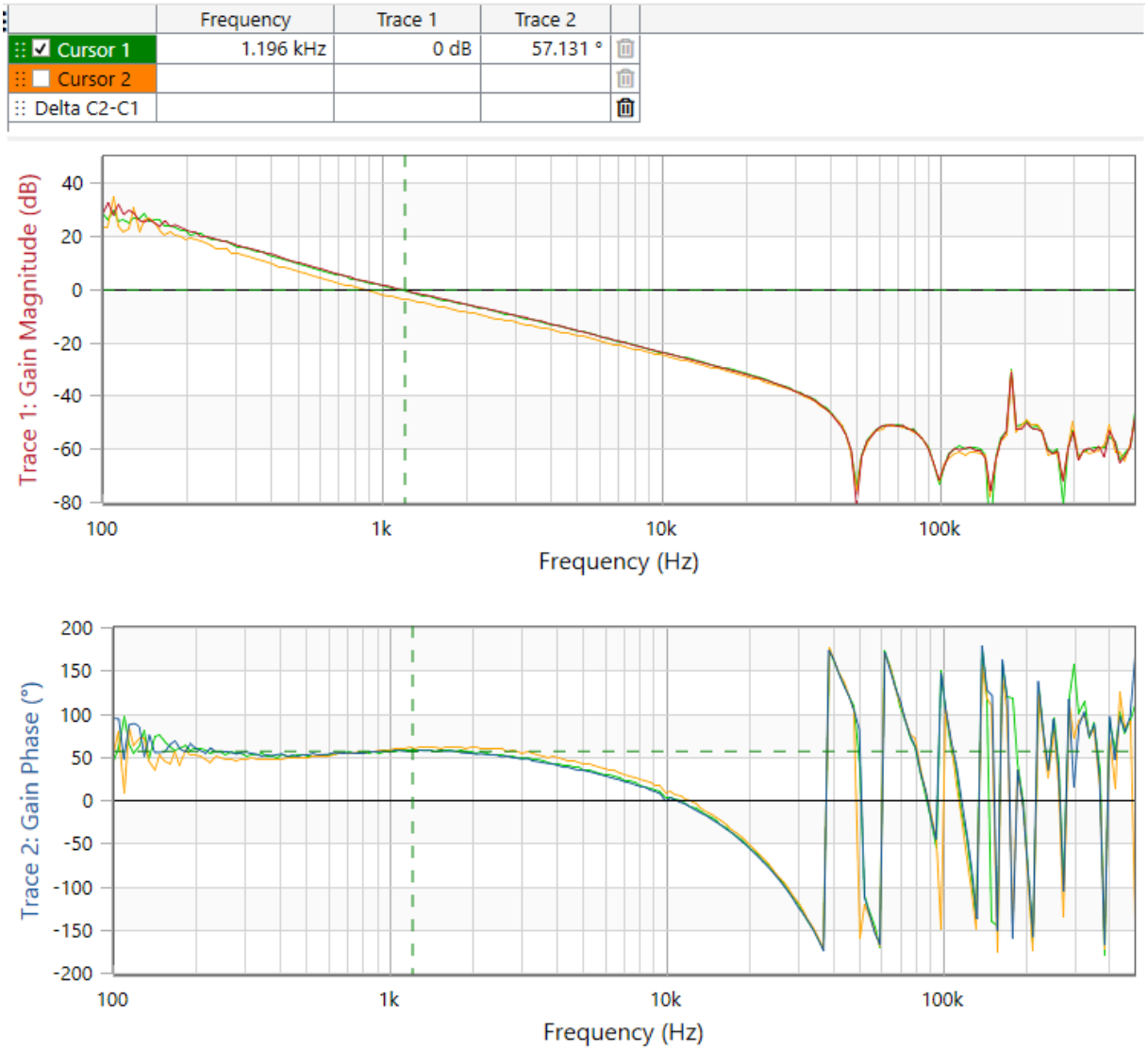


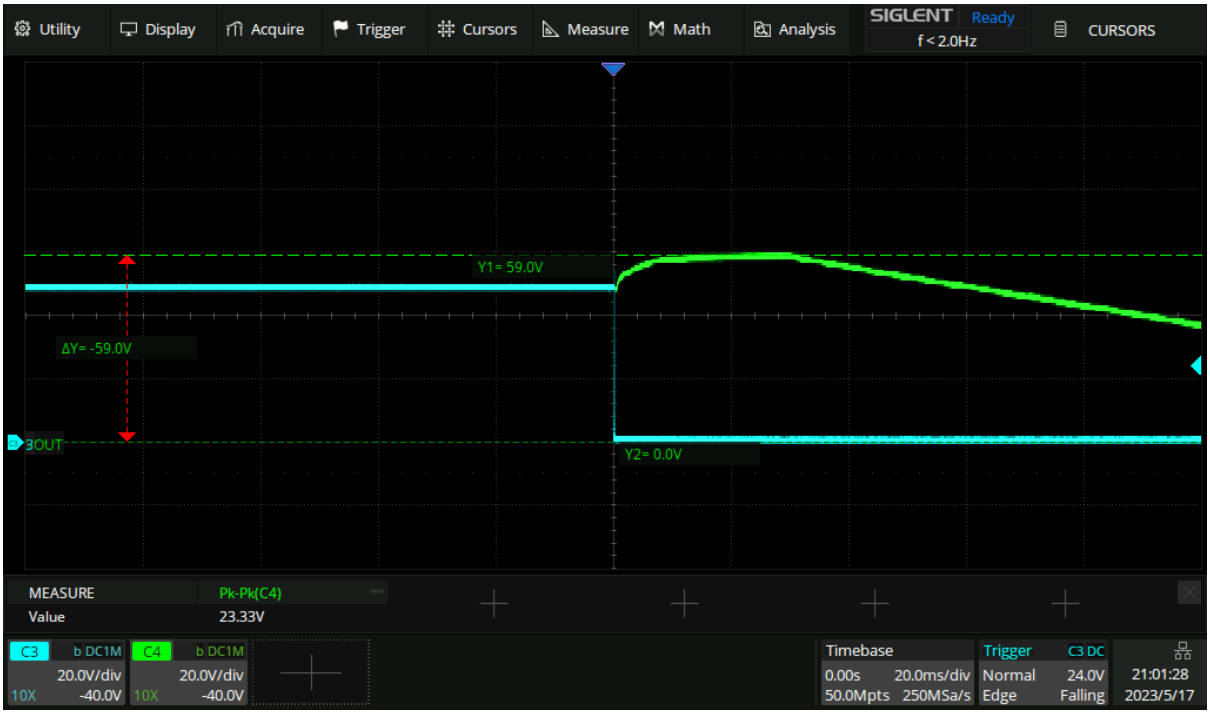
Table 41. **Output voltage loop measurement summary**

Load	Crossover	Phase margin
1 kW	1.12kHz	57
2 kW	0.86kHz	56

10.6 Overvoltage protection

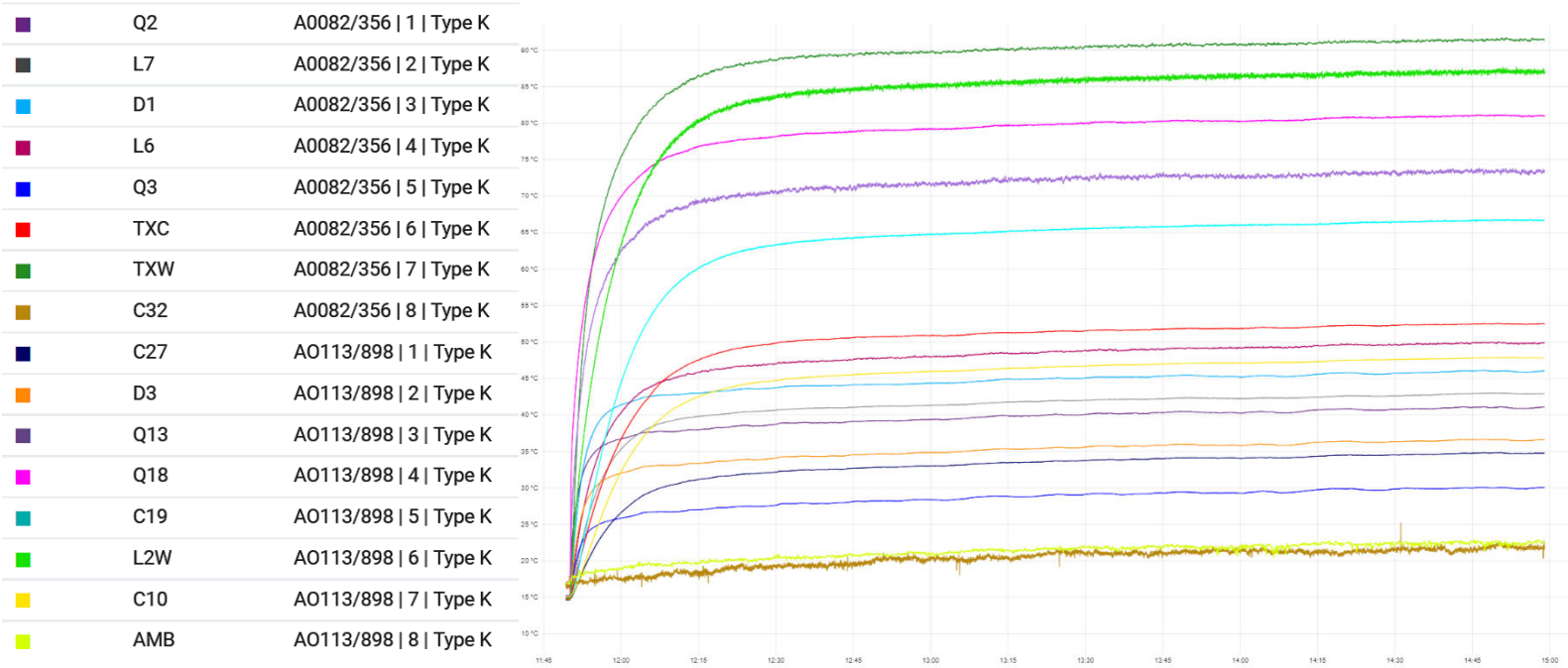
OVP set point is 59 V. Tested by disconnecting the Vout feedback network from the ADC – i.e. opening the control loop. A secondary feedback path for the output voltage triggers an external interrupt that then shuts down the converter.

Figure 89. **Overvoltage protection test**



10.7 Thermals

Figure 90. Thermal data from various key components. Recorded at 230Vac input, 2 kW output.



The hottest temperature recorded is 91°C on the secondary winding of the main power transformer. Ambient temperature averaged at 21°C. This means that maximum ambient of 50°C the secondary winding would reach 120°C, which is the maximum allowable working temperature for the insulation used within the transformer based on the derating rules.

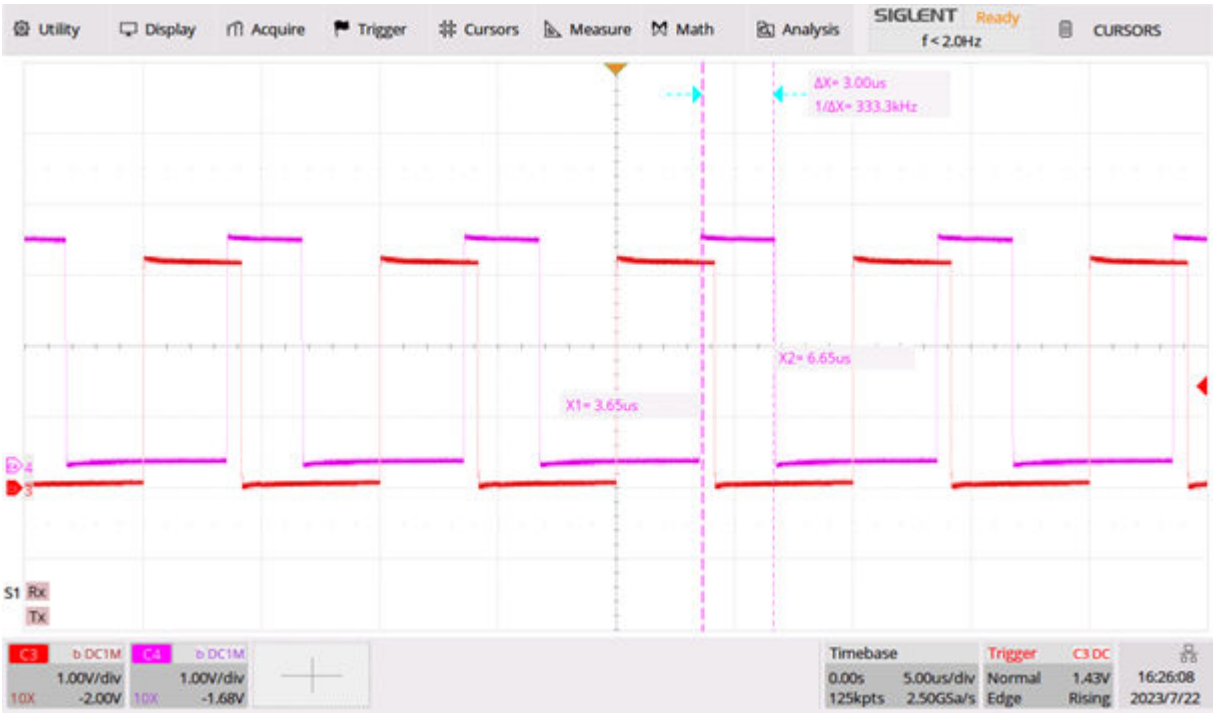
The secondary side synchronous rectifier FET, which is attached directly to the secondary winding of the transformer was the second hottest component, reaching 81°C. This is the case temperature, so assuming a maximum allowable case temperature of 110°C, this would mean that at the maximum ambient of 50°C the case would be around the allowable maximum of 110°C.

10.8 ADC ISR timing duration

The main ADC has been configured to sample the output voltage and output current of the PSFB converter. The ADC is triggered when the compare unit 4 match occurs of Timer C. This sampling point is updated at runtime to occur in the middle of the power delivery cycle to ensure that the signal measured is clean. This means that the sampling point moves as the effective duty cycle changes.

When the sample and conversion is complete, the ADC interrupt is triggered. A GPIO pin is then set high as the MCU enters the ISR as shown on Channel 4 in Figure 91. Two controllers are run within this ADC interrupt service routine. These are the controllers for the voltage loop and current loop of the PSFB converter.

Figure 91. PWM (C3) and ADC ISR duration (Ch4)



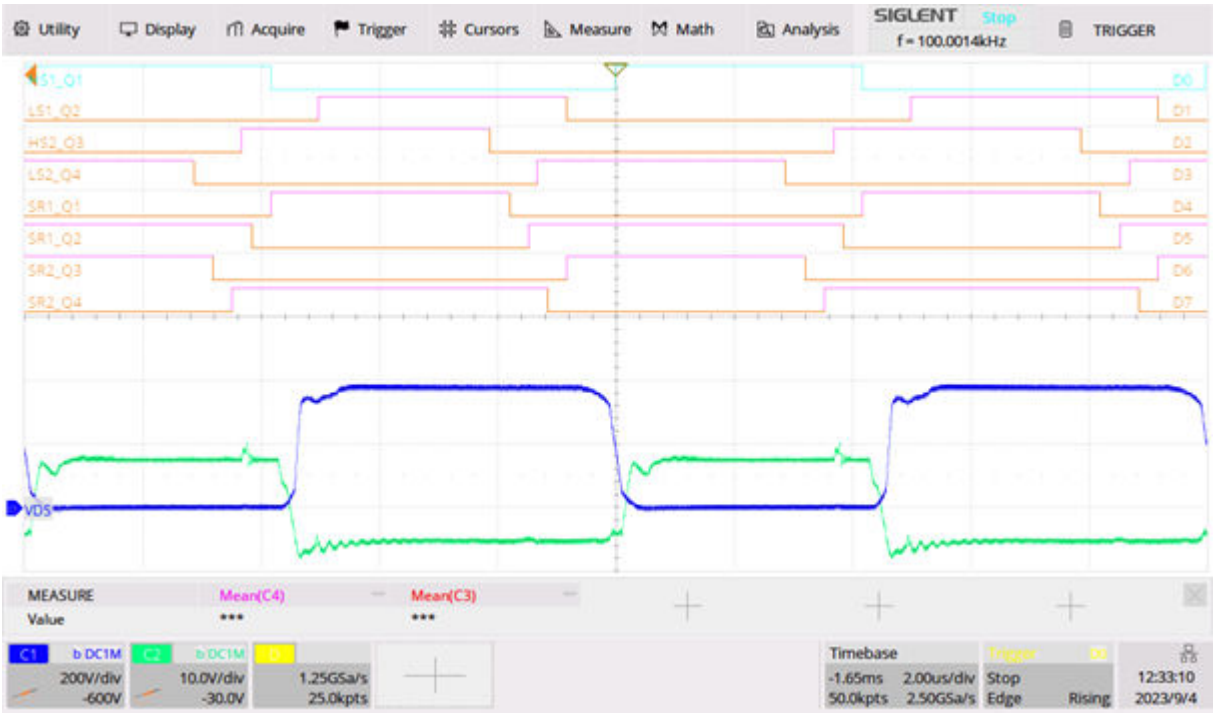
The duration of the ISR is measured in Figure 91 as 3µs. This timing measurement includes both 3p3z controllers and also the calculation and update of the new dead-time based on the output load to ensure wide range ZVS. This measurement does not include the time required to push and pop the stack before and after the ISR, however there is still clearly ample bandwidth remaining on the MCU to run other controllers or implement other functions.

10.9 Switching waveforms

To achieve zero-voltage switching at light loads, the deadtime inserted between the high-side and low-side MOSFETs in each half-bridge configuration is increased. This allows time for the reduced energy in the primary side of the transformer to fully charge and discharge the parasitic capacitances across the MOSFETs.

In Figure 92 the logic signals for the switching waveforms are sown (D0-D7) alongside the drain-source (Ch1) and gate-source voltage (Ch2) for switch Q1. Despite the light load, ZVS is still achieved as the drain-source voltage collapses to zero before the gate-source voltage rises above the gate-source threshold voltage.

Figure 92. **Switching waveforms at light load (48 V@1A)**



The deadtime between Q1 and Q2 is highlighted in the figure below.

Figure 93. **Zoom in of switching waveforms at light loads (48 V@1A)**

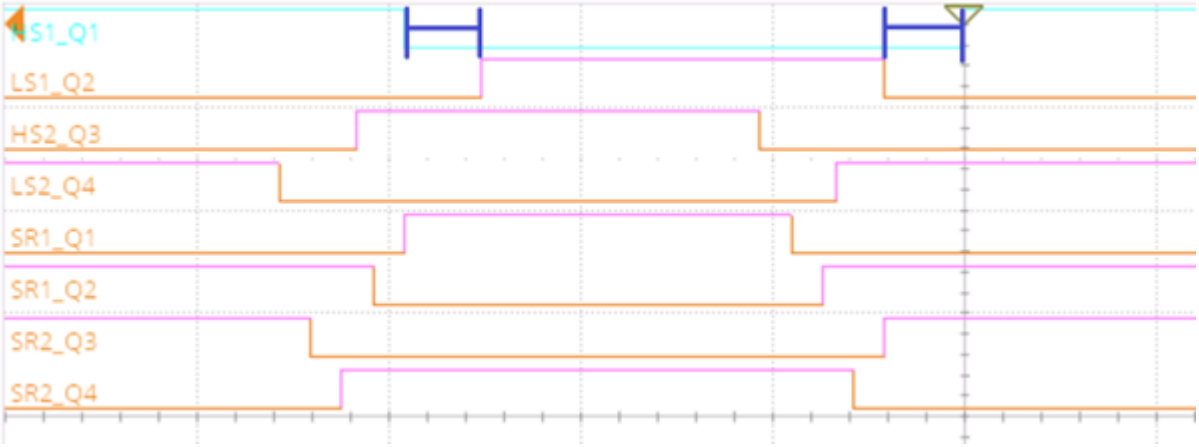
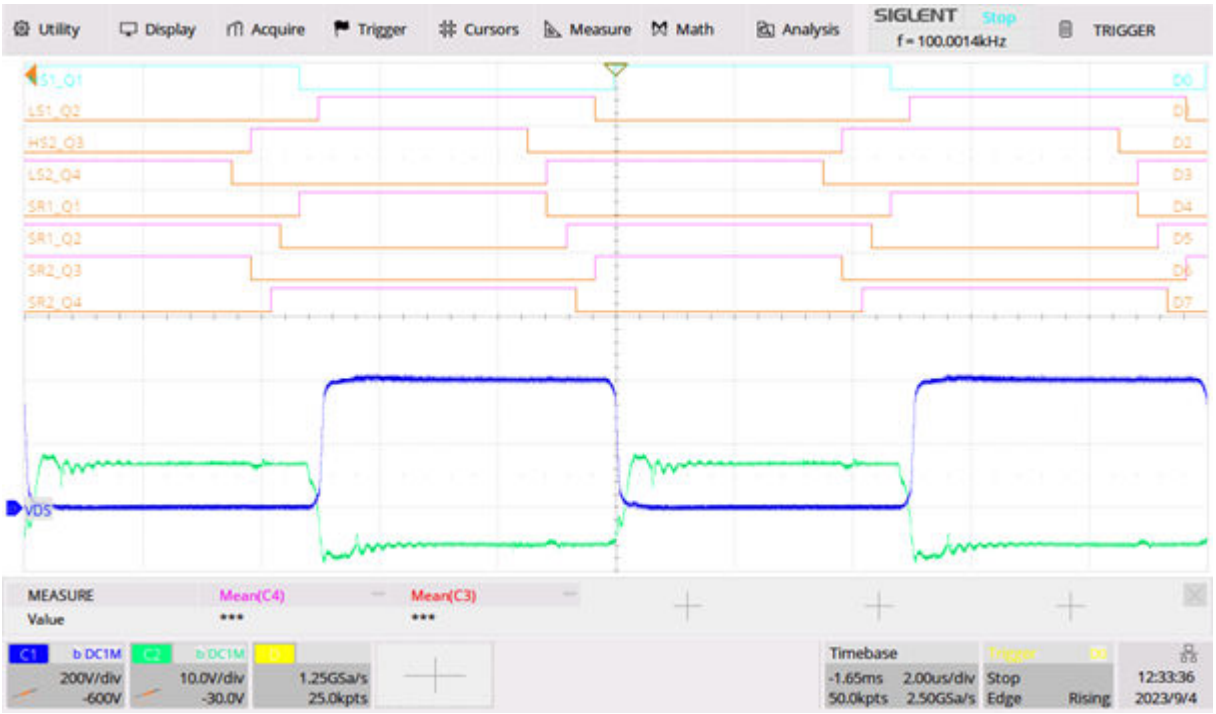


Figure 94 shows the deadtime reducing between the switching waveforms of Q1 and Q2 as the load increases. This maximizes the available duty cycle and reduces the circulating current, improving overall efficiency. ZVS is still maintained as can be seen from the drain-source (Ch1) and gate-source voltage (Ch2) for switch Q1.

Figure 94. **Switching waveforms at mid-load (48 V@21A). Deadtime reduces as load increases.**



11 Summary

This application note has detailed the design and operation of the digitally controlled PSFB converter using the STEVAL-ISA172V3 evaluation kit. The controllers for this AC-DC PSU have been implemented using the STM32G4 MCU from STMicroelectronics.

The PSFB converter has been stabilized to achieve a high crossover frequency and phase margin with an ideal transient response. The software tool ST WDS from Biricha can be used to perform the calculations required to stabilize the converter and obtain the controller coefficients.

There are several webinars that have been created to accompany this application note. Please visit: www.biricha.com/st to access the webinars related to this EVM.

Biricha digital Power also runs regular hands-on training workshops that cover the principles of power supply design, the fundamentals of control theory, the transition to the discrete-time domain and step-by-step embedded programming. These workshops are beneficial to both analog power supply design engineers who need to get familiar with digital power and embedded systems engineers who need to understand how to design and stabilize digital power supplies.

For more information on these workshops please visit: www.biricha.com/st

12 Regulatory compliance information

Notice for US Federal Communication Commission (FCC)

For evaluation only; not FCC approved for resale

FCC NOTICE - This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter 3.1.2.

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For evaluation purposes only. This kit generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to Industry Canada (IC) rules.

À des fins d'évaluation uniquement. Ce kit génère, utilise et peut émettre de l'énergie radiofréquence et n'a pas été testé pour sa conformité aux limites des appareils informatiques conformément aux règles d'Industrie Canada (IC).

13 Custom evaluation boards information

Notice: *This/these evaluation board(s) is/are custom designed and built according to specific requests from the user (You), and is/are destined for evaluation and testing of ST products in a research and development setting.*

By using or installing (as applicable) this evaluation kit, you accept all the terms of the EVALUATION BOARD TERMS OF USE available at: www.st.com/epla.

14 Appendix

14.1 Download Links

- Discovery Kit schematic and PCB design files: www.st.com/stm32g4-dpower-disco
- Workshops and training: www.biricha.com/st
- Project, ST WDS, Bode Analyzer Suite downloads:
- www.biricha.com/ST-Discovery-Kit

Revision history

Table 42. **Document revision history**

Date	Version	Changes
11-Sep-2026	1	Initial release.

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