STEVAL-ISA172V3 - 2 kW CCM Interleaved PFC AC-DC application note

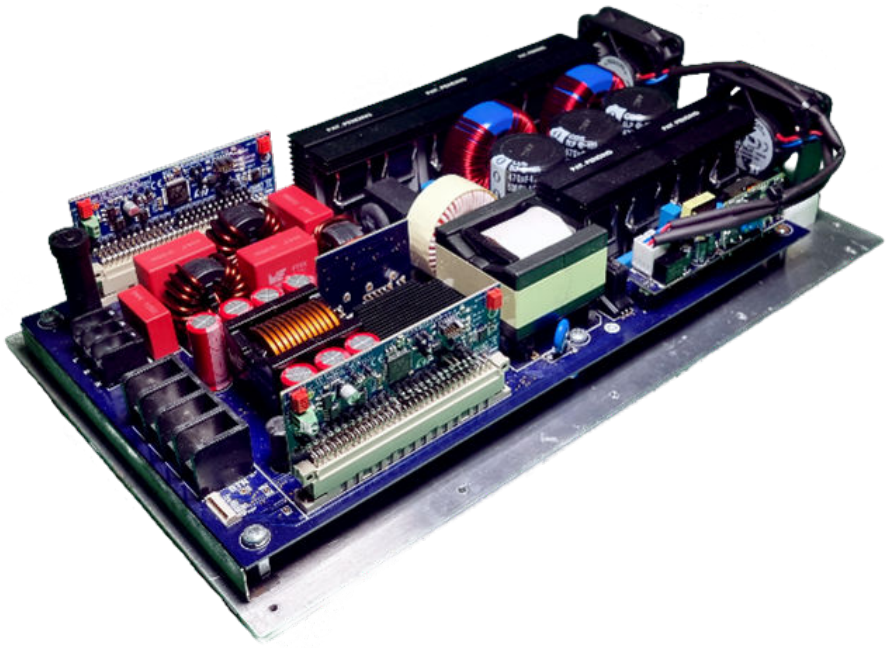
Introduction

The STEVAL-ISA172V3 is a 2kW single-output, fully digital switch mode AC-DC power supply designed for high-performance applications. This evaluation module (EVM) features two main sections: a two-phase interleaved power factor corrector (PFC) and a DC-DC phase-shifted full-bridge converter, each controlled by an STM32G474 microcontroller for precise regulation and efficient operation.

The interleaved PFC is composed of two boost converters operating 180° out of phase, utilizing 600 V MDmesh M6 Power MOSFETs to achieve high efficiency, and interleaved to reduced input current ripple. In the downstream stage, a DC-DC phase-shifted full-bridge converter based on MDmesh DM6 Power MOSFETs steps down the voltage with the help of a high-frequency transformer. The primary-to-secondary turns ratio is selected to maintain optimal efficiency and regulation throughout the entire operating range.

On the primary side of the transformer, zero voltage switching (ZVS) operation of the phase-shifted full-bridge converter minimizes switching losses and improves overall efficiency. On the secondary side, synchronous rectification (SR) is employed to reduce conduction losses. The output voltage waveform is rectified using STripFET Power MOSFETs and then smoothed by the output filter, ensuring a stable and low-noise output voltage for the target application.

Figure 1. STEVAL-ISA172V3 2 kW AC-DC EVM



*Notice: For dedicated assistance, submit a request through our online support portal at **www.st.com/support**.*

1 Disclaimers for safety

Danger: *Use the kit only after applying a fire-resistant protective cover. The protective cover is not included in the kit package.*

There is a danger of serious personal injury, property damage, or death due to electrical shock and burn hazards if the kit or its components are improperly used or installed incorrectly.

Warning: *The kit is not electrically isolated from the high-voltage supply AC-DC input.*

The evaluation kit is directly linked to the mains voltage. No insulation is ensured between the accessible parts and the high voltage. All measurement equipment must be properly isolated from the mains before powering the kit.

When using an oscilloscope with the evaluation kit, the oscilloscope must be isolated from the AC line.This precaution reduces the risk of electric shock when touching a single point in the circuit, but does NOT prevent electric shock when simultaneously touching two or more points in the circuit.

Caution: *During assembly, testing, and operation, the evaluation kit presents several inherent hazards, including but not limited to bare wires, moving or rotating parts and hot surfaces. All operations involving transportation, installation, commissioning, operation, servicing, and maintenance of the kit must be performed exclusively by Skilled Persons, as defined in standard IEC 62368-1, who are trained and experienced in power electronic systems and aware of the associated hazards.*

The board has to be connected directly on the mains. Non-isolated parts at high-voltage levels are present on both sides of the PCB .

Work area safety:

- The work area must be clean and tidy.
- Do not work alone while the kit is powered.
- Protect the work area against unauthorized access by means of suitable barriers and warning signs.
- Any system architecture supplying power to the evaluation kit must include additional control and protective devices in accordance with applicable safety regulations, technical equipment standards, and accident prevention rules.

Electrical safety:

- Remove the power supply from the evaluation kit and electrical loads before performing any electrical measurement.
- Arrange the measurement setup, wiring, and configuration with particular attention to the high voltage section.
- Power the kit only after the setup has been completed and verified.
- Fuse protection is not included with this evaluation kit.

Danger: *Do not touch the evaluation kit when it is powered or immediately after it has been disconnected from the voltage supply as several parts and power terminals containing potentially energized capacitors need time to discharge, and heat-sinks and transformers may still be extremely hot.*

Personal safety:

- Always wear appropriate personal protective equipment (PPE), such as insulating gloves and safety glasses.
- Take adequate precautions to prevent accidental contact with hazardous parts.
- Use suitable protective shields, such as insulating box with interlocks.

2 AC-DC PSU HIGH VOLTAGE WARNING

Operation of the AC-DC PSU involves high voltages. These voltages have the potential to be lethal and users are advised to take adequate safety precautions. Before applying any electrical power, the user is advised to read and familiarize themselves with the use and operation of the AC-DC PSU.

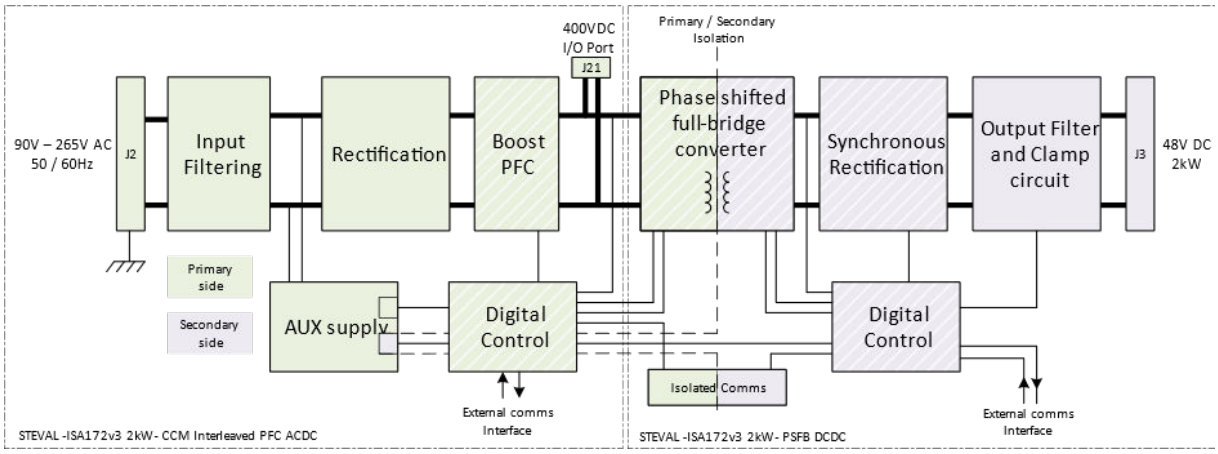
3 Overview of the complete 2 kW AC-DC converter

This overview considers the complete design of the 2kW AC-DC PSU. The design stages are described in greater detail in two separate but related application notes: 'STEVAL-ISA172V3 2 kW - CCM interleaved PFC AC-DC' and 'STEVAL-ISA172V3 2 kW - PSFB DC-DC'.

The first application note, 'STEVAL-ISA172V3 2 kW - CCM interleaved PFC AC-DC', discusses the auxiliary (AUX), primary rectification, boost PFC, and digital control stages. The second application note, 'STEVAL-ISA172v3 2 kW - PSFB DC-DC', covers the phase-shifted full-bridge converter, synchronous rectifier, output filter, and clamp stages.

The 2kW AC-DC PSU is a digitally controlled power supply capable of operating in various modes, configurable through debugging options set via the STLINK programming interface. By default, the AC-DC PSU operates with an AC input voltage range of 90 to 265 Vrms at 50/60 Hz, generating an isolated and regulated 40-54 Vdc output (48 Vdc nominal) up to 2 kW.

Figure 2. 2 kW AC-DC converter block diagram



A bidirectional DC port (J21) is included, allowing users to tap up to 2 kW from the output of the boost PFC stage or input up to 400 V DC to power the downstream DC-DC stage, which consists of the phase-shifted full-bridge converter and synchronous rectifier.

The AC-DC PSU comprises input filtering and rectification, two digitally controlled power stages, output filtering, a low-power AUX supply, and an isolated communication and control interface for configuration and control. Cooling fans and a temperature monitoring function are also integrated into the design.

3.1 Digitally controlled main power stages

The digital control algorithms used on both the STEVAL-ISA172V3 2 kW - CCM interleaved PFC AC-DC and the STEVAL-ISA172V3 2 kW - PSFB DCDC, are implemented using the STMicroelectronics STM32G474 MCU.

The STM32G474 MCU is a feature-rich 32-bit Arm Cortex®-M4. For this implementation, the microcontrollers are fitted to two identical small ‘daughter’ cards STEVAL-DPSG474M that plug into connectors J4 and J5 of the main power PCB. MCU power is provided by two isolated power rails from the AUX supply. For the STEVAL-ISA172V3 2 kW - CCM interleaved PFC AC-DC, the MCU power supply is referenced to the input ground, GND1, and for the STEVAL-ISA172V3 2 kW - PSFB DCDC, the supply is referenced to the output ground, GND2.

The voltage and current sensing for both digital controllers is filtered and scaled on the main power PCB and connected to the input pins of the ADC onboard the microcontroller. Similarly, control of the MOSFET is provided by the configurable high-resolution timer (HRTIM) modules onboard the microcontrollers. There are programmable LEDs that can provide visual indication of the operation of functions. Programming and debug access is provided by JTAG interface and can be performed using an STLINK programmer available separately. Reading of the state variables during operation is possible by means of the STLINK and a computer running the STM32CubeIDE and evaluation board project.

The digital control loops manage two primary power switching stages: the boost power factor corrector (PFC) and the phase-shifted full-bridge (PSFB) converter, and synchronous rectifier. The digitally controlled PSFB power stage employs zero-voltage switching (ZVS) and synchronous rectification to maximize efficiency and achieve optimal EMI performance.

3.2 Boost PFC output–external bidirectional port

The boost PFC stage includes an external port (J21) that allows the 400V DC rail to be ‘tapped off’ for use in applications other than the phase shifted full bridge converter stage contained in the AC-DC PSU. It also allows for the phase-shifted full bridge converter stage contained in the AC-DC PSU to be powered by an external DC source. This externally provided source can be in any of two ranges 50 to 60 V DC to allow low voltage testing and 350 V to 400 V DC to provide the full power of the phase shifted full bridge converter stage contained in the AC-DC PSU.

3.3 Simplified operation of the complete AC-DC converter

The AC input voltage is rectified using a simple 4 diode bridge to provide an unregulated DC voltage VIN_PFC (a rectified sinusoid shape). This voltage is connected to the input of a boost PFC stage that boosts the voltage to a regulated 400Vdc (nominal) - VBUS. This boost stage ensures that the input current tracks the AC input voltage waveform and that the input current is in phase with the voltage–this will lead to a near unity power factor and an input current waveform that has little harmonics above the fundamental. This is needed to meet legislative requirements regarding input current harmonics, such as EN-61000-3-2.

A large storage capacitance on the output of the boost stage provides a hold-up, that will maintain operation of the converter in the event of a momentary interruption of the AC input.

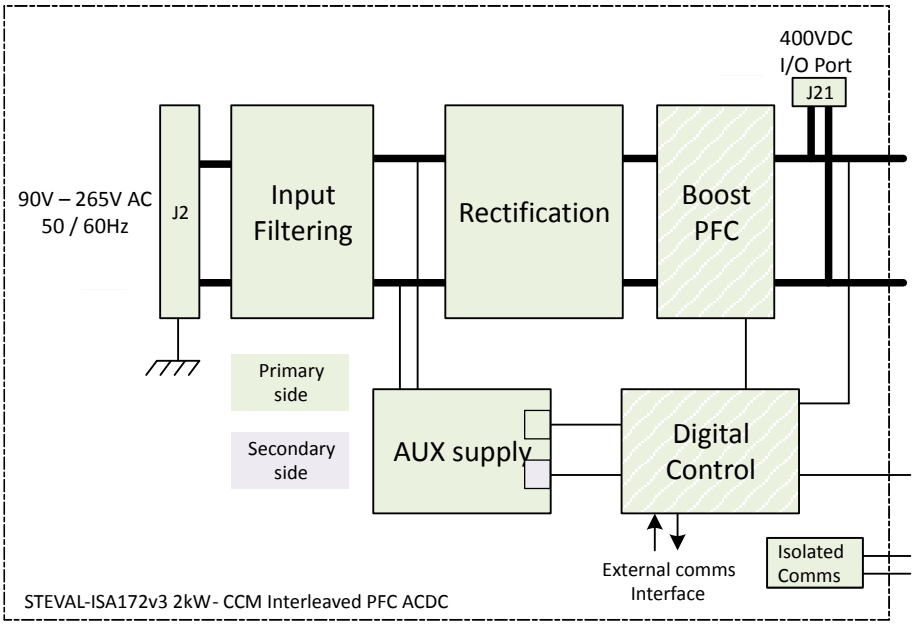
The main power stage of the converter is a phase shifted, full bridge topology, which provides an isolated and regulated 48 V DC (nom.) output voltage. An advantage to this approach is improved efficiency over a conventional full bridge by way of zero voltage switching that reduces component stress and EMI. To further improve the overall efficiency, synchronous rectifiers are used in the output stage. A simple LC output filter provides a low ripple DC output voltage.

An I²C communication interface is provided (referenced to the secondary ground) that allows configuration and control of the power stage. The unit is fan cooled with a temperature monitoring.

The converter can be configured to operate in constant voltage (CV) mode (from 40 V to 55 Vdc, with a ±1% set tolerance) or constant current (CC) mode (0 A to 42 A, with a ±10% set tolerance). It is also possible to power the PSFB converter externally via J21 from a DC input in the range 350 to 400 Vdc and also in a low voltage mode (60 Vdc in 4.8 Vdc out) to aid in test and fault diagnosis.

4 Input Filtering and Rectification stage

Figure 3. **PFC stage blocks diagram**



4.1 Input filtering and rectification stage overview

The input filter stage of the AC-DC converter consists of 2 main elements: short duration ‘spike’ protection and a multistage common mode filter. It also includes a simple in line 20 A overcurrent protection input fuse (F1).

For high-speed, short duration surges (<1 ms) a varistor (V1, B72650M271K72) and a transient voltage suppression diode or ‘tranzorb’ (D57, 1.5SMC550CA) are connected directly across the AC input. These devices are not intended to protect the input stage from extended overvoltage conditions; they are solely designed to protect against short-duration, energy-limited surges. The joule rating (or watt-seconds) of the devices determines the clamping capability of the input stage.

For conducted emissions EMC compliance, a multistage common mode filter is used. X class capacitors are connected across the input supply (L-N) and Y class capacitors between L and N and chassis.

4.2 Rectification of the AC input

A conventional (non-active) 4 diode full-bridge rectifier is used to convert the 50/60 Hz AC input to an unregulated DC bus that tracks the input voltage (VIN_PFC). The voltage of this DC bus will vary in line with the input voltage; however, the peak will be between 128 V DC and 375 V DC (AC rms * √2). The implementation actually uses two full-bridge rectifiers in parallel to manage the heat dissipation within the full bridge rectifier package at low line.

Voltage sensing of both the AC input and the unregulated DC input is provided by simple potential dividers and differential op amps. The sensed voltages are connected through simple RC filters to the analog to digital Converters (ADC) of the primary side MCU.

Table 1. **Monitor signals for the input supply stage**

Signal function	Schematic signal name	Digital Controller signal name
Input Voltage sense (L & N)	Vin_P, Vin_P	PRI_ADCx_MAIN_VOLTAGE_CHANNEL_PIN
Input Current	*Iin*	PRI_ADCx_SHUNT_CURRENT_CHANNEL_PIN
Rectified Input Voltage	VIN_PFC	PRI_ADCx_RECT_VOLTAGE_CHANNEL_PIN

4.3 Conventional full-bridge converter – Non-ZVS operation

The input filter stage includes high voltage capacitors that are charged during normal operation. To remove any stored energy in the input filter stage in a predictable time frame when disconnecting the converter from the supply, high value bleed resistors are connected across the input supply and also on the output of the bridge rectifier.

This is a safety legislative requirement to ensure that voltage across the input X capacitors has fallen to less than 60 Vdc one second after disconnection from the mains input.

5 Aux supply stage

Electrical power for all the control circuitry on both the primary and secondary sides of the converter is provided by a low power isolated flyback topology converter stage. Operating in discontinuous mode (DCM), the flyback provides three outputs across three windings, regulated by cross-regulation of the primary 15 V winding.

There are two windings referenced to primary side, and one on the secondary:

- Primary side referenced: +5V_pri_aux, +VCC_pri_aux
- Secondary side referenced: +5V_sec_aux

The flyback converter stage uses peak current control and is designed around the ST VIPER PWM (U6, VIPER317HDTR). This PWM incorporates a high voltage Primary switch (MOSFET) and current sensing as well as voltage feedback and compensation pins, to regulate the output voltage.

Start-up of the AUX converter is achieved by the PWM sourcing a small amount of current from the drain of the primary MOSFET. This current allows the Vcc pin to charge the capacitance connected externally (C42). Once the Vcc pin rises above the PWM undervoltage lockout level, the primary MOSFET will operate and switch current through the primary winding of T2. Once operating the voltage across the +VCC_pri_aux winding connection from the output of the flyback is used to maintain the voltage on the Vcc pin.

5.1 AUX control strategy and voltage regulation

Unlike the main power stages (boost PFC and full-Bridge converter), which use digital control, the low power AUX converter operates purely in the analog domain. Given the low power and simplicity of this stage make, the more cost-effective, off-the-shelf VIPER317 single IC controller is preferable to implementing digital control.

AUX stage output voltage regulation is provided by two methods:

1. Direct analog feedback of one of the output voltages (+VCC_pri_aux)
   To control the output voltage, the primary referenced output VCC_pri_aux is rectified and connected through a potential divider to the feedback (FB) pin of the PWM (U6). As the voltage sensed by the FB pin varies the PWM adjusts the ON time (duty cycle) of the MOSFET. Simple compensation is provided (C68, R41 and C70) to ensure that the VCC_pri_aux output remains stable. A further regulator PS3 is provided, to drop the nominal voltage of VCC_pri_aux (≈15V nom) to a regulated +5V_pri_aux to power the MCU 3.3V LDO.
2. Cross-regulation between the windings of the flyback wound inductors.
   To maintain regulation for the other two outputs (+5V_sec_aux and VCC_sec_aux) close coupling (cross-regulation) of the output windings of the ‘flyback’ transformer provide regulation to ensure that the output voltages remain sufficiently in limits. In simple terms the flux passing through the controlled winding (VCC_pri_aux) also passes through the windings of the other two outputs. As the voltage developed across an inductor is proportional to its inductance (which is a fixed number of turns on the inductor’s core) and the flux density, the voltage will be closely regulated provided that the loads are not too dissimilar.

6 Interleaved boost stage

To meet legislative requirements, the AC-DC converter design needs reduce input current harmonics to levels below those specified in the EN61000-3-2 standard. As a result, the AC-DC PSU should have near unity power factor (PF) when operating at significant loads. This is achieved with a digitally controlled interleaved boost power factor corrector (PFC) stage, which achieves near unity PF by modulating the input current to be as in phase with the AC line voltage as possible.

The interleaved PFC stage uses two separate boost power stages with separate boost inductors and switches. The MOSFET switches are controlled by the MCU and are operated 180° out of phase, such that the current in each inductor is also out of phase. When operating at equal duty cycles, which are line and load dependent, the resulting current waveforms drawn from the supply cancel each other, resulting in significantly reduced current ripple from the supply.

A requirement of the boost PFC topology is that the output voltage (VBUS) of the stage must always be greater than the input. This ensures that the boost stage operates throughout the full range of the input voltage sine wave.

For this design, the boost PFC output voltage (VBUS) is set at 410 V DC (nom), which is accessible at J21.

6.1 Boost stage operation

Figure 4. Basic boost PFC stage

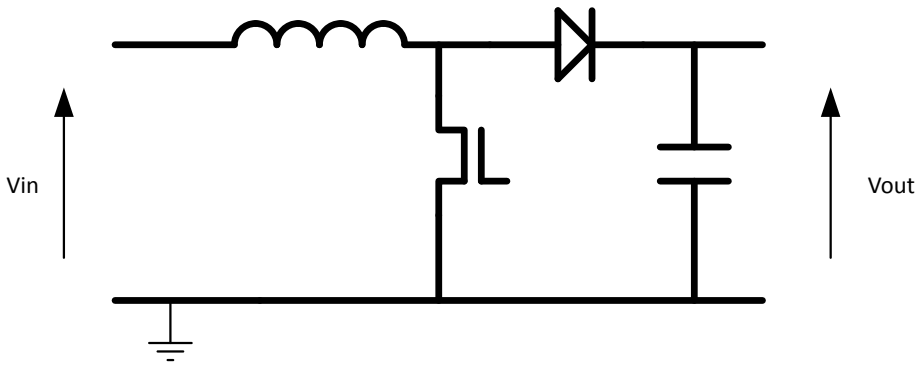


Figure 4 shows the simple topology of the Boost converter. For the purposes of this application note, the following describes the operation of one half of the interleaved boost PFC; that is, a single inductor and MOSFET. The second inductor and MOSFET of the interleaved PFC operate in parallel and are 180° out of phase.

The input of the Boost PFC stage is connected to a DC source (VIN_PFC), which is the rectified AC input. At the start of a switching cycle, the MOSFET is turned ON providing a current path through the inductor to Gnd. Current rises through the inductor linearly and establishes a magnetic field. When the MOSFET is turned OFF (open circuit) the inductor attempts to maintain the current flow through its winding as the field collapses (it is not possible to instantly change direction of current in an inductor). As a result, the end of the inductor connected to the supply (VIN_PFC) goes negative with respect to the other end of the inductor, which effectively means the voltage (collapsing) across the inductor is in series with the supply voltage. Voltages in series sum together and as such the voltage on the output of the inductor connected to the diode is the sum of the input voltage (VIN_PFC) plus the voltage developed across the inductor. This voltage will be higher than the voltage across the output capacitor so the diode will be forward biased allowing the current to flow through the diode, raising the voltage on the capacitor and the load. At the start of the next switching cycle, when the MOSFET turns ON again, the diode becomes reverse-biased, preventing the current from flowing back into the MOSFET. At steady-state, therefore, the output voltage across the Boost capacitor will always be greater than the input voltage.

Control of the interleaved boost PFC stage requires the digital controller to monitor the current through the inductors and the voltages on the input and output at once per switching cycle. This interleaved boost PFC stage is switching at a frequency of 70 kHz.

Table 2. Monitor signals for the boost PFC stage

Signal function	Schematic name	Digital controller signal name
Rectified Input Voltage	VIN_PFC	PRI_ADCx_RECT_VOLTAGE_CHANNEL_PIN

Signal function	Schematic name	Digital controller signal name
Boost Voltage	VBUS	PRI_ADCy_VBUS_CHANNEL_PIN
Boost Current	IBUS	PRI_ADCx_SHUNT_CURRENT_CHANNEL_PIN

6.2 How the boost stage improves power factor

To achieve unity power factor as near as possible to unity, the current drawn from the input supply needs to be in phase with the voltage; that is, the load needs to appear as resistive. as possible to the AC source.

In this application, the AC input supply voltage is a sine wave at a frequency of between 50 and 60 Hz. The phase-shifted full-bridge converter will present a complex, non-linear load and certainly not appear as a resistive load. To achieve a good power factor, the interleaved boost PFC needs to be able to modulate the current drawn from the supply so that it matches the sine wave of the input voltage.

In normal operation, the output voltage of the boost stage will be higher than the input voltage, and as such it is possible to operate the boost PFC over the full range of the input voltage sine wave. By modulating the duty cycle (or ON time) of the boost MOSFETs, the average current thought the inductor will vary. Modulating the MOSFETs duty cycle to the shape of the input voltage, the average current can therefore be made to follow the shape of the AC voltage. In essence, the load (current demand) presented to the AC input voltage is modulated to mimic a resistor; the voltage and current will therefore be in phase and represent a high-power factor.

To achieve the necessary modulation of the MOSFETs and corresponding supply current, the controller needs to monitor the waveform of the input voltage (50/60Hz AC sine wave) and current demand of the load. This is achieved by the current and voltage monitor circuits (sheet 4, U1 and U10 and supporting components), the outputs of which are connected to analog to digital converter (ADC) inputs of the Primary side MCU. The signals provided to the controller are listed in Table 2.

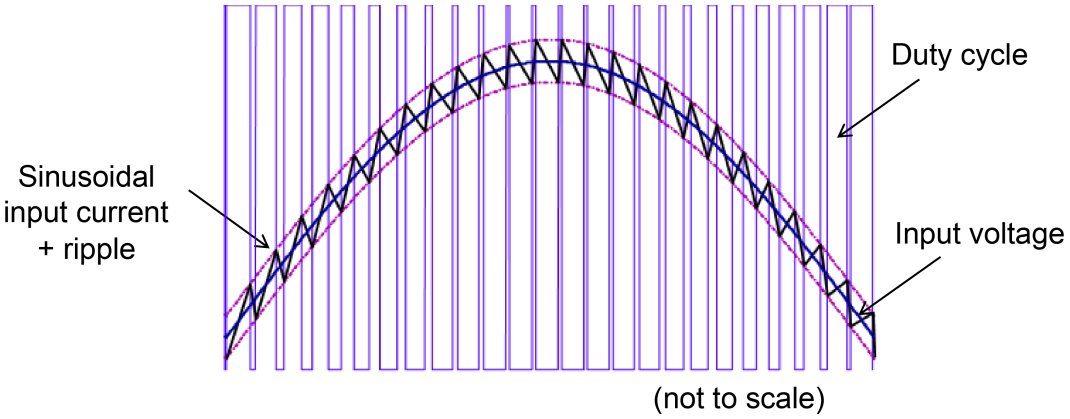
7 Average current mode control for PFC explained

7.1 Average current mode step-by-step

The main role of the PFC stage is to reduce the input current harmonics to below the levels specified in the standard. Ideally, the input current to the PFC stage would be a pure sinusoid at the same frequency as the line voltage and in phase with the line voltage. This would imply that there are no harmonics above the fundamental, 50 or 60Hz. By definition, this would therefore have a power factor of 1 as there would be no reactive power and all power delivered to the AC-DC would be real power, consumed by the end load and the efficiency losses in the AC-DC stage.

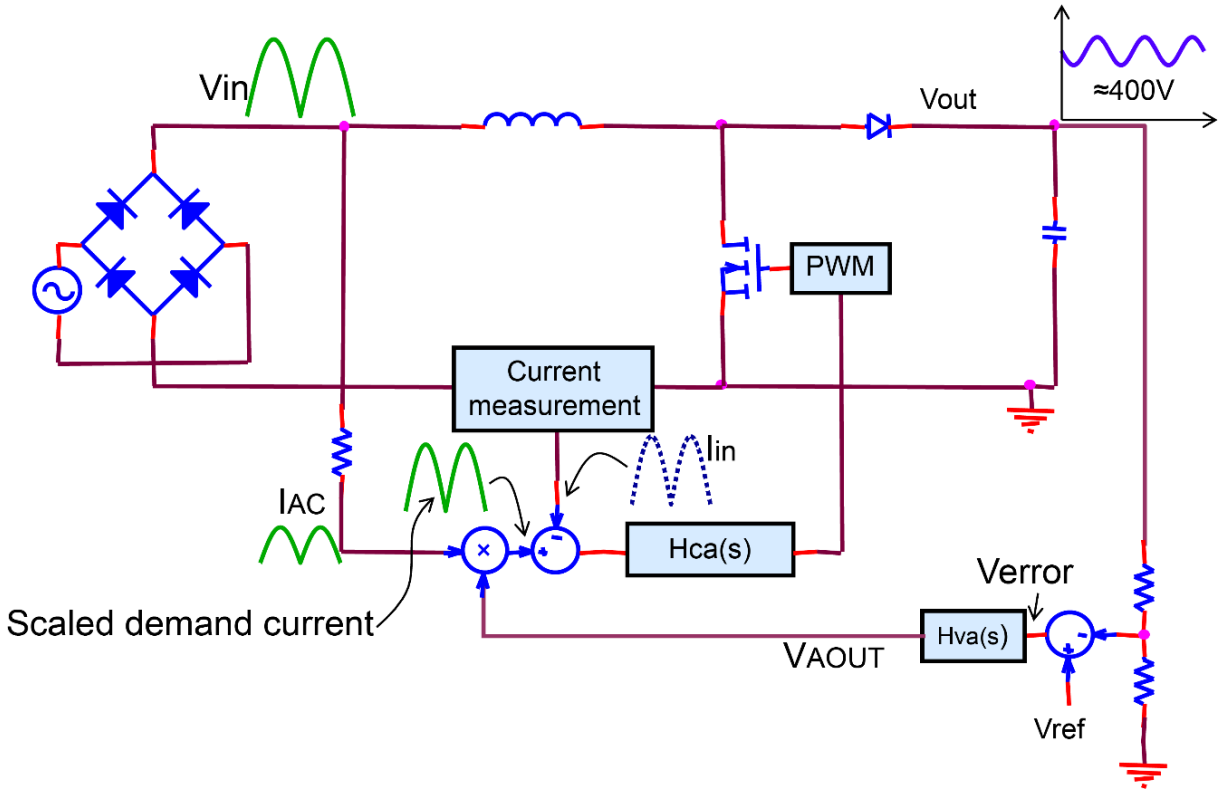
In order to achieve this, the PFC stage must be able to control the shape of the input current. For the CCM boost PFC, this is achieved by an average current mode control scheme. As the name suggests, the control loop aims to regulate the average current in the PFC input inductor in such a way as to shape it into a sinusoid in phase with the input voltage. To achieve this, the duty of the boost PFC switch is modulated in a sinusoidal manner as shown in the following figure.

Figure 5. Inductor current modulation to track input voltage



Under average current mode control for PFC, there are two loops: a very slow reacting outer voltage loop that ensures that the output voltage is always greater than peak rectified mains voltage, and a very fast inner current loop which ensures the input current tracks a sinusoidal reference. This sinusoidal reference is often derived from the line voltage, as this ensures the demand current reference is always in phase with the voltage.

Figure 6. **Average current mode control loops**



In Figure 6, the output of the voltage loop, VAOUT, is used to scale this initial value of demand current in order to compensate for changes in the load. This provides good load regulation. However, the loop gain of this voltage loop must be very low to ensure that it does not interfere with the main operation of the PFC stage, which is to shape the current. Therefore, a PFC voltage loop will typically have a low crossover frequency of between 5-10 Hz. This means that it may take several hundred milliseconds to recover from load transients on the PFC output. This is normal, however, and the downstream DC-DC converter should have been designed to operate down to ~80-90% of the nominal PFC bus voltage.

To compensate for changes in the line, it is typical to implement some form of input voltage feed forward control technique. In this design, the initial value of demand current, which is derived from the line voltage, is divided by the RMS value of the input voltage squared. This means that if the RMS input voltage falls, then the input current rises. This ensures that the input power remains constant despite any changes in the line; for example, during a brown out condition.

This control method and its implementation is discussed in great detail during the Biricha Digital Power Supply Design Workshops with STM32. Please see www.biricha.com/st for more information on these workshops.

7.2 Boost PFC plant transfer functions

Under average current mode control, the boost power stage has two control loops and thus two plant transfer functions.

In the “Average Current Mode Control of Switching Power Supplies” application note by Lloyd Dixon, the plant transfer functions for both the current and voltage loops of the boost converter are described. These plant transfer functions are approximations, and work well for the frequency range where the individual control loops are dominant.

7.3 Voltage loop

The voltage loop plant transfer function consists of a single pole at the origin as shown in Equation 1.

$$H_{P_VL}(s) = \frac{1}{s\,C_{out}} \times \frac{P_{in}}{\Delta V_{AOUT} \times V_{out}} \quad (1)$$

The gain of the voltage loop plant is dependent on the size of the PFC bulk capacitance, C_{out}, the input power, P_{in}, the PFC output voltage, V_{out}, and the maximum swing of the voltage loop controller, ΔV_{AOUT}. In a digital implementation, the ΔV_{AOUT} term is replaced by an equivalent term as there is no longer a voltage error amplifier. This is discussed later in the digital implementation section of this application note.

7.4 Current loop

The current loop plant transfer function also consists of a single pole at the origin as shown in Equation 2.

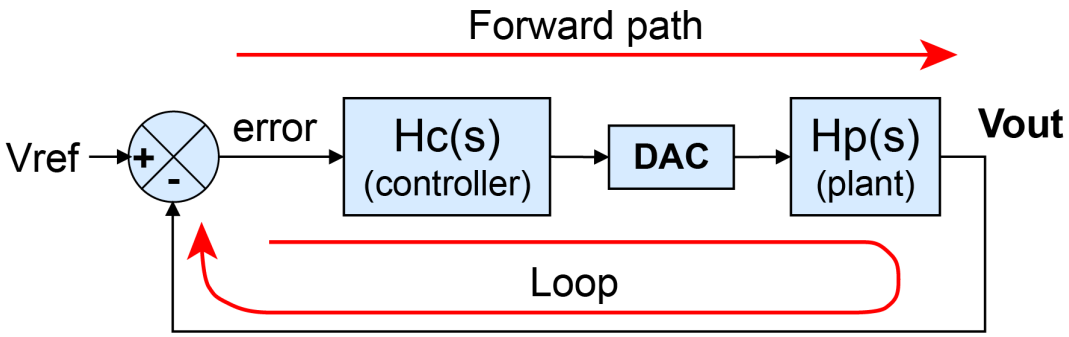
$$H_{P_CL}\left(s\right) = \frac{V_{OUT}}{s\ L_{BOOST}} \times \frac{R_{SENSE}}{V_{RAMP}} \quad (2)$$

The gain of the current loop plant is dependent on the size of the PFC boost inductor, L_{BOOST}, the output voltage, V_{out}, the current sense resistor, R_{SENSE}, and the PWM modulators ramp height V_{RAMP}. In a digital implementation, an analog ramp is not used to generate the PWM, therefore this term is normalized to 1. The PWM module gain of the MCU is included in the loop gain as part of the digital gains section later in this application note.

8 Average current mode compensator design for PFC

8.1 Loop stability criteria

Figure 7. Closed-loop and open-loop transfer functions



Consider the simple control loop shown in Figure 7. In this figure, the “Forward” and “Loop” paths of the control loop have been identified. The transfer function for the closed-loop system is given in Equation 3.

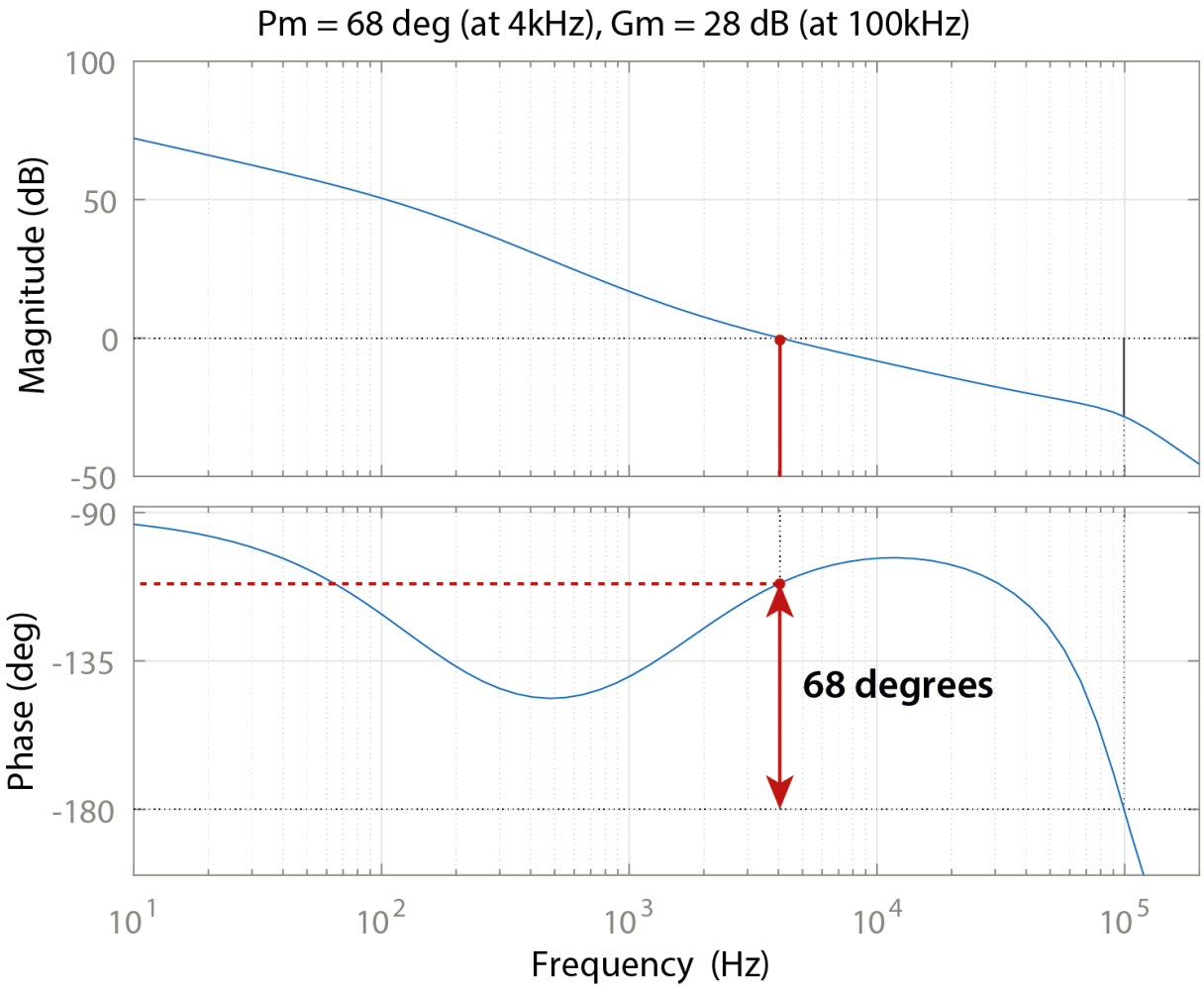
$$\mathrm{TF} = \frac{\mathrm{Forward}}{1-\mathrm{Loop}} \tag{3}$$

The closed-loop transfer function can be derived by applying this to Figure 7:

$$H_{CL}(s) = \frac{Foward}{1-(-Loop)} \tag{4}$$

The loop response, which is also called the “open-loop”, is the compensator transfer function $H_c(s)$ combined with the plant or power stage transfer function Hp(s) and also includes the modulator gain – the PWM block. The Bode plot of a typical loop response for a peak current mode converter is shown in the figure below.

Figure 8. **Open-loop Bode plot of buck converter: plant and compensator**



Several terms can be defined from this Bode plot. The first is the crossover frequency. This is the frequency at which the gain plot crosses the 0 dB axis. If the gain plot is falling at a rate of 20 dB/decade around the crossover frequency, then below the crossover frequency (at a lower frequency, going left on the frequency X-axis) the gain plot will have positive gain; i.e., it will have a gain that is greater than 1.

At the crossover frequency, the value of the phase in the open-loop will determine the stability of the closed-loop system. If the phase is -180 or less with a gain greater than or equal to 1, then the closed-loop system will become unstable. This can be seen from the denominator of Equation 4.

To ensure stability, the phase of the open-loop system must therefore be greater than -180 at the crossover frequency. This term is defined as the phase margin and is the amount by which the phase is above the -180° at the crossover frequency. Typically, the compensator will be designed such that the phase margin is 45° or more at the crossover frequency. A phase margin of 45° would equate to a loop phase of -135°. Therefore, the loop phase is 45° above the -180° point of instability. In Figure 8, the phase margin is shown as 68 degrees.

8.2 Crossover and phase margin specification

The choice of crossover frequency and phase margin will determine how well the converter responds to line and load transients. In typical DC-DC applications, the higher the crossover frequency, the faster the response and recovery in the time domain. However, with PFC pre-regulators, there are certain limitations that must be observed.

For the voltage loop the crossover frequency should ideally be one decade below two-times line frequency. This is because the voltage loop must not actively reject the 100 Hz ripple that appears on the output voltage. This 100 Hz ripple is the result of the current loop tracking the input voltage waveform ensuring that the input current is a sinusoid in phase with the input voltage. If the voltage loop crossover frequency is too high, (i.e., above 10 Hz), then the input current waveform will be distorted and have higher harmonics.

The phase margin of the voltage loop should be large enough to ensure a stable response and recovery to load transients, typical values are in the range of 50 to 60 degrees. Based on this, the crossover and phase margin specification for the voltage loop can be defined:

Voltage loop stability specification

- Crossover frequency: 7 Hz
- Phase margin: 50 degrees

For the PFC current loop there are a different set of requirements. The PFC current loop should typically have a high crossover frequency, usually between 1/10th and 1/20th of the switching frequency. The crossover frequency must not be higher than 1/6th of the switching frequency otherwise there may be sub-harmonic oscillations as discussed in [ref]. Furthermore, the PFC current loop must be optimized for reference tracking ability at 100Hz as this is the frequency of the rectified sinusoidal reference that tracks the input voltage waveform.

This typically sets an upper limit on the phase margin requirement. A high phase margin will mean that the compensator zero needs to be pushed lower in frequency – this will erode the low frequency gain and specifically the reference tracking ability around 100 Hz. As a result, a phase margin of between 40 and 45 degrees is typical for PFC current loops, provided that this does not result in any oscillations at the extremes of line and load.

Current loop stability specification

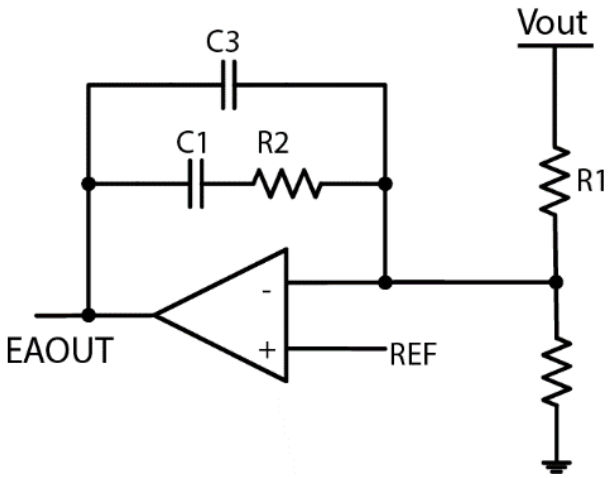
- Crossover frequency: 1/10th to 1/20th of switching frequency
- Phase margin: Around 40-45 degrees

8.3 Types of compensators

A compensator needs to be designed and added into the loop in order to shape the loop response to meet the desired crossover frequency and phase margin specifications. In the analog domain, a compensator usually consists of an inverting op amp with a compensation network of capacitors and resistors around the negative feedback path. The combinations of capacitors and resistors determine the location of the poles and zeros of the compensator.

There are typically two types of compensators that are used for stabilizing power supplies. These are universally referred to as the Type II and Type III compensator. For peak and average current mode control, the Type II compensator is typically used. The Type III is usually used for compensation of voltage-mode controlled converters as a Type III has an extra pole/zero pair required to compensate for the double pole of the voltage-mode plant transfer function. The circuit for a Type II compensator is shown in Figure 9.

Figure 9. Type II compensator implemented in analog using op amp



The transfer function for this circuit can be derived using the standard transfer function for an inverting op-amp. For brevity, the full transfer function has been included without derivation in Equation 5.

$$H_C\left(s\right) = \left(\frac{\omega_{CP0}}{s}\right)\frac{\left(\frac{s}{\omega_{CZ1}} + 1\right)}{\left(\frac{s}{\omega_{CP1}} + 1\right)} \quad (5)$$

The transfer function in Equation 5 has one zero, one pole, and a pole at the origin. The locations of these zeros and poles are determined by the capacitors and resistors in the compensation network according to Equations 6, 7, and 8.

$$\omega_{CZ1} = \frac{1}{R_2 C_1} \tag{6}$$

$$\omega_{CP0} = \frac{1}{R_1(C_1 + C_3)} \tag{7}$$

$$\omega_{CP1} = \frac{(C_1 + C_3)}{R_2 C_1 C_3} \tag{8}$$

In digital, this compensator will be implemented on the MCU, and the translation from analog to digital will be discussed in the next chapter.

8.4 Compensator pole/zero placement

For the PFC control loops, two compensators need to be designed. One for the slow voltage loop and another for the fast current loop. The locations of the poles and zeros of these compensators need to be selected such that, when the compensator is combined with the relevant plant transfer function, the open-loop frequency response meets the stability criteria of:

- desired crossover frequency
- desired phase margin at the crossover
- a shallow slope of -20 dB/decade around the crossover

There are several different methods that can be applied to achieve this. In this application note, the straightforward and intuitive method of pole/zero placement to achieve desired phase margin and crossover frequency is applied.

8.4.1 Voltage loop

The voltage loop compensator poles and zeros are placed such that point of maximum phase boost occurs equidistantly between the compensator zero and pole. The compensator's pole at the origin, or gain, is then calculated such that, when combined with the voltage loop plant, the loop crossover frequency occurs at this point of maximum phase boost. This will also ensure that the loop around crossover is around -20 dB/decade.

To achieve this, the compensators real pole and zero must be placed using the following two equations.

$$\omega_{cp1_VL} = \omega_{X_VL} \times \tan(\varphi_m) + \sqrt{(\omega_{X_VL})^2 + (\omega_{X_VL} \times \tan(\varphi_m))^2} \tag{9}$$

$$\omega_{cz1_VL} = \frac{\omega_{X_VL}^2}{\omega_{cp1_VL}} \tag{10}$$

Where is the desired phase margin in radians and is the desired crossover frequency in radian/s.

Once these pole and zero locations are known, the pole at the origin, or gain of the compensator, can be calculated using the following Equation 11.

$$\omega_{cp0_VL} = \frac{\omega_{X_VL}}{\frac{P_{IN}}{\Delta V_{AOUT} \times V_{OUT}} \times \frac{1}{\omega_{X_VL} \times C_{OUT}} \times \frac{\sqrt{\left(\frac{\omega_{X_VL}}{\omega_{cz1_VL}}\right)^2 + (1)^2}}{\sqrt{\left(\frac{\omega_{X_VL}}{\omega_{cp1_VL}}\right)^2 + (1)^2}}} \tag{11}$$

So, the final term of the voltage loop compensator to calculate is the pole at the origin. As the name implies, this compensator pole is at the origin, and therefore setting the position of the pole at the origin is, in fact, changing the gain and not moving the pole. This can be used to adjust the crossover frequency of the loop. Adding the pole at the origin to the compensator will introduce the constant -20 dB/decade gain roll-off, which is desirable around the crossover frequency.

The gain contributions from all of the other poles and zeros in the system must be taken into account in order to determine the exact gain required by the compensator to achieve the desired crossover frequency. The equality given in Equation 12 must be solved for the compensator pole at the origin:

$$20log_{10}\left|H_{P_VL}(j\omega)\right| + 20log_{10}\left|H_{C_VL}(j\omega)\right| = 0dB \quad (12)$$

8.4.2 Current loop

The current loop compensator is designed in a similar manner. As discussed previously, the compensator zero must not be placed at a too low frequency otherwise it would reduce the low frequency gain and impair the reference tracking ability of the compensator. Therefore, the compensator design starts with the placement of the compensator pole. This is placed at half the switching frequency or one decade above the crossover frequency, whichever is greater.

This ensures that the compensator pole as little impact on the phase margin at crossover and allows the compensator zero to be placed at as high a frequency as possible to achieve the desired phase margin.

$$\omega_{cp1_CL} = \pi \times F_S \quad (13)$$

The compensator zero can then be calculated in order to achieve the specified phase margin (Biricha, 2020). This is achieved by solving the equality shown in Equation 14 for the compensator zero .

$$\angle\left(H_{P_CL}(j\omega) \cdot H_{C_CL}(j\omega)\right) = \omega_{cz1_CL} = \frac{\omega_{X_CL}}{tan\left[\phi_m + tan^{-1}\left(\frac{\omega_{X_CL}}{\omega_{cp1_CL}}\right)\right]} \quad (14)$$

Finally, the compensators pole at the origin, or gain, can be calculated as follows:

$$\omega_{cp0_CL} = \frac{\omega_{X_CL}}{\frac{V_{OUT} \times R_{SENSE}}{\omega_{X_CL} \times L \times V_{RAMP}} \times \frac{\sqrt{\left(\frac{\omega_{X_CL}}{\omega_{cz1_CL}}\right)^2 + (1)^2}}{\sqrt{\left(\frac{\omega_{X_CL}}{\omega_{cp1_CL}}\right)^2 + (1)^2}}} \quad (15)$$

For this application note, the software tool Biricha ST PLD will be used to perform the calculations and is available for download free of charge from the Biricha website: www.biricha.com/st-pld. This tool will be discussed in detail through means of a complete design example later in this application note.

9 Discrete-time controller

9.1 Bilinear transform

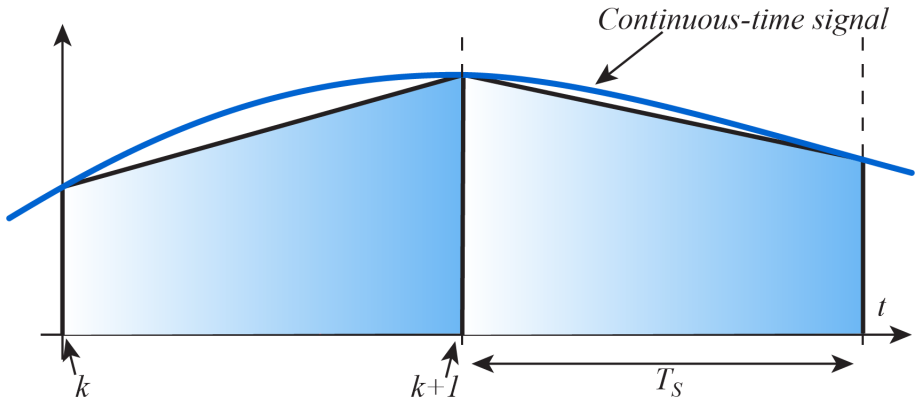
With the poles and zeros of the compensator placed in the continuous-time domain, the s-domain, they must be converted into the discrete-time domain to implement the controller on the MCU. To implement the discrete-time controller, the continuous-time Type III compensator, which was discussed in the previous section, will be converted into its discrete-time equivalent.

There is a direct mapping between the continuous-time domain, the s-domain, and the discrete-time domain, the z-domain. The relationship is shown in Equation 16.

$$z = e^{sT} \tag{16}$$

There are several different methods that can be used to covert an s-domain transfer function into the discrete-time z-domain. A commonly used method is the bilinear transform (also called the Tustin or trapezoidal transform). This transform approximates the continuous-time signal based on a trapezoid from k to k+1. An example of this is shown in the fiure below.

Figure 10. Continuous time signal sampled in discrete time using a trapezoidal approximation

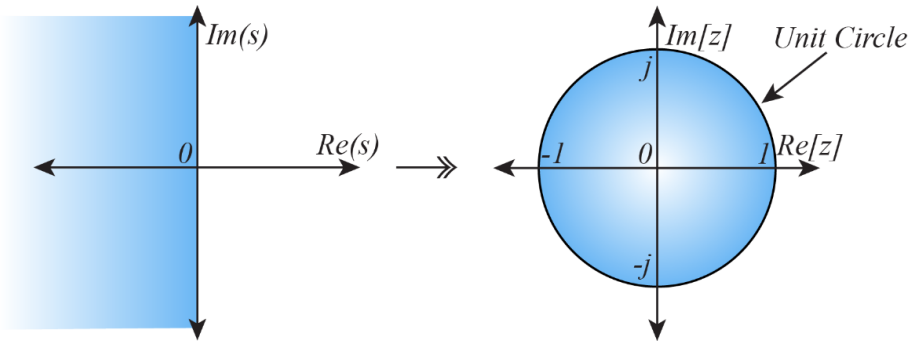


This trapezoidal approximation gives rise to the transform given in Equation 17.

$$s \leftarrow \frac{2}{T_S}\frac{1 - z^{-1}}{1 + z^{-1}} \tag{17}$$

This transform has the advantage that a system with stable (i.e., left-hand plane) poles and zeros will transform into a system with stable z-domain poles and zeros. The stable region in the z-domain is the area on or inside the unit circle. Therefore, the mapping is shown in the figure below.

Figure 11. Trapezoidal approximation mapping from s to z-domain



There will inevitably be some distortion with the mapping given that the entirety of the left-hand s-plane is mapped to the unit circle in the z-domain. However, this distortion is only significant as the frequency approaches the sampling frequency. For this power supply application, most of the compensator poles and zeros are significantly below the sampling frequency. Furthermore, the crossover frequency has been specified as between 1/10th to 1/20th of the sampling frequency and there will be no significant distortion from the mapping around this frequency.

However, this transform does not include the effects of the pure time delays in the discrete-time system and there will be an additional phase roll-off that is not considered here. This will manifest itself as a phase erosion at the crossover frequency and this must be taken into account when the compensator is being designed.

9.2 2p2z controller

The bilinear transform is applied to the s-domain Type II compensator by replacing every instant of ‘s’ in the s-domain transfer function with the bilinear mapping. The initial substitution is given in Equation 18 and the simplified result is given in Equation 19.

$$H_C\left[z\right] = \left(\frac{\omega_{CP0}}{\frac{2}{T_S}\frac{1-z^{-1}}{1+z^{-1}}}\right)\frac{\left(\frac{\frac{2}{T_S}\frac{1-z^{-1}}{1+z^{-1}}}{\omega_{CZ1}}+1\right)}{\left(\frac{\frac{2}{T_S}\frac{1-z^{-1}}{1+z^{-1}}}{\omega_{CP1}}+1\right)} \tag{18}$$

$$H_C[z] = \frac{B_2\, z^{-2} + B_1\, z^{-1} + B_0}{-A_2\, z^{-2} - A_1\, z^{-1} + 1} \tag{19}$$

In the discrete-time z-domain, the transfer function now has two z-domain poles and two z-domain zeros. Therefore, this controller is now referred to as a two-pole two-zero controller or 2p2z for short.

The numerator of the transfer function has been grouped into like terms consisting of ‘B’ coefficients and likewise, the denominator has been grouped into like terms consisting of ‘A’ coefficients. These coefficients are given in Equation 20 to Equation 24.

$$B_0 = \frac{T_S \times \omega_{CP0} \times \omega_{CP1} \times (2 + T_S \times \omega_{CZ1})}{(2 \times (2 + T_S \times \omega_{CP1}) \times \omega_{CZ1})} \tag{20}$$

$$B_1 = \frac{{T_S}^2 \times \omega_{CP0} \times \omega_{CP1}}{(2 + T_S \times \omega_{CP1})} \tag{21}$$

$$B_2 = \frac{T_S \times \omega_{CP0} \times \omega_{CP1} \times (-2 + T_S \times \omega_{CZ1})}{(2 \times (2 + T_S \times \omega_{CP1}) \times \omega_{CZ1})} \tag{22}$$

$$A_1 = \frac{4}{(2 + T_S \times \omega_{CP1})} \tag{23}$$

$$A_2 = \frac{-(2 - T_S \times \omega_{CP1})}{(2 + T_S \times \omega_{CP1})} \tag{24}$$

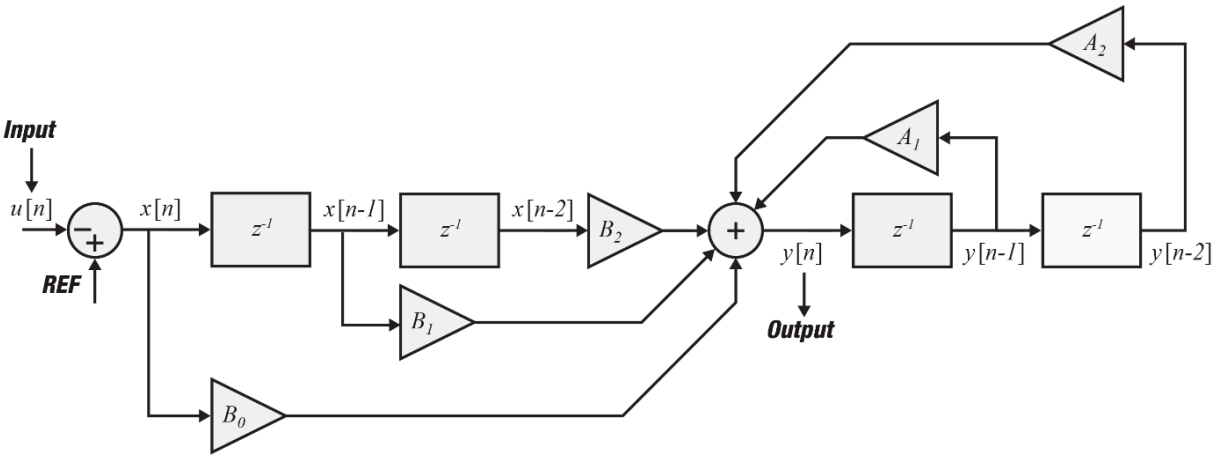
There is no need to calculate these controller coefficients by hand as the software tool Biricha ST WDS available from www.biricha.com/st-wds will perform these calculations for you.

Finally, now that the controller is in the discrete-time 2p2z form, it can be converted into a linear differential equation which can be easily implemented on the MCU. This takes advantage of the shifting property of the z-domain transfer function and converts from z-domain to discrete sample in Equation 25.

$$y[n] = A_1 y[n-1] + A_2 y[n-2] + B_0 x[n] + B_1 x[n-1] + B_2 x[n-2] \tag{25}$$

Where y[n] is the output for the current sampling interval. The structure of this controller is depicted in the following figure.

Figure 12. 2p2z controller structure



For the fast current loop of this average current mode converter, the output of the controller during this sampling interval would be the new demand average current value that will be used in the following switching period. Therefore, there is now an equation which can implement the analytically designed controller and will be calculated by the MCU at every sampling interval when there is a new sample available.

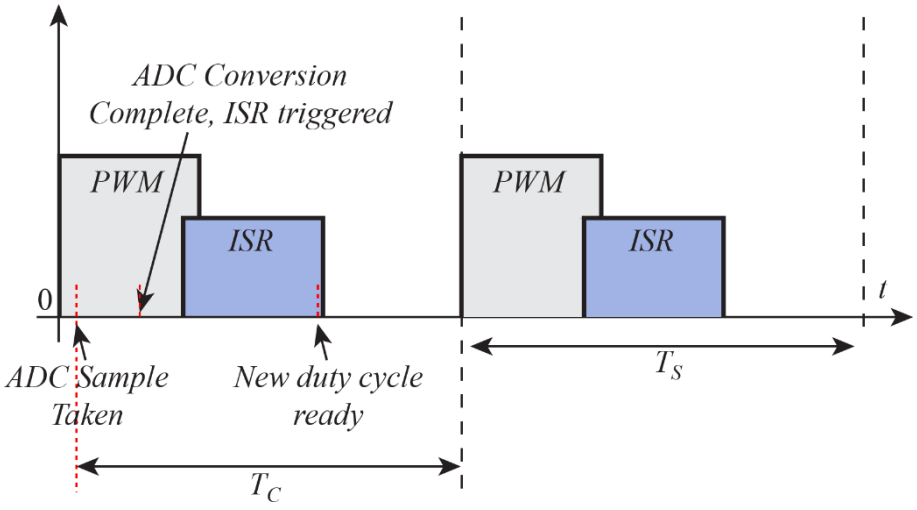
9.3 Pure time delays

In this discrete-time digital system, there are additional time delays that are not present in the equivalent analog continuous-time system. A pure time delay in the discrete-time system will result in a phase delay that is proportional to the frequency and time delay.

There are two sources of time delay in the digital system. The first is the time from which the output voltage sample was taken, to the time at which it was used. This is referred to as the calculation delay. In effect, the older the sample the more phase delay will be associated with the sample. For example, a convenient time to trigger the ADC and sample the output voltage and inductor current will be in the middle of the PWM switching cycle. This will ensure that the average current is being sampled away from the switching edges. In this case, the voltage will be sampled, converted and used in the controller to provide the new value of duty. This sampling and calculation time may take several hundred nanoseconds and the new demand peak current value will be ready to use towards the end of that switching period.

This situation is described in the following figure.

Figure 13. Sources of delay within the discrete-time system



However, as the new duty cycle value will not be used until the following switching cycle, the total time delay for this calculation time is considered to be half of the switching period.

The second contribution to the time delay is that of the zero-order-hold introduced by this sampled data system. The ADC is triggered once per switching cycle, this sampled data is used to calculate the new value of duty cycle value and that duty cycle value is then held constant for the remainder of the next switching period by the HRTIM module. Therefore, there is an additional zero-order-hold in this system. The frequency response of a ZOH is given in Equation 26.

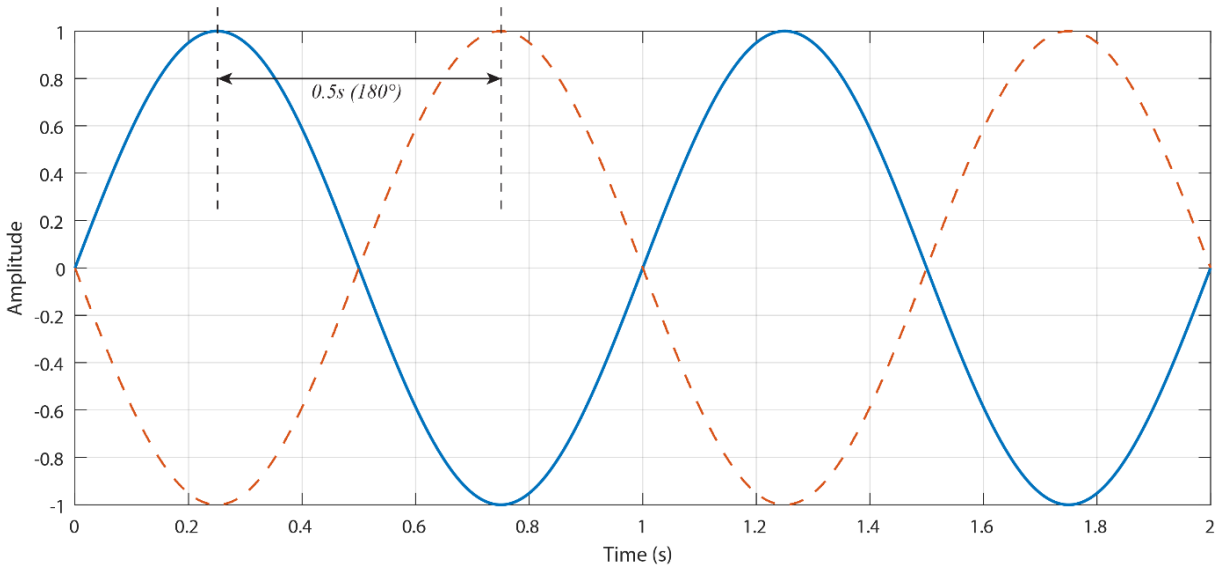
$$F_{ZOH}(j\omega) = \frac{1 - e^{-j\omega T_S}}{j\omega} \tag{26}$$

This can be shown to be a complex number expressed in polar form, and therefore the phase angle is given in Equation 27.

$$\angle F_{ZOH}(j\omega) = -\omega\frac{T_S}{2} \tag{27}$$

To understand how this phase angle can relate to a time delay, consider as an example the 1Hz sine wave shown in Figure 14. If this sine wave were delayed by 0.5 seconds, the result would be the sine wave shown as a dashed line in Figure 14.

Figure 14. Time delay relationship to phase delay



It is clear from this that the time-delayed sine wave now has a phase delay of 180°. Therefore, the equation to calculate the phase delay of a sine wave given the pure time delay T_D is given in Equation 28.

$$p.d. = -2\pi f T_D \tag{28}$$

This indicates that there will be some phase delay across all frequencies, however, when $T_D \ll 1/f$, the phase delay will be negligible. This will be true for very low frequencies assuming that the phase delays in the digital system can be kept to a minimum.

The frequency at which this phase delay could become a concern would be the crossover frequency of the open-loop system as this is where the phase margin is defined. Therefore, the amount of phase loss at the crossover frequency can be calculated given the known time delays in the digital system.

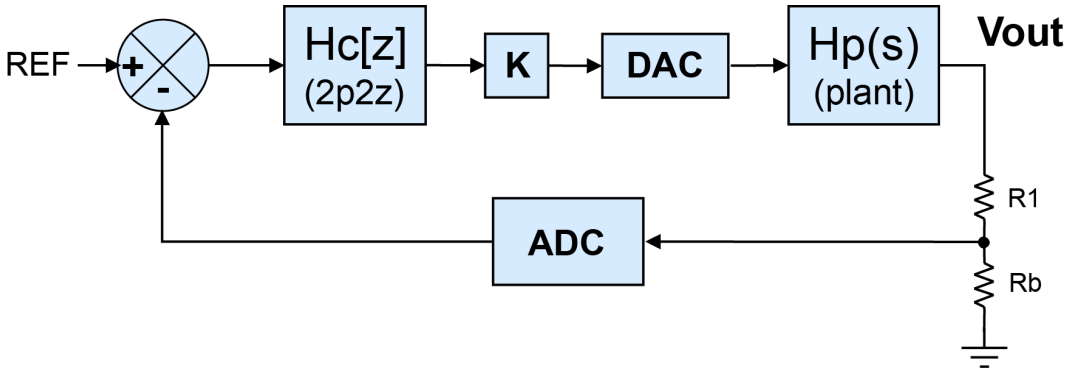
$$p.e. = -2\pi f_X T_D \tag{29}$$

The expected phase erosion at the crossover frequency can be added to the desired phase margin such that this phase loss is compensated for at design time. This can be achieved by adding the expected phase erosion to the phase margin specified in Equation 29. This will adjust the location of the compensator zero to add the require phase boost and compensate for this phase loss such that the resulting overall phase margin meets the specification.

9.4 Digital gains

The compensator poles and zeros have been analytically calculated to achieve the specified crossover frequency and phase margin. If the additional gains within the digital system are not accounted for, then the overall loop gain, and thus phase margin, will be incorrect.

Figure 15. Additional gains within the digital system



Consider the block diagram of the digital control loop shown in Figure 15. The output voltage, Vout, will need to be scaled down to a voltage suitable for sampling by the ADC onboard the MCU. This is the purpose of the potential divider formed by R1 and Rb. This will also determine the setpoint value that the controller must regulate to. The gain of the pre-ADC scaling potential divider can be calculated in Equation 30.

$$G_{PD} = \frac{R_b}{R_1 + R_b} \tag{30}$$

Then the ADC on the MCU will convert the voltage, which is between 0 V and 3.3 V, and provide a 12-bit output, a number between 0 and 4095. Therefore, the gain of the ADC can be calculated using Equation 31.

$$G_{ADC} = \frac{2^{12} - 1}{3.3V} \tag{31}$$

The output of the controller will be used to update the DAC register, which will set the demand peak current level for the internal comparator. The 12-bit DAC gives an output voltage of 3.3V for an input of 4095. Therefore, the DAC gain can be calculated using Equation 32.

$$G_{DAC} = \frac{3.3V}{2^{12} - 1} \tag{32}$$

In order to achieve the correct loop gain, the controller must negate these additional gains. That is achieved using the scaling factor K, which can be calculated in Equation 33.

$$K = \frac{1}{G_{PD} G_{ADC} G_{DAC}} \tag{33}$$

Finally, the ADC output is compared with the digital reference set point. This digital reference must be in the same scaling as the ADC output and take into account the divider on the input of the ADC. Therefore, the reference can be calculated using Equation 34.

$$REF = V_{OUT} G_{PD} G_{ADC} \tag{34}$$

10 Digital average current mode implementation

For the digital implementation, the MCU needs to sample the input voltage, output voltage and the inductor current. These signals will require preconditioning before feeding to the ADC for sampling. These issues are discussed in this section along with the block diagram for the digital implementation.

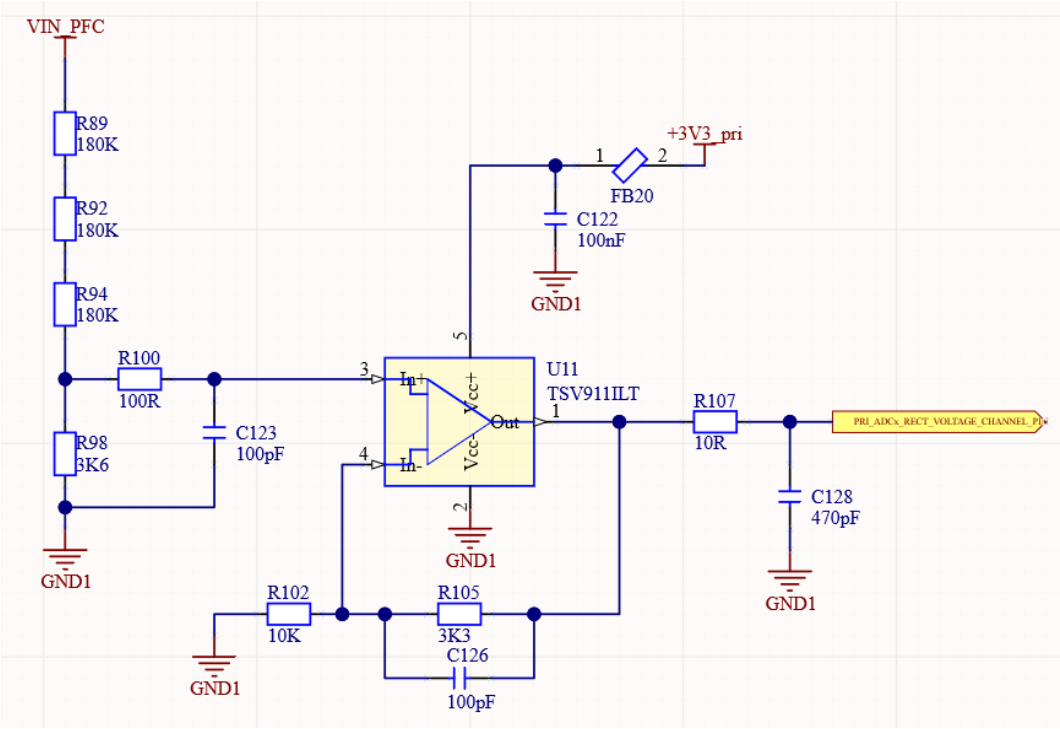
10.1 Sampling the input voltage

The input voltage is used as both the reference to the current loop controller, to ensure the input current tracks input voltage and is in phase with it, and also to provide the voltage feedforward term to provide good line regulation.

The input voltage, for universal mains input, can be up to 265 Vac. This needs to be scaled down to 3.3 V to be sampled by the ADC. Therefore, a scaling factor of 0.0088 is used. This is achieved using a potential divider and op-amp buffer as shown in Figure 16.

The input voltage scaling needs to be taken into account in the software project to negate the additional gains introduced by this pre-ADC sampling divider and buffer.

Figure 16. Input voltage scaling (schematic)

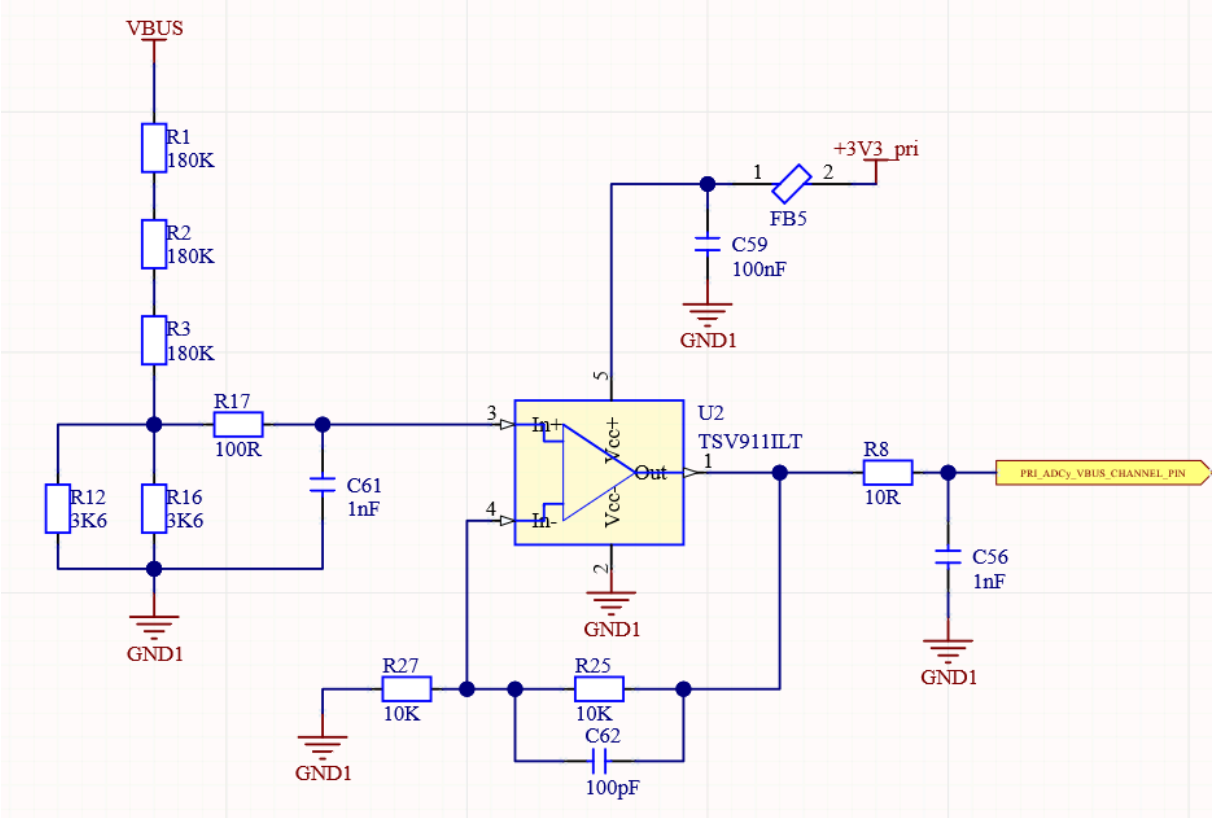


10.2 Sampling the output voltage

The output voltage is sampled and compared with the demand output voltage to calculate the voltage error. This is then used as an input to the slow voltage loop controller the output of which closes the voltage loop.

The nominal output voltage is between 400-410 Vdc. However, considering an overshoot after a large load step, the output voltage could reach up to 450 Vdc. Therefore, a scaling factor or 0.0066 is used to scale this down to the 3.3 V maximum required by the ADC. This is again achieved using a potential divider and op amp buffer as shown in the following figure.

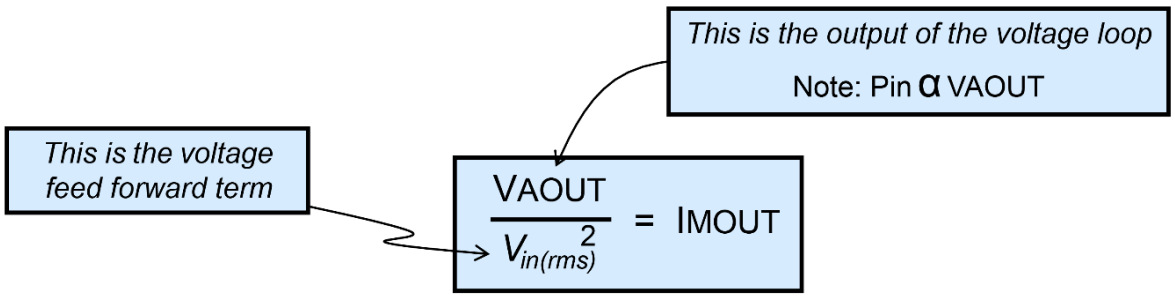
Figure 17. **Output voltage scaling (schematic)**



10.3 Calculating the demand current reference

The output of the voltage loop controller and input-voltage feedforward filter are used as inputs to the multiplier block shown below. This is the IMOUT term in the software example. IMOUT is then multiplied by the instantaneous value of the input voltage at that moment in time to give the demand average current value for that switching cycle.

Figure 18. **Demand current reference block diagram**



The demand current can then be calculated in Equation 35.

$$I_{REF} = I_{in(pk)}\sin(\omega t) I_{MOUT} \quad (35)$$

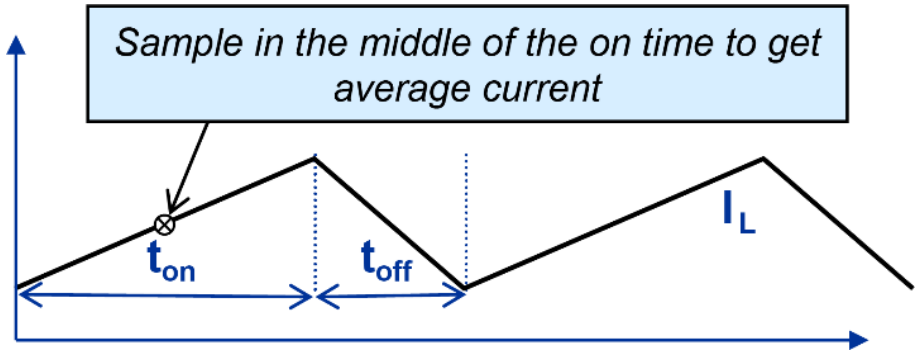
Where $I_{in(pk)}\sin(\omega t)$ is the sampled input voltage converted to a current.

10.4 Sampling the average current

The traditional analog average current mode control scheme implementation typically senses the return current and the current averaging operation happens automatically within the continuous time control loop. For a digital implementation, the average current must be accurately sampled using the ADC onboard the STM32 MCU.

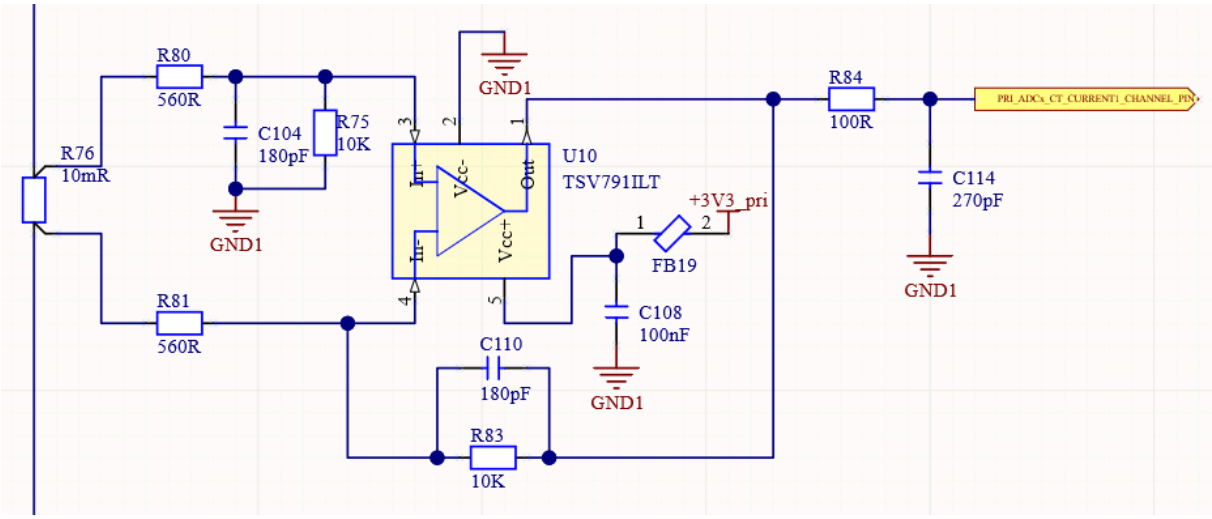
To obtain the average current, inductor current in each phase is sampled in the middle of the on time of the switch. This equates to the middle of the rise of the inductor current, and in CCM, this is the average current.

Figure 19. Sample principle for the average current



To sample the current, a current sense resistor is used on the source of the PFC MOSFET. The voltage across this resistor is then scaled by a differential amplifier as shown in Figure 20. The overall gain is 17.86. In theory, this would allow measuring a peak current of 18.5 A through the 10 mR current sense resistor.

Figure 20. Average current measurement scaling (schematic)

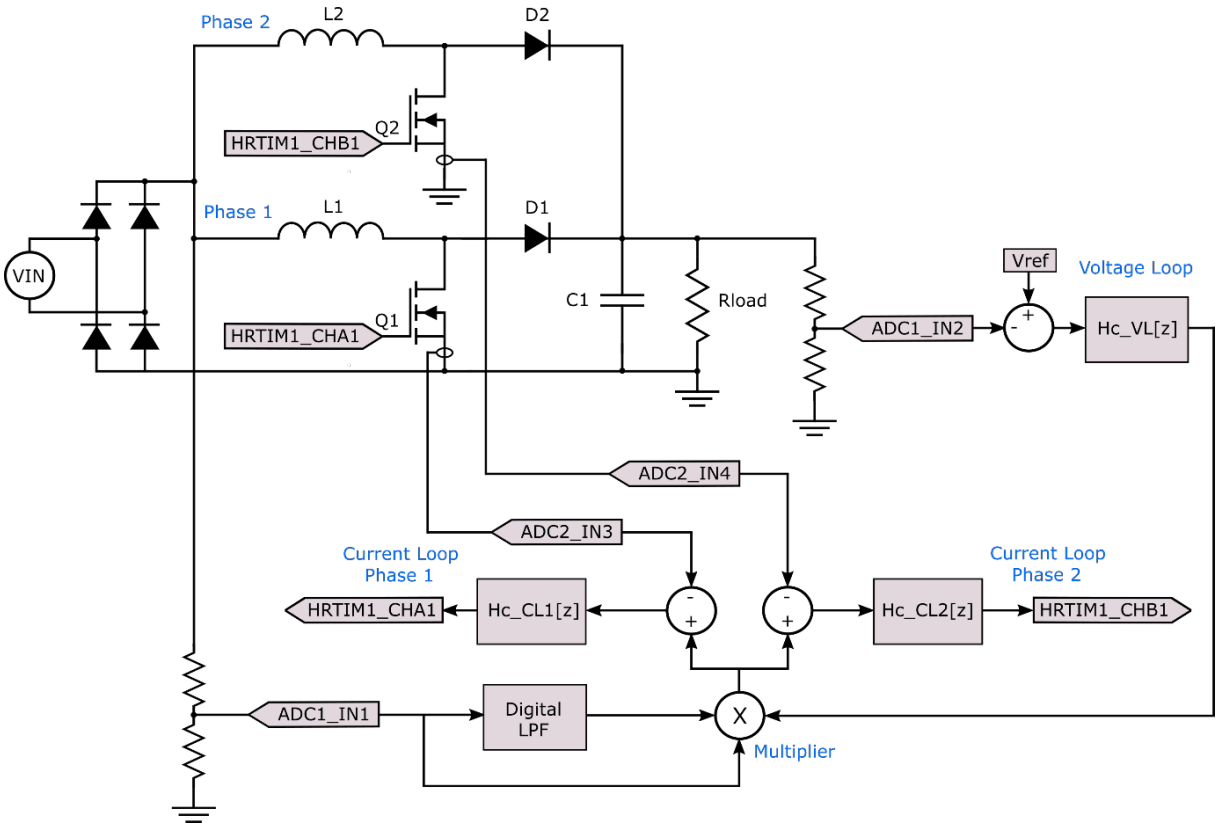


10.5 Final block diagram

The block diagram for the digital average current mode implementation is shown in Figure 21.

This illustrates the operation for a system with one interleaved boost power stage. The output of the multiplier, scaled by the instantaneous value of the input voltage, is compared to the sampled average inductor current. The difference between these two values, the error term, is then used as an input to the current loop controller. The output of the current loop controller is the new demand value of duty cycle for the following switching period. This closes the current loop.

Figure 21. **Digital implementation of peak current mode control**



11 Software implementation

11.1 Targeted application

The following configuration sets up the STM32G474 MCU to operate the CCM Boost PFC under average current mode using the onboard peripherals, including the ADC, DMA, HRTIM, and DAC. The example software project to accompany this application note is called “STEVAL-ISA172V3-primary” and is available from www.biricha.com/STEVAL-ISA172V3

11.2 Peripheral configuration using STM32CubeMX

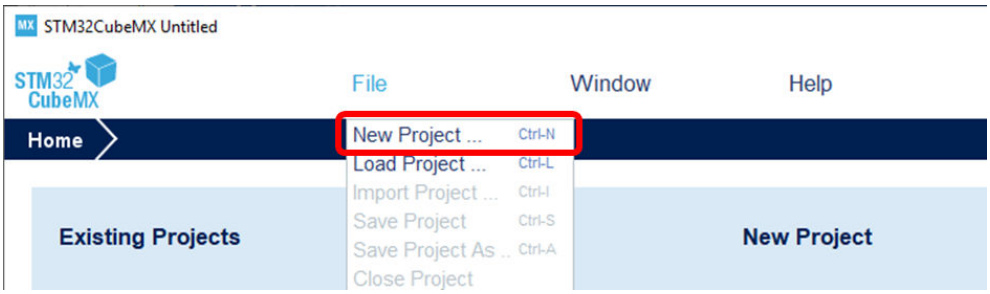
The following section contains step-by-step instructions for recreating the STM32CubeMX project for the boost PFC stage under average current mode control on the STEVAL-ISA172V3 kit. This complete project can be downloaded by following the links provided within this application note appendix. However, the full configuration is included here for completeness.

Step 1. Open STM32CubeMX by clicking on the [**MX**] icon.

We will now create a new STM32CubeMX "Project". This project configures the MCU peripherals and also generates an IAR project. IAR is used to compile and link the code as well as for programming and debugging the MCU.

Step 2. Within the STM32CubeMX window click on [**File**]>[**New Project**].

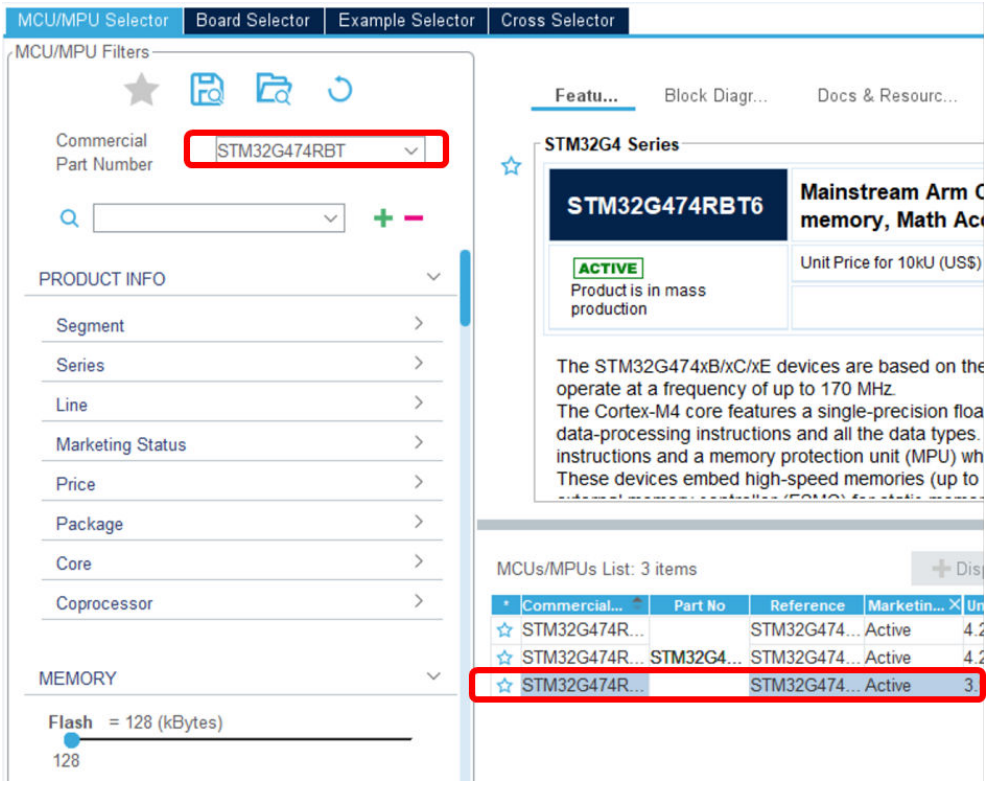
Figure 22. STM32CubeMX new project creation window



The new project device selector window will now open.

Step 3. Within this window, click on the [**MCU/MPU selector**] tab and filter the MCUs by entering *STM32G474RBT* in the [**Commercial Part Number box**].

Figure 23. STM32CubeMX MCU/MPU selection

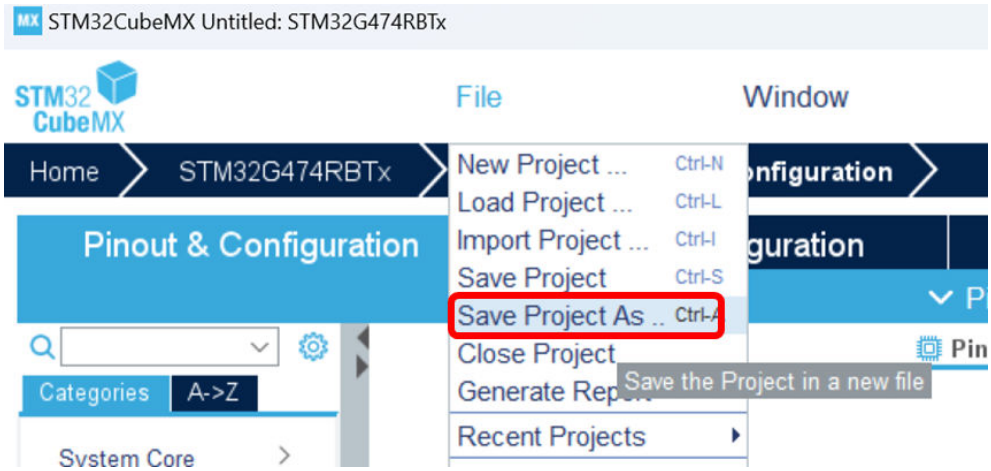


This should filter down the available MCUs on the right-hand side of this window to include the *STM32G474RBT6* option.

Step 4. Double-click on this MCU within the table.

Step 5. Before making any changes to the project, save the project by going to [**File**]>[**Save project As..**].

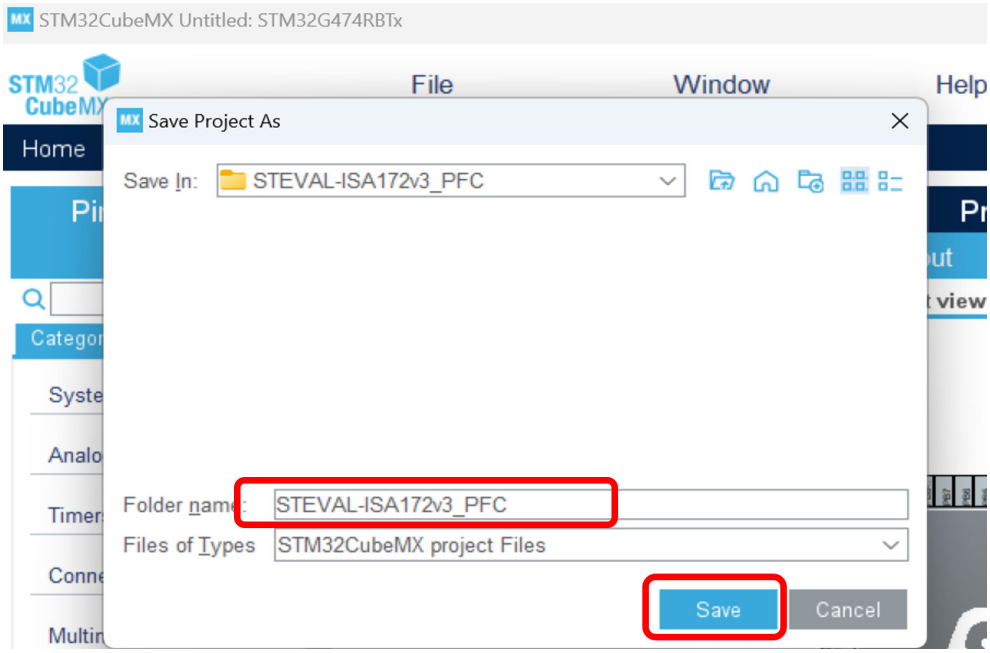
Figure 24. STM32CubeMX MCU/MPU save project



The name which you give to the folder, *Folder name*, will also be the name of the project. If this folder does not exist it will be created for you.

Step 6. Click [**Save**] when done.

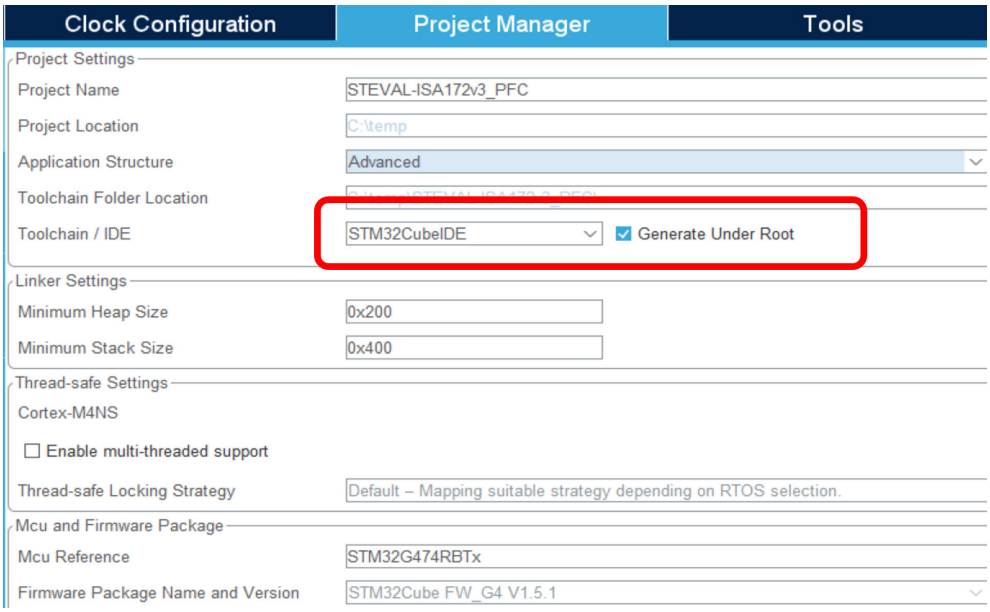
Figure 25. Save project window



Step 7. On the right-hand side of the main window, click [**Project Manager**] and select your preferred toolchain and version from the dropdown list as shown below.

This application note will be using the STM32CubeIDE tool.

Figure 26. STM32CubeMX project manager configuration



11.2.1 Clock Configuration

Before configuring the clock, the MCU pins for the high-speed external oscillator must be configured.

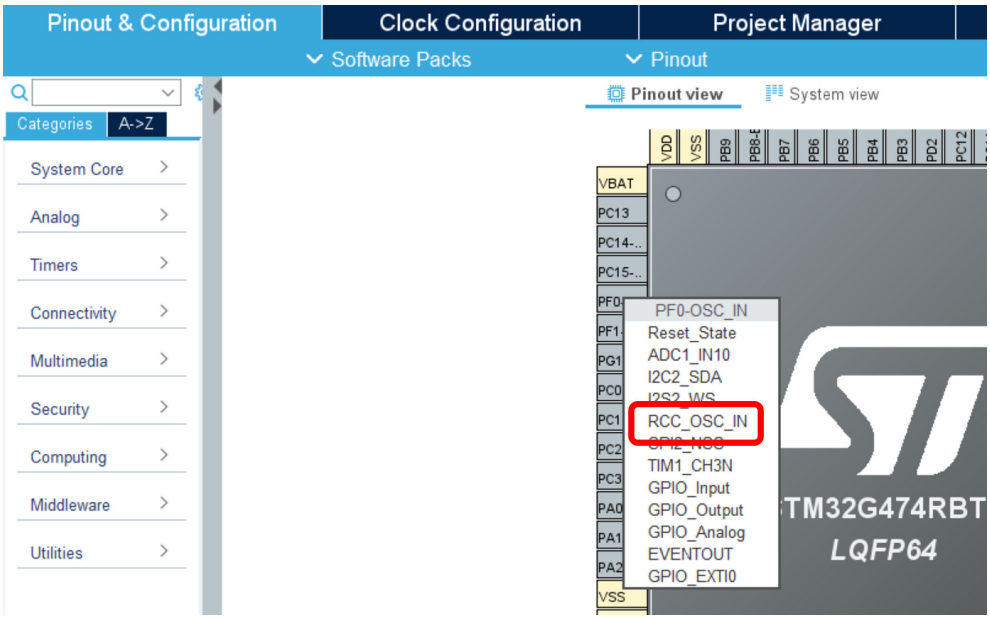
Step 1. Select the [**Pinout & Configuration**] tab along the top of the main STM32CubeMX window.

Step 2. Locate the pin *PF0-OSC_IN* and left click on it.

A menu will pop up with the configuration options for this pin.

Step 3. Select [**RCC_OSC_IN**] from the list.

Figure 27. Clock pin configuration window



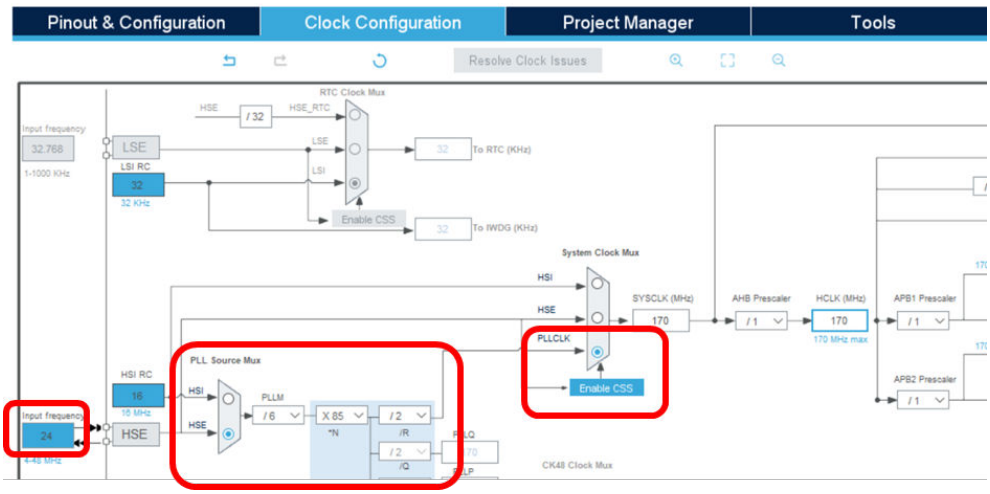
Step 4. Repeat this for *PF1-OSC_OUT* and select [**RCC_OSC_OUT**].
Both of these pins should now be highlighted green.

Step 5. Select the [**Clock Configuration**] tab along the top of the main STM32CubeMX window.

Step 6. Locate the following settings and change as described below.
These settings are highlighted in the image below.

- Input Frequency: 24 MHz
- PLL Source Mux: HSE
- PLLM: /6
- *N X85
- System Clock Mux: PLLCLK

Figure 28. Clock configuration window



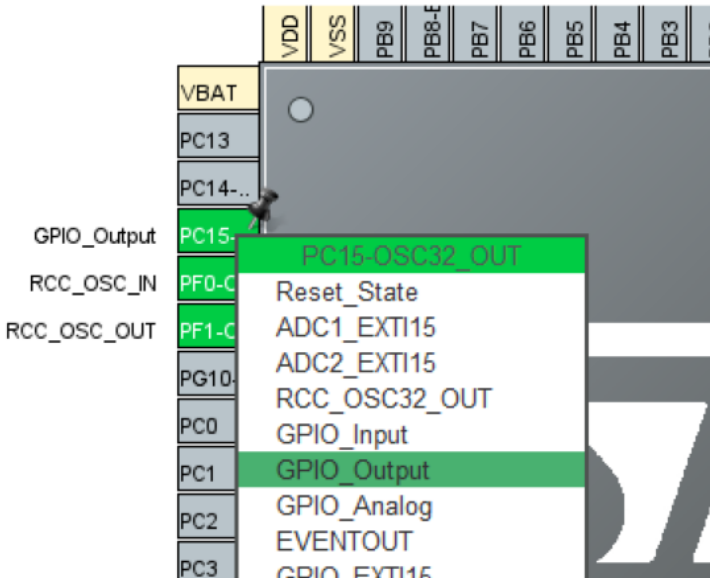
11.2.2 GPIO Peripheral configuration

For this application note, a digital pin will be configured to allow timing measurements to be performed.

Step 1. On the [**Pinout & Configuration**] tab, locate the pin PB9 towards the top left of the microcontroller.

Step 2. Left click on the pin PC15 and select [**GPIO_Output**] as shown below.

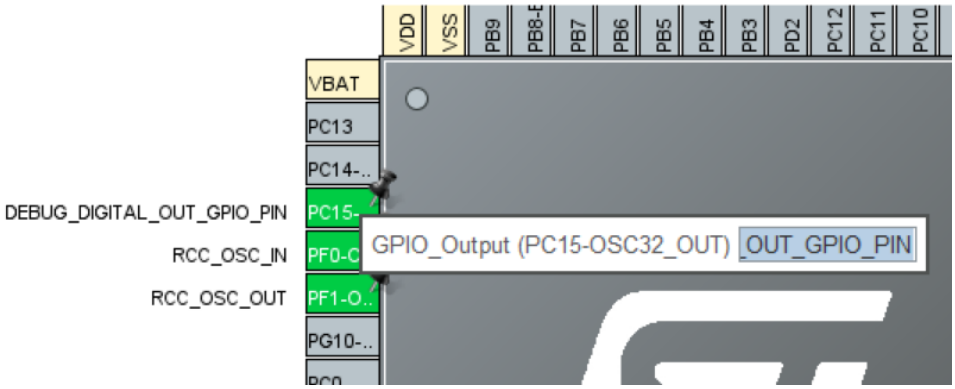
Figure 29. GPIO pin configuration window



Step 3. Then, right click on PC15 and select [**Enter User Label**].
This allows us to change the name of the pin so that it can be easily referenced within our code.

Step 4. This pin will be called [**DEBUG_DIGITAL_OUT_GPIO_PIN**]. Enter this in the popup box as per the image below.

Figure 30. STM32CubeMX GPIO output pin renaming



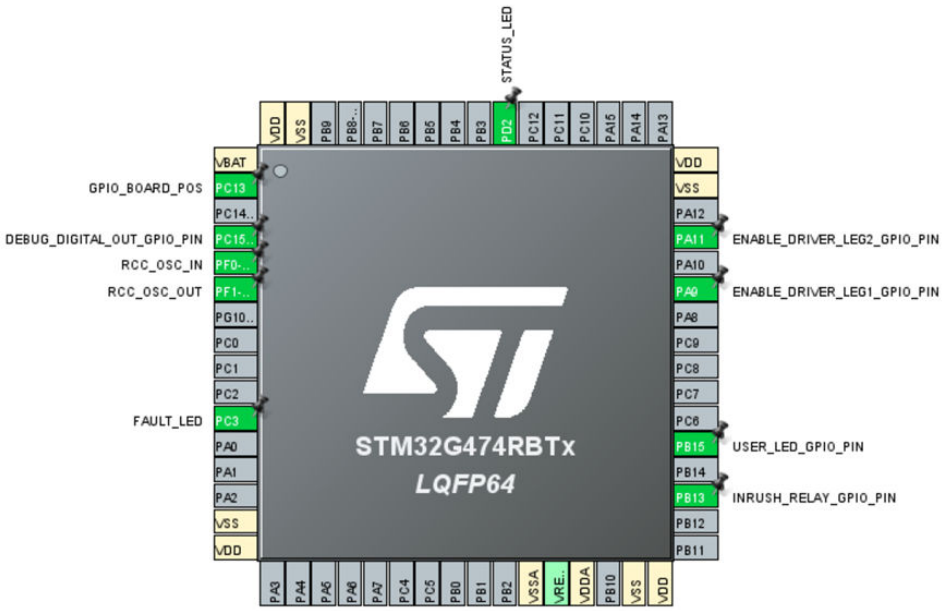
Step 5. Repeat this configuration process for the pins in the following table. The peripheral pins will be configured later.

Table 3. GPIO pin configurations

Pin	Input or Output	Name
PA9	Output	ENABLE_DRIVER_LEG1_GPIO_PIN
PA11	Output	ENABLE_DRIVER_LEG2_GPIO_PIN
PB13	Output	INRUSH_RELAY_GPIO_PIN
PB15	Output	USER_LED_GPIO_PIN
PC3	Output	FAULT_LED
PD2	Output	STATUS_LED
PC13	Input	GPIO_BOARD_POS

The pins should then be configured as per the image below.

Figure 31. All renamed GPIOs



The GPIO configuration is now complete.

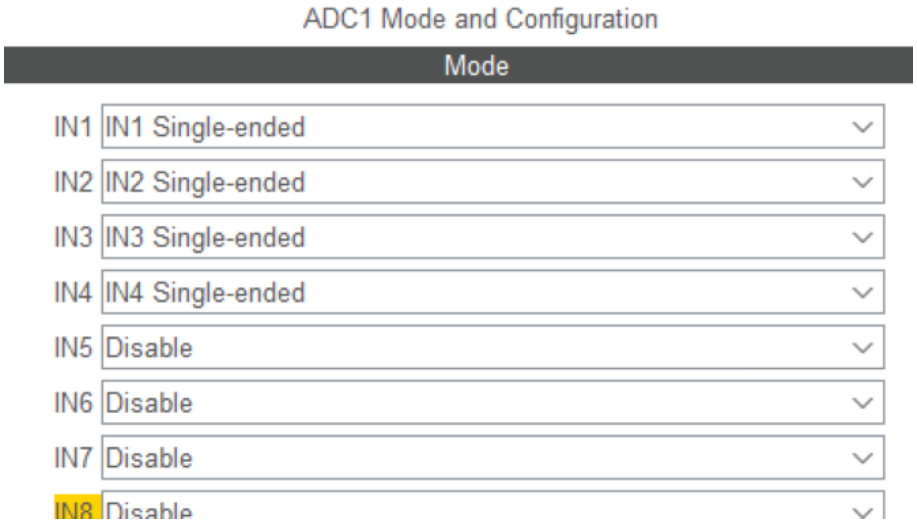
11.2.3 ADC/FMAC peripheral configuration

The peripherals can now be configured.

Step 1. On the top menu, select [**Pinout & Configuration**] and then on the left-hand pane, expand the [**Analog**] list and select [**ADC1**].

Step 2. Set ADC inputs IN1 and IN4 as [**single-ended**] using the drop-down box as per the image below. These will be used to sample the input currents and voltages.

Figure 32. ADC1 pin configuration window



Step 3. On the pin-out view on the right-hand side, rename these pins to reflect the signal that is being sampled as per the table below.

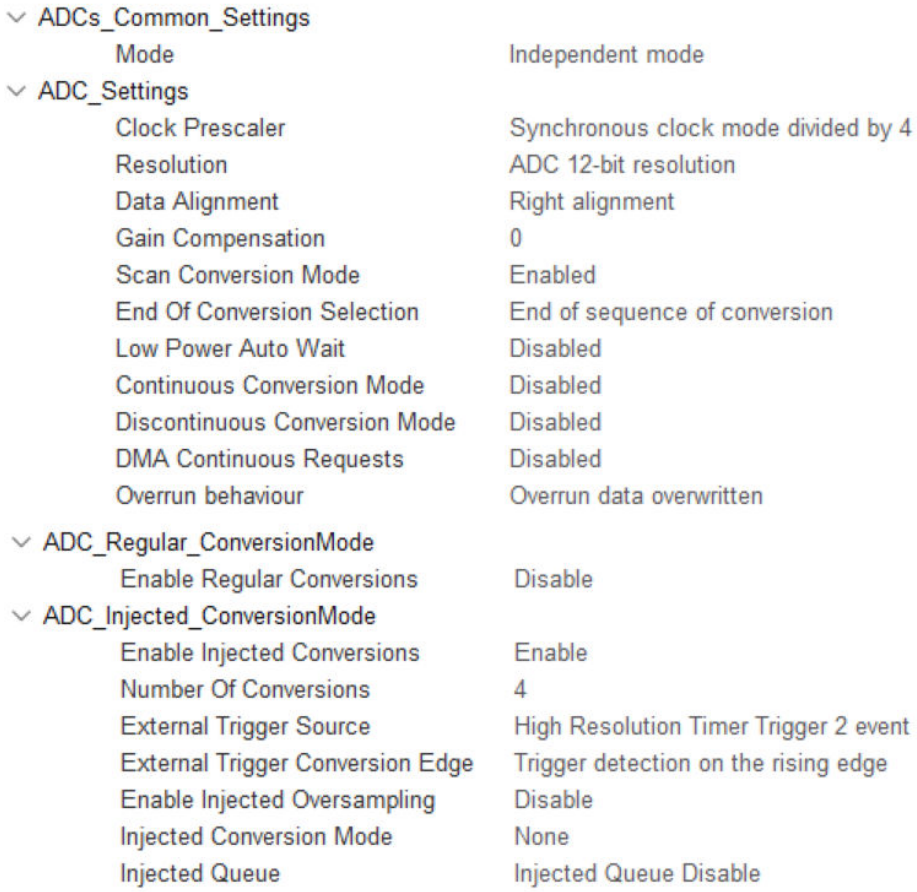
Table 4. ADC1 pin configurations

Pin	ADC Channel	Name
PA0	ADC1 IN1	ADCx_SHUNT_CURRENT_CHANNEL_PIN
PA1	ADC1 IN2	ADCx_CT_CURRENT1_CHANNEL_PIN
PA2	ADC1 IN3	ADCx_MAIN_VOLTAGE_CHANNEL_PIN
PA3	ADC1 IN4	ADCx_RECT_VOLTAGE_CHANNEL_PIN

Step 4. In the ADC1 configuration pane, click [**Parameter Settings**] and apply the following settings:

- Scan Conversion Mode: Enabled (need to add the number of conversions first)
- End of Conversion Selection: End of conversion sequence
- Overrun behavior: Overrun data overwritten
- Enable regular conversions: Disabled
- Enable injection conversions: Enabled
- Number of conversions: 4
- External trigger source: High resolution Timer Trigger 2 Event
- External trigger conversion edge: Trigger detection on rising edge

Figure 33. ADC1 mode configuration



The conversion ranks are now entered. This is the order in which the ADC inputs will be sampled:
Rank 1:

- Channel: Channel 2
- Sampling Time: 12.5 cycles
- Offset Number: No offset

Rank 2:

- Channel: Channel 1
- Sampling Time: 24.5 cycles
- Offset Number: No offset

Rank 3:

– Channel: Channel 3
– Sampling Time: 24.5 cycles
– Offset Number: No offset

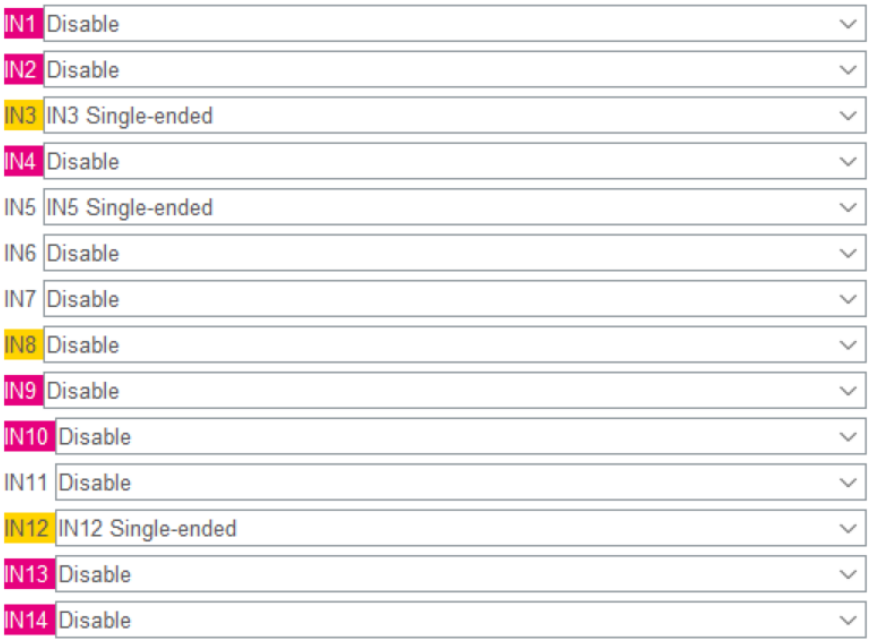
Rank 4:

– Channel: Channel 4
– Sampling Time: 24.5 cycles
– Offset Number: No offset

This completes the configuration of ADC1.

Step 5. Next, select [**ADC2**] from the left-hand pane and enable IN3, IN5 and IN12 as *single-ended* using the drop-down box as per the image below.

Figure 34. ADC2 pin configuration window



Step 6. On the pinout view on the right-hand side, rename this ADC pin to reflect the signal that is being sampled as per the table below.

Table 5. STM32CubeMX ADC2 pin renaming

Pin	ADC Channel	Name
PA6	ADC2 IN3	ADCy_VBUS_CHANNEL_PIN
PC4	ADC2 IN5	ADCz_CT_CURRENT2_CHANNEL_PIN
PB2	ADC2 IN12	ADCy_TEMP_CHANNEL_PIN

Step 7. In the ADC2 configuration pane, apply the following settings:

- Scan Conversion Mode: Enabled (need to add the number of conversions first)
- End of Conversion Selection: End of conversion sequence
- Overrun behavior: Overrun data overwritten
- Enable regular conversions: Disabled
- Enable injection conversions: Enabled
- Number of conversions: 4
- External trigger source: High resolution Timer Trigger 4 Event
- External trigger conversion edge: Trigger detection on rising edge

Figure 35. ADC2 mode configuration window



The conversion ranks are now entered. This is the order in which the ADC inputs will be sampled:
Rank 1:

- Channel: Channel 5
- Sampling Time: 12.5 cycles
- Offset Number: No offset

Rank 2:

- Channel: Channel 5
- Sampling Time: 12.5 cycles
- Offset Number: No offset

Rank 3:

- Channel: Channel 3
- Sampling Time: 24.5 cycles
- Offset Number: No offset

Rank 4:

– Channel: Channel 12
– Sampling Time: 24.5 cycles
– Offset Number: No offset

The ADC2 configuration is now complete.

11.2.4 Comparator and DAC configuration

The remaining analog peripherals can now be configured.

Step 1. From the left-hand side analog peripheral list, enable the comparator module 1, *COMP1*, by ticking the [**Input [+]**] box and select [**Input [-]**] as *3/4 Internal Vref*.

This comparator module will be used to detect an overcurrent condition of the PFC MOSFETs.

Step 2. The COMP2 non-inverting input pin can be renamed as listed in Table 6 on the Pinout Configuration diagram to match the signal that is being routed to it.

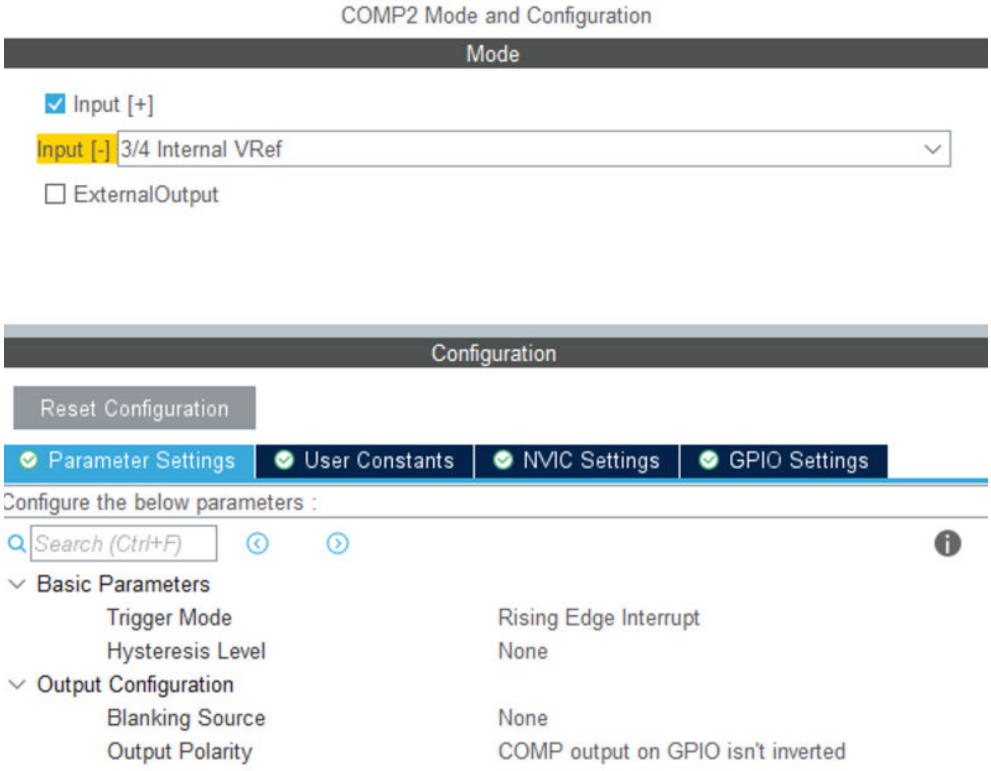
In this case, the current transducer for phase 2.

Table 6. COMP2 pin configurations

Pin	Comp input	Name
PA7	COMP2 Input [+]	COMP2_INP_CT2

Step 3. For the configuration options, set the [**Trigger Mode**] to *Rising Edge Interrupt*. The configuration should now match the figure below.

Figure 36. COMP2 configuration window



Step 4. Repeat this process for COMP4. Now, the current transducer for phase 1 is being routed to the non-inverting input, so rename the following pin according to the following table.

Table 7. COMP4 pin configurations

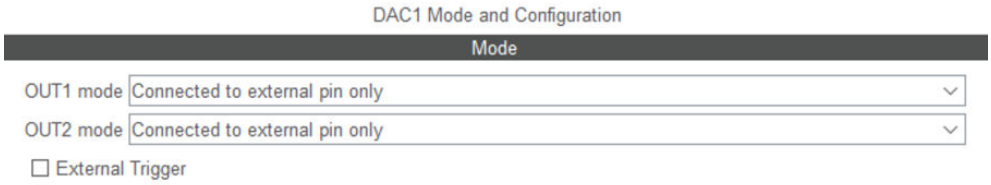
Pin	Comp input	Name
PB0	COMP4 Input [+]	COMP4_INP_CT1

This process can be repeated for COMP6 which can be used to monitor the return current; however, this option is not used on this EVM.

Step 5. The on-board DAC is used for debugging real-time signals using the oscilloscope. Set DAC1 [**Out 1 Mode**] to *Connected to External Pin Only* and repeat this for the [**Out 2 Mode**].

The pins will not be renamed as they have no other function.

Figure 37. DAC1 configuration window



None of the DAC configuration settings need to be changed from default as presented in Figure 37

11.2.5 HRTIM configuration

Next, the hi-resolution timer module will be configured to generate the PWM.

Step 1. On the left-hand side peripherals pane, expand the [**Timers**] category and click on [**HRTIM1**].

The PSFB converter requires multiple timers to be configured for the input bridge FETs, synchronous rectification FETs and the active clamp FET.

Step 2. The EVM has two interleaved PFC stages, and therefore two timers must be configured in order to drive the switches of each stage. For this example, [**Timer A**] and [**Timer B**] are required to drive the switches. Furthermore, the [**Master Timer**] is used to synchronize the two phases and [**Timer C**] is used to run the slow voltage loop – this requires no external output. As there is only a single low-side MOSFET, only timer outputs TA1 and TB1 outputs are required. Enable these as in the figure below.

Table 8. HRTIM pin configurations

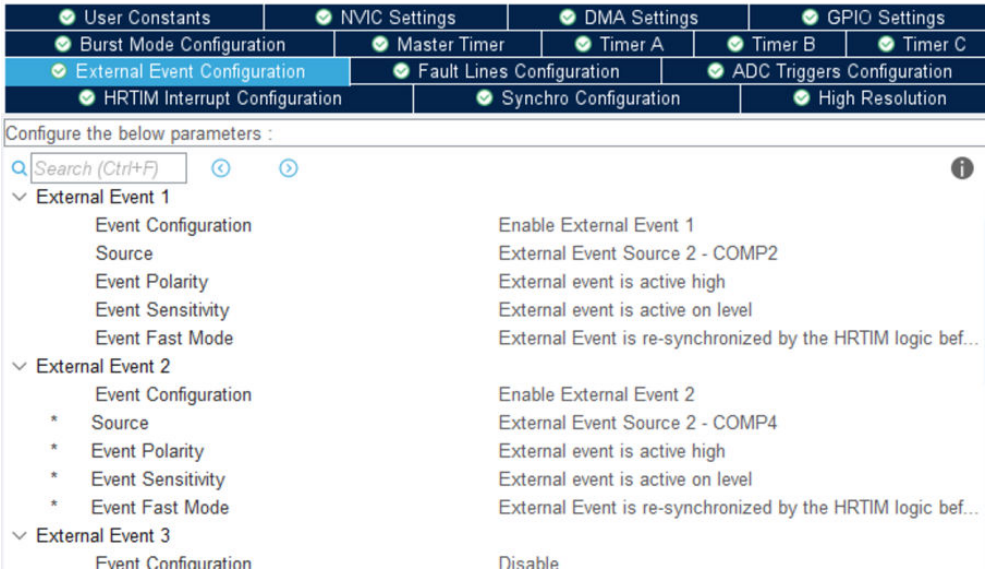
Pin	PWM Output	Name
PA8	Timer A Out 1	PWM_LEG1_GPIO_PIN
PA10	Timer B Out 1	PWM_LEG2_GPIO_PIN

Step 3. Next, within the HRTIM1 configuration pane, click on [**External Event Configuration**]. Here we will connect the output of the comparator to the HRTIM module. Under [**External Event 1**] change the [**Event Configuration**] to *Enable External Event 1*.

The source of the external event is, by default, *External Event Source 2 – COMP2*. This is the comparator configured in the previous step.

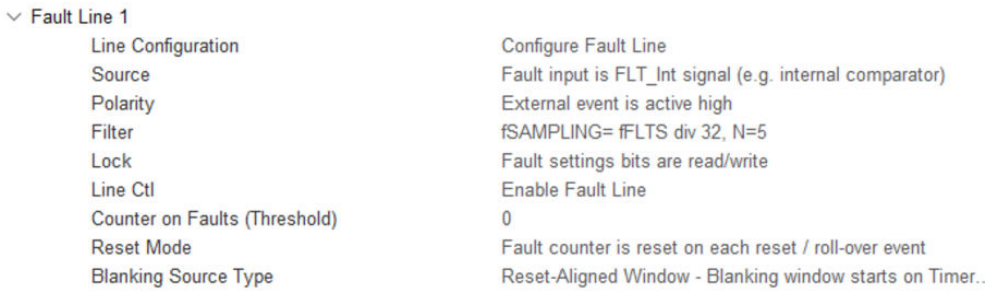
Step 4. Repeat this for the second comparator. Under [**External Event 2**], change the [**Event Configuration**] to *Enable External Event 2*. The source of the external event is, by default, *External Event Source 2 – COMP4*. This is shown in the following figure.

Figure 38. HRTIM external event configurations



Step 5. Now click the [**Fault Lines Configuration**] tab. For [**Fault Line 1**] set the [**Line Configuration**] to *Configure Fault Line*. Configure some filtering, set the [**Filter**] to *fSAMPLING = fFLTS div 32*, N=5". This is shown in the following figure.

Figure 39. HRTIM fault line configuration window



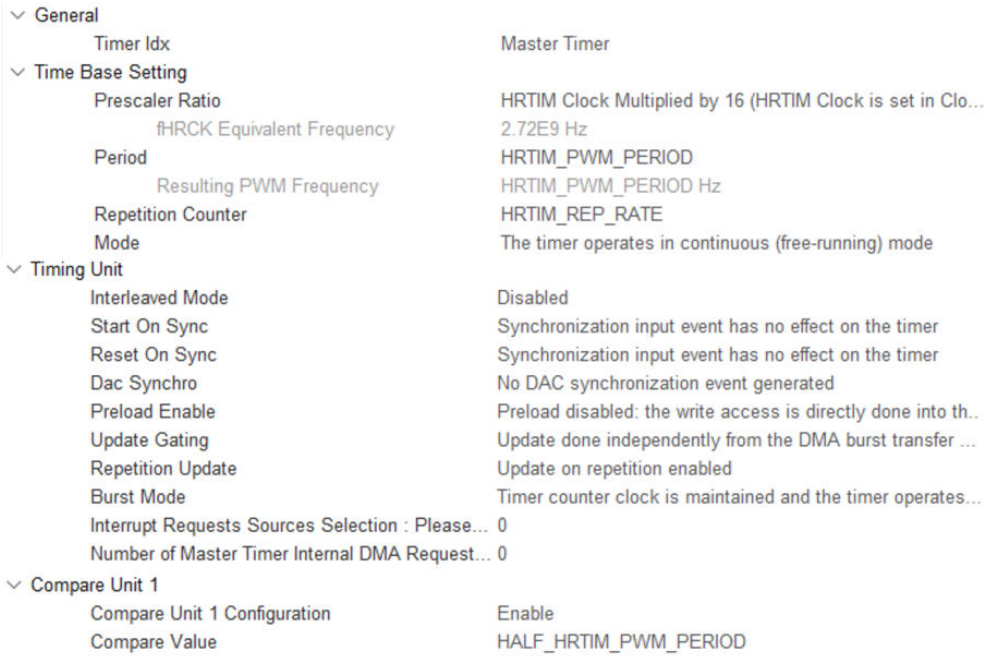
Step 6. Before configuring the individual timers, the master timer should be configured. Click on the [**Master Timer**] configuration tab. Within the time base settings, change the [**Prescaler Ratio**] to [**HRTIM Clock Multiplied by 16**] as the PFC stage is switching at a relatively low frequency of 70 kHz, a high pre-scaler is not required.

Step 7. In the text entry box next to [**Period**], click the cog icon, and check the [**No Check**] setting. You may need to do this for several settings where text is entered instead of numbers. This will allow you to set the period value to *HRTIM_PWM_PERIOD*. The period will then be calculated in the code using a #define statement. The [**Repetition Counter**] is set to [**HRTIM_REP_RATE**].

Step 8. The next section on the [**Master Timer**] configuration tab is the timing unit settings. Here, change [**Preload Enable**] to [**Preload Disables**] and [**Repetition Update**] to *Update on repetition enabled*. Finally, enable [**Compare Unit 1**] and set the [**Compare Value**] to *HALF_HRTIM_PWM_PERIOD*.

This completes the master time configuration. The configuration options should look like the figure below.

Figure 40. HRTIM Master timer configuration window



Step 9. Now click on the [**Timer A**] configuration tab. First, the time base settings must be configured. Set the [**Prescaler Ratio**] to *HRTIM Clock Multiplied by 16*.

Step 10. Then, in the text entry box next to [**Period**] click the cog icon, and check the [**No Check**] setting. This will allow you to set the period value to *HRTIM_PWM_PERIOD*.

The period will then be calculated in the code using a `#define` statement.

Step 11. The next section on the [**Timer A**] configuration tab is the timing unit settings. Here, change the [**Repetition Update**] to *Update on repetition enabled*.

This will allow the master time to update the counter of this timer ensuring correct phase shift between the PWM outputs.

Step 12. For [**Number of Faults to enable**], type in *1*. For the [**1st Fault Source**] set *Fault 1 enabled*.

Step 13. Under [**Reset Trigger Sources Selection**], type in *1*, and select *The timer counter is reset upon master timer period event* from the drop-down box.

This will force Timer A to be in sync with the master timer.

Step 14. Under [**Interrupt Requests Sources Selection**] set this to *1*.

This will be set to a compare unit that will be configured for this timer in the next step.

Step 15. The compare units can now be configured as shown in Figure 44. The compare units are compared the counter register of this timer and actions can be taken when the compare units match the counter or the counter is greater than the compare unit value. For this average current mode PFC implementation, all four compare units will need to be configured as per Table 9. In order to enter these values, the [**No Check**] option must be selected for each [**Compare Value**] by clicking on the cog icon next to the text entry box.

Table 9. HRTIM comparison configuration

Compare unit	Compare value	Description
1	(uint16_t)(DUTY_CYCLE_MIN/2)	Sets the point at which the switch turns on
2	CS_BLANKING	The first few nanoseconds of the switching period to ignore switch spikes
3	(uint16_t)(DUTY_CYCLE_MIN/2)+1	Sets the point at which the switch turns off
4	HALF_HRTIM_PWM_PERIOD+ADC_SAMPLE_DELAY	The middle of the switching period to trigger the ADC

The other settings for each compare unit do not need to be changed from the default.

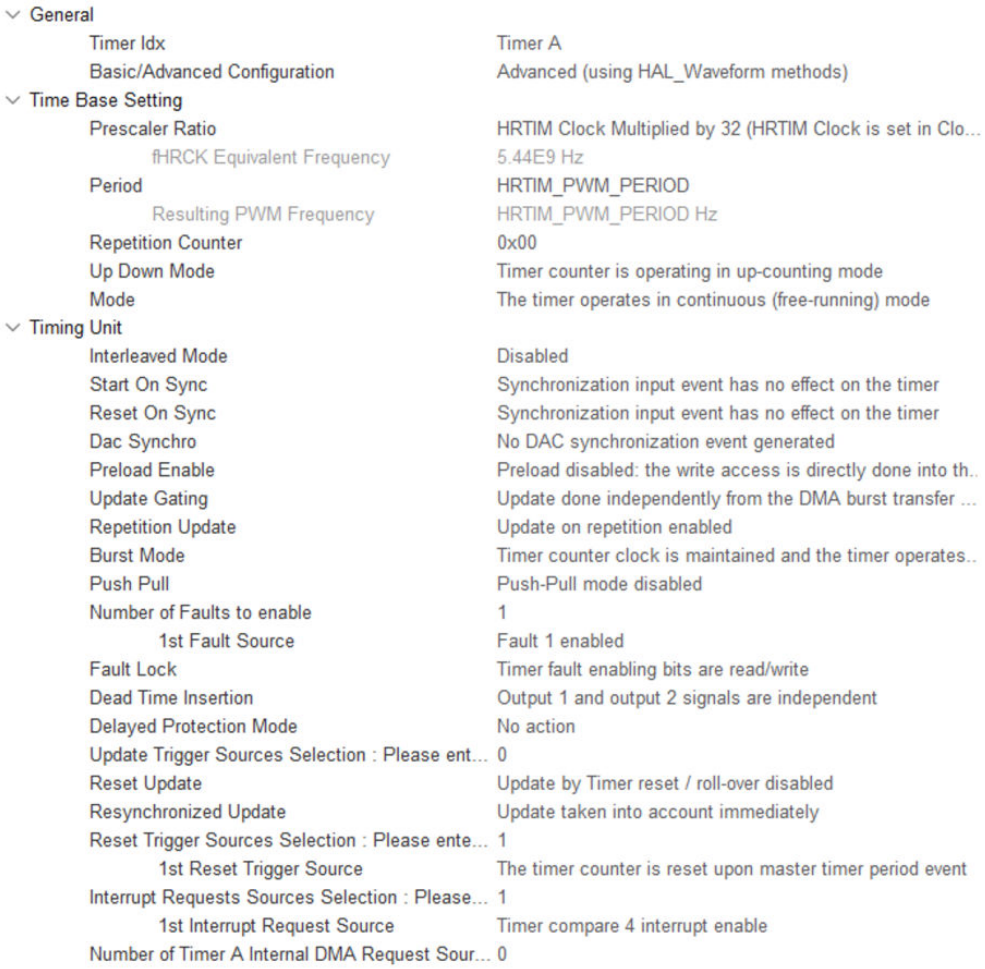
Figure 41. HRTIM TimerA comparator configuration window



Step 16. Now that the compare units have been configured, compare unit 4 can be selected as the trigger source for the interrupt request in the timing unit settings.

The timing units settings are complete and should match the figure below.

Figure 42. HRTIM TimerA configuration window



Step 17. The last section to configure on the [**Timer A**] configuration tab is the [**Output 1 Configuration**] as shown in Figure 43.

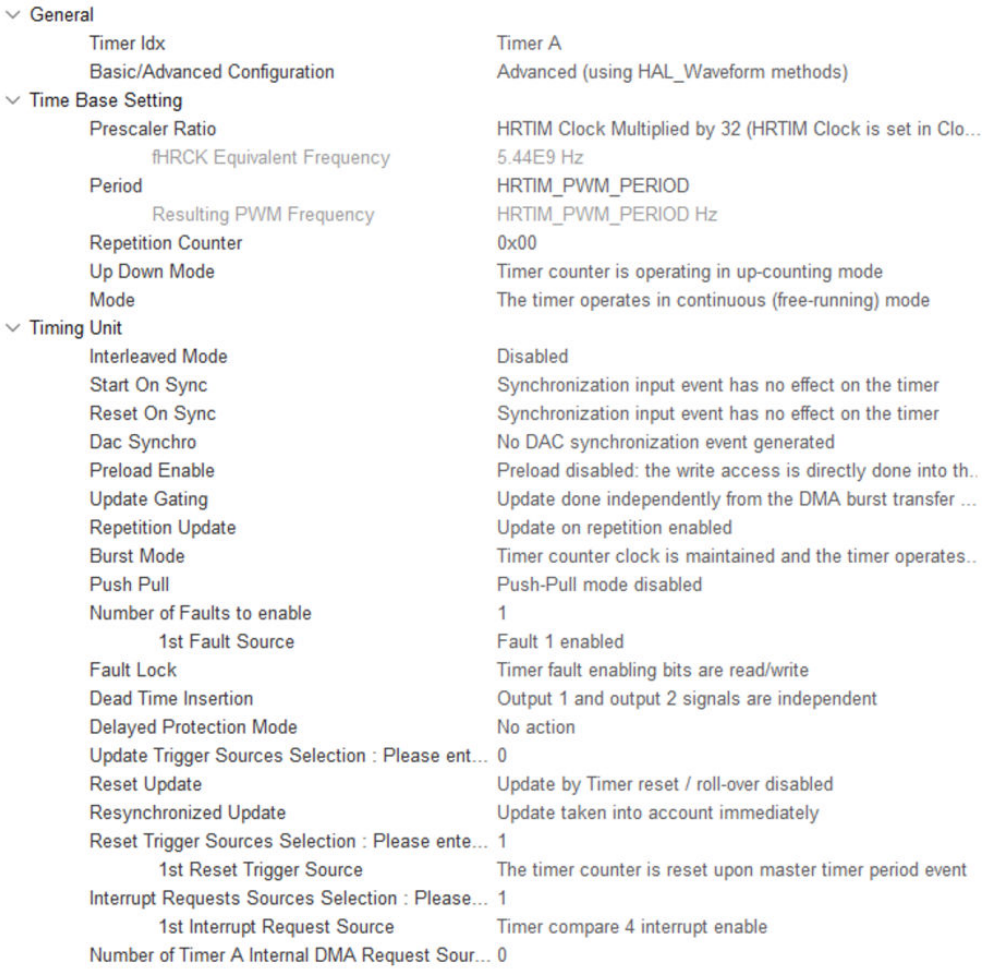
This is located towards the bottom of the tab.

Step 18. Under the [**Output 1 Configuration**] section, change the [**Set Source Selection**] number to *1*. Change the [**1st Set Source**] event to *Timer compare 1 event forces the output to its active state*.

Step 19. Change the [**Reset Source Selection**] number to *2*. Change the [**1st Reset Source**] event to *Timer compare 3 event forces the output to its inactive state*. Then change the [**2nd Reset Source**] event to *External event 2 forces the output to its inactive state*.

Step 20. Then set the [**Fault Level**] to *Output at inactive level when in FAULT state*.

Figure 43. HRTIM output1 configuration



Step 21. This process must now be repeated for [**Timer B**].

The only change in settings from the above are:

– Under the [**Reset Trigger Sources Selection**], the [**1st Reset Trigger Source**] should be set to *The timer is reset upon master timer Compare 1 event*.

– Set up [**External Event 1**] filtering rather than 2.

– Under the [**Output 1 Configuration**]>[**Reset Source Selection**], the [**2nd Reset Source**] should be set to *External Event 1 forces the output to its inactive state*.

Step 22. Moving on to [**Timer C**] configuration. This timer is used to run the slow loop functions within the PFC controller; therefore, it must be configured at a much slower operation frequency. On the [**Timer C**] configuration, tab set the time base settings [**Prescaler Ratio**] to *HRTIM Clock Divided by 4*.

Step 23. Then, in the text entry box next to [**Period**] set a decimal value of *6100*. This should result in a frequency of just less than 7 kHz. However this setting is not important as the slow loop interrupt will be triggered with another method, using repetition updates. Therefore, set the [**Repetition Counter**] value to decimal *10*.

Step 24. Within the timing unit settings, change [**Repetition Update**] to *Update on repetition enabled*.

This allows the master time to update the counter of this timer ensuring that is in sync with the other timers.

Step 25. Under [**Reset Trigger Sources Selection**] type in *1* and select *The timer counter is reset upon master timer period event* from the drop-down box. Under [**Interrupt Requests Sources Selection**], set this to *1*. The [**1st Interrupt Request Source**] is set to *Timer repetition interrupt enable*.

No compare units or outputs are configured for Timer C.

The final settings for Timer C should match the figure below.

Figure 44. HRTIM TIMERC configuration

∨ General	
Timer Idx	Timer C
Basic/Advanced Configuration	Advanced (using HAL_Waveform methods)
∨ Time Base Setting	
Prescaler Ratio	HRTIM Clock Divided by 4 (HRTIM Clock is set in Clock ...
fHRCK Equivalent Frequency	4.25E7 Hz
Period	6100
Resulting PWM Frequency	6967 Hz
Repetition Counter	10
Up Down Mode	Timer counter is operating in up-counting mode
Mode	The timer operates in continuous (free-running) mode
∨ Timing Unit	
Interleaved Mode	Disabled
Start On Sync	Synchronization input event has no effect on the timer
Reset On Sync	Synchronization input event has no effect on the timer
Dac Synchro	No DAC synchronization event generated
Preload Enable	Preload disabled: the write access is directly done into th..
Update Gating	Update done independently from the DMA burst transfer ...
Repetition Update	Update on repetition disabled
Burst Mode	Timer counter clock is maintained and the timer operates..
Push Pull	Push-Pull mode disabled
Number of Faults to enable	0
Fault Lock	Timer fault enabling bits are read/write
Dead Time Insertion	Output 1 and output 2 signals are independent
Delayed Protection Mode	No action
Update Trigger Sources Selection : Please ent...	0
Reset Update	Update by Timer reset / roll-over disabled
Resynchronized Update	Update taken into account immediately
Reset Trigger Sources Selection : Please ente...	1
1st Reset Trigger Source	The timer counter is reset upon master timer period event
Interrupt Requests Sources Selection : Please...	1
1st Interrupt Request Source	Timer repetition interrupt enable
Number of Timer C Internal DMA Request Sour...	0

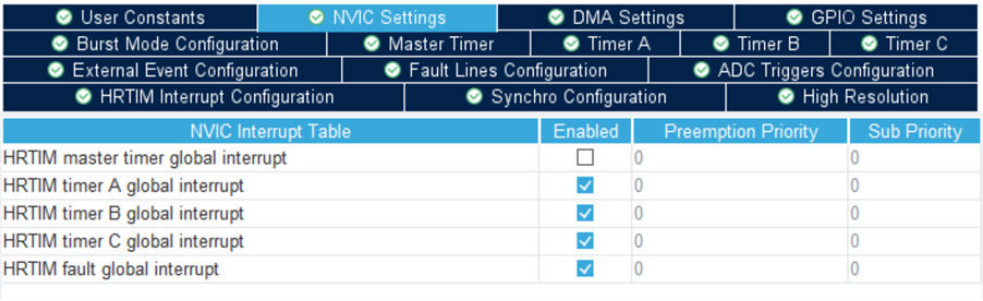
The interrupt table should match Figure 45.

Step 26. Then, select the [**NVIC**] configuration option along the row of HRTIM configuration tabs. This allows the interrupts to be for each timer. From the table, enable the following interrupts:

- "**HRTIM timer A global interrupt**"
- "**HRTIM timer B global interrupt**"
- "**HRTIM timer C global interrupt**"
- "**HRTIM fault global interrupt**"

The interrupt table should match the figure below.

Figure 45. HRTIM interrupts configuration window



Step 27. Furthermore, under the [**HRTIM Interrupt Configuration**] tab, set the [**1st Interrupt Source**] as the *Fault 1 Interrupt*.

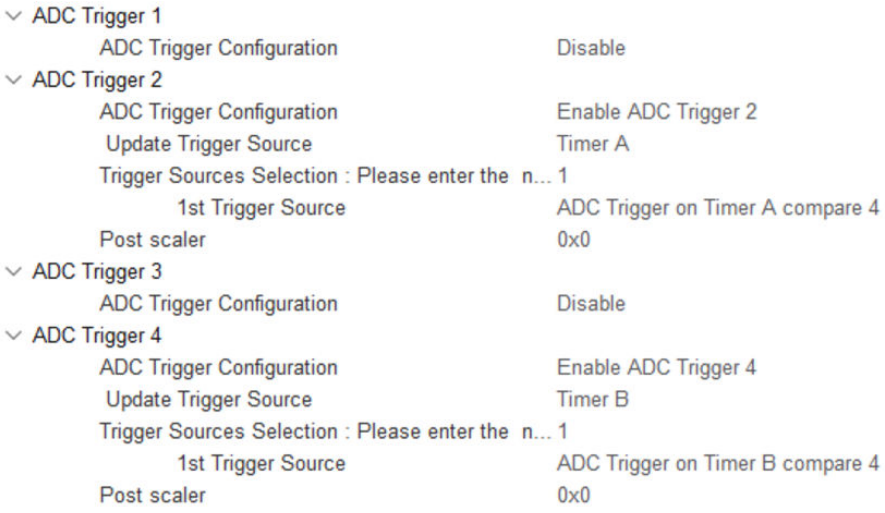
Step 28. Finally, the ADC trigger must be configured for the HRTIM1 module. Under [**HRTIM1**], select the [**ADC Triggers Configuration**] tab. Enable the [**ADC Trigger 2**] and set the [**Update Trigger Source**] to *Timer A*, enter the number of [**Trigger Sources Selection**] as *1*. From the [**1st Trigger Source**] drop down box, select *ADC Trigger on Timer A compare 4*

This is the event which will trigger the ADC for leg 1 of the interleaved PFC.

Step 29. Repeat this for leg 2. Enable the [**ADC Trigger 2**] and set the [**Update Trigger Source**] to *Timer B*, enter the number of [**Trigger Sources Selection**] as *1*. From the [**1st Trigger Source**] drop down box, select *ADC Trigger on Timer B compare 4*.

The ADC triggers should now look like the following figure.

Figure 46. HRTIM ADC usage configuration window



11.2.6 USART configuration

The USART module is used to provide communication between the primary and secondary side MCUs on the evaluation board. This allows the primary MCU to inform the secondary that the PFC bus is at the nominal voltage and the output can be started for example.

Step 1. To enable the USART, scroll down on the left-hand side peripherals list to [**Connectivity**] and expand this heading. Select [**USART1**] and change the [**mode**] to *Asynchronous*.

Step 2. Pins PB7 and PB6 are physically connected to the USART transceiver on the daughter card for this evaluation board. Therefore, you will need to manually move the USART RX pin from PC5 to PB7. To do this, simply left click on [**PB7**] and scroll down to the [**USART1_RX**] option and select it.

The pin should turn green and PC5 should go back to gray.
No configuration options need to be changed from default for this peripheral.

11.2.7 IRQ configuration

By default, STM32CubeMX will create interrupt handlers for the configured peripherals. These will be created in a separate interrupt handler .c file within our project. If the user wishes to create their own interrupt handler function, then the automatic generation of the IRQ handler function must be disabled for that peripheral.

In this application note, we are writing our own SysTick and Timer interrupt handler functions, so automatic generation of this IRQ handler must be disabled.

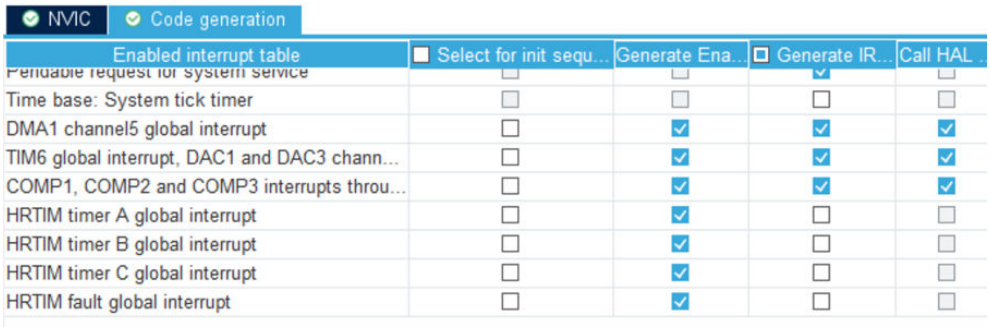
Step 1. To do this, click on the [**NVIC**] sub-category in the [**System Core**] category on the left-hand side of the window.

Step 2. Click on the [**Code Generation**] tab. Untick the [**Generate IRQ handler**] checkbox for:

- *Time base: System tick timer*
- *HRTIM timer A global interrupt*
- *HRTIM timer B global interrupt*
- *HRTIM timer C global interrupt*
- *HRTIM fault global interrupt*

The interrupt table should match the figure below.

Figure 47. NVIC configuration window



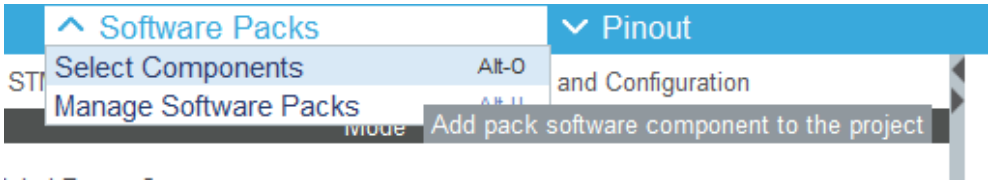
11.2.8 Debug Pins

Step 1. Finally, again under [**System Core**], click on the [**SYS**] peripheral and set the [**Debug**] mode to *Serial*.

11.3 Digital Power Pack Configuration using STM32CubeMX

With the X-CUBE-DPower pack installed, the option to configure the pack will be available from the [**Software Packs**]>[**Select Components**] menu option in STM32CubeMX.

Figure 48. Digital Power pack selection window



Step 1. To configure the X-CUBE-DPower pack for controlling the PFC stage of the PSU, the options shown in the following figure are selected. First, the [**Application**] is set to *PFC* under the [**Device**] options.

Step 2. Both [**PolesZeros Controller**] and [**Legacy**] options are ticked under the [**Library**] options and in the [**AC-DC_converter**] options the [**Interleaved Boost**] converter is selected.

Figure 49. Digital Power pack configuration window

STMicroelectronics.X-CUBE-DPower	✓	0.0.6	
Device DSMPS	✓	1.0.0	
Application	✓	1.0.0	PFC
Library Digital Power Converter	✓	1.1.0	
PolesZeros Controler	✓	1.1.0	☑
Legacy	✓	1.0.0	☑
AC-DC_converter in CCM	✓	1.0.0	
Totem Pole		1.0.0	☐
Interleaved Boost	✓	1.0.0	☑
DC-DC_converter in CCM		1.0.0	
Buck			Not selected
Boost		1.0.0	☐
Phase-Shifted Full-Bridge		1.0.0	☐

With these options selected, the X-CUBE-DPower pack will now be available under the [**Software Packs**] section of the [**Categories**] toolbar on the left-hand pane of STM32CubeMX.

Figure 50. Digital Power pack configured



11.3.1 Project settings

Step 1. With the X-CUBE-DPower pack enabled and pack options configured for the PSFB converter, the following [**mode**] options should be selected.

Figure 51. Digital Power pack mode selection



Step 2. The user must then configure the parameters according to their specific application. The parameters populated by default are those required for the STEVAL-ISA172V3 board.

Figure 52. PFC board parameters - 1

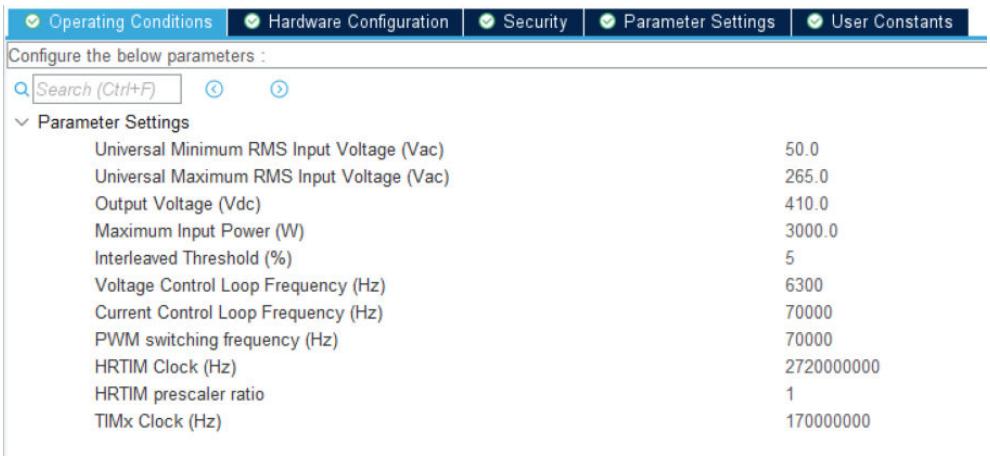


Table 10. PFC board parameter descriptions - 1

Parameter	Description
Parameter	**Description**
VinRmsMinV	Undervoltage level for the input voltage RMS (V)
VinRmsMaxV	Overvoltage level for the input voltage RMS (V)
Vout	Desired output bus voltage (V). This must be greater than peak of rectified input voltage.
PinMaxW	Calculates a ball-park figure for the saturation level of the voltage controller, to avoid excessive integral wind up. It is computed as [((GADC)*(GADC)*(G3)*(G2)*(Rsense))]
InterleavedThreshold	Symmetrical hysteresis driven value (in %) to turn on/off interleaved phases capability
VOLTAGE_CONTROL_LOOP_FREQ	Execution frequency of Vout control loop (Hz) (choose a submultiple of PWM frequency). For example, it is 5000 for the MB1971 LLC board, and 6300 for the PFC part and 50000 for the PSU part of the STEVAL-ISA172V3 kit.
CURRENT_CONTROL_LOOP_FREQ	Execution frequency of Iout control loop (Hz) (choose a submultiple of PWM frequency) For example, it is 70000 for the STEVAL-ISA172V3 kit
SWITCHING_FREQ_HZ	PWM signals frequency (Hz)
HRTIM_CLK_HZ	Clock frequency of the HRTimer (Hz)
TIMx_CLK_HZ	Clock frequency of the TIMx used for COMP blanking window (OCP) (Hz)

Figure 53. **PFC board parameters - 2**

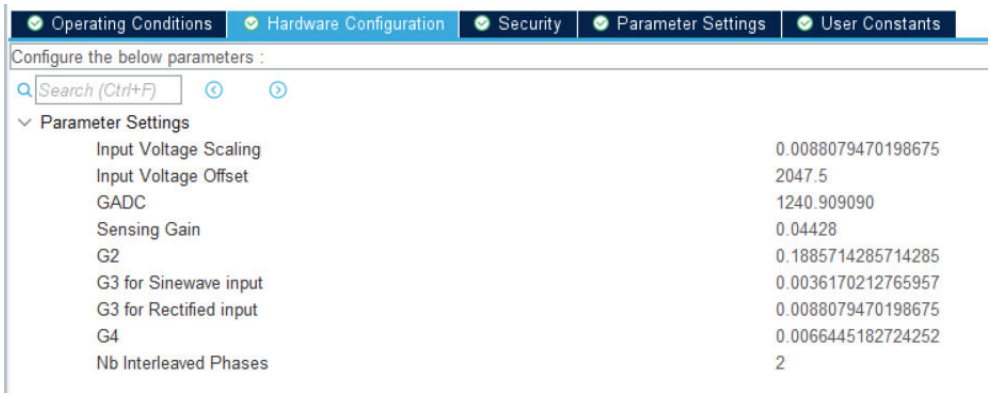


Table 11. **PFC board parameter descriptions - 2**

Parameter	Description
Vin_Offset	AC offset value for sampled input voltage, Vin: It is computed as [(1.65f*GADC)] for the STEVAL-ISA172V3 kit.
GADC	Scaling ADC gain: it is computed as (12-bit ADC / ADC Vref) = (4095.0f/3.3f)
G2	Scaling of the current sense input, Iin: when op amp/shunt resistor method is used, it is computed as [(2.0f/1000.0f)*(27000.0f/(100.0f+470.0f))], based on STEVAL-ISA172V3 kit, when transformer method is used, it is computed as [(10.0f/1000.0f)*(1.0f+(10000.0f/560.0f))], based on STEVAL-ISA172V3 kit. When transformer method is used, it is computed as [(1/200)*100*(1.5/(1.5+4.7))], based on STEVAL-ISA172V2 kit
G3	Scaling of a sine wave input voltage, Vin: it is computed as [(+5.1f/(470.0f*3.0f))], based on STEVAL-ISA172V3 kit
G3_RECT	Scaling of a rectified input voltage, Vin: it is computed as [(+3.6f/((180.0f*3.0f)+(3.6f)))*(1.0f+(3.3f/10.0f))], based on STEVAL-ISA172V3 kit
G4	Scaling of the output voltage, Vbus it is computed as [(+3.6f/(3.6f+(180.0f*3.0f)))] for the STEVAL-ISA172V3 board.
NbInterleavedPhases	Number of interleaved phases available. It is used for the maximum power per phase computation.

Figure 54. **PFC board parameters - 3**

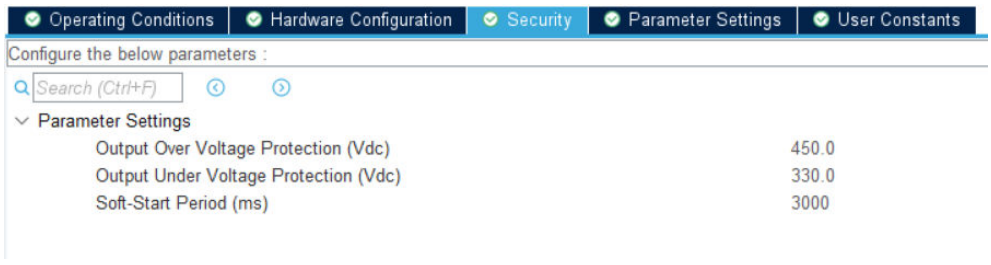
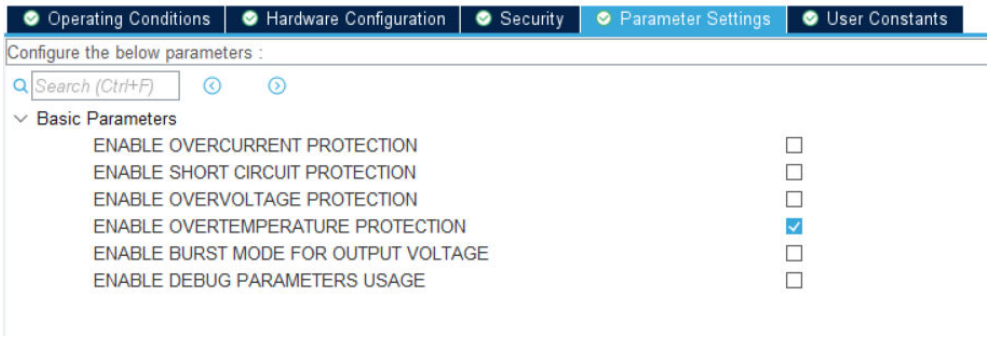


Table 12. **PFC board parameter descriptions - 3**

Parameter	Description
OVP	Overvoltage protection level for the output bus voltage (V). When the output bus voltage is above this level the PWM output is blanked.
UVP	Undervoltage protection level for the output bus voltage (V). When the output bus voltage is below this level a flag is set and this is communicated to the secondary DC-DC stage.
SOFT_START_MS	Soft-start period (ms). This is the duration of the ramp-up from starting voltage (peak of rectified input) to steady state output voltage.

Figure 55. **PFC board parameters - 4**

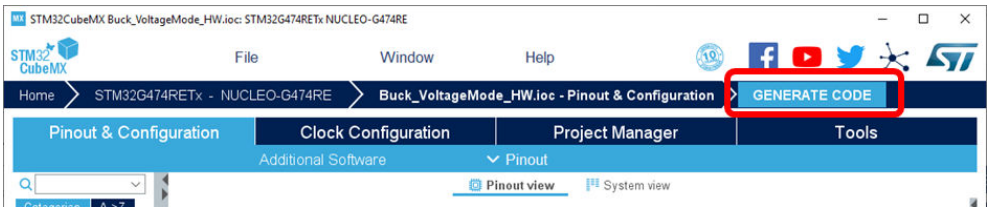


11.4 Code Generation Configuration using STM32CubeMX

Step 1. Finally, generate the project by clicking the [**GENERATE CODE**] button.

This will create the necessary project files for the selected IDE and include Digital Power functions within the auto-generated .c/.h files. In this example STM32CubeIDE from STMicroelectronics is used.

Figure 56. **STM32CubeMX generate code button**



Step 2. A prompt will appear once the project files have been created which asks if you would like to open the project. Click [**Open project**] to load the project into the selected IDE.

Figure 57. **Code generation prompt window**



Step 3. The main.c file contains the code for this project, open the main.c file and read the comments.

11.4.1 Project implementation

The generated project structure consists of multiple layers:

- Standard project files:
  - main.c/.h
  - stm32g4xx_hal_msp.c/.h
  - stm32g4xx_it.c/.h
  - system_stm32g4xx.c/.h
- Application specific files:
  - app_dpower.c/.h
  - PFC_Control_Layer.c/.h
  - PFC_IRQ_Handlers.c
  - PFC_Lib_Conf.h
- Common board support files:
  - DPC_Communication.c/.h
  - DPC_Miscellaneous.c/.h
  - DPC_STM32_Interface.c/.h

Having set up the parameters for the PFC stage in STM32CubeMX, the user need only modify the main.c/.h and stm32g4xx_it.c/.h files to add their own application specific code.

In this section, the digital Power implementation in the source files is described by identifying its specific functions.

11.5 Program flow description

The main.c file contains the majority of the code for setting up and initializing the peripherals. Some of the code within this file has been automatically generated by the STM32CubeMX tool as per the configuration process in the previous step of this application note

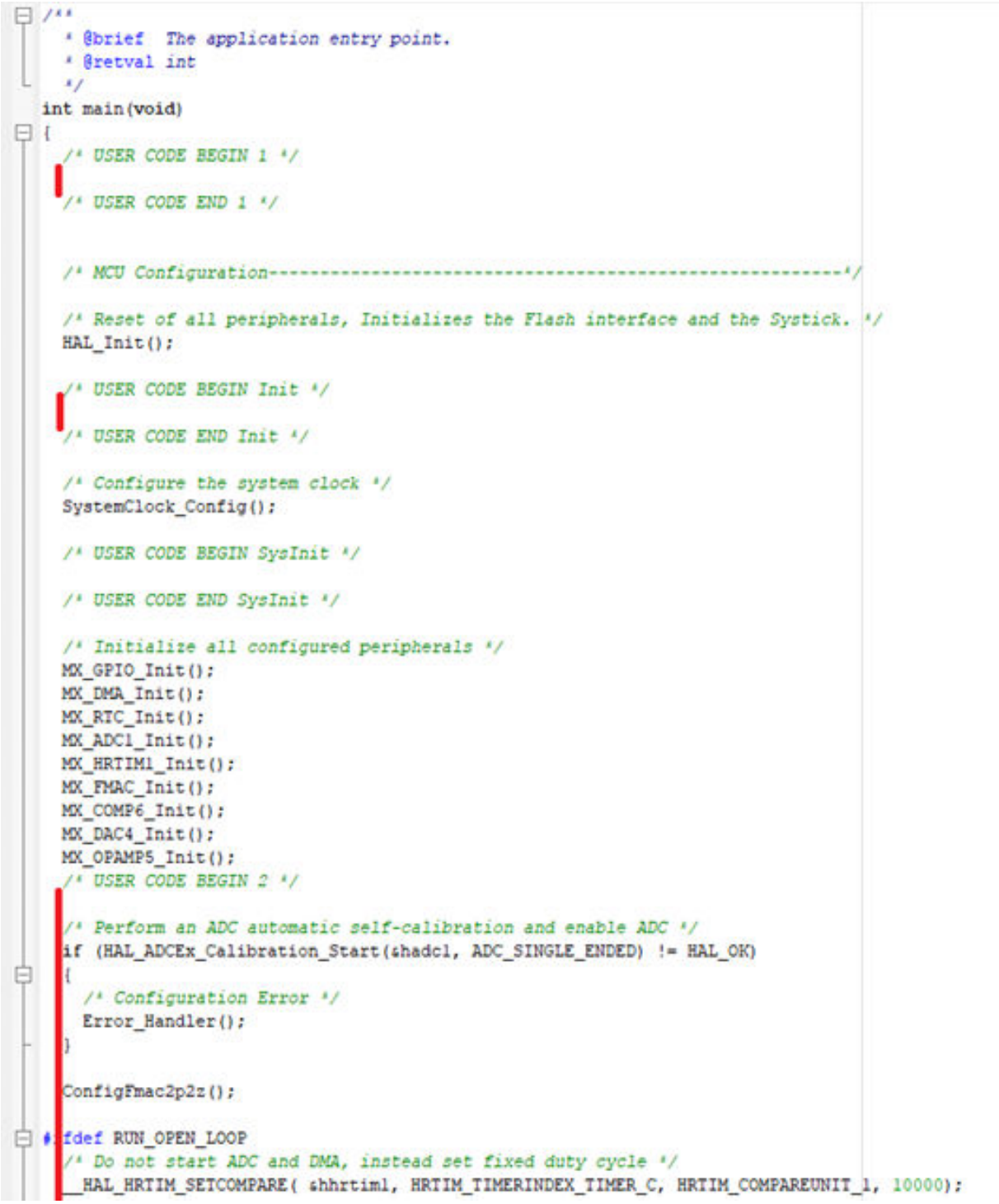
Within these code files, there are comments similar to *USER CODE BEGINS HERE* and *USER CODE ENDS HERE*. It is essential that any additional code added to the project is kept between these two comments. This is because, outside of these comments, the code is automatically generated by the STM32CubeMX tool.

If any changes are made to the project configuration within the tool, and the code is regenerated by clicking [**GENERATE CODE**], the additional changes made outside of these comment bounds will be lost.

Keeping user code within these comment bounds ensure that the code persists after the next time the code is regenerated using the STM32CubeMX tool.

The figure below shows examples of the user code locations highlighted in red.

Figure 58. **Example of user code locations in main.c**



```
/**
  * @brief  The application entry point.
  * @retval int
  */
int main(void)
{
  /* USER CODE BEGIN 1 */

  /* USER CODE END 1 */


  /* MCU Configuration--------------------------------------------------------*/

  /* Reset of all peripherals, Initializes the Flash interface and the Systick. */
  HAL_Init();

  /* USER CODE BEGIN Init */

  /* USER CODE END Init */

  /* Configure the system clock */
  SystemClock_Config();

  /* USER CODE BEGIN SysInit */

  /* USER CODE END SysInit */

  /* Initialize all configured peripherals */
  MX_GPIO_Init();
  MX_DMA_Init();
  MX_RTC_Init();
  MX_ADC1_Init();
  MX_HRTIM1_Init();
  MX_FMAC_Init();
  MX_COMP6_Init();
  MX_DAC4_Init();
  MX_OPAMP5_Init();
  /* USER CODE BEGIN 2 */

  /* Perform an ADC automatic self-calibration and enable ADC */
  if (HAL_ADCEx_Calibration_Start(&hadc1, ADC_SINGLE_ENDED) != HAL_OK)
  {
    /* Configuration Error */
    Error_Handler();
  }

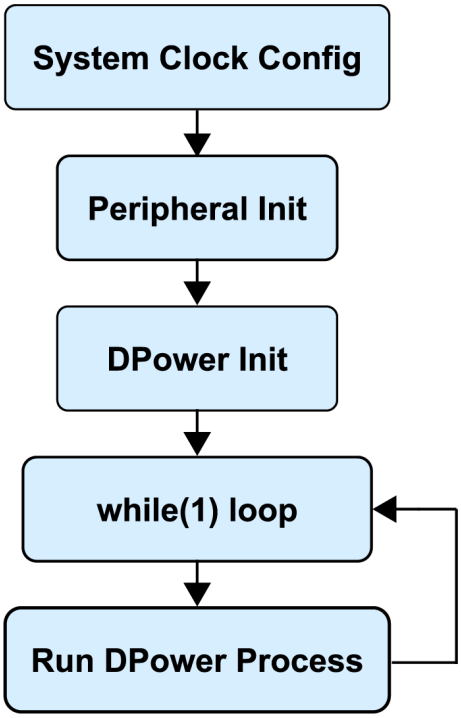
  ConfigFmac2p2z();

#ifdef RUN_OPEN_LOOP
  /* Do not start ADC and DMA, instead set fixed duty cycle */
  __HAL_HRTIM_SETCOMPARE( &hhrtim1, HRTIM_TIMERINDEX_TIMER_C, HRTIM_COMPAREUNIT_1, 10000);
```

The structure of the main function within main.c is represented in Figure 59. This is the function that the MCU will jump to after power-on; the entry point within the code. Therefore, this function contains calls to all of the initialization functions to set up the peripherals onboard the MCU. After this, the controller for the PFC stage is set up and initialized with the calculated coefficients.

Finally, the ADC is started and begins sampling and the PWM outputs are enabled to drive the switches. The set up and initialization process contains two functions from the X-CUBE-DPower pack.

Figure 59. **Program flow within main.c**



11.5.1 MX_DPower_Init();

The MX_DPower_Init() function is responsible for initializing the peripherals required for controlling the PFC stage, in this case it is an interleaved CCM Boost PFC.

The init function starts by configuring the PFC converter's controller structure using the `PFC01_configFloat()` function from the Biricha Digital Power Library. This function sets up the controller with the specified switching frequency, slow loop frequency and soft-start time.

Next, the function initializes the 2p2z (2-pole, 2-zero) controller used to close and stabilize the fast current loop using the controller coefficients calculated using ST-PLD. This is repeated for each phase of the interleaved PFC as there is an individual current loop controller to regulate the current in each phase.

Following this, the voltage-feed-forward filter is initialized. This is used to filter the sampled input voltage and provide a good line-to-output regulation. The coefficients for this filter are again obtained using ST-PLD. In a similar manner, the RMS filter is also initialized and this is used to check for under/over-voltage conditions on the input.

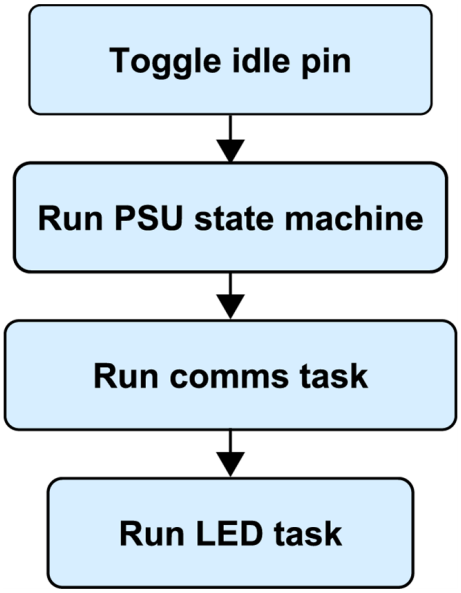
Finally the slow voltage loop controller is initialized using the PFC01_vLoopFloatInit() function from the Biricha Digital Power Library. This function accepts the 2p2z voltage loop controller coefficients calculated by ST-PLD as well as the desired output voltage, under-voltage and over-voltage limits specified by the user in STM32CubeMX.

The DPower init function also initializes the ADC peripherals. These are used to measure the input voltage, current in each phase, output voltage and operating temperature of the converter. The `HAL_ADCEx_Calibration_Start()` calibrates the ADC for single ended conversion. The ADCs are started in injected mode, triggered by the HRTIM peripheral, as the results will be read later in the HRTIM interrupt service routine.

The function then sets up the DAC which provides the real-time peak-current limit for the PFC FETs based on the sensed switch current and also the second DAC output for debugging purposes, allowing internal signals to viewed in real time on the oscilloscope.

Finally, the init function enables the HRTIM counter which drives the PWM output. This will also trigger the ADC sampling and start the process of the HRTIM interrupt service routines that are used to run the fast and slow control loops within this PFC system.

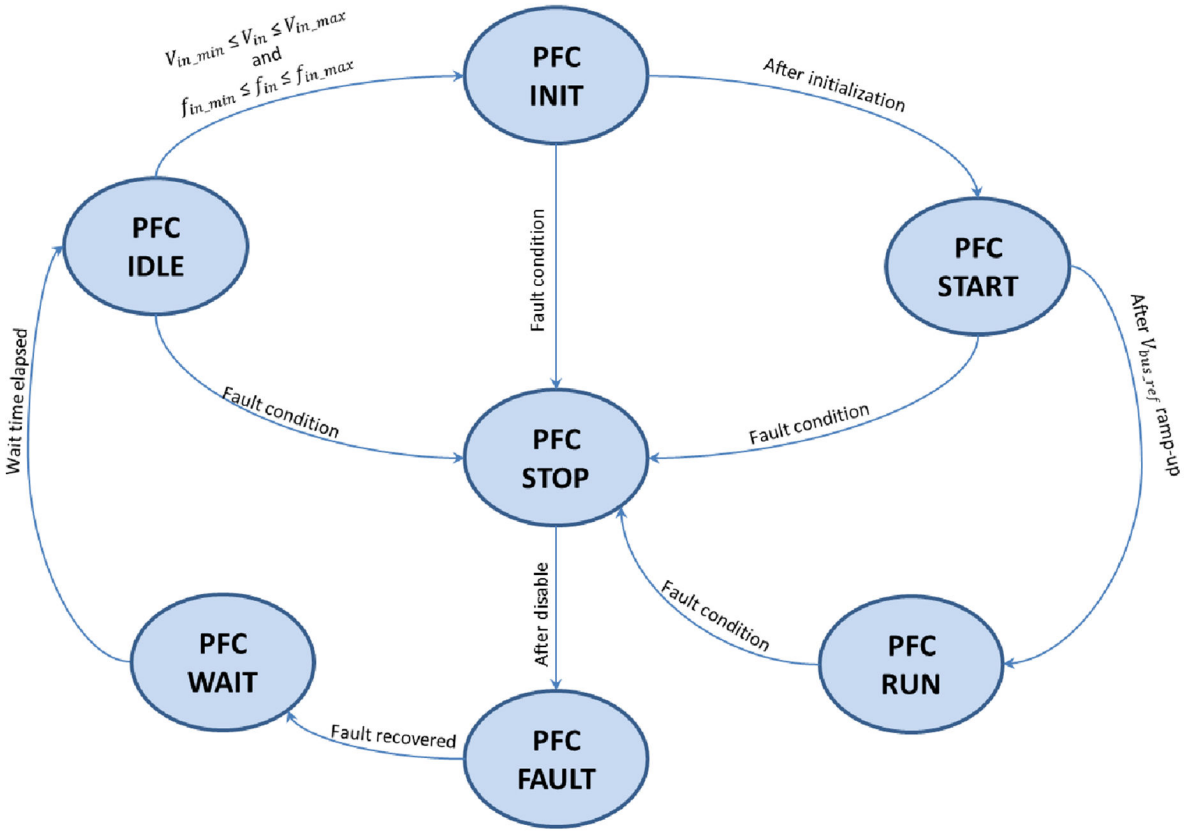
Figure 60. **Program flow within MX_DPower_Init() function**



11.5.2 MX_DPower_Process();

The `MX_DPower_Process()` function is called repeatedly to monitor, control and transition between operating states of the PFC stage. The function achieves this by use of a finite state machine.

Figure 61. **PFC software state-machine flowchart**



The function enters a switch statement that contains a case for each state in the finite state machine. The current state of the machine is indicated by the `myPfc.m_PFC_State` variable within the PFC control structure, which can take on the following values:

- PFC_IDLE: This state is used to wait for the input voltage and frequency conditions to be satisfied before starting to switch the PFC stage. If the conditions are met, the next state is set to PFC_INIT.
- PFC_INIT: This state enables the PWM outputs of the converter. A delay timer is set for the ramp-up duration. This is used to detect if the converter failed to reach the voltage set point in the allowed time, indicating a problem at the output of the converter. The LED is set to blink quickly until the ramp-up is complete. When the voltage loop begins ramping up the next state is set to PFC_START.
- PFC_START: This state is used to wait for a specified time in order to allow the output voltage to ramp up to the desired set point. When the output voltage is within tolerance and the delay time has elapsed, the under voltage and over temperature checks are enabled. The *PFC_START_UP_OK* flag is then set and the next state is set to PFC_RUN.
- PFC_RUN: Under normal operating conditions, no actions are taken within the state machine when operating in this state. The under- and overvoltage conditions are checked as part of the slow voltage loop in the interrupt service routine. It is this ISR that will cause a transition to a different state.
- PFC_STOP: This state is used to disable the converter. The main PWM is disabled and the input relay is opened. Any system fault is stored in the *m_PFC_Last_System_Fault* element of the PFC structure, undervoltage and overtemperature checks are disabled and the *PFC_START_UP_OK* flag is cleared. The next state is set to PFC_FAULT.
- PFC_ERROR: This state is used to filter out temporary error of the converter. The following state is PFC_WAIT until all expected trials are over. Then, depending on error condition, the next state is either PFC_FAULT or either PFC_IDLE.
- PFC_FAULT: This is a persistent state which can only be exited when there is *PFC_NO_ERROR* present in the *m_PFC_System_Fault* fault flags. When all errors are cleared, a delay timer is initialized and the next state is set to PFC_WAIT.
- PFC_WAIT: This state waits for the delay timer to expire, for the input voltage to be above the minimum threshold and for the output capacitors to be charged to 80% of the peak rectified input voltage value before closing the input in-rush relay and setting the next state to PFC_IDLE.

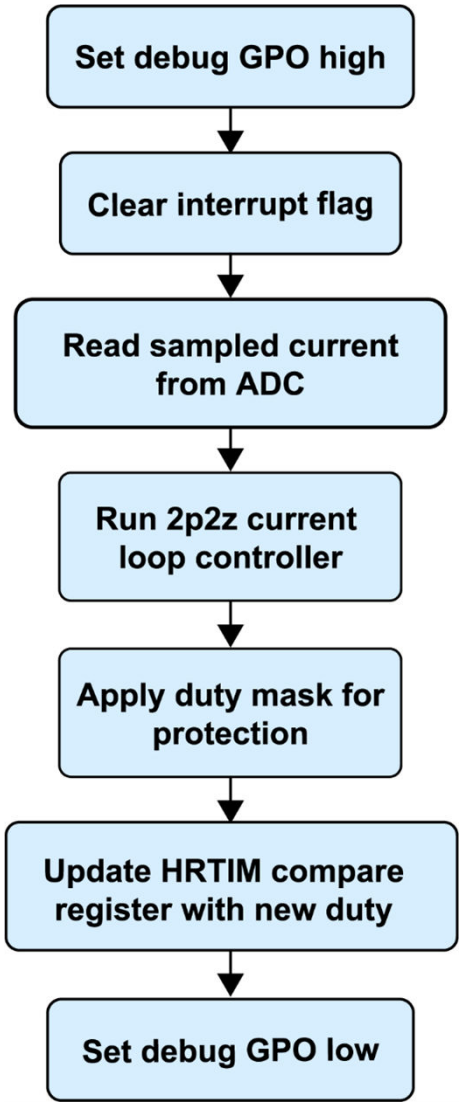
Following execution of the state machine, the DPower process task sends the state of the PFC stage to the secondary side of the PSU using the isolated UART interface. This is used by the downstream DCDC stage to determine if the output of the DCDC stage should ramp up or shutdown.

11.6 Interrupt service routines

In this example, the PFC stage is a two-phase interleaved CCM Boost PFC. The fast-current loop control for each phase is implemented using the HRTIM interrupt from the timer output driving that phase. In this case, these are the `HRTIM1_TIMA_IRQHandler()` and `HRTIM1_TIMB_IRQHandler()` interrupts within the DPC_IRQ_Handlers.c file.

The X-CUBE-DPower pack automatically generates both the fast current loop ISRs and the slow voltage loop ISR, implemented as `HRTIM1_TIMC_IRQHandler()`, and includes the functions necessary to run the controllers responsible for stabilizing the PFC stage. Figure 62 and Figure 63 present the software flow of these ISRs.

Figure 62. **HRTIM1_TIMA_IRQHandler() function is & HRTIM1_TIMB_IRQHandler() flowchart**



11.7 HRTIM1_TIMA_IRQHandler() / HRTIM1_TIMB_IRQHandler()

The `HRTIM1_TIMA_IRQHandler()` and `HRTIM1_TIMB_IRQHandler()` functions are the interrupt service routines for Timer A and B of the HRTIM peripheral, respectively. When an interrupt is triggered by the HRTIM timer A or B, these functions are called to handle the interrupt. Both of the fast current loop interrupt routines operate in the same manner, with the exception of running the controller dedicated to that phase, and therefore only `HRTIM1_TIMA_IRQHandler()` will be covered here.

First, the ISR sets a debug pin high and clears the interrupt flag for this timer within the HRTIM peripheral, which indicates that the interrupt has been serviced and allows for future interrupts to occur.

The function then reads both the total return current and the individual phase current from the ADC and stores them in the local variables `m_PFC_Isense_TX1` and `m_PFC_Isense_RTN`. The sample that will be used in the current loop controller will depend on the definition of CT_TRANSFORMERS_SENSING or SHUNT_RESISTOR_SENSING. In this example, the individual phase current is used and therefore this is stored in the feedback element of the 2p2z current controller structure.

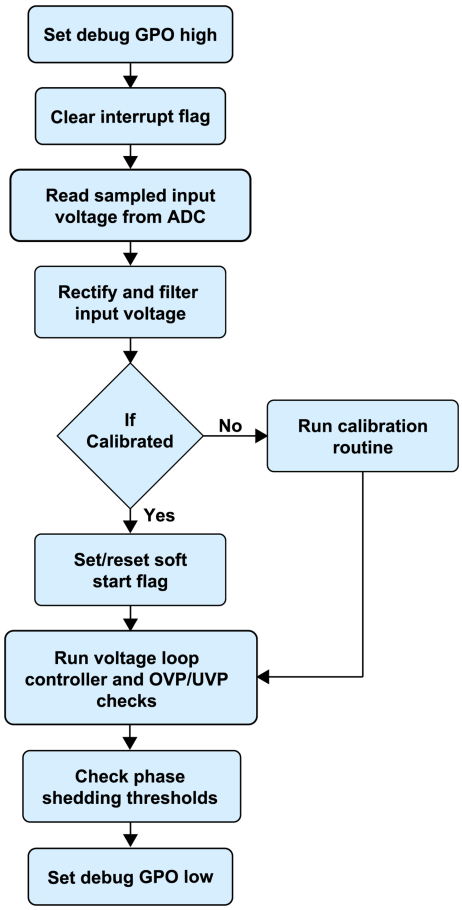
The ISR then calls another function, `PFC01_iLoopFloat()`, passing it the `myPfc` object and the number of the phase that is being calculated, in this case 0. This function executes the 2p2z linear difference equation and calculates duty cycle of the PWM signal ready for the next switching period.

After the `PFC01_iLoopFloat()` function returns, the value of duty is set to the output of the iLoop2p2z controller structure, divided by 2 as this is center aligned to the middle of the switching period, and bitwise ANDed with `myPfc.m_DutyMask`. The bitwise AND provides a quick way of shutting down the PWM output (within one switching cycle) in case of over or undervoltage errors.

Finally, the ISR sets the compare register value of the HRTIM timer to the value of duty ready for the next switching cycle.

At the end of the ISR function, the GPIO pin is set to low to allow the duration of the ISR to be measured using an oscilloscope.

Figure 63. HRTIM1_TIMC_IRQHandler() flowchart



11.8 HRTIM1_TIMA_IRQHandler() / HRTIM1_TIMB_IRQHandler()

The Timer C ISR is used to implement the slow-voltage loop. The slow-voltage loop is responsible for filtering the input voltage and calculating the input voltage feed forward (VFF) term to provide good line regulation, closing the voltage loop to provide reasonable load regulation and calculating the new demand current value for use in the fast current loop interrupt routines.

This ISR is again automatically generated by the X-CUBE-DPower pack. The ISR begins by setting a debug pin high and clearing the Timer C interrupt flag. The ADC samples of the input voltage are read and stored in local variables for processing. In this example, the AC input voltage is measured with an offset applied. Therefore, within this ISR the offset is subtracted and the value converted to an absolute/positive value for later use in the RMS filter.

The sampled input voltage is also passed through a high frequency filter, `FILT_2p2zFloatInline()`, which is optional, as this rectified input voltage shape can be used as a reference for the fast current loop. Any noise on this signal could cause the current loop to draw non-sinusoidal current, so additional filtering may be required.

Alternatively, a sinusoidal reference can be generated in software using the `sinf()` function. Given that `sinf()` would produce a current reference that contains no harmonics above the fundamental, this may result in lower input current total harmonic distortion. However, this will be at the expense of higher computational load as the mathematically generated reference needs to be phase locked to the sampled input voltage.

The ADC sampled output voltage is then stored in the voltage loop controller feedback element and logic then determines if it should start the soft-start routine. The soft-start is only allowed to start if the ADC values have been calibrated and the `myPfc.m_PFC_State` variable is in the PFC_START, PFC_RUN or PFC_INIT states.

The calibration routine also runs within this ISR. The ADC values can be calibrated at start-up if required. This may be useful for op-amps that have a significant offset voltage. The objective of the calibration routine is to take 100 samples from the ADC before any switching takes place. This can then be averages and subtracted from every subsequent ADC sample.

The `PFC01_vLoopFloat()` function from the Biricha Digital Power Library is then called. This function executes all of the filters and performs the 2p2z controller calculating the new demand value of current ready for use in the fast current loop ISRs. This function also monitors the under- and overvoltage conditions and sets the duty mask value accordingly.

This slow loop ISR also monitors the threshold for turning on and off the phases in an interleaved PFC. Typically at light loads some of the PFC phases are shut down to minimize losses and optimize operation under CCM. To achieve this, the power output of the voltage loop is monitored and the phases are enabled or disabled using the `PFC01_enablePhaseFloat()` function.

Finally, during debug, DAC1 Ch1 can be used to monitor the state of internal signals. This is useful for confirming correct operation and that sampled ADC values are clean and representative of the signal being sampled. The internal variable being output to the DAC can be changed by updating the `m_DAC_output` variable used in the switch statement.

Before leaving the ISR, the debug pin is set low allowing the duration of the slow loop ISR to be monitored using an oscilloscope.

11.9 2p2z controller coefficients

The 2p2z controller coefficients are defined in the header file, main.h. This can be easily accessed by locating the *main.h* `#include` towards the top of the main.c file, right-clicking on *main.h* and selecting [**Open main.h**] from the menu. Within this header file, there are several defines for the pin names which have been automatically generated by STM32CubeMX.

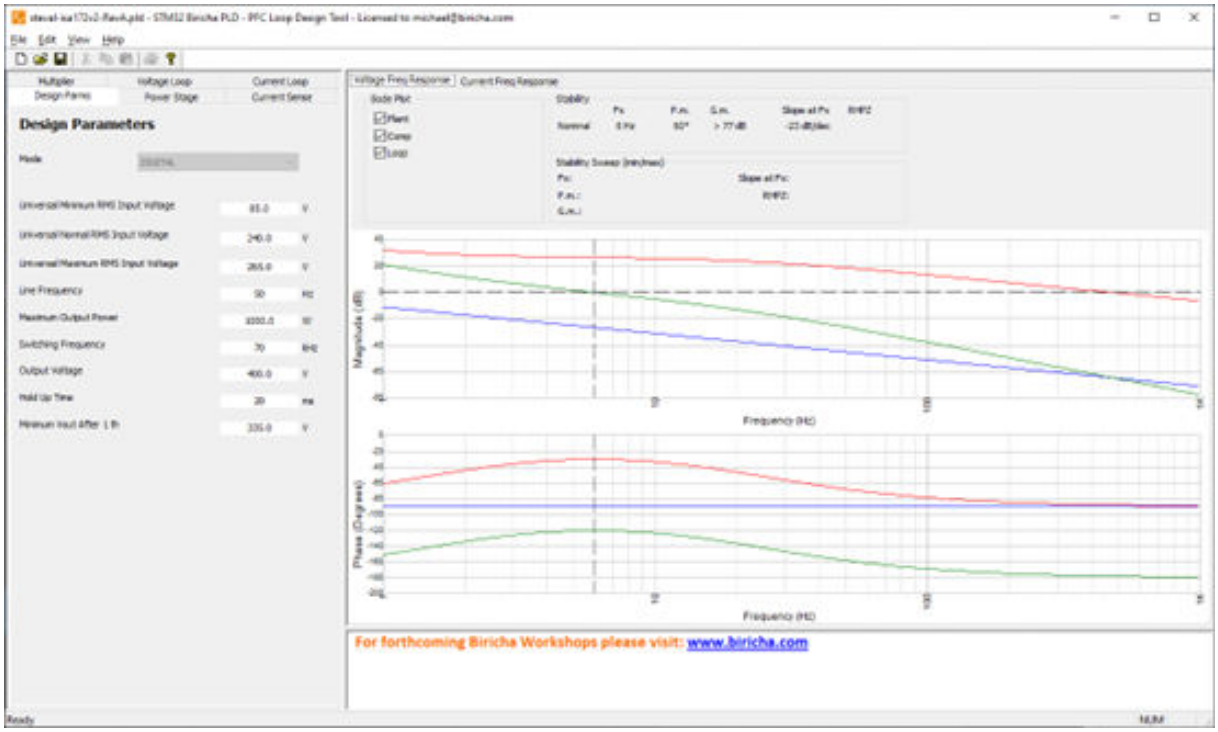
Further down this file, there is a `/* USER CODE BEGIN Private defines */` section where the definitions for the FMAC configuration begin. The controller coefficients are defined below the FMAC configuration parameters. These coefficients (B0, B1, B2, A1, A2) are given in a fixed-point hexadecimal form. Earlier in this application note, it was shown how the compensator poles and zeros, in the continuous-time domain, are converted into discrete-time controller coefficients. The last step required is to convert these discrete-time controller coefficients into fixed point form for use on the fixed point FMAC.

11.10 ST PLD configuration

The power supply design tool ST PLD from Biricha will be used to generate the controller coefficients for the voltage loop controller, current loop controller and input voltage feed-forward filter used for this digital PFC implementation. ST PLD is free-to-use and can be download for free from the Biricha website, visit www.biricha.com/st-pld for more information.

The .pld file associated with this application note is included in the project downloads in the appendix of this application note. However, the process for re-creating the PLD project settings is included here for completeness.

Figure 64. **Biricha ST PLD**



The initial screen of ST PLD is shown in Figure 64. The left-hand pane is used for entering the specification of the PFC stage along with the other pertinent design parameters. The right-hand pane displays the control loop Bode plots.

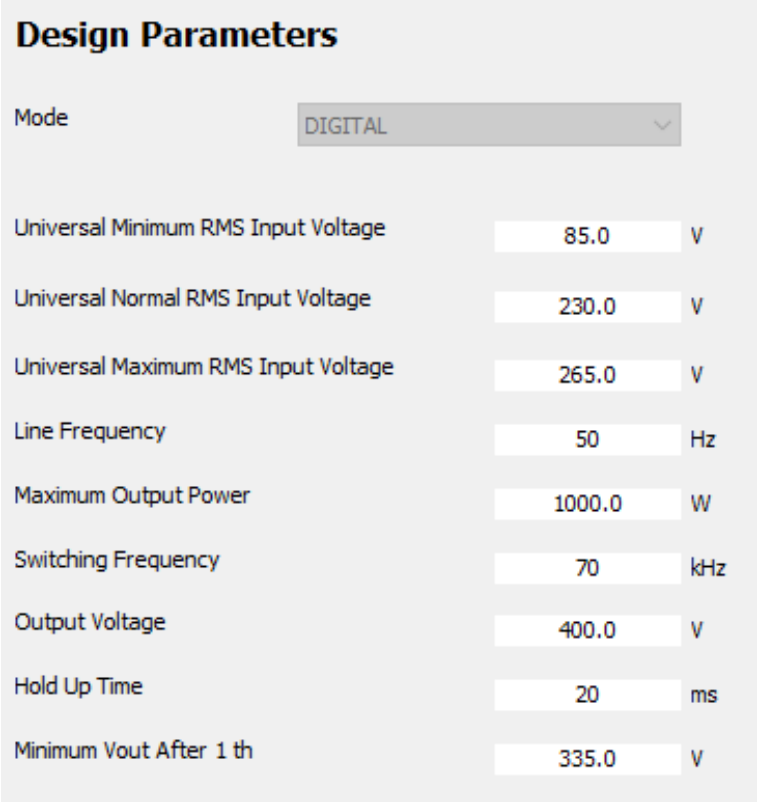
Step 1. To calculate the digital controller coefficients, the PFC specification must first be entered. This is entered on a 'per-phase' basis. For example, if you are designing a 2 kW interleaved PFC, with each stage handling 1 kW, then the specification to be entered here should be the specification for the 1 kW phase. On the [**Design Params**] tab, enter the specification shown in the following table.

Table 13. STEVAL-ISA172V3 specification per PFC stage

Design Params Tab Parameter	Value
Universal Minimum RMS Input Voltage	85.0
Universal Nominal RMS Input Voltage	230.0
Universal Maximum RMS Input Voltage	265.0
Line Frequency	50
Maximum Output Power	1000
Switching Frequency	70
Output Voltage	400
Hold Up Time	20
Minimum Vout After 1 th	335

The [**Specification**] tab should now look like the screenshot shown below.

Figure 65. ST PLD Design Parameters Tab



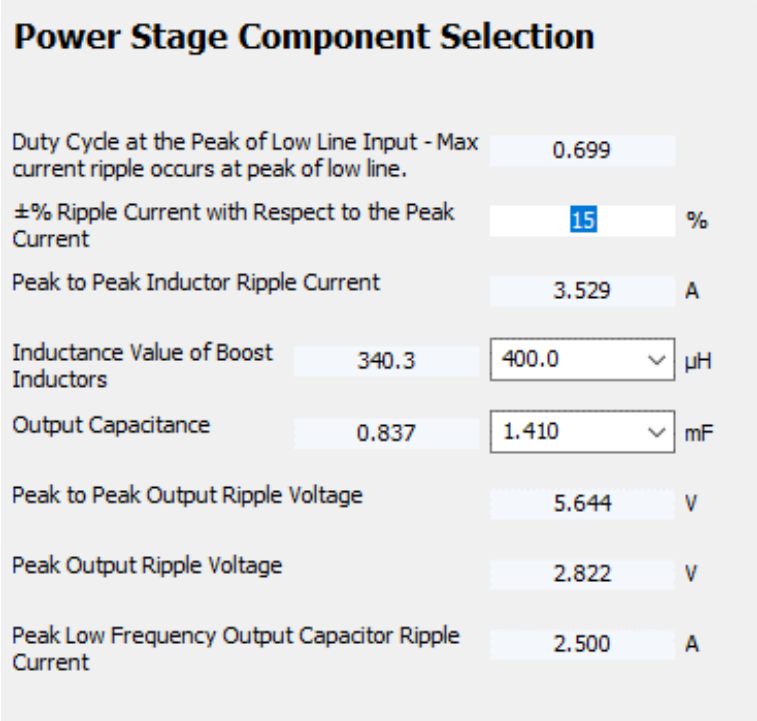
Step 2. Next, click on the [**Power Stage**] tab and enter the specification shown in the following table.

Table 14. Power stage parameters

Power Stage Tab Parameter	Value
% ripple current	15
Inductance Value of Boost Inductors	400.0
Output Capacitance	1.410

The [**Power stage**] tab should now look like the screenshot shown below.

Figure 66. ST PLD Power Stage tab



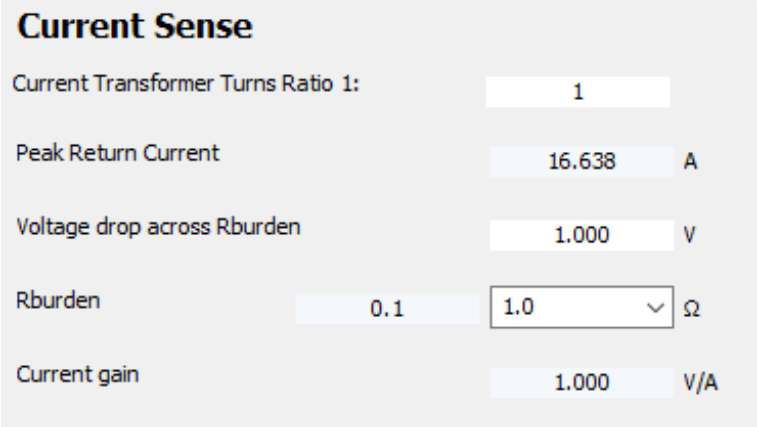
Step 3. Next, click on the [**Current Sense**] tab and enter the specification shown in the table below.

Table 15. Current sense parameters

Current sense tab parameter	Value
Current Sense Tab Parameter	Value
Current Transformer Turns Ratio 1:	1
Voltage drop across Rburden	1.0
Rburden	1.0

The [**Current Sense**] tab should now look like the screenshot shown in the figure below.

Figure 67. ST PLD Current Sense Tab



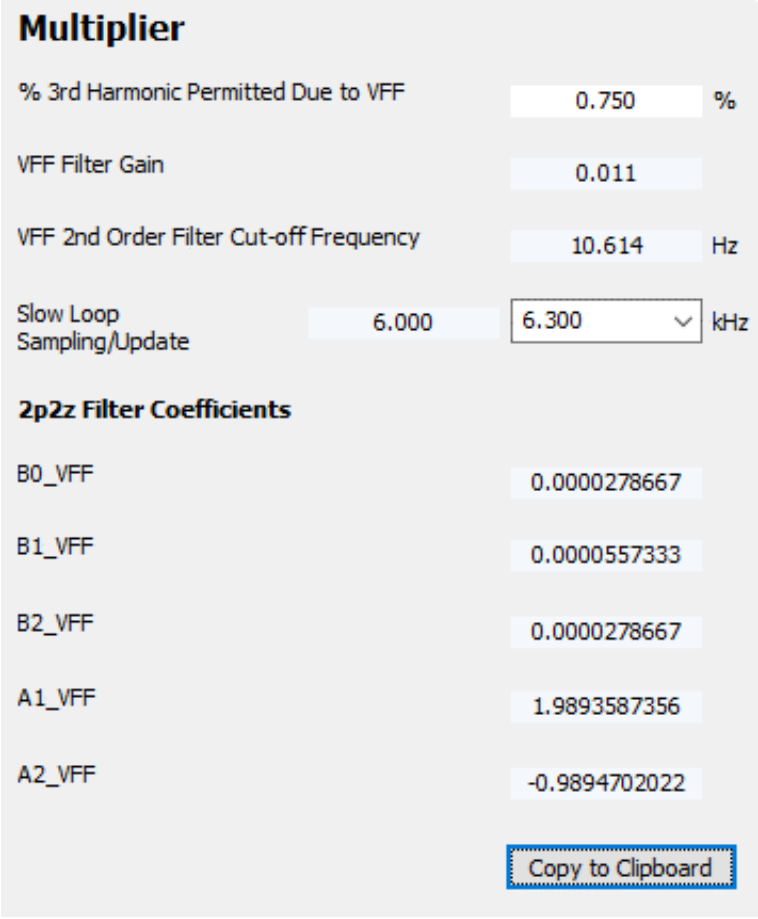
Step 4. On the next tab, [**Multiplier**], the input voltage feed-forward filter is designed. This filter reduces the 2nd harmonic component on the sampled input voltage to a level that is low enough to meet the 3rd harmonic component requirement specified in this tab. This is because 2nd harmonic component on VFF will appear as 3rd harmonic on the line current due to the multiplier action. In order to design this filter, PLD needs to know the sampling frequency of the slow loop where this filter is calculated. These values are given in the following table.

Table 16. Multiplier parameters

Multiplier Tab Parameter	Value
% 3rd Harmonic Permitted due to VFF	0.75%
Slow Loop Sampling/Update	6.3kHz

The [**Multiplier**] tab should now look like the screenshot shown in the figure below.

Figure 68. ST PLD Multiplier Tab



Step 5. Now that the filter coefficients have been calculated, they need to be copied into the main.h header file containing the controller coefficients within the PFC project. If you are using the example project for this EVM, this has already been done. Click the [**Copy to Clipboard**] button.

The following coefficients should now be on your clipboard:

```
#define B0_VFF (+0.0000278666522609)
#define B1_VFF (+0.0000557333045218)
#define B2_VFF (+0.0000278666522609)
#define A1_VFF (+1.9893587355575171)
#define A2_VFF (-0.9894702021665608)
```

These are the voltage loop coefficients that are used within the example application.

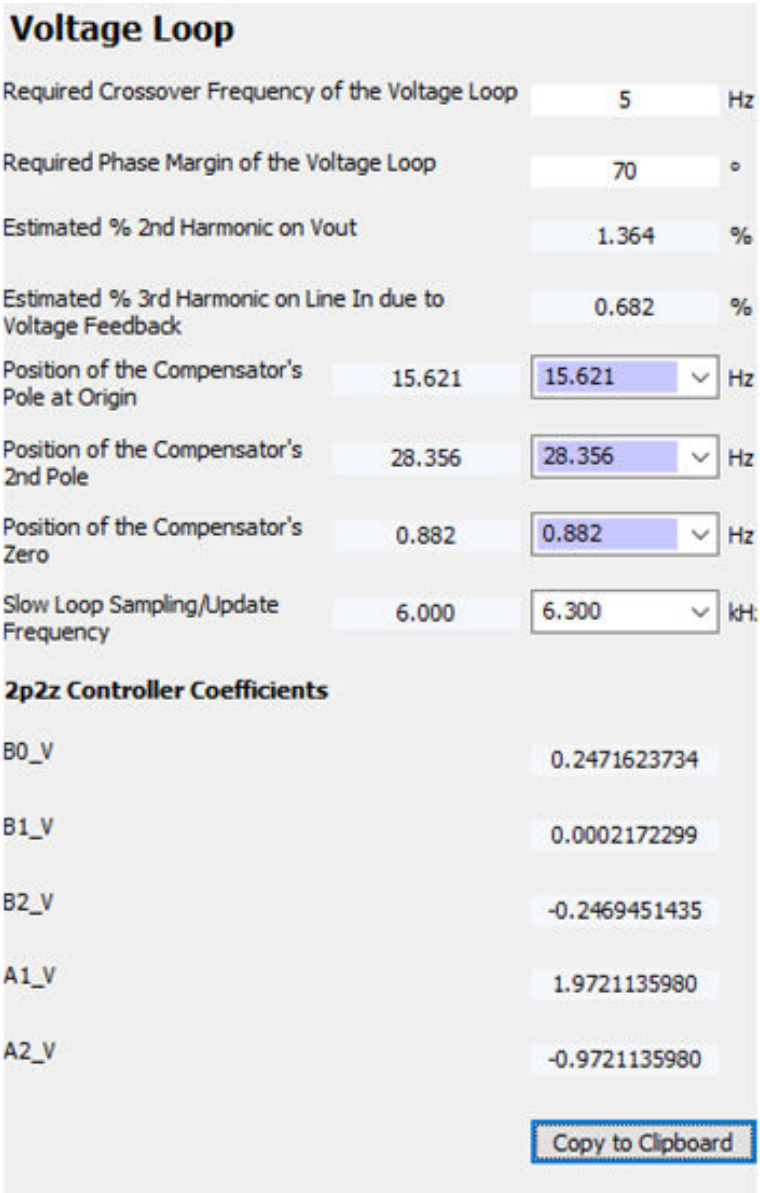
Step 6. On the next tab, [**Voltage Loop**], the compensator for the voltage loop is designed. The voltage loop is designed to meet a specified crossover frequency and phase margin. PLD will then automatically calculate the poles and zeros in the continuous time and perform the discrete time transform based on the specified slow loop calculation frequency. These values are given in the following table.

Table 17. Voltage Loop parameters

Voltage Loop Tab Parameter	Value
Crossover frequency of voltage loop	5Hz
Phase margin of voltage loop	70 degrees
Slow loop update frequency	6.3kHz

The [**Voltage Loop**] tab should now look like the screenshot shown in the figure below.

Figure 69. ST PLD Voltage Loop Tab



Step 7. Now that the filter coefficients have been calculated, they need to be copied into the main.h header file containing the controller coefficients within the PFC project. If you are using the example project for this EVM, this has already been done. Click the [**Copy to Clipboard**] button.

The following coefficients should now be on your clipboard:

```
#define B0_V (+0.2471623733508778)
#define B1_V (+0.0002172298785784)
#define B2_V (-0.2469451434722993)
#define A1_V (+1.9721135979711808)
#define A2_V (-0.9721135979711807)
```

These are the voltage loop coefficients that are used within the example application.

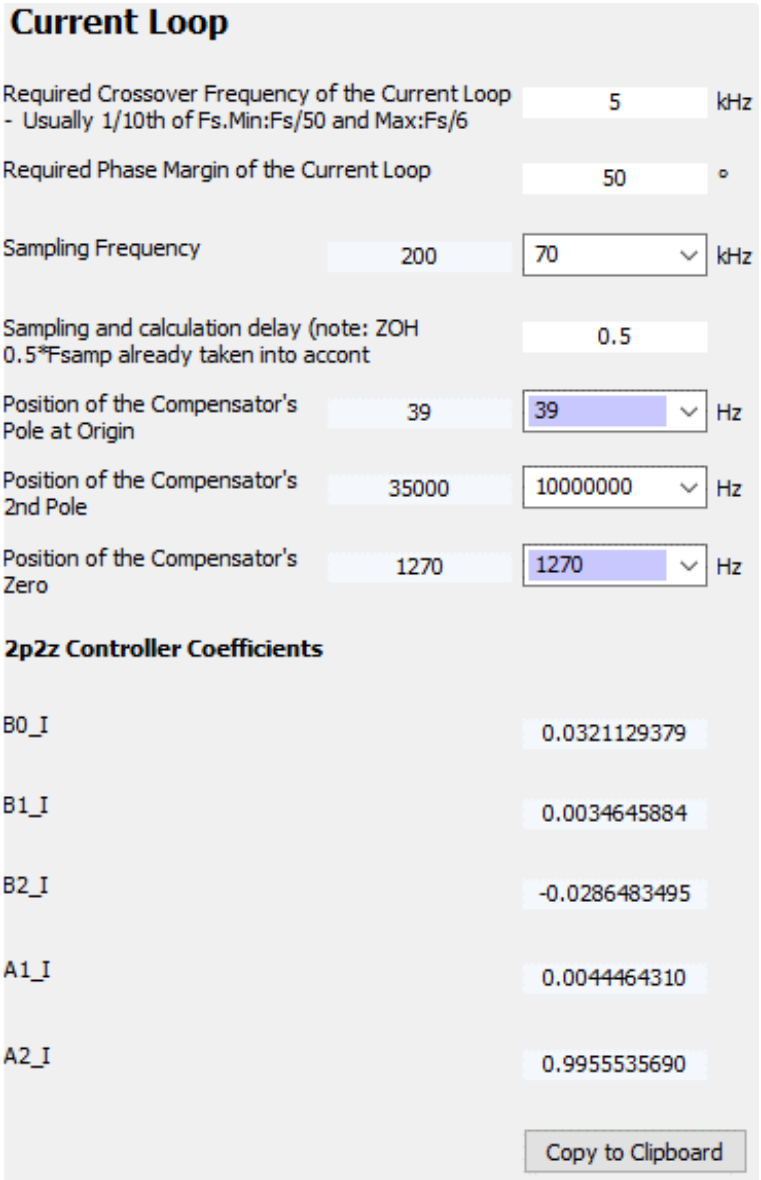
Step 8. The last configuration tab is [**Current Loop**]. These values are given in the following table.

Table 18. Current Loop parameters

Current Loop Tab Parameter	Value
Required crossover frequency	5kHz
Required phase margin	50 degrees
Sampling frequency	70kHz
Sampling and calculation delay	0.5
Position of the Compensator's 2nd Pole	10000000

The [**Current Loop**] tab should now look like the screenshot shown in the figure below.

Figure 70. ST PLD Current Loop Tab



Step 9. Now that the filter coefficients have been calculated, they need to be copied into the main.h header file containing the controller coefficients within the PFC project. If you are using the example project for this EVM, this has already been done. Click the [**Copy to Clipboard**] button.

The following coefficients should now be on your clipboard:

```
#define B0_I (+0.0321129378954740)
#define B1_I (+0.0034645884443276)
#define B2_I (-0.0286483494511464)
#define A1_I (+0.0044464310059411)
#define A2_I (+0.9955535689940589)
```

These are the voltage loop coefficients that are used within the example application.

12 Getting started

12.1 2 kW AC-DC PSU modes of operation.

Operational modes for the AC-DC PSU are as described in the following section. Selection of modes other than the default (Mode 1) requires the explicit selection of the mode required by changing defines in the code (e.g. #define LOW_VOLTAGE), recompiling and reflashing the MCU. To reconfigure into a different mode, the AC-DC PSU needs to be powered OFF, the MCU reflashed, and then powered ON.

12.1.1 Operational mode 1 – Boost PFC operation, AC input 48 V DC output.

Boost PFC stage derives its power from the 90 to 265Vrms, 50 / 60Hz AC input from J3, boosting to 410V DC output (nom) and operating the Phase shifted full bridge converter and Synchronous Rectifier stage to deliver 48V DC output (nom) at up to 2kW to J2.

This is the default mode of operation.

12.1.2 Operational mode 2 – Boost PFC operation, AC input, 400 V DC ‘tap-off’ no 48 V DC output.

Boost PFC stage derives its power from the 90 to 265 Vrms, 50 / 60Hz AC input from port J3, boosting to 410 V DC output (nom) and allowing the power to be drawn from the bidirectional port J21.

In this mode, the phase-shifted full-bridge converter and synchronous rectifier stage is not operating and there is no power available on the output connector J2.

12.1.3 Operational mode 3 – Boost PFC operation, AC or DC input, ‘tap-off’ of a reduced power DC output.

The boost PFC stage derives its power from a reduced input from port J3 in the range of 35 to 40 Vac or 50-55 Vdc, to power the boost PFC stage. The boost PFC stage output is at a reduced level of 60 V DC output and this can be ‘tapped off’ from port J21.

In this mode, the phase-shifted full-bridge converter and synchronous rectifier stage is not operating and there is no power available on the output connector J2.

12.1.4 Operational mode 4 – NO Boost PFC operation, External DC input full power 48 V DC output.

AC-DC PSU derives reduced power (50-60 Vdc) from the external bidirectional port (J21) and operates the phase-shifted full-bridge converter and synchronous rectifier stage to deliver 4.8 V DC output at up to 100 W on the output connector J2.

In this mode, the boost PFC stage is disabled.

12.1.5 Operational mode 5 – NO Boost PFC operation, External DC input reduced power 60 V DC output.

AC-DC PSU derives reduced power (50-60 Vdc) from the external port (J21) and operates the phase-shifted full-bridge converter and synchronous rectifier stage to deliver 4.8 V DC at up to 100 W from J2.

In this mode, the boost PFC stage is disabled.

12.1.6 Undocumented operational modes

Any attempted operation of the AC-DC PSU outside of the above-described modes will result in indeterminate operation and shall be avoided.

12.1.7 User modified firmware modes of operation

It is possible for the user to alter the firmware to set up modes of operation different to those described herein. Any such modifications will need to be carefully considered and are at the risk of the user.

12.2 AC-DC PSU test operation – general configuration

For purposes of test, the AC-DC PSU will be considered as a single complete design encompassing both the STEVAL-ISA172V3 2 kW - CCM Interleaved PFC AC-DC and STEVAL-ISA172V3 2 kW - PSFB DCDC application notes.

As well as the high voltage, high power AC input mode (up to 2 kW), the AC-DC PSU can operate in low power, low voltage mode, either from an AC source or DC source. By utilizing the AC input [J3] or bidirectional port [J21], and configuring an appropriate test mode, it is possible to test each stage separately.

Table 19. STEVAL-ISA172V3 2kW operational modes

Mode	Input Voltage J3	Input Voltage J21	AC or DC Input?	Output Voltage J21	Output Voltage J2	Power Level
1	90-265cVac ⚠	N/A	AC	N/A(1) ⚠	48 V DC	Up to 2 kW (thermally derated to 1 kW at <220 Vac)
2	90-265cVac ⚠	N/A	AC	400 V DC ⚠	N/A	Up to 2 kW (thermally derated to 1 kW at <220 Vac)
3	35 – 40 Vac 50-55 Vdc	N/A	AC or DC	N/A(1) ⚠	4.8 V DC	Up to 100 W
4	N/A	400cVdc ⚠	DC	N/A	48 V DC	Up to 2 kW
5	N/A	50 – 60 Vdc	DC	N/A	5 V DC	Up to 100 W

1. *Voltage is present but not intended for use.*

12.2.1 AC-DC PSU test operation – prerequisites

It is assumed that the operator is competent in the use of electrical / electronic test equipment and is familiar with relevant safe operating procedures in relation to use of voltages up to and including 450 V DC.

It is recommended that the user fully familiarize themselves with the contents of both application notes [STEVAL-ISA172V3 2 kW - CCM interleaved PFC AC-DC and STEVAL-ISA172V3 2 kW - PSFB DCDC].

Operation of the AC-DC PSU shall only be permitted in a dry lab environment and that all electrical connections be made using insulated connectors with no exposed conductors.

Use of current limited power sources with suitable RCD protection is recommended.

Prior to connecting the AC-DC PSU to any electrical connection, ensure that all the screws and fittings are secure and that there are no loose parts or FOD in the unit.

Ensure that a risk assessment has been performed, documented, and reviewed. It is recommended that no solo-working is permitted when working on voltages above SELV.

Connections between the laptop and the digital controllers should use the isolated USB in circuit debugger, ST-LINK/V2-ISOL shown in Figure 71.

Ensure the laptop that connects to the digital controller board (STEVAL-DPSG474M) and is configured with the correct IDE and firmware versions for the controllers (see EVM website for latest firmware revision information).

Figure 71. ST-LINK/V2 isolated USB in circuit debugger



12.2.2 Initial low power operation – Mode 3, Low Voltage DC input and Low Voltage DC output

Initial testing of the AC-DC PSU will be at a reduced power level – Mode 3, and uses a low voltage DC input. In this mode, the output voltage of the PSU will be 4.8 V DC and during operation,

12.2.3 Initial connection checks

Refer to the general test configuration in Figure 72.

Step 1. Connect the AC-DC PSU to a 55V DC, current limited supply – max 2A (do NOT turn on at this point).

Step 2. Connect a 10W (2.5 Ω) load to bidirectional port J21 and to the output port J2 of the AC-DC PSU. These loads can be fixed resistors or electronic loads, but must have sufficient power capacity to safely dissipate the electrical power / heat.

Step 3. Connect a digital voltmeter (or DMM configured appropriately) across J21 and the DC output J2.

Step 4. Connect the laptop to the digital controllers using the isolated USB in circuit debugger ST-LINK/V2.

Figure 72. AC-DC PSU general test configuration – DC input test mode

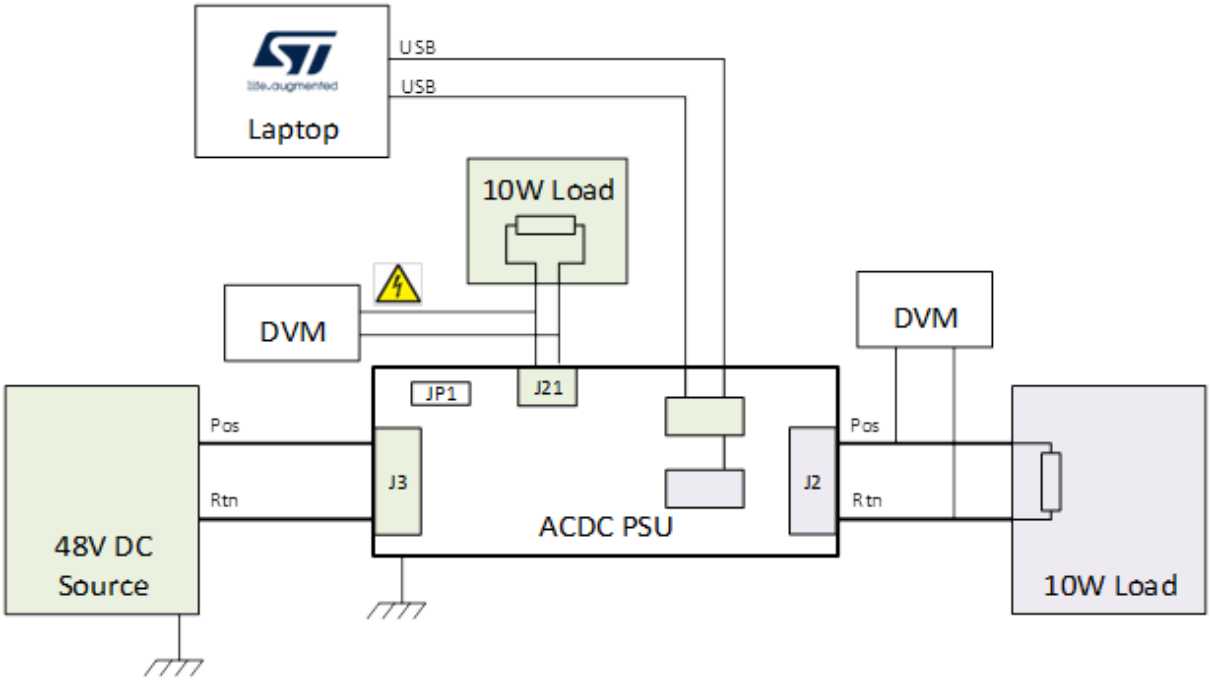


Table 20. AC-DC PSU test configuration electrical connections

Connection	Signal	Schematic signal name	Notes
J3 pin 1	55 V DC positive	LIVE*	AC or DC input (mode dependent)
J3 pin 3	55 V DC return	NEUTRAL*	AC or DC input (mode dependent)
J2 pin 1, 2	5 V DC output	VOUT_SENSE	DC output
J2 pin 3, 4	5 V DC return	GND2	DC output

12.2.4 Initial power up – Boost PFC stage, 60 V DC output

Step 1. With the connections as described above, enable the 55 V DC electrical power source.

Step 2. Confirm the current demand is no greater than 500 mA.
The boost PFC stage will begin to operate.

Step 3. Confirm the DVM connected to J21 displays 60 V DC.

Step 4. Ensure that the current drawn from the DC source does not exceed 1A. If the current drawn is higher, switch OFF the 55 V DC source and check the test configuration.

12.2.5 Measuring Boost PFC stage, 60 V DC output

Step 1. Observe the DVM indicating ~60 V DC present on the AC-DC PSU output.
If an electronic load with a current meter is used, a figure of ~500 mA should be displayed.

Step 2. Increase the load on the PFC stage of the PSU by reducing resistance of the load at J21– up to a maximum of 60 W (1 A) and confirm that the output stays within limits.

12.2.6 Noise and ripple measurement of the Boost PFC output

Configuring an oscilloscope to display the AC content of the output will allow the noise and ripple to be measured.
Recommended method: 100 MHz oscilloscope

Step 1. Select AC coupled on measuring channel.

Step 2. Reduce amplitude of channel to 100 mV/division (adjust as necessary during measurement).

Step 3. Set time base of channel to 100 µs/division (adjust as necessary during measurement).

Step 4. Connect oscilloscope probe center to positive output (J21 pin 1) as close to output as possible; probe negative to return (J21 pin 2).

Step 5. Measure and confirm the level of noise and ripple on the 60 V DC output.

Note: It may be necessary to increase the time base (200 µs, 500 µs, 1 ms) to display any voltage ripple as the frequency of the ripple is likely to be lower than the noise content.

12.2.7 Initial power up – phase-shift full-bridge converter stage, 4.8 V DC output

With the boost PFC stage operating (as described above), perform the following:

Step 1. Set power demand on the J21 (60 V DC) output to 10 W.

Step 2. Confirm the current demand is no greater than 500 mA.
The phase-shift full-bridge stage will begin to operate.

Step 3. Confirm the DVM connected to J2 displays 4.8 V DC.

Step 4. Ensure that the current drawn from the DC source does not exceed 1 A.
If the current drawn is higher, switch OFF the 55 V DC source and check the test configuration.

12.2.8 Measuring DC output

Step 1. Observe the DVM indicating ~4.8 V DC present on the AC-DC PSU output.
The lengths of the connections between the output of the AC-DC PSU and the load/DVM will affect the voltage reading.

Step 2. Increase the load on the AC-DC PSU up to a maximum of 48 W by reducing resistance of the load on the main 4.8 V output J2, and confirm that the output voltage remains within limits.

12.2.9 Noise and ripple measurement of the Phase Shift Full bridge output

Configuring an oscilloscope to display the AC content of the output will allow the noise and ripple to be measured.
Recommended method: 100 MHz oscilloscope,

Step 1. Select AC coupled on measuring channel.

Step 2. Reduce amplitude of channel to 100 mV/division (adjust as necessary during measurement).

Step 3. Set time base of channel to 100 µs/division (adjust as necessary during measurement).

Step 4. Connect oscilloscope probe center to positive output (J2 pin 1) as close to output as possible; probe negative to return (J2 pin 3).

Step 5. Measure and confirm the level of noise and ripple on the PSFB PSU output.

Note: It may be necessary to increase the time base (200 µs, 500 µs, 1 ms) to display any voltage ripple as the frequency of the ripple is likely to be lower than the noise content.

12.2.10 Turn-off and reconfiguration

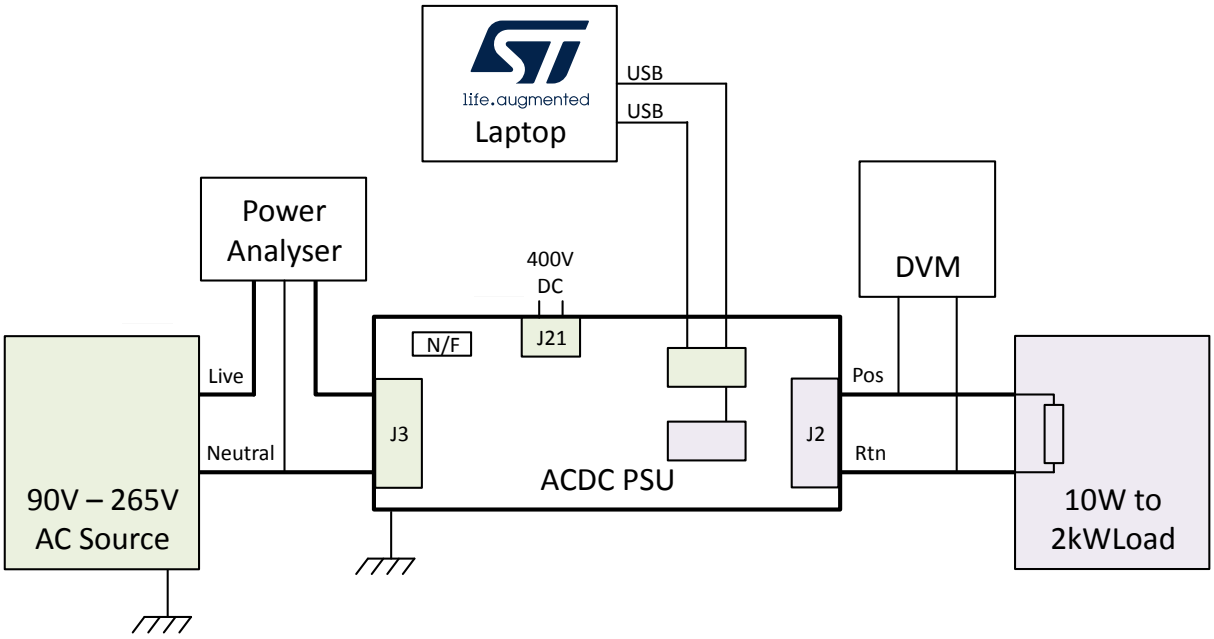
Step 1. Disable the DC source and reconfigure the test environment as necessary.

Operation of the AC-DC PSU in other modes will require the hardware and firmware to be reconfigured, refer to the previous section for the different modes of operation.

12.3 Operation of the AC-DC PSU in Mode 1 – default, 230 Vac input, 48 V DC output up to 2 kW

General configuration of the AC-DC PSU operating in mode 1 – default.

Figure 73. AC-DC PSU general test configuration – AC input mode 1



12.3.1 Initial connection checks

Step 1. Connect the AC-DC PSU to a 90-265 V AC current limited supply – max 10 A for 230 Vac input (do not turn ON at this point).

Step 2. Connect a variable load, initially set to 48 W (or 1 A), to the output of the AC-DC PSU. Ensure that the load has sufficient power capacity to safely dissipate the electrical power/heat.

Step 3. Connect a volt meter (or DMM configured appropriately) across the DC output.

Table 21. AC-DC PSU test configuration electrical connections – AC input mode 1

Connection	Signal	Schematic signal name	Notes
J3 pin 1	90-265 V AC live	LIVE*	AC input (mode dependent)
J3 pin 3	90-265 V AC neutral	NEUTRAL*	AC input (mode dependent)
J2 pin 1, 2	48 V DC output	VOUT_SENSE	DC output
J2 pin 3, 4	48 V DC return	GND2	DC output
J21 pin 1	400 V DC output	VBUS	PFC boost output (400 V DC)
J21 pin 2	400 V DC return	GND1	PFC boost output (400 V DC)

12.3.2 Power up of Boost PFC stage, 90-265 V AC input, 400 V DC output

Step 1. With the connections as described above, enable the 90-265 V AC power source.

Step 2. After the PFC bulk caps have charged, confirm that the current demand is no greater than 500 mA.

Step 3. Confirm the DVM connected to J21 displays 400 V DC .

12.3.3 Power up of Phase Shift Full bridge converter stage, 90-265 V AC input, 48 V DC output

Step 1. With the boost PFC stage operating (as described above), confirm the DVM connected to J2 displays 48 V DC.

Step 2. Ensure that the current drawn from the AC source does not exceed 0.5 A. If the current drawn is higher, switch OFF the 90-265 V AC input and check the test configuration.

12.3.4 Measuring 48 V DC output

Step 1. Observe the DVM indicating ~48 V DC present on the AC-DC PSU output. The lengths of the connections between the output of the AC-DC PSU and the load/DVM will affect the voltage reading.

Step 2. Increase the load on the AC-DC PSU up to a maximum of 2 kW by reducing resistance of the load and confirm that the output voltage stays within limits.

12.3.5 Noise and ripple of the Phase Shift full bridge PSU output

Configuring an oscilloscope to display the AC content of the output will allow the noise and ripple to be measured.

Recommended method: 100 MHz oscilloscope

Step 1. Select AC coupled on measuring channel

Step 2. Reduce amplitude of channel to 100 mV/division (adjust as necessary during measurement)

Step 3. Set time base of channel to 100 µs/division (adjust as necessary during measurement)

Step 4. Connect oscilloscope probe centeras close to output as possible to positive output; probe negative to return

Step 5. Measure and confirm the level of noise and ripple on the AC-DC PSU output.

Note: It may be necessary to increase the time base (200 µs, 500 µs, 1 ms) to display any voltage ripple as the frequency of the ripple is likely to be lower than the noise content.

12.3.6 Load regulation of the AC-DC PSU

The AC-DC PSU does not use remote voltage sensing, so the voltage measured across the load as it increases will drop proportionately. This effect can be minimized by connecting the DVM as close to the output of the AC-DC PSU as practical, ideally directly to the pins of J2.

12.4 Runtime configuration

When the project has been generated using STM32CubeMX, there should be minimal configuration required by the user within the IDE. Any changes made manually to autogenerated functions will be overwritten the next time the user regenerates the code within STM32CubeMX.

Only code located within `/*USER CODE … BEGIN */` and `/*USER CODE … END */` tags, or in custom user added files, will persist.

12.4.1 User modalities and debug

The app_dpower.h file contains a set of defined user modalities. These modalities determine the operation of the converter and can be used to help debug or verify correct operation. The following table details the list of user modalities along with a brief description of their function.

Although these settings can be added in or commented out manually for debugging purposes, persistent behavior should be configured by modifying the parameters using the X-CUBE-DPower pack via STM32CubeMX.

Table 22. User modalities

User modality	Description
LOW_VOLTAGE	When defined, all inputs and outputs are divided by a factor of 10. This allows for safe low voltage testing from a 23 Vac source providing 40 Vdc at the output.
DC_INPUT	When defined, the PFC stage will operate from a DC input. If this is not defined the PFC stage will look for a zero crossing of the input voltage even to start the soft start. Therefore, it would not start from a DC input.

12.5 Overall usage

The STM32 MCU control cards installed on the evaluation board come pre-flashed with the example software. This example software implements the full functionality as described in this application note and the accompanying application note for the PSFB converter. To re-program the MCU card that controls the PFC stage, the user must first compile the project associated with this application note.

The following dependencies are required to do this:

- PC with Windows 7 or later
  STM32 compatible IDE, such as STM32CubeIDE or IAR Embedded Workbench or Keil µVision
- STM32CubeMX (from v6.5.0) together with STM32Cube FW library for G4 (from v1.5.1) installed

To get started:

Step 1. Ensure that the any mains input is disconnected. There must be no voltage present on the board, all capacitors must have fully discharged. Check this with a DMM before connecting anything to the board.

Step 2. Connect the ST-LINK/V2 ISO debugger to the JTAG header on the PFC control card.

Step 3. Apply 3.3 V to power the MCU via test pins TP46 (+3.3 V) and J7 (GND).

12.6 Loading the project

The PFC example project for this EVM, as well as the associated ST-PLD design files, are available within the Digital Power pack, X-CUBE-DPOWER, for STM32CuebMX.

See https://www.st.com/content/st_com/en/ecosystems/stm32-digital-power.html for more information on this pack.

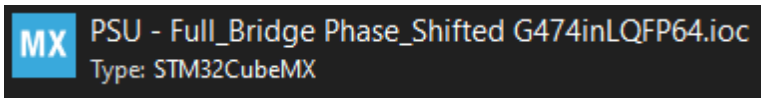
Step 1. With the pack installed, locate the example .ioc file from the pack's file references directory.

The directory is typically located in:
C:\Users\<user>\STM32Cube\Repository\Packs\STMicroelectronics\X-CUBE-DPower\<version>\CubeMX Files References

Step 2. Open STM32CubeMX by clicking on the [**PFC - Interleaved Boost G474inFQFP64.ioc**] as shown below.

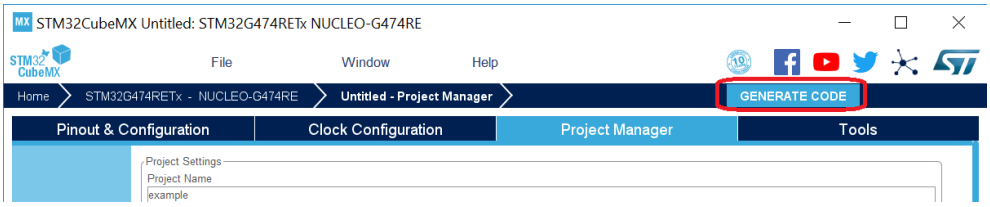
Note: The icon and the path may be different

Figure 74. PSFB example icon



Step 3. Generate the project by clicking the [**GENERATE CODE**] button in STM32CubeMX.

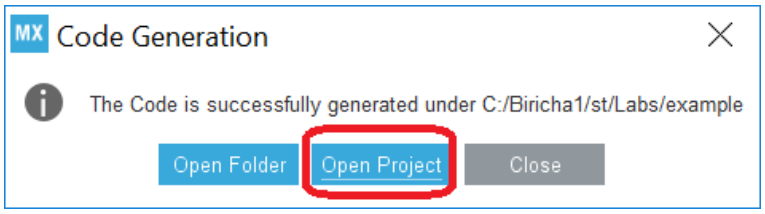
Figure 75. PFC example code generation



This will generate the project for your selected IDE. In this case, it will be an STM32CubeIDE project.

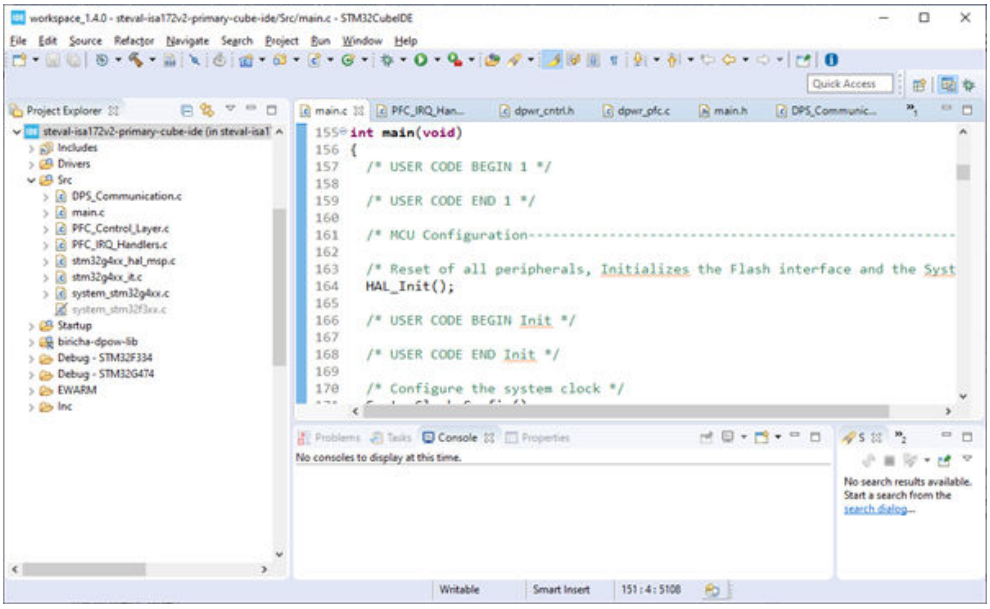
Step 4. When prompted with the dialog box, open the project by clicking [**Open project**].

Figure 76. PFC example Open Project



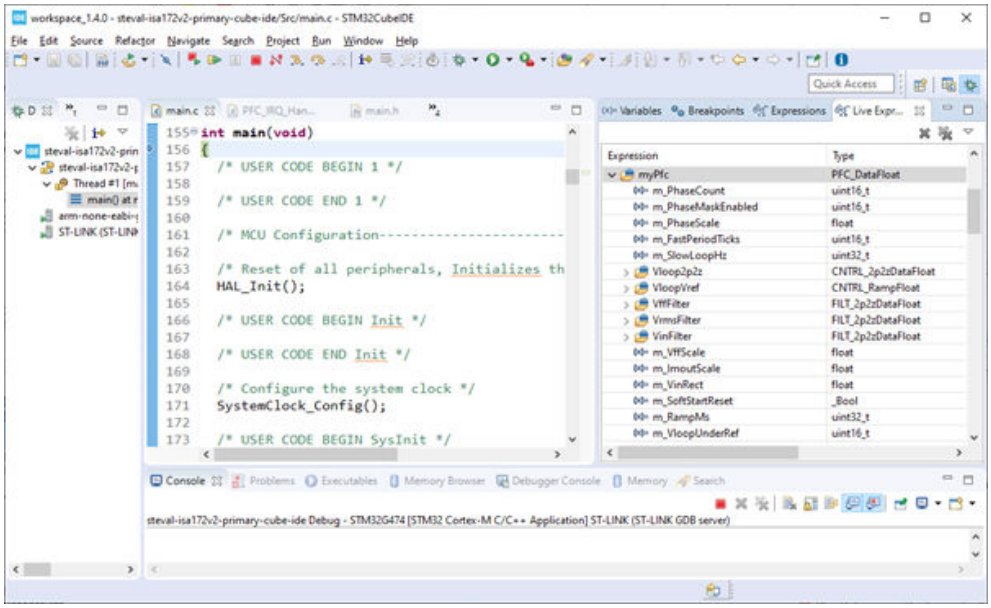
This will open STM32CubeIDE, or the IDE that you have selected under the [**Project Manager**] tab.

Figure 77. PFC example open in IDE



Step 5. Inside the IDE, click the [**Debug**] icon that  will compile and download your code to the MCU. The code is now ready to run. The IDE will move the program counter to your `int main(void)` function.

Figure 78. PFC example int main(void) function



Step 6. The buttons along the top menu bar have the functions described below. Click the [**Go**] button to run the code.

–  Resume – This runs the code

–  Suspend – This halts the code

–  Terminate – This terminates the debug session

–  Reset - This resets the MCU and sets the code start back to the beginning

Step 7. Click [**Terminate**]  to end the debug session.

The firmware has now been downloaded into the microcontroller flash and as such, the IDE can now be closed if the debugging features are not being used. The same program will restart each time power is applied to the MCU as it is running from the MCU flash.

Step 8. Close the IDE.

13 Measured results

In this section the PFC stage of the EVM is tested and the measurement results are captured and discussed. The tests performed include:

- Line and Load Regulation:
  - Line and load regulation tests are conducted to evaluate the stability of the output voltage under different input voltage levels and load conditions. The results demonstrate the ability of the EVM to maintain a stable output voltage as the input voltage and load currents change within the specified range.
- Efficiency:
  - Efficiency tests were performed to determine the power conversion efficiency of the EVM under various load conditions. The results provide a clear picture of the overall efficiency of the EVM, highlighting its performance in terms of energy conversion and losses.
- Input Voltage/Current Waveforms:
  - The input voltage and current waveforms were analyzed to understand the behavior of the EVM under different AC input conditions. This analysis helps to ensure that the input current waveform follows the input voltage waveform, maintaining a high power factor and low harmonic distortion.
- Input Current Harmonics (EN61000-3-4):
  - Input current harmonics tests were conducted following the EN61000-3-4 standard to evaluate the EVM's compliance with the harmonic current limits. The test results indicate the performance of the interleaved Boost PFC in reducing input current harmonics and maintaining a high power factor.
- Voltage Dips and Interruptions (EN61000-4-11):
  - The EVM was subjected to voltage dips and interruptions tests as per the EN61000-4-11 standard to assess its performance under momentary interruptions and reductions in the AC input voltage. The results provide insights into the EVM's ability to maintain stable operation during such events.
- PFC Loop Measurement:
  - PFC voltage loop measurements were taken to evaluate the dynamic response of the control loop under different load conditions. This assessment helps to understand the stability and robustness of the PFC control loop.
- Conducted Emissions (EN55032):
  - The EVM conducted emissions were measured in accordance with the EN55032 standard to ensure compliance with the electromagnetic compatibility (EMC) requirements. The results demonstrate the effectiveness of the EVM input filter in mitigating conducted emissions.
- Radiated Emissions (EN55032):
  - Radiated emissions tests were conducted following the EN55032 standard to evaluate the EVM compliance with the radiated emissions limits. The test results provide insights into the EVM overall electromagnetic performance and help to identify areas where improvements may be required.

In the following sections, each test result will be discussed in detail, highlighting the performance of the EVM and any potential areas for optimization.

13.1 Line and load regulation

The line and load regulation, as well as power factor and efficiency are recorded across the entire output voltage and current range.

Table 23. Line and load regulation @ 230Vac, 48 V output

Test ID	Input voltage (source)	Input voltage (conn)	Input current (A)	Input Freq (Hz)	Input (Real) Power (W)	Input PF	Output voltage (V)	Output current (A)	Output Power (W)	Efficiency	Status
0	230	230.4	0.825	50	9.7	0.12	48.183	0	0	0.00%	PASSED
1	230	230.3	1.013	50	115.28	0.55	48.177	2.082	100.329	78.10%	PASSED
2	230	230.1	1.324	50	219.7	0.76	48.172	4.169	200.816	86.30%	PASSED
3	230	230.1	1.692	50	321.73	0.86	48.171	6.247	300.915	89.90%	PASSED
4	230	229.9	2.085	50	423.62	0.91	48.168	8.333	401.386	92.00%	PASSED
5	230	229.8	2.521	50	526.51	0.93	48.16	10.419	501.786	93.00%	PASSED
6	230	229.6	2.952	50	630.15	0.95	48.163	12.497	601.912	93.80%	PASSED
7	230	229.5	3.375	50	738.25	0.97	48.165	14.584	702.419	93.70%	PASSED
8	230	229.5	3.815	50	843.18	0.98	48.163	16.67	802.859	94.00%	PASSED
9	230	229.4	4.264	50	947.96	0.98	48.153	18.748	902.767	94.20%	PASSED
10	230	229.3	4.713	50	1053.26	0.98	48.156	20.834	1003.29	94.30%	PASSED
11	230	229.2	5.204	50	1163.64	0.98	48.153	22.92	1103.676	94.10%	PASSED
12	230	229.1	5.652	50	1269.26	0.99	48.15	24.998	1203.666	94.30%	PASSED
13	230	229.1	6.105	50	1375.85	0.99	48.15	27.084	1304.105	94.30%	PASSED
14	230	229	6.567	50	1485.09	0.99	48.148	29.171	1404.525	94.20%	PASSED
15	230	228.9	7.028	50	1592.13	0.99	48.146	31.249	1504.492	94.20%	PASSED
16	230	228.8	7.49	50	1699.2	0.99	48.137	33.337	1604.743	94.20%	PASSED
17	230	228.7	7.955	50	1807.08	0.99	48.13	35.415	1704.518	94.20%	PASSED
18	230	228.6	8.43	50	1915.97	0.99	48.127	37.501	1804.81	94.10%	PASSED
19	230	228.5	8.9	50	2024.47	0.99	48.118	39.587	1904.859	94.10%	PASSED
20	230	228.4	9.374	50	2133.11	1	48.11	41.666	2004.549	94.00%	PASSED

Table 24. **Line and load regulation @ 230 Vac, 40 V output**

Test ID	Input voltage (source)	Input voltage (conn)	Input current (A)	Input Freq (Hz)	Input (Real) Power (W)	Input PF	Output voltage (V)	Output current (A)	Output Power (W)	Efficiency	Status
22	230	230.4	0.825	50	10.25	0.12	40.289	0	0	0.00%	PASSED
23	230	230.4	0.966	50	96.66	0.49	40.221	2.099	84.416	76.80%	PASSED
24	230	230.2	1.218	50	185.83	0.71	40.211	4.201	168.936	84.80%	PASSED
25	230	230.1	1.517	50	273.18	0.82	40.206	6.304	253.453	88.50%	PASSED
26	230	230.1	1.833	50	358.59	0.88	40.197	8.398	337.584	90.70%	PASSED
27	230	230	2.17	50	445.34	0.92	40.196	10.501	422.082	92.10%	PASSED
28	230	229.9	2.551	50	533.36	0.93	40.197	12.603	506.606	92.80%	PASSED
29	230	229.8	2.914	50	621.33	0.95	40.191	14.698	590.71	93.10%	PASSED
30	230	229.7	3.277	50	709.87	0.96	40.195	16.8	675.275	93.60%	PASSED
31	230	229.6	3.644	50	802.09	0.97	40.184	18.903	759.592	93.40%	PASSED
32	230	229.5	4.016	50	890.45	0.98	40.178	20.997	843.613	93.70%	PASSED
33	230	229.5	4.396	50	979.43	0.98	40.167	23.099	927.849	93.80%	PASSED
34	230	229.4	4.785	50	1069.32	0.98	40.169	25.202	1012.339	93.80%	PASSED
35	230	229.3	5.208	50	1164.14	0.98	40.166	27.296	1096.379	93.40%	PASSED
36	230	229.2	5.593	50	1254.73	0.99	40.159	29.399	1180.625	93.40%	PASSED
37	230	229.1	5.977	50	1345.26	0.99	40.157	31.501	1265.017	93.50%	PASSED
38	230	229.1	6.366	50	1437.69	0.99	40.145	33.606	1349.123	93.40%	PASSED
39	230	229	6.755	50	1528.47	0.99	40.141	35.698	1432.951	93.40%	PASSED
40	230	228.9	7.152	50	1620.62	0.99	40.144	37.803	1517.548	93.30%	PASSED
41	230	228.8	7.549	50	1712.81	0.99	40.137	39.905	1601.687	93.30%	PASSED
42	230	228.8	7.943	50	1804.12	0.99	40.136	42	1685.708	93.20%	PASSED

Table 25. **Line and load regulation @ 230Vac, 55 V output**

Test ID	Input voltage (source)	Input voltage (conn)	Input current (A)	Input Freq (Hz)	Input (Real) Power (W)	Input PF	Output voltage (V)	Output current (A)	Output Power (W)	Efficiency	Status
43	230	230.4	0.825	50	9.2	0.12	55.227	0	0	0.00%	PASSED
44	230	230.3	1.004	50	111.69	0.54	55.213	1.822	100.581	80.60%	PASSED
45	230	230.2	1.329	50	220	0.76	55.215	3.639	200.925	86.20%	PASSED
46	230	230.1	1.7	50	323.34	0.86	55.213	5.458	301.371	89.60%	PASSED
47	230	230	2.081	50	423.13	0.91	55.215	7.276	401.724	92.10%	PASSED
48	230	229.9	2.516	50	526.04	0.93	55.199	9.093	501.915	93.20%	PASSED
49	230	229.8	2.944	50	628.55	0.95	55.2	10.91	602.244	93.90%	PASSED
50	230	229.7	3.367	50	731.79	0.96	55.198	12.727	702.534	94.40%	PASSED
51	230	229.7	3.798	50	839.02	0.97	55.192	14.545	802.754	94.40%	PASSED
52	230	229.5	4.243	50	943.46	0.98	55.2	16.362	903.183	94.60%	PASSED
53	230	229.5	4.695	50	1048.9	0.98	55.198	18.188	1003.91	94.80%	PASSED
54	230	229.4	5.182	50	1158.29	0.98	55.189	20.005	1104.037	94.50%	PASSED
55	230	229.3	5.627	50	1263.23	0.99	55.184	21.822	1204.239	94.70%	PASSED
56	230	229.2	6.075	50	1368.73	0.99	55.188	23.637	1304.5	94.70%	PASSED
57	230	229.1	6.533	50	1476.22	0.99	55.181	25.457	1404.726	94.70%	PASSED
58	230	228.9	6.99	50	1582.74	0.99	55.181	27.272	1504.877	94.70%	PASSED
59	230	228.9	7.447	50	1689.6	0.99	55.177	29.091	1605.174	94.70%	PASSED
60	230	228.7	7.913	50	1796.48	0.99	55.179	30.909	1705.516	94.80%	PASSED
61	230	228.6	8.374	50	1903.66	0.99	55.18	32.726	1805.819	94.80%	PASSED
62	230	228.5	8.84	50	2011.05	1	55.167	34.551	1906.078	94.70%	PASSED
63	230	228.5	9.31	50	2118.65	1	55.166	36.369	2006.325	94.70%	PASSED

Table 26. **Line and load regulation @ 120Vac, 48 V output**

Test ID	Input voltage (source)	Input voltage (conn)	Input current (A)	Input Freq (Hz)	Input (Real) Power (W)	Input PF	Output voltage (V)	Output current (A)	Output Power (W)	Efficiency	Status
64	120	120.9	0.551	60	9.35	0.34	48.202	0	0	0.00%	PASSED
65	120	120.7	1.209	60	117.66	0.9	48.197	2.082	100.369	76.30%	PASSED
66	120	120.5	2.098	60	224.2	0.94	48.186	4.169	200.873	84.30%	PASSED
67	120	120.3	2.897	60	327.52	0.98	48.188	6.247	301.016	88.10%	PASSED
68	120	120.2	3.734	60	431.11	0.99	48.187	8.333	401.54	90.30%	PASSED
69	120	120	4.619	60	539.41	1	48.178	10.419	501.971	90.80%	PASSED
70	120	119.8	5.503	60	646.34	1	48.179	12.499	602.206	91.40%	PASSED
71	120	119.6	6.409	60	754.86	1	48.175	14.585	702.661	91.80%	PASSED
72	120	119.4	7.34	60	866.88	1	48.169	16.67	802.969	91.70%	PASSED
73	120	119.2	8.242	60	975.45	1	48.171	18.748	903.106	91.90%	PASSED
74	120	119	9.169	60	1086.79	1	48.167	20.836	1003.612	92.00%	PASSED
75	120	118.8	10.092	60	1197.24	1	48.167	22.92	1104.009	92.00%	PASSED
76	120	118.7	11.014	60	1307.33	1	48.161	25	1204.049	92.20%	PASSED
77	120	118.6	11.954	60	1419.86	1	48.164	27.084	1304.495	92.10%	PASSED
78	120	118.4	12.903	60	1532.97	1	48.155	29.173	1404.817	92.10%	PASSED
79	120	118.3	13.851	60	1646.02	1	48.157	31.249	1504.842	92.00%	PASSED

Table 27. **Line and load regulation @ 120Vac, 40 V output**

Test ID	Input voltage (source)	Input voltage (conn)	Input current (A)	Input Freq (Hz)	Input (Real) Power (W)	Input PF	Output voltage (V)	Output current (A)	Output Power (W)	Efficiency	Status
80	120	120.9	0.551	60	10	0.35	40.306	0	0	0.00%	PASSED
81	120	120.8	1.042	60	97.75	0.89	40.248	2.082	83.815	75.30%	PASSED
82	120	120.6	1.829	60	188.43	0.92	40.233	4.169	167.721	82.80%	PASSED
83	120	120.5	2.491	60	275.9	0.96	40.228	6.247	251.297	86.80%	PASSED
84	120	120.3	3.174	60	362.25	0.98	40.224	8.333	335.187	89.10%	PASSED
85	120	120.2	3.888	60	450.11	0.99	40.215	10.419	419.003	90.30%	PASSED
86	120	120	4.64	60	541.89	1	40.209	12.497	502.508	90.50%	PASSED
87	120	119.9	5.388	60	632.16	1	40.231	14.584	586.712	91.00%	PASSED
88	120	119.7	6.144	60	723.26	1	40.218	16.67	670.424	91.20%	PASSED
89	120	119.6	6.909	60	814.59	1	40.21	18.748	753.845	91.40%	PASSED
90	120	119.5	7.686	60	908.28	1	40.211	20.834	837.746	91.30%	PASSED
91	120	119.3	8.442	60	999.66	1	40.19	22.92	921.158	91.50%	PASSED
92	120	119.1	9.224	60	1093.46	1	40.194	25	1004.87	91.40%	PASSED
93	120	118.9	10.006	60	1187.01	1	40.178	27.084	1088.204	91.50%	PASSED
94	120	118.8	10.792	60	1280.94	1	40.174	29.173	1171.981	91.50%	PASSED
95	120	118.7	11.583	60	1375.3	1	40.165	31.249	1255.114	91.40%	PASSED

Table 28. **Line and load regulation @ 120Vac, 55 V output**

Test ID	Input voltage (source)	Input voltage (conn)	Input current (A)	Input Freq (Hz)	Input (Real) Power (W)	Input PF	Output voltage (V)	Output current (A)	Output Power (W)	Efficiency	Status
96	120	120.9	0.547	60	8.99	0.34	55.229	0	0	0.00%	PASSED
97	120	120.8	1.175	60	113.79	0.9	55.229	1.822	100.61	78.90%	PASSED
98	120	120.6	2.102	60	224.57	0.94	55.236	3.639	201.001	84.10%	PASSED
99	120	120.4	2.91	60	329.02	0.98	55.222	5.458	301.422	87.80%	PASSED
100	120	120.3	3.726	60	430.49	0.99	55.222	7.276	401.778	90.40%	PASSED
101	120	120.1	4.606	60	538.03	1	55.22	9.093	502.111	91.10%	PASSED
102	120	119.9	5.482	60	643.71	1	55.209	10.908	602.229	91.80%	PASSED
103	120	119.7	6.375	60	750.94	1	55.211	12.727	702.701	92.20%	PASSED
104	120	119.6	7.302	60	861.94	1	55.204	14.545	802.934	92.10%	PASSED
105	120	119.4	8.199	60	970.12	1	55.204	16.362	903.252	92.40%	PASSED
106	120	119.2	9.122	60	1081.16	1	55.202	18.188	1003.983	92.40%	PASSED
107	120	119	10.036	60	1190.62	1	55.192	20.005	1104.097	92.50%	PASSED
108	120	118.9	10.959	60	1300.49	1	55.195	21.822	1204.462	92.60%	PASSED
109	120	118.6	11.886	60	1411.5	1	55.184	23.639	1304.507	92.60%	PASSED
110	120	118.5	12.826	60	1523.17	1	55.189	25.457	1404.932	92.60%	PASSED
111	120	118.3	13.766	60	1635.9	1	55.182	27.272	1504.926	92.60%	PASSED

13.2 Efficiency

The efficiency tests are performed by measuring the input voltage, input current and power factor versus the output voltage and current across various input voltage levels and load levels.

The equation used for calculating the efficiency is as follows with Equation 36:

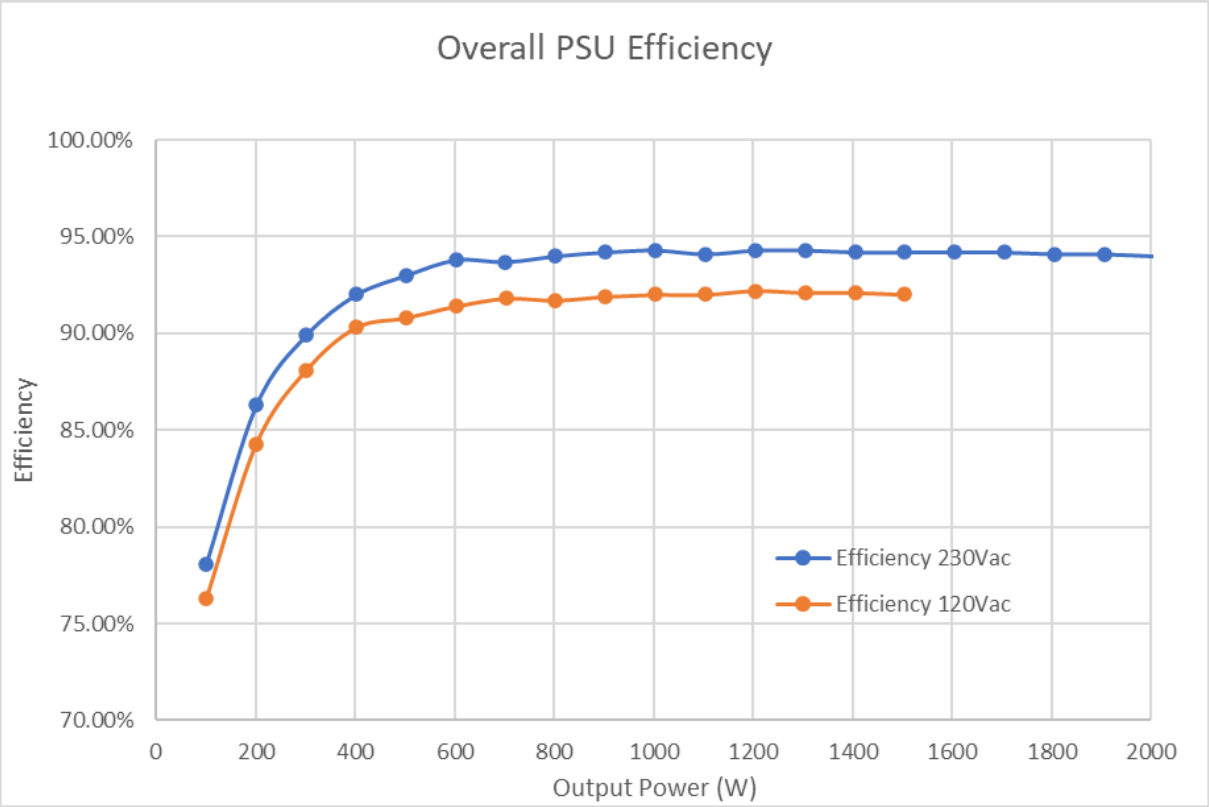
$$Eff = \frac{V_{OUT} \cdot I_{OUT}}{V_{AC(RMS)} \cdot I_{AC(RMS)} \cdot PF} \quad (36)$$

As the RMS current as measured on the input side contains all of the harmonic currents, including reactive power, the input power is multiplied by the power factor to obtain the real input power.

This test provides insights into the EVM performance in terms of energy conversion and enables the evaluation of the overall design and component selection. The results can be utilized to identify opportunities for optimization and improvement, ultimately leading to a more energy-efficient and environmentally friendly power supply solution. Additionally, the efficiency measurements help to ensure that the EVM complies with relevant industry standards and energy efficiency requirements.

The peak efficiency, at nominal output voltage, is measured as 93.4% with a 1000W load (50% rated). Highest overall efficiency is measured as 94.8% at 55V output and 50% load. Note that the external fans are excluded during the efficiency test.

Figure 79. Overall PSU efficiency measured with 48 V output (nominal)



13.3 Input voltage/current waveforms

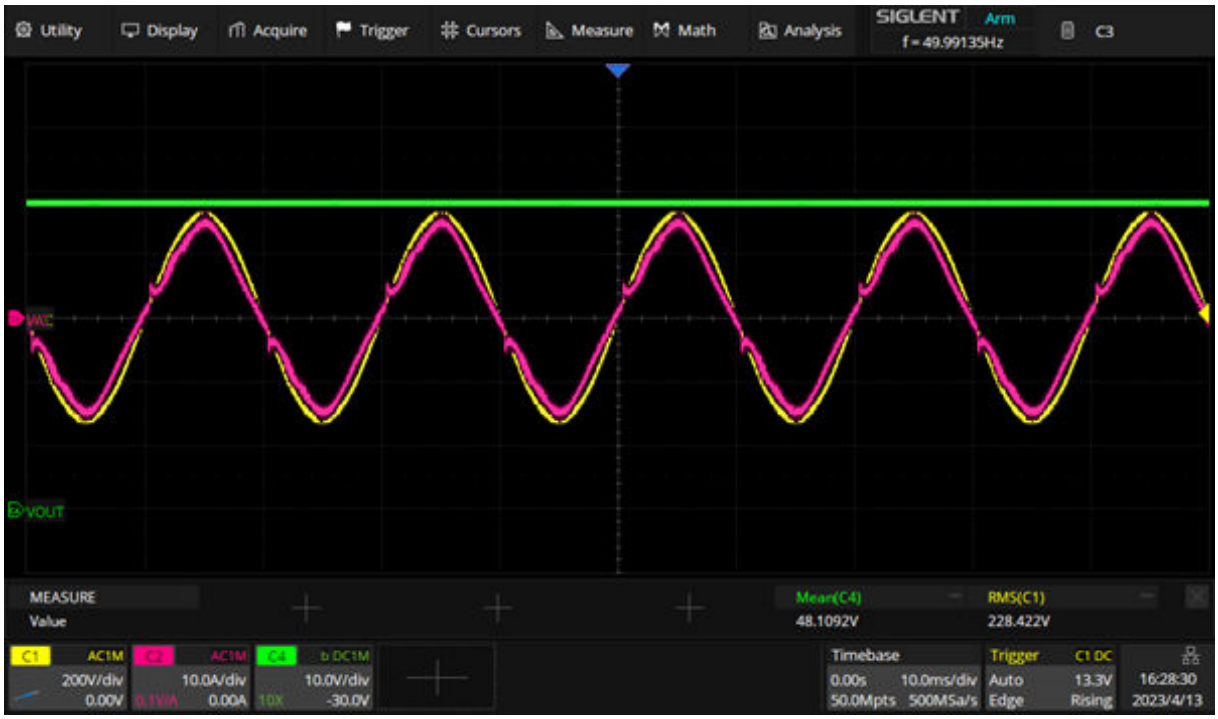
In this section, the measurement results for the input voltage and input current are presented. A well-tuned PFC control loop should exhibit a close relationship between the input voltage and current waveforms, ideally with the current waveform following the shape of the input voltage waveform. This ensures a high power-factor and minimizes total harmonic distortion, reducing the impact of the power supply on the power grid.

During the tests, the input voltage and current waveforms were captured using the oscilloscope with a differential voltage probe and current clamp. The PSU is operated tested at nominal 230Vac and 120Vac under various load conditions. By analysing the shape, phase relationship, and distortion of these waveforms, we can assess the performance of the PFC stage, as well as the effectiveness of the input filtering on the input current ripple.

In Figure 80, the PSU is supplied with 230Vac and loaded at the maximum load of 2kW. The input current tracks the input voltage very well, however there is a small distortion visible shorty after zero crossing. This is due to the discontinuous conduction mode (DCM) to continuous conduction mode (CCM) transition of the PFC inductor current. The behavior of the control loop under DCM is different to that of CCM. When the inductor enters CCM, the inductor current overshoots and the control loop correct for this over time.

This could be improved by either increasing the inductance of the PFC inductors to ensure CCM operation for more of the line cycle, increasing the switching frequency or by implementing slew rate limiting around zero crossing.

Figure 80. TEST_ID_20_LOAD_REGULATION (230 Vac, 100% load)



With 120 Vac input in Figure 81, the DCM to CCM transition occurs at the same inductor current level, however the overall inductor current is higher due to the reduced input voltage. This means than the THD of the inductor current waveform is lower when operating from a low line input voltage. However, for EN61000-3-2 the input current harmonics are measured with a 230 Vac source.

Figure 81. **TEST_ID_77_LOAD_REGULATION (120 Vac, 65% load)**



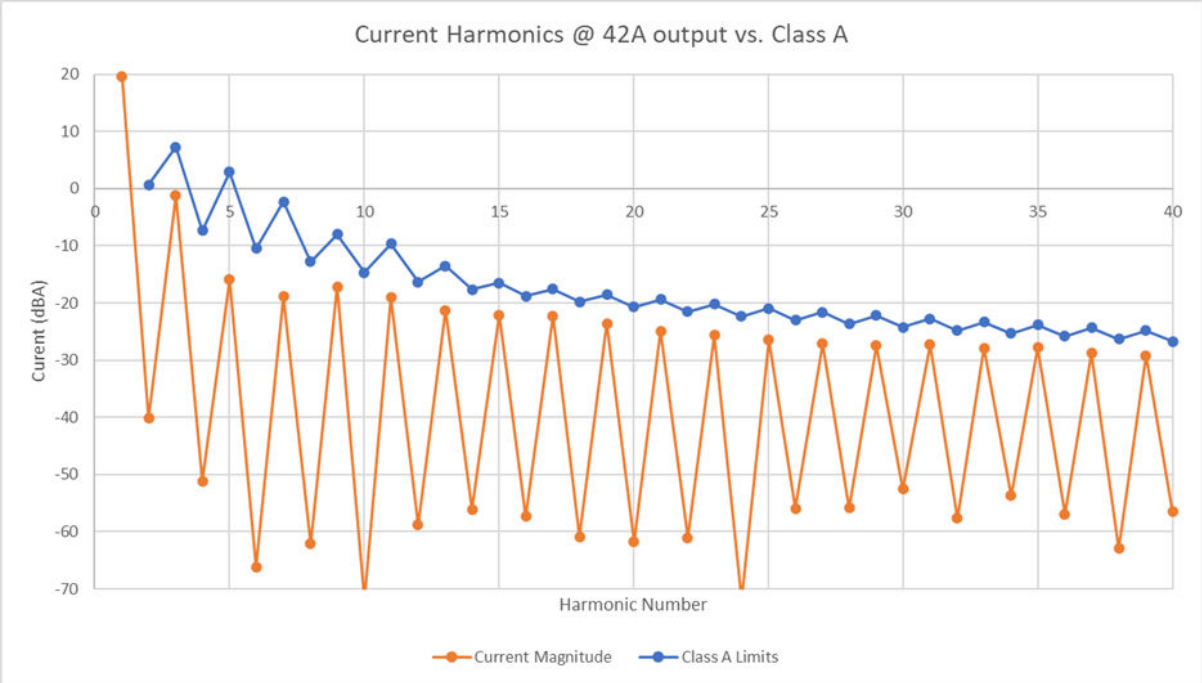
(Input current probe 20 A max.)

13.4 Input current harmonics (EN61000-3-2)

This section presents the measurement results for the input current harmonics of the EVM. A harmonic analyzer is used to measure the harmonic distortion present in the input current waveform and these measured harmonics are then compared to the limits imposed by the standard.

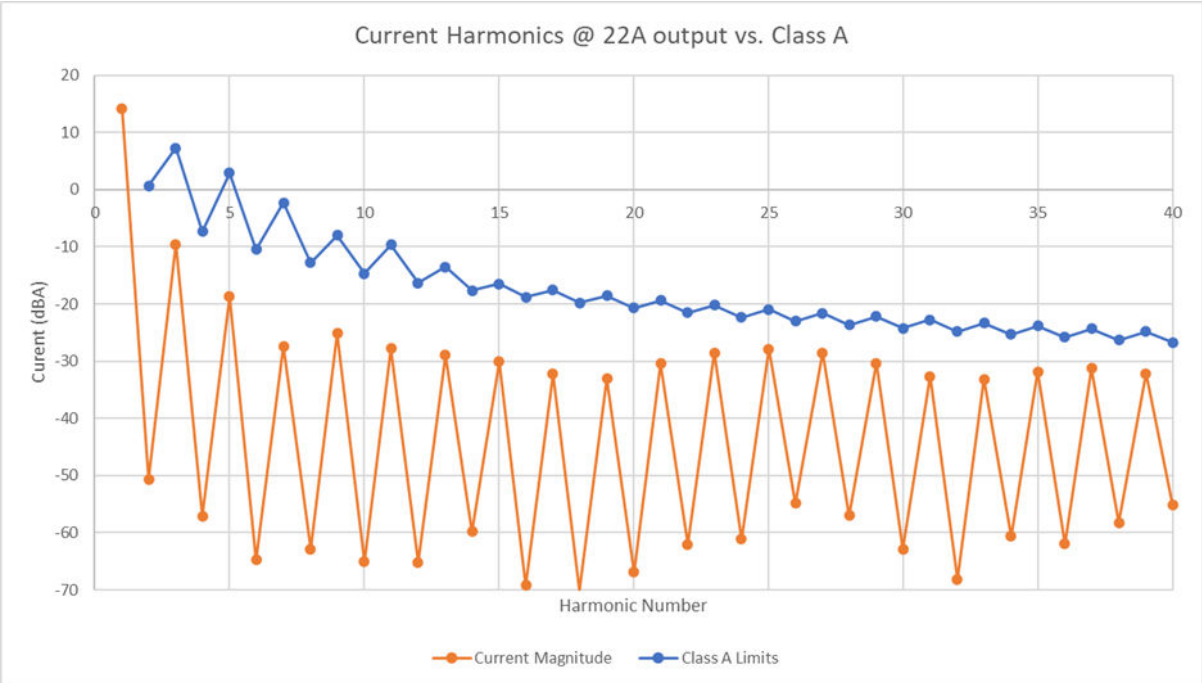
For this power supply, the Class A limits from EN61000-3-2 are applied. In Figure 82 the PSU is operating at full load, 2 kW, from a 230 Vac input. The measured harmonics are displayed in orange and compared to the limits in blue. The measured harmonics are all below the limits demonstrating a clear pass for this PSU.

Figure 82. Input current harmonics, 230 Vac input, 2 kW (48V@42A) output vs. Class A



Typically, the power supply will be tested at maximum rated load. However, it is important to ensure compliance across the entire load range. For example, in Figure 83, the test is performed again at 1 kW output, half load, and the power supply still shows a clear pass when compared to the limits from the standard.

Figure 83. Input current harmonics, 230 Vac input, 1kW (48V@22A) output vs. Class A



In Table 29 the total harmonic distortion (THD) is measured for different key power levels. Generally speaking, as the output power is reduced the THD will increase [PB1] [MH2] as the circulating current in the reactive components of the input filter will become a larger component of the overall input current in tandem with the distorted input current due to the DCM/CCM transition.

Table 29. **Total harmonic distortion as measured on PM6000 at 230 Vac**

Output Power	Power Factor	A THD
2000W (100%)	0.9988337	7.4%
1000W (50%)	0.9823269	9.8%
400W (20%)	0.9098646	14.2%

13.5 Voltage dips/interruptions (EN61000-4-11)

Voltage dips and interruptions can occur on the power grid due to various reasons, such as faults, load changes, or switching events. Power supplies must be able to cope with these fluctuations without compromising the output voltage quality or causing damage to the connected load. These tests simulate real-world scenarios where the input voltage may momentarily drop or be completely lost. The response of the EVM to such events is crucial in determining its overall reliability and robustness.

There are three performance criteria defined by the standard:

- Performance criteria A: no change in operating status. That is, output voltage is not changed during/after dip or interruption.
- Performance criteria B: there is a loss of function during the test. The operating parameters return to normal after the test. That is, the output voltage may deviate from its intended value, but will return to normal after the test.
- Performance criteria C: There is a loss of function during the test and manual intervention is required to restore functionality after the test. That is, the user needs to turn the device off and on.

The standard does not specify a pass/fail criteria, only that the PSU should be functional after the tests. The table below lists the desired performance criteria for each test.

Table 30. **Dips and interruption tests performed**

Test	Type	Percent Dipped	Voltage	Duration	Desired performance criteria
1	Dip	20%	230Vac > 184Vac	5s (250 cycles)	A
2	Dip	30%	230Vac > 161Vac	500ms (25 cycles)	A
3	Dip	60%	230Vac > 92Vac	100ms (5 cycles)	B
4	Int	100%	230Vac > 0Vac	20ms (1 cycle)	B
5	Int	100%	230Vac > 0Vac	10ms (0.5 cycle)	B
6	Int	100%	230Vac > 0Vac	5s (250 cycles)	B

Figure 84. **Test 1: 5s (250 cycles), 20% dip, 2 kW load**

Result: performance criteria A



Figure 85. **Test 1: 5s (250 cycles), 20% dip, 1 kW load**

Result: performance criteria A



Figure 86. **Test 2: 500ms (25 cycles), 30% dip, 2 kW load**

Result: performance criteria B



Figure 87. **Test 2: 500ms (25 cycles), 30% dip, 1 kW load**

Result: performance criteria A



Figure 88. **Test 3: 100ms (5 cycles), 60% dip, 2 kW load**

Result: performance criteria B



Figure 89. **Test 3: 100ms (5 cycles), 60% dip, 1 kW load**

Result: performance criteria B



Figure 90. Test 4: 20ms (1 cycle), 100% dip, 2 kW load

Result: performance criteria B



Figure 91. Test 4: 20ms (1 cycle), 100% dip, 1 kW load

Result: performance criteria A



Figure 92. **Test 5: 10ms (0.5 cycle), 100% dip, 2 kW load**

Result: performance criteria A



Figure 93. **Test 5: 10ms (0.5 cycle), 100% dip, 1 kW load**

Result: performance criteria A



The results of the dips and interruptions tests are summarized in Table 31. The PSU meets the desired performance criteria when operating at half load. At full load, the PSU cannot maintain the 2kW output during 30% dip. However, this is because the current loop of the PFC stage needs to be optimized for the lower input voltage. An improvement to the firmware would be to adjust the PFC current loop controller coefficients based on the input voltage at the moment in time.

Nevertheless, there is no minimum performance criteria specified by the standard – so the PSU does still pass this test.

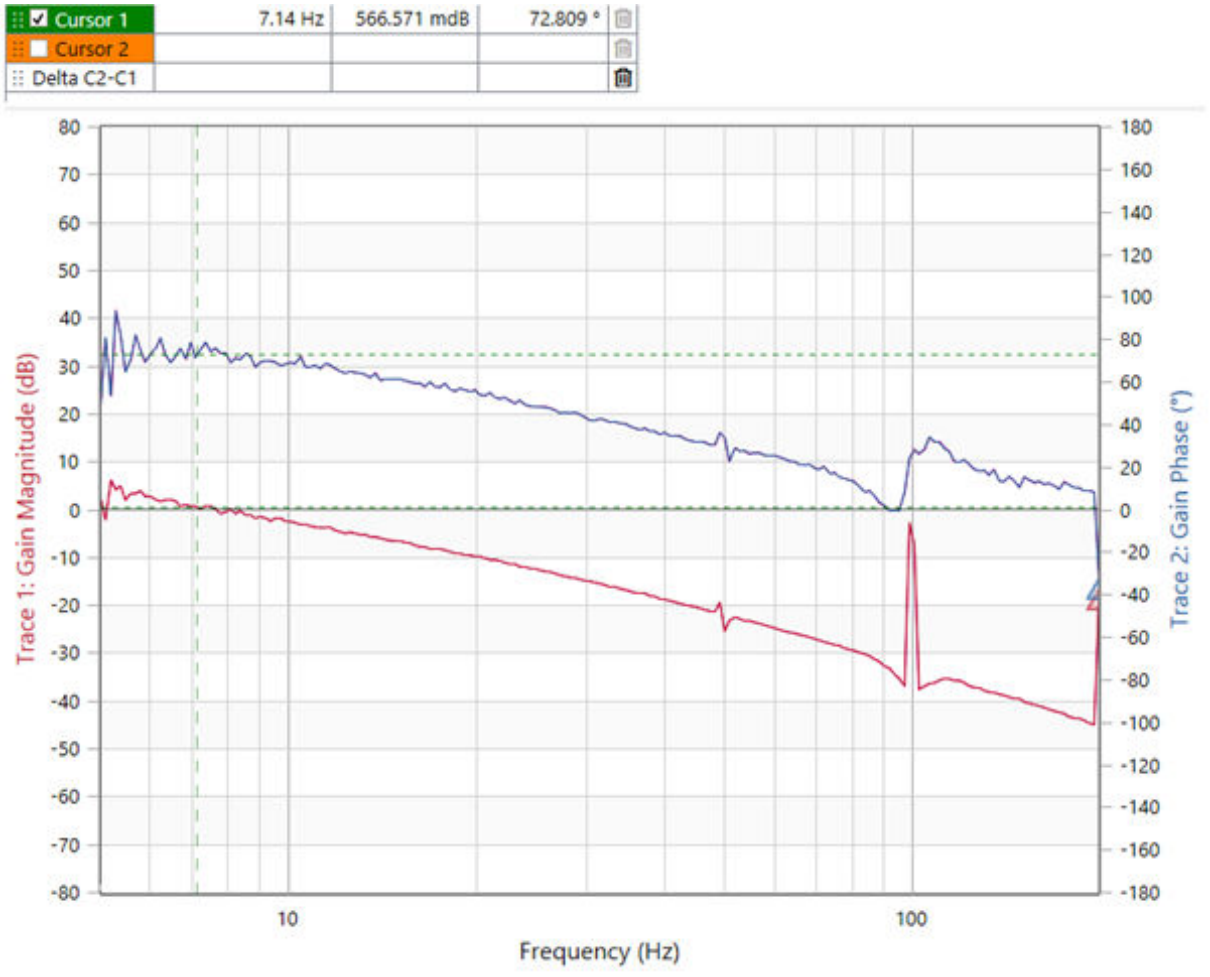
Table 31. Dips and interruption test results

Test	Type	Percent Dipped	Voltage	Duration	Perf @1kW	Perf @2kW
1	Dip	20%	230Vac > 184Vac	5s (250 cycles)	A	A
2	Dip	30%	230Vac > 161Vac	500ms (25 cycles)	A	B
3	Dip	60%	230Vac > 92Vac	100ms (5 cycles)	B	B
4	Int	100%	230Vac > 0Vac	20ms (1 cycle)	A	B
5	Int	100%	230Vac > 0Vac	10ms (0.5 cycle)	A	A
6	Int	100%	230Vac > 0Vac	5s (250 cycles)	B	B

13.6 PFC voltage loop

The PFC voltage loop is measured using the Bode 100 VNA from Omicron Lab. The voltage loop of the PFC stage must have a low crossover frequency, between 5 Hz and 10 Hz, to ensure that it does not interfere with the main job of the PFC stage which is to regulate the input current. However, the loop still must be stable to ensure that the PFC output voltage is maintained and regulated. In Figure 94, the voltage loop is measured with a crossover frequency of 7 Hz and a phase margin of 70 degrees. This meets the stability criteria and ensures that the closed loop response of the voltage loop will be stable.

Figure 94. PFC voltage loop measurement measured at 1 kW



13.7 Conducted emissions (EN55032) [pre-comp data]

Figure 95. **Conducted emissions set up with resistive load**

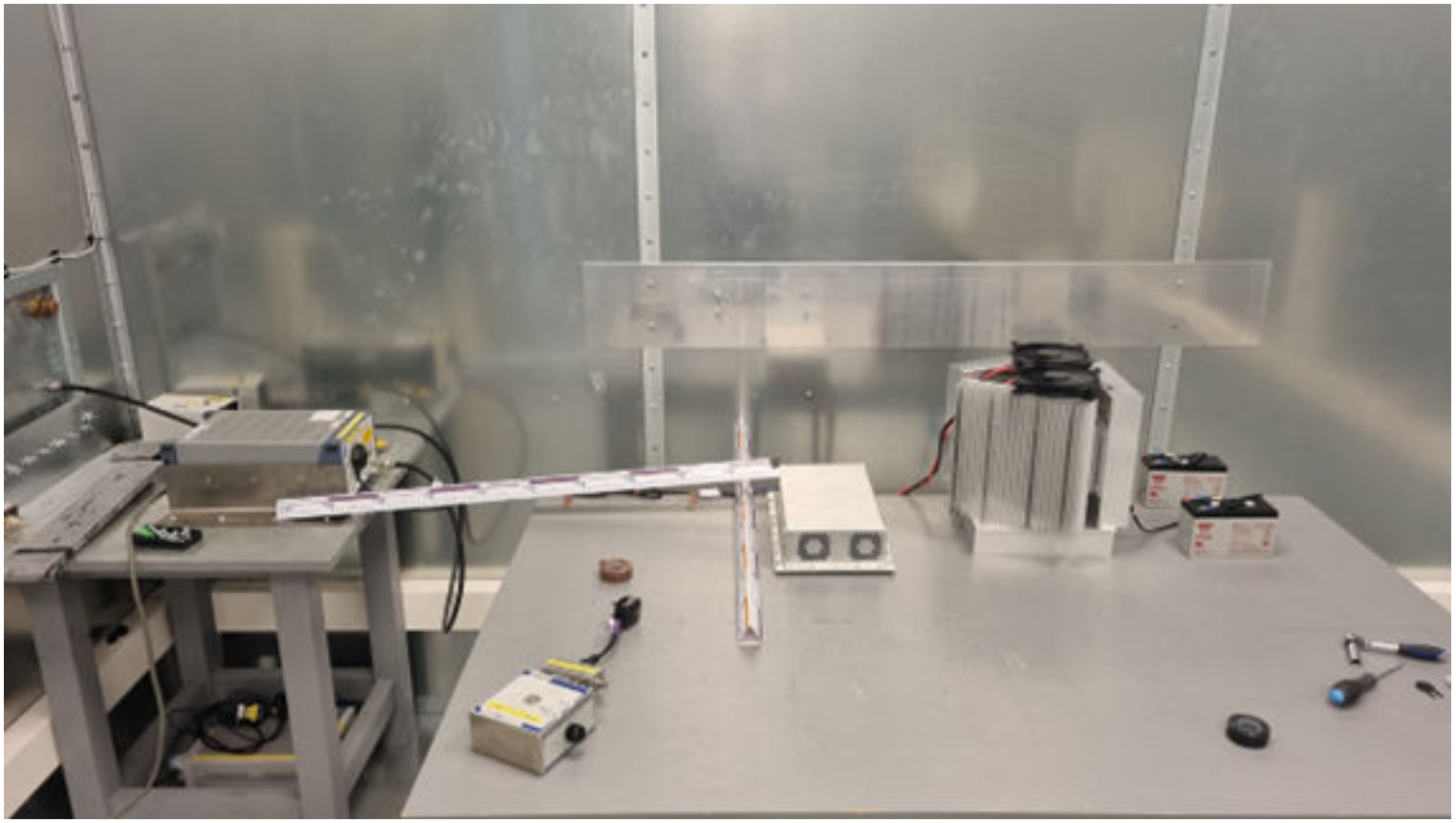


Figure 96. **Conducted emissions measurement on line**

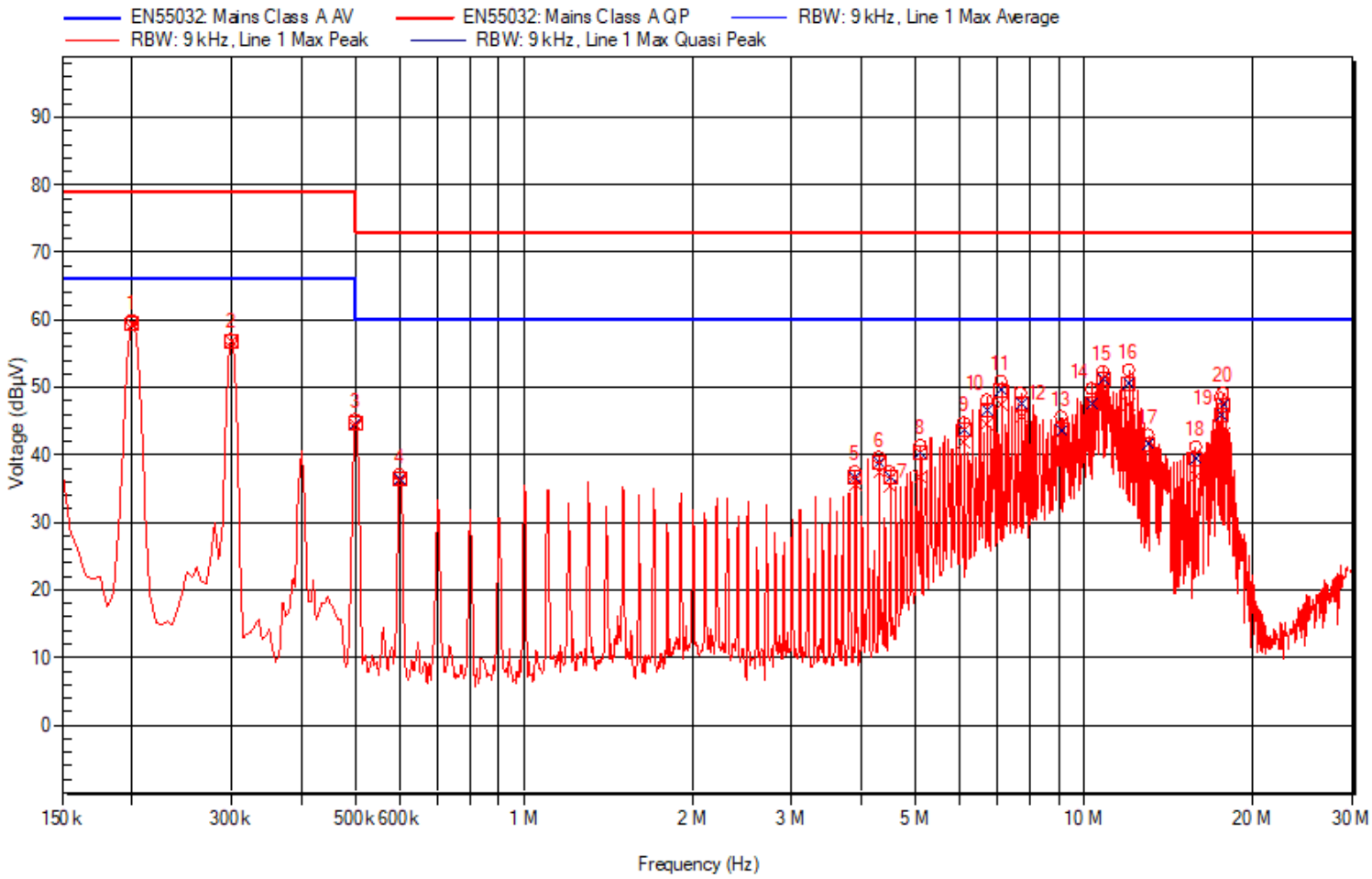


Table 32. **Conducted emissions harmonics measured on line**

Frequency	Peak	Peak Correction	Average	Average Limit	Average Difference	Average Correction	Average Status	Quasi-Peak	Quasi-Peak Limit	Quasi-Peak Difference	Quasi-Peak Correction	Quasi-Peak Status
200 kHz	59.8 dBµV	10 dB	59.4 dBµV	66 dBµV	-6.58 dB	10 dB	Pass	59.4 dBµV	79 dBµV	-19.55 dB	10 dB	Pass

Frequency	Peak	Peak Correction	Average	Average Limit	Average Difference	Average Correction	Average Status	Quasi-Peak	Quasi-Peak Limit	Quasi-Peak Difference	Quasi-Peak Correction	Quasi-Peak Status
300 kHz	57.1 dBµV	10 dB	56.8 dBµV	66 dBµV	-9.19 dB	10 dB	Pass	56.8 dBµV	79 dBµV	-22.16 dB	10 dB	Pass
500 kHz	45.2 dBµV	9.8 dB	44.5 dBµV	60 dBµV	-15.53 dB	9.8 dB	Pass	44.6 dBµV	73 dBµV	-28.41 dB	9.8 dB	Pass
600 kHz	37.1 dBµV	9.8 dB	36.2 dBµV	60 dBµV	-23.8 dB	9.8 dB	Pass	36.4 dBµV	73 dBµV	-36.65 dB	9.8 dB	Pass
3.9 MHz	37.4 dBµV	10.2 dB	35.7 dBµV	60 dBµV	-24.34 dB	10.2 dB	Pass	36.8 dBµV	73 dBµV	-36.25 dB	10.2 dB	Pass
4.3 MHz	39.6 dBµV	10.2 dB	37.4 dBµV	60 dBµV	-22.62 dB	10.2 dB	Pass	38.9 dBµV	73 dBµV	-34.14 dB	10.2 dB	Pass
4.5 MHz	37.5 dBµV	10.2 dB	35.3 dBµV	60 dBµV	-24.67 dB	10.2 dB	Pass	36.7 dBµV	73 dBµV	-36.29 dB	10.2 dB	Pass
5.1 MHz	41.4 dBµV	10.2 dB	36.7 dBµV	60 dBµV	-23.3 dB	10.2 dB	Pass	40.3 dBµV	73 dBµV	-32.69 dB	10.2 dB	Pass
6.1 MHz	44.7 dBµV	10.3 dB	41.9 dBµV	60 dBµV	-18.07 dB	10.3 dB	Pass	43.7 dBµV	73 dBµV	-29.25 dB	10.3 dB	Pass
6.7 MHz	48 dBµV	10.3 dB	44.6 dBµV	60 dBµV	-15.38 dB	10.3 dB	Pass	46.6 dBµV	73 dBµV	-26.4 dB	10.3 dB	Pass
7.1 MHz	50.8 dBµV	10.3 dB	47.5 dBµV	60 dBµV	-12.55 dB	10.3 dB	Pass	49.6 dBµV	73 dBµV	-23.37 dB	10.3 dB	Pass
7.7 MHz	49.1 dBµV	10.3 dB	45.7 dBµV	60 dBµV	-14.32 dB	10.3 dB	Pass	47.6 dBµV	73 dBµV	-25.39 dB	10.3 dB	Pass
9.101 MHz	45.7 dBµV	10.4 dB	40.6 dBµV	60 dBµV	-19.39 dB	10.4 dB	Pass	43.7 dBµV	73 dBµV	-29.34 dB	10.4 dB	Pass
10.3 MHz	49.7 dBµV	10.4 dB	44.7 dBµV	60 dBµV	-15.35 dB	10.4 dB	Pass	47.6 dBµV	73 dBµV	-25.37 dB	10.4 dB	Pass
10.8 MHz	52.3 dBµV	10.5 dB	47.2 dBµV	60 dBµV	-12.76 dB	10.5 dB	Pass	51.2 dBµV	73 dBµV	-21.78 dB	10.5 dB	Pass
12.001 MHz	52.5 dBµV	10.5 dB	47.4 dBµV	60 dBµV	-12.6 dB	10.5 dB	Pass	50.5 dBµV	73 dBµV	-22.47 dB	10.5 dB	Pass
13 MHz	43 dBµV	10.6 dB	36.9 dBµV	60 dBµV	-23.1 dB	10.6 dB	Pass	41.6 dBµV	73 dBµV	-31.41 dB	10.6 dB	Pass
15.8 MHz	41.1 dBµV	10.7 dB	36.8 dBµV	60 dBµV	-23.16 dB	10.7 dB	Pass	39.5 dBµV	73 dBµV	-33.54 dB	10.7 dB	Pass
17.501 MHz	48.3 dBµV	10.6 dB	42.1 dBµV	60 dBµV	-17.89 dB	10.6 dB	Pass	46 dBµV	73 dBµV	-27.04 dB	10.6 dB	Pass

Frequency	Peak	Peak Correction	Average	Average Limit	Average Difference	Average Correction	Average Status	Quasi-Peak	Quasi-Peak Limit	Quasi-Peak Difference	Quasi-Peak Correction	Quasi-Peak Status
17.7 MHz	49.1 dBµV	10.6 dB	43.1 dBµV	60 dBµV	-16.87 dB	10.6 dB	Pass	47.5 dBµV	73 dBµV	-25.53 dB	10.6 dB	Pass

Figure 97. Conducted emissions measurement on neutral

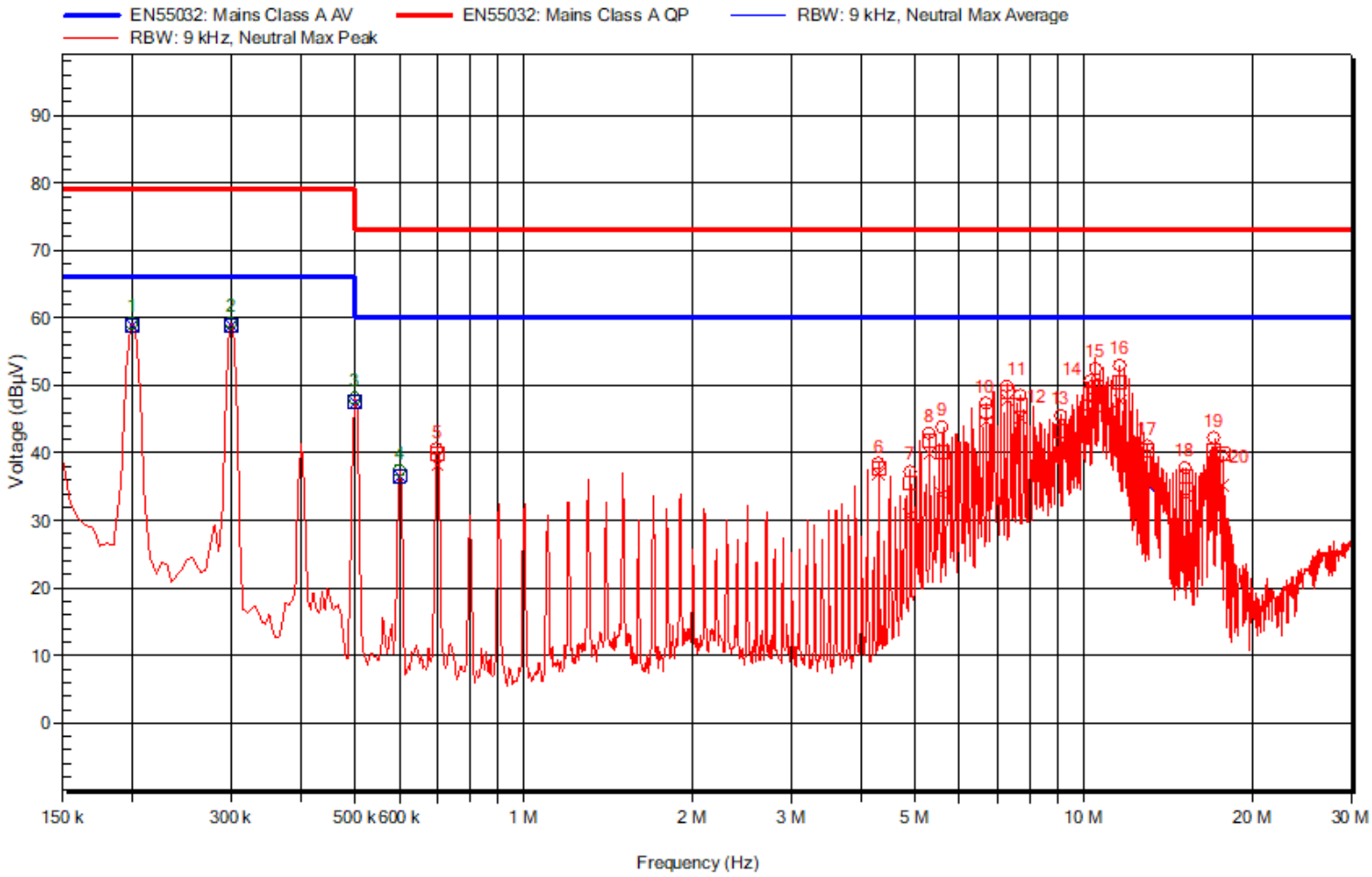


Table 33. **Conducted emissions harmonics measured on neutral**

Frequency	Peak	Peak Correction	Average	Average Limit	Average Difference	Average Correction	Average Status	Quasi-Peak	Quasi-Peak Limit	Quasi-Peak Difference	Quasi-Peak Correction	Quasi-Peak Status
200 kHz	59.2 dBµV	10 dB	58.8 dBµV	66 dBµV	-7.22 dB	10 dB	Pass	58.9 dBµV	79 dBµV	-20.13 dB	10 dB	Pass
300 kHz	59.2 dBµV	10 dB	58.9 dBµV	66 dBµV	-7.08 dB	10 dB	Pass	59 dBµV	79 dBµV	-20.04 dB	10 dB	Pass
500 kHz	48 dBµV	9.8 dB	47.4 dBµV	60 dBµV	-12.58 dB	9.8 dB	Pass	47.6 dBµV	73 dBµV	-25.43 dB	9.8 dB	Pass
600 kHz	37.4 dBµV	9.8 dB	36.5 dBµV	60 dBµV	-23.49 dB	9.8 dB	Pass	36.6 dBµV	73 dBµV	-36.36 dB	9.8 dB	Pass
700 kHz	40.6 dBµV	9.9 dB	38.3 dBµV	60 dBµV	-21.73 dB	9.9 dB	Pass	39.9 dBµV	73 dBµV	-33.14 dB	9.9 dB	Pass
4.3 MHz	38.4 dBµV	10.2 dB	37 dBµV	60 dBµV	-23.04 dB	10.2 dB	Pass	37.7 dBµV	73 dBµV	-35.31 dB	10.2 dB	Pass
4.9 MHz	37.2 dBµV	10.2 dB	30.8 dBµV	60 dBµV	-29.24 dB	10.2 dB	Pass	35.5 dBµV	73 dBµV	-37.53 dB	10.2 dB	Pass
5.3 MHz	42.9 dBµV	10.2 dB	40 dBµV	60 dBµV	-20.04 dB	10.2 dB	Pass	41.9 dBµV	73 dBµV	-31.09 dB	10.2 dB	Pass
5.6 MHz	43.8 dBµV	10.2 dB	34 dBµV	60 dBµV	-26.05 dB	10.2 dB	Pass	40.2 dBµV	73 dBµV	-32.78 dB	10.2 dB	Pass
6.7 MHz	47.3 dBµV	10.3 dB	44.6 dBµV	60 dBµV	-15.38 dB	10.3 dB	Pass	46.2 dBµV	73 dBµV	-26.83 dB	10.3 dB	Pass
7.3 MHz	49.9 dBµV	10.3 dB	47.9 dBµV	60 dBµV	-12.14 dB	10.3 dB	Pass	49.2 dBµV	73 dBµV	-23.84 dB	10.3 dB	Pass
7.7 MHz	48.5 dBµV	10.3 dB	45.1 dBµV	60 dBµV	-14.9 dB	10.3 dB	Pass	47 dBµV	73 dBµV	-25.99 dB	10.3 dB	Pass
9.1 MHz	45.5 dBµV	10.4 dB	39.9 dBµV	60 dBµV	-20.09 dB	10.4 dB	Pass	43.2 dBµV	73 dBµV	-29.83 dB	10.4 dB	Pass
10.301 MHz	50.7 dBµV	10.4 dB	45.6 dBµV	60 dBµV	-14.38 dB	10.4 dB	Pass	48.8 dBµV	73 dBµV	-24.15 dB	10.4 dB	Pass
10.501 MHz	52.5 dBµV	10.4 dB	46.8 dBµV	60 dBµV	-13.24 dB	10.4 dB	Pass	49.7 dBµV	73 dBµV	-23.34 dB	10.4 dB	Pass
11.6 MHz	52.9 dBµV	10.5 dB	47.7 dBµV	60 dBµV	-12.27 dB	10.5 dB	Pass	50.5 dBµV	73 dBµV	-22.5 dB	10.5 dB	Pass
13 MHz	41 dBµV	10.6 dB	35.4 dBµV	60 dBµV	-24.64 dB	10.6 dB	Pass	40.3 dBµV	73 dBµV	-32.68 dB	10.6 dB	Pass

Frequency	Peak	Peak Correction	Average	Average Limit	Average Difference	Average Correction	Average Status	Quasi-Peak	Quasi-Peak Limit	Quasi-Peak Difference	Quasi-Peak Correction	Quasi-Peak Status
15.201 MHz	37.7 dBµV	10.7 dB	33.7 dBµV	60 dBµV	-26.34 dB	10.7 dB	Pass	36.5 dBµV	73 dBµV	-36.55 dB	10.7 dB	Pass
17.101 MHz	42.2 dBµV	10.7 dB	35.1 dBµV	60 dBµV	-24.89 dB	10.7 dB	Pass	40.4 dBµV	73 dBµV	-32.61 dB	10.7 dB	Pass
17.701 MHz	39.6 dBµV	10.6 dB	35.3 dBµV	60 dBµV	-24.7 dB	10.6 dB	Pass	39.8 dBµV	73 dBµV	-33.21 dB	10.6 dB	Pass

13.8 Radiated emissions (EN55032) [pre-comp data]

Figure 98. Radiated emissions set up in 3 m chamber

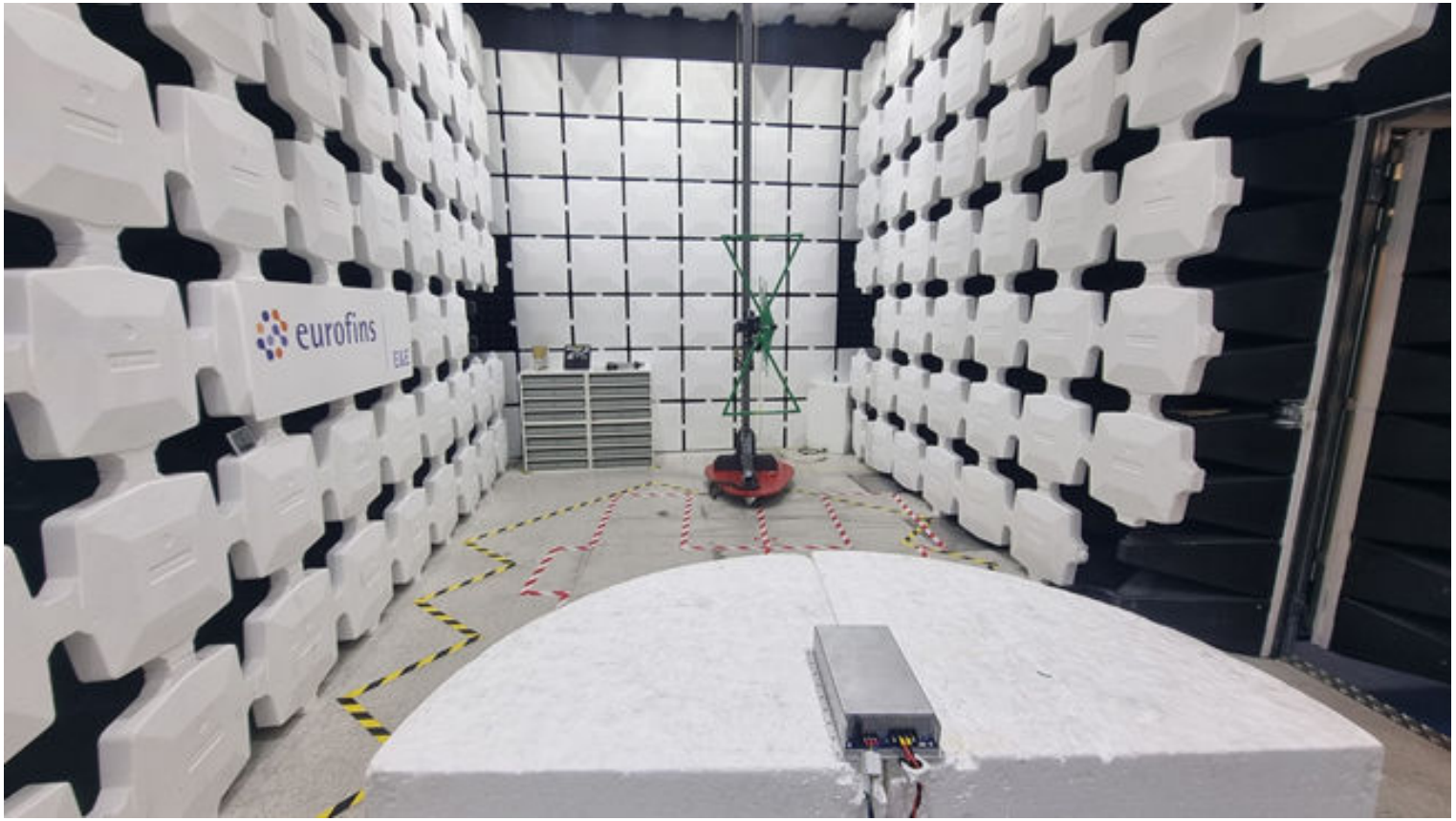


Figure 99. **Radiated emissions set up in 3 m chamber, resistive loads**

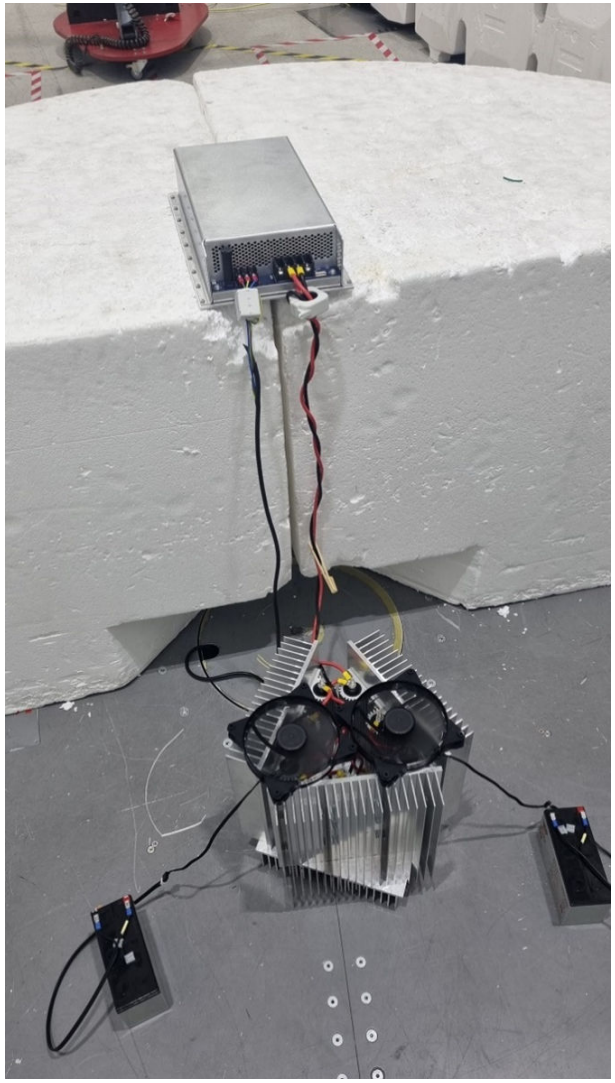


Figure 100. **Radiated emissions results 3 m chamber**

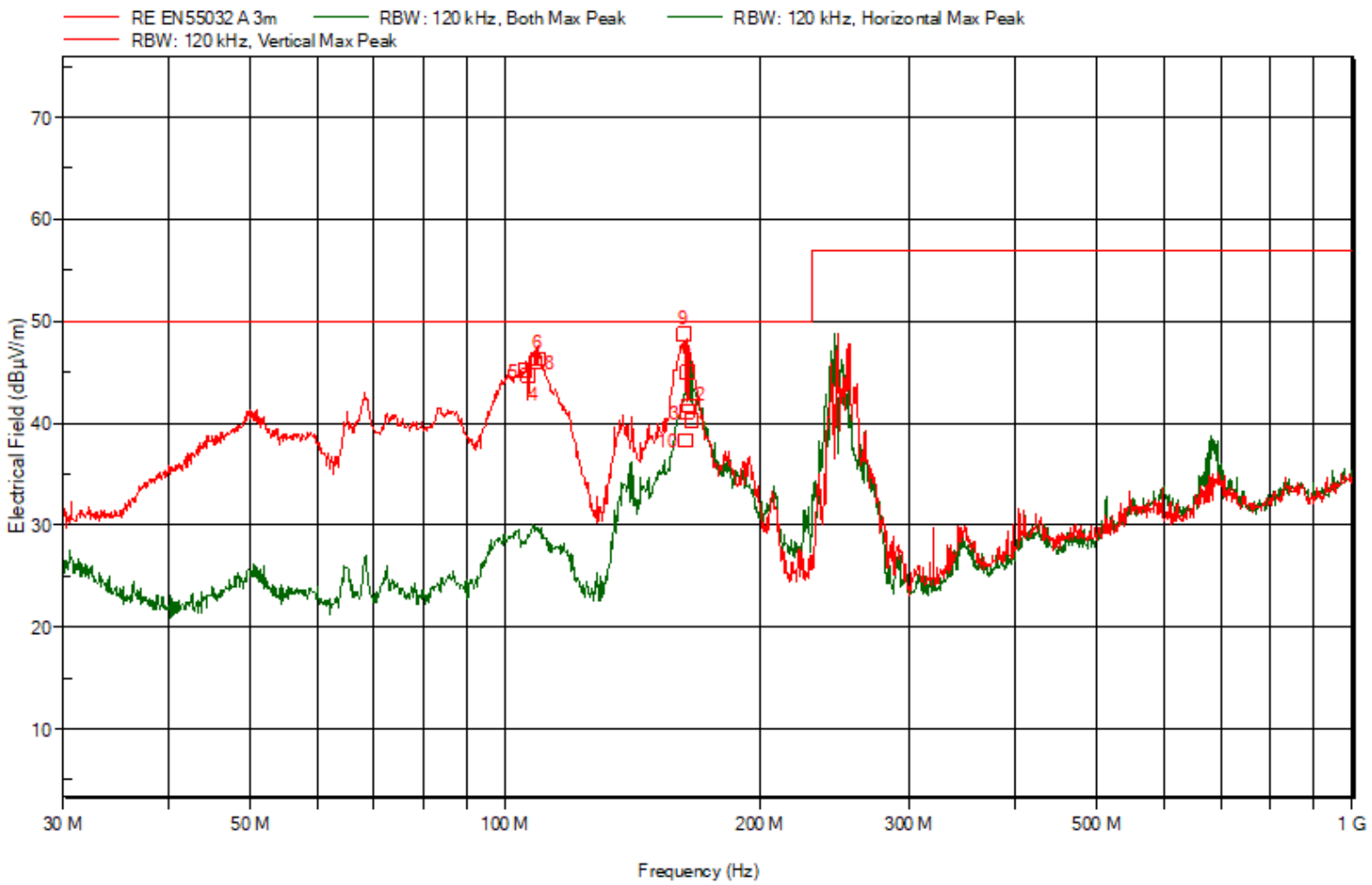


Table 34. **Radiated emissions results in 3 m chamber**

Peak Number	Frequency	Quasi-Peak	Quasi-Peak Limit	Quasi-Peak Difference	Quasi-Peak Correction	Quasi-Peak Status	Status	Angle	Height	Polarization
1	165.72 MHz	40.3 dBµV/m	50 dBµV/m	-9.7 dB	15.7 dB	Pass	Pass	80 degrees	1.7 m	Horizontal
2	165 MHz	41.7 dBµV/m	50 dBµV/m	-8.3 dB	15.7 dB	Pass	Pass	285 degrees	1.6 m	Horizontal
3	163.74 MHz	41.1 dBµV/m	50 dBµV/m	-8.9 dB	15.9 dB	Pass	Pass	280 degrees	1.6 m	Horizontal

Peak Number	Frequency	Quasi-Peak	Quasi-Peak Limit	Quasi-Peak Difference	Quasi-Peak Correction	Quasi-Peak Status	Status	Angle	Height	Polarization
4	106.32 MHz	44.7 dBµV/m	50 dBµV/m	-5.3 dB	17.5 dB	Pass	Pass	270 degrees	1 m	Vertical
5	105.54 MHz	45.2 dBµV/m	50 dBµV/m	-4.8 dB	17.4 dB	Pass	Pass	265 degrees	1 m	Vertical
6	109.14 MHz	46.3 dBµV/m	50 dBµV/m	-3.7 dB	17.9 dB	Pass	Pass	220 degrees	1 m	Vertical
7	164.16 MHz	45.0 dBµV/m	50 dBµV/m	-5.0 dB	15.8 dB	Pass	Pass	180 degrees	1 m	Vertical
8	108.54 MHz	45.9 dBµV/m	50 dBµV/m	-4.1 dB	17.8 dB	Pass	Pass	225 degrees	1 m	Vertical
9	162.42 MHz	48.7 dBµV/m	50 dBµV/m	-1.3 dB	15.9 dB	Pass	Pass	149 degrees	1 m	Vertical
10	163.38 MHz	38.3 dBµV/m	50 dBµV/m	-11.7 dB	15.9 dB	Pass	Pass	360 degrees	1 m	Vertical

14 Summary

This application note has detailed the design and operation of the digitally controlled 2kW AC-DC PSU, focusing on the PFC stage of the PSU. The closed loop control has been implemented using the STM32G474 MCU from STMicroelectronics.

Implementation of a digital voltage feed-forward filter, digital voltage loop and digital current loop allows the PFC stage to achieve a high power factor with low input current harmonics across a wide load range. The software tool Biricha ST-PLD was used to obtain the controller coefficients for these controllers, available for free from: www.biricha.com/st-pld

Furthermore, the efficiency of the PFC stage is improved by the use of phase shedding - turning off one phase at light loads. The state of the PFC converter is also communicated to the secondary side via an isolated communication interface which allows the downstream DCDC converter to start up and shut down based on the state of the PFC bus.

There are several webinars that have been created to accompany this application note. Please visit: www.biricha.com/st to access the webinars related to this EVM.

Biricha Digital Power also runs regular hands-on training workshops for STM32 MCU that cover the principles of power supply design, the fundamentals of control theory, the transition to the discrete-time domain and step-by-step embedded programming. These workshops are beneficial to both analog power supply design engineers who need to get familiar with digital power and embedded systems engineers who need to understand how to design and stabilize digital power supplies.

For more information on these workshops please visit: www.biricha.com/st

15 Regulatory compliance information

Notice for US Federal Communication Commission (FCC)

For evaluation only; not FCC approved for resale

FCC NOTICE - This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter 3.1.2.

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For evaluation purposes only. This kit generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to Industry Canada (IC) rules.

À des fins d'évaluation uniquement. Ce kit génère, utilise et peut émettre de l'énergie radiofréquence et n'a pas été testé pour sa conformité aux limites des appareils informatiques conformément aux règles d'Industrie Canada (IC).

16 Custom evaluation boards information

Notice: *This/these evaluation board(s) is/are custom designed and built according to specific requests from the user (You), and is/are destined for evaluation and testing of ST products in a research and development setting.*

By using or installing (as applicable) this evaluation kit, you accept all the terms of the EVALUATION BOARD TERMS OF USE available at: www.st.com/epla.

17 References

Biricha. (2020). Biricha Digital Power Workshops. *Digital Power Supply Design Using STM32*.

18 Appendix

18.1 Download Links

- STEVAL-ISA172V3 schematic and PCB design files: STEVAL-ISA172V3
- Workshops and training: www.biricha.com/st
- Project, ST-PLD, Bode Analyzer Suite downloads: www.biricha.com/steval-isa172v3

Revision history

Table 35. **Document revision history**

Date	Version	Changes
11-Sep-2026	1	Initial release.

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