How to implement an NFC coil multiplexer for multi-antenna switching

Introduction

NFC technology is becoming increasingly popular for products in consumer electronics, moving away from its strict use as a card reader.

This document applies to the NFC transceivers indicated in Table 1. It describes the basic solution of the switching sequence when the device operates with more than one antenna, the physical effects and signals, and a complete solution in form of a prototype.

Table 1. Applicable products

Type	Product RPNs
ST25 NFC readers	ST25R200, ST25R3916, ST25R3918, ST25R3916B, ST25R3917B, ST25R500

1 Acronyms

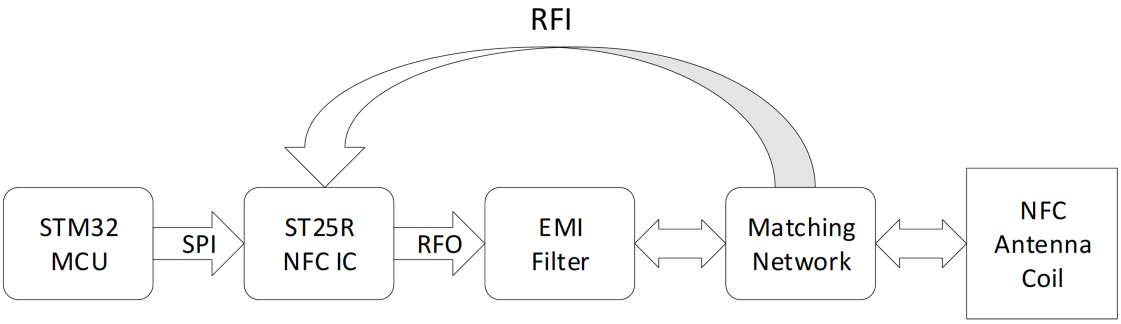
Table 2. List of acronyms

Acronym	Definition
NFC	Near field communication
WLC	Wireless charging
Q - factor	Quality factor
EMI	Electromagnetic interference
HW	Hardware
SW	Software
PA	Power amplifier
GUI	Graphical user interface
IC	Integrated circuit
MCU	Main controlling unit
NMOS	N-doped silicon metal oxid semiconductor
VNA	Vector network analyzer
ID	Identity

2 Current working status

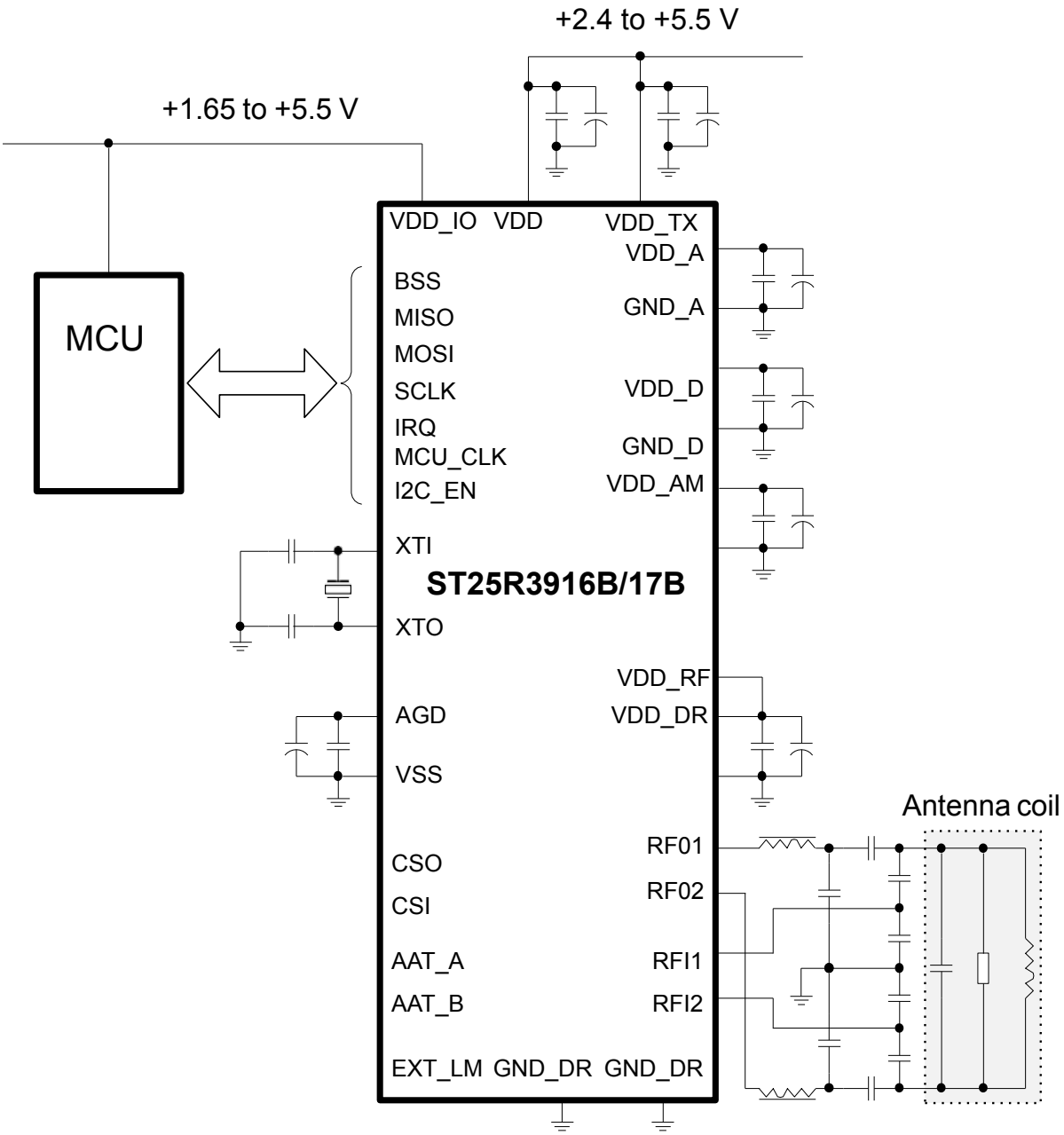
An NFC network includes a coil and a matching network, as shown in Figure 1. The matching impedance is adapted to the antenna form factor.

Figure 1. Block diagram of an NFC reader



The RFO pins of the ST25R3916B are differential square signals with a frequency of 13.56 MHz. This means that the maximum amplitude of the signal is equal to the supply voltage, which is 5 V. The minimum is the ground potential (0 V).

Figure 2. **System diagram (single antenna driving)**

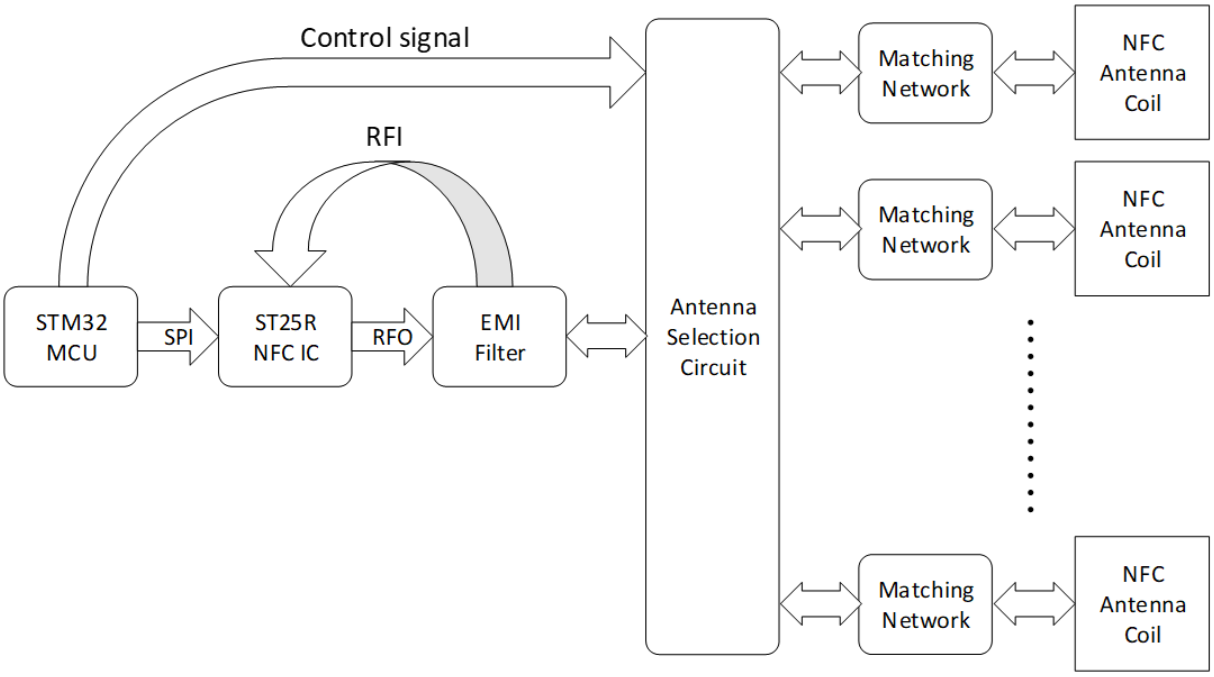


If a second antenna is connected to the same network on the RFO output pins, the system does not work because it is not possible to match two different antennas to one output. The antennas must be separated.

3 Solution with more antennas

As shown in Figure 3, each antenna is individually tuned, hence it can be individually designed. The switch selects the antennas, allowing the user to choose between different NFC coils.

Figure 3. Block diagram of an NFC reader with multiplexed antennas



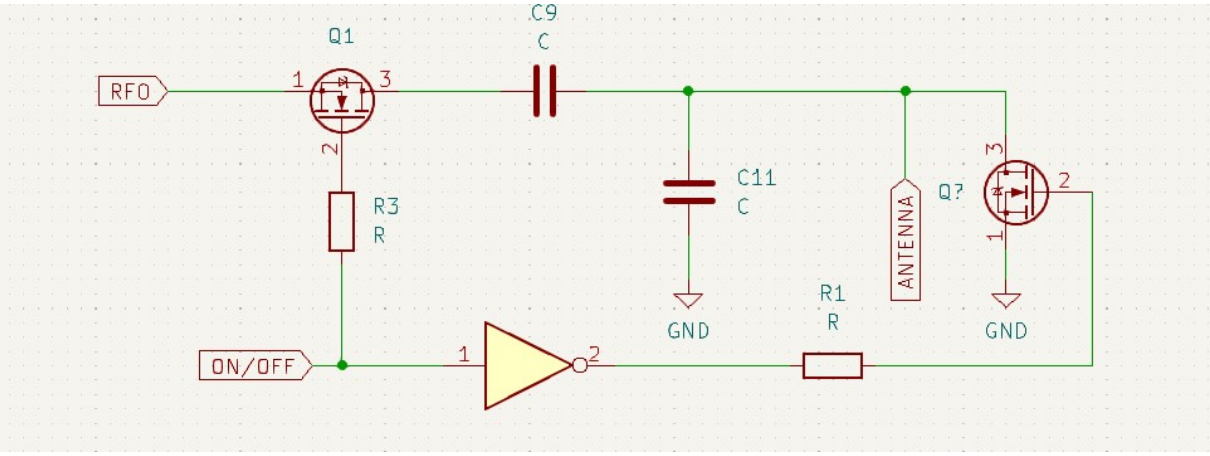
The selection must be made from a separate multiplexing IC or from the GPIO pins of the MCU controller. The number of available GPIO pins must be at least equal to the number of antennas used.

4 The basic solution of the switching sequence

In a system with more than one antenna, an NMOS switching transistor creates a separation circuit. This means that each antenna has its own matching network.

In Figure 4, a serial NMOS switch (Q1) disconnects the matching network and the antenna from the RFO terminals of the chip. The NMOS transistor has a parasitic capacitance, which leads to a parasitic current in the matching network. For this reason, a second NMOS transistor is connected in parallel to the antenna. This pulls down the floating open side of the matching network. In this case, no parasitic current in the coil can cause a field that would read tags on this antenna.

Figure 4. Switching block of one antenna in the multiplexer

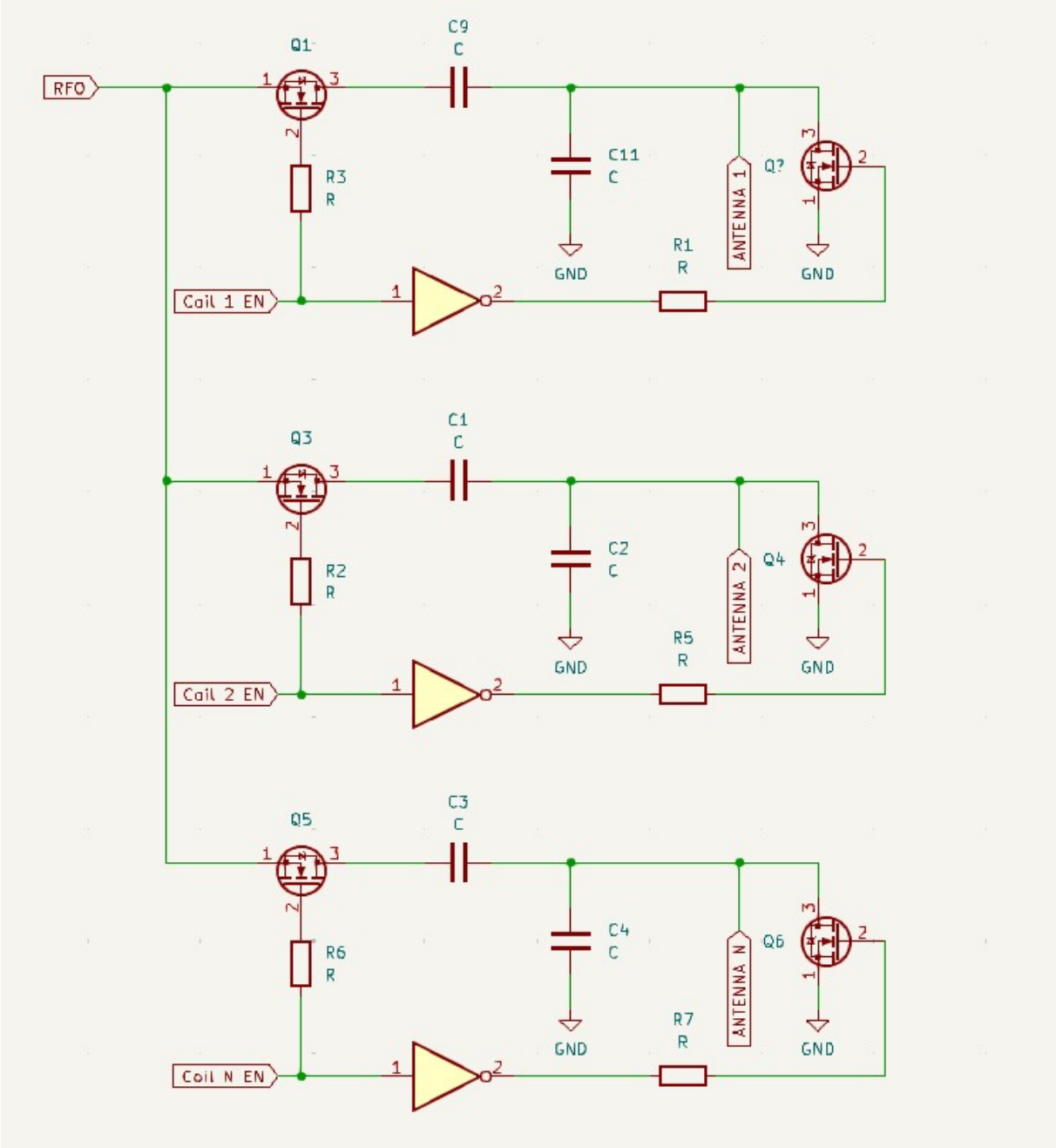


If the voltage at the NMOS gate is equal to or lower than the voltage at the source, the transistor is turned off and does not conduct current through the RFO path to the coil. This is the case when the gate of the NMOS transistor is pulled to GND.

To turn on the transistor, the gate voltage must be raised above the RFO voltage plus the threshold voltage of the transistor. In this case 12 V is high enough to drive the transistor into saturation. Now, the NMOS transistor is turned on and drives the RFO path to the coil.

The antenna is ON.

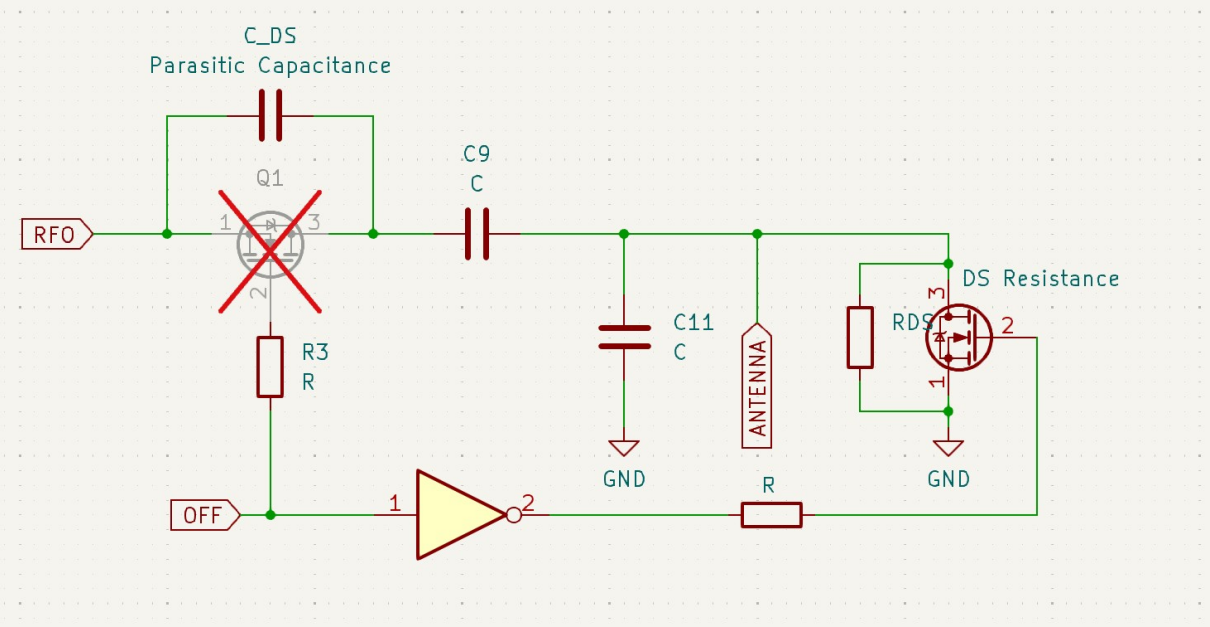
Figure 5. **Schematic of a multiplexer in single ended mode**



5 Impedance grounding during off state

When the antenna is not in use, the RFO switches have a small parasitic capacitance, which causes crosstalk. To suppress this effect, it is necessary to pull down the RFO pins to GND. This is possible using additional NMOS transistors, connected in parallel with the parallel matching capacitors.

Figure 6. Parasitic components

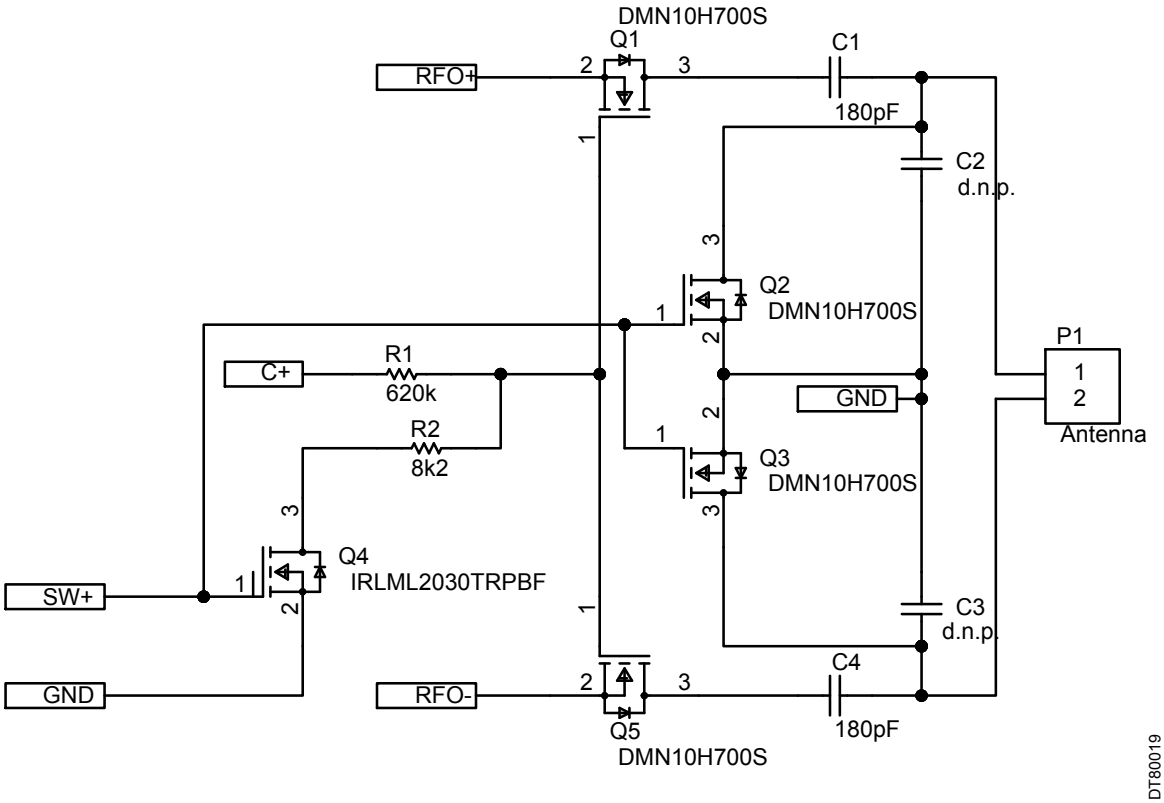


6 Schematics

Each antenna has a basic element, assembled in the complete system.

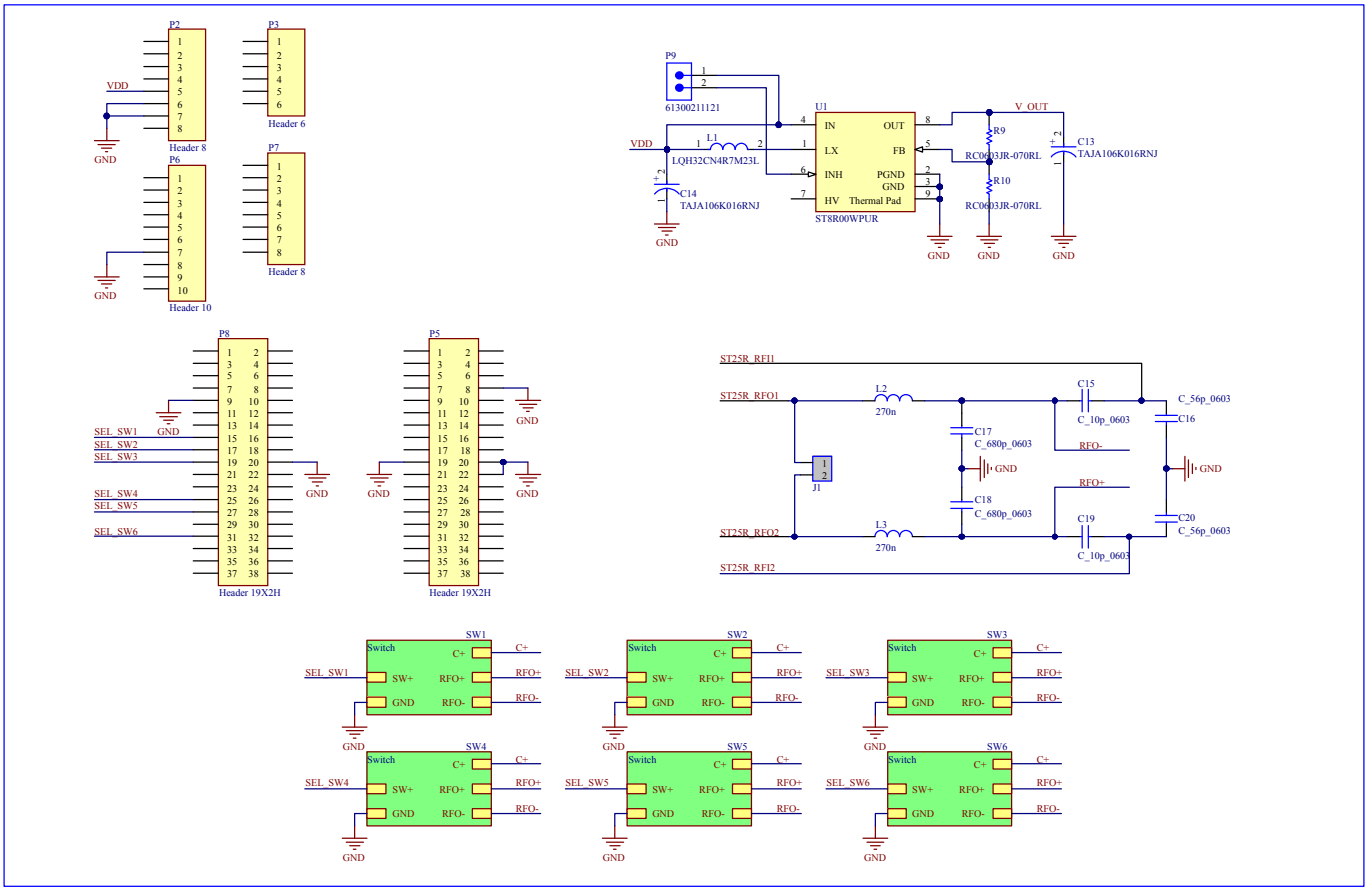
All antennas use the same switching element, whose schematic is shown in Figure 7. It comprises the RFO switching MOSFETs (Q1 and Q5), the grounding MOSFETs (Q2 and Q3), and one controlling MOSFET for the RFO switches (Q4). The ratio and value of R1 and R2 are chosen in a way that Q4 can pull the gate of Q1 and Q5 to ground. If Q4 is high ohmic the gate of Q1 and Q5 should reach the high level of the net C+. Thus their value also depend on the used transistor.

Figure 7. Single switching module



- Source from external boost converter
  An external boost converter (in this case the ST8R00W device) is used to control the gate voltage of the RFO MOSFET. This is useful if more than four antennas are used, as in Figure 8. The cascade supply also loads the RFO ports of the ST25R3916B device, causing losses.

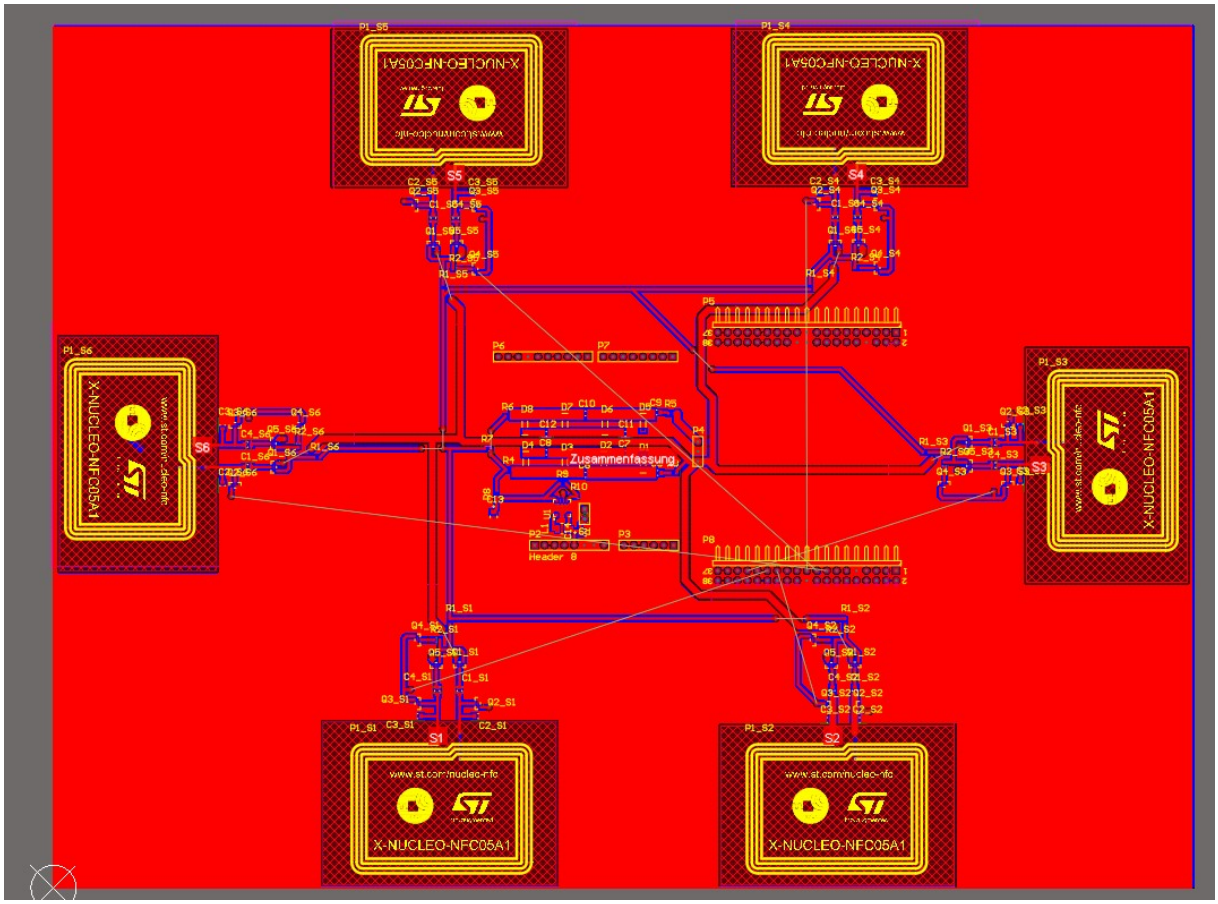
Figure 8. **6-antenna multiplexer**



6.1 PCB design

The prototype is based on a copper PCB (30 cm x 23 cm), milled on an LPKF CNC milling machine.

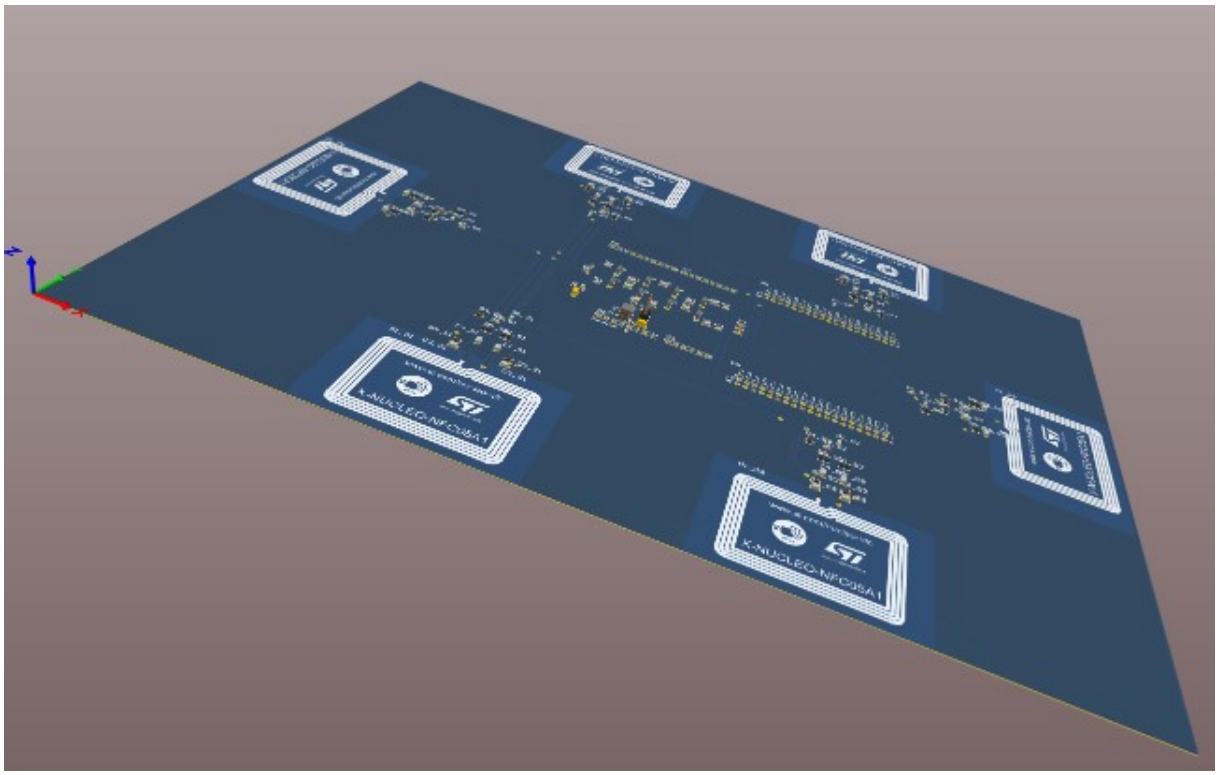
Figure 9. PCB design for a 6-antenna multiplexer



The board is double-sided, with pure copper islands connected to the ground plane to reduce emissions and parasitics. The EMI filter has been modified on the NFC05 demonstration board. This board is connected to the antenna matrix board together with a Nucleo L476 board to control the antenna switching.

In Figure 10, the headers of the Nucleo switching board are on the right, and the NFC05 board are on the left. The boards are placed on the antenna board from below.

Figure 10. 3D view of the board



Viewed from below, the Nucleo board is on the left and the NFC05 is on the right. The red twisted cable is used to connect the VNA to the RFO pins and capture the Smith chart of the individual antennas.

Figure 11. PCB bottom view

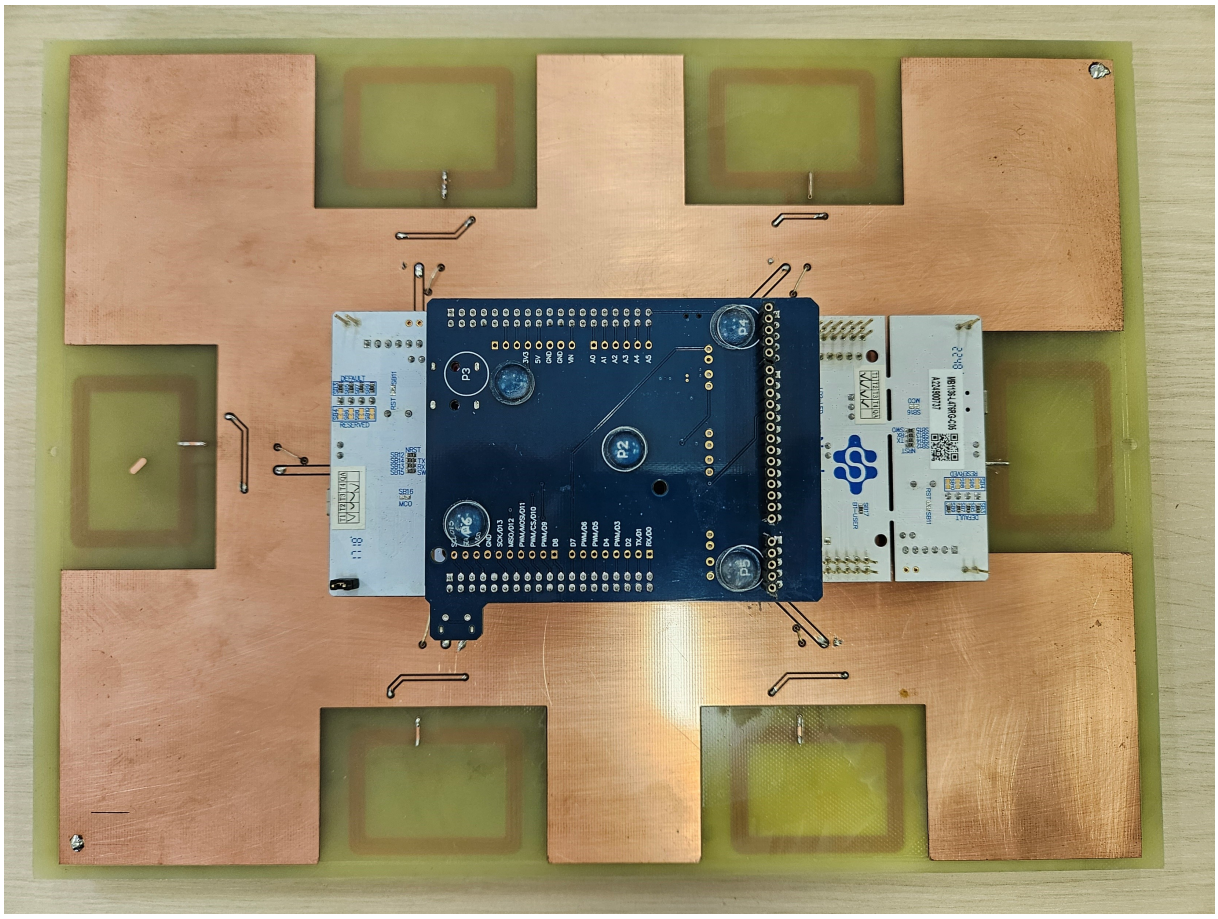
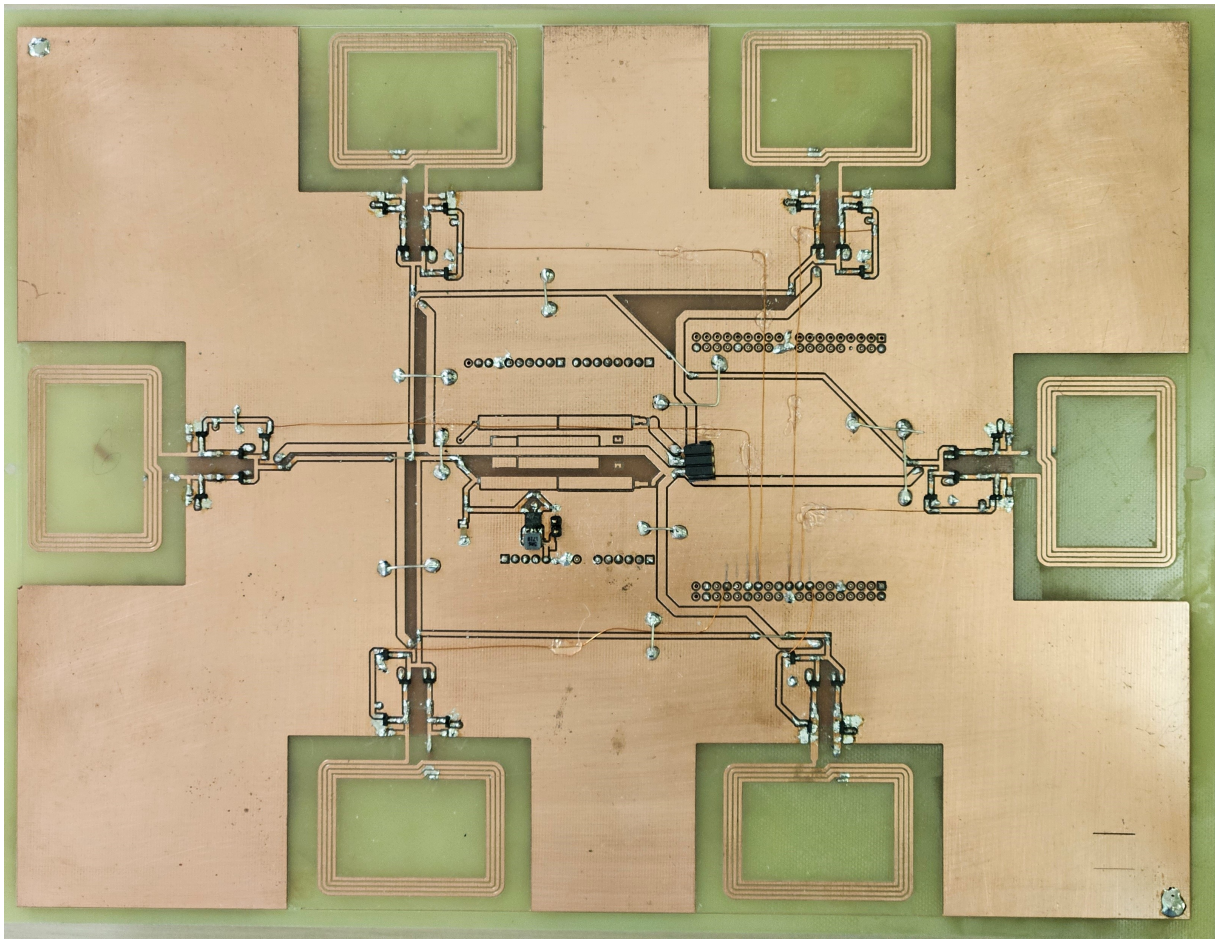


Figure 12. **Top view of the machined PCB**

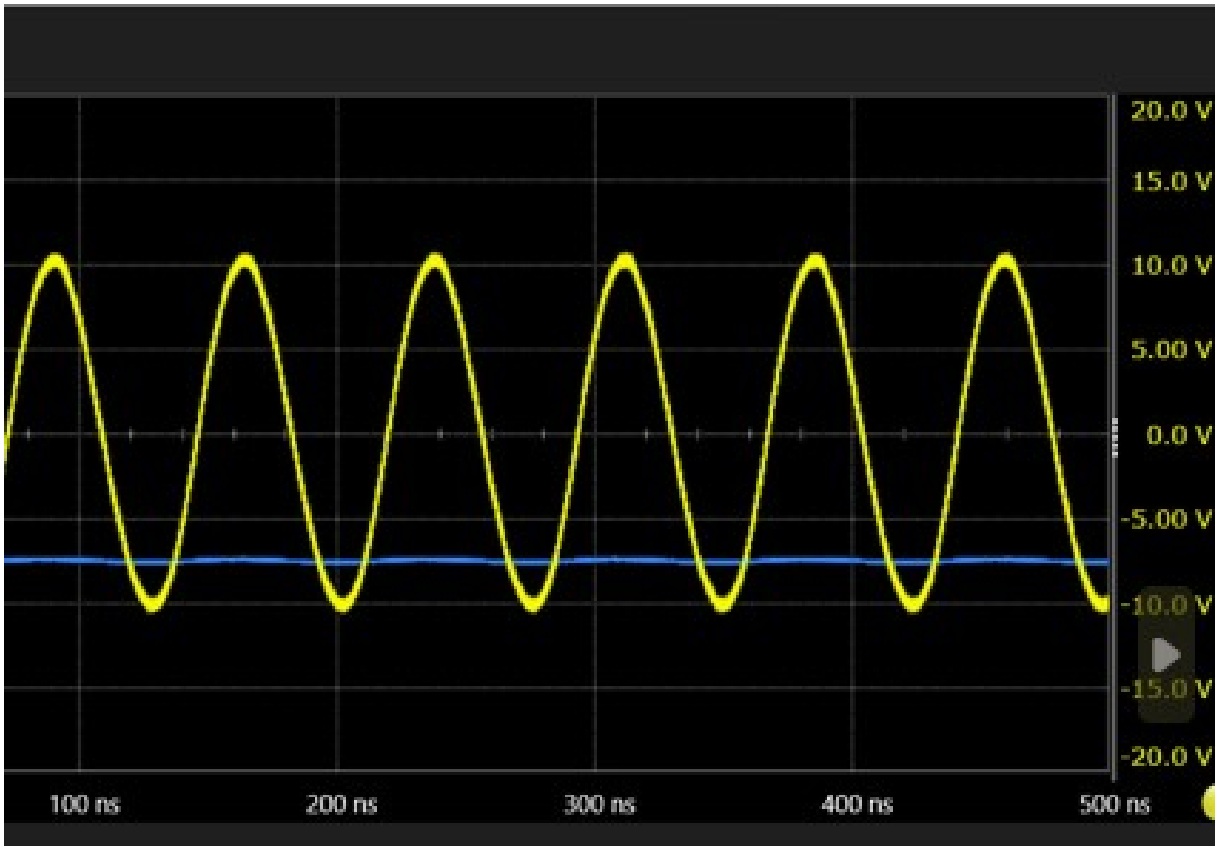


7 Tests

7.1 Signal quality

The 13.56 MHz main signal is measured differentially at the output ports after the matching network. The antenna is unloaded for this measurement.

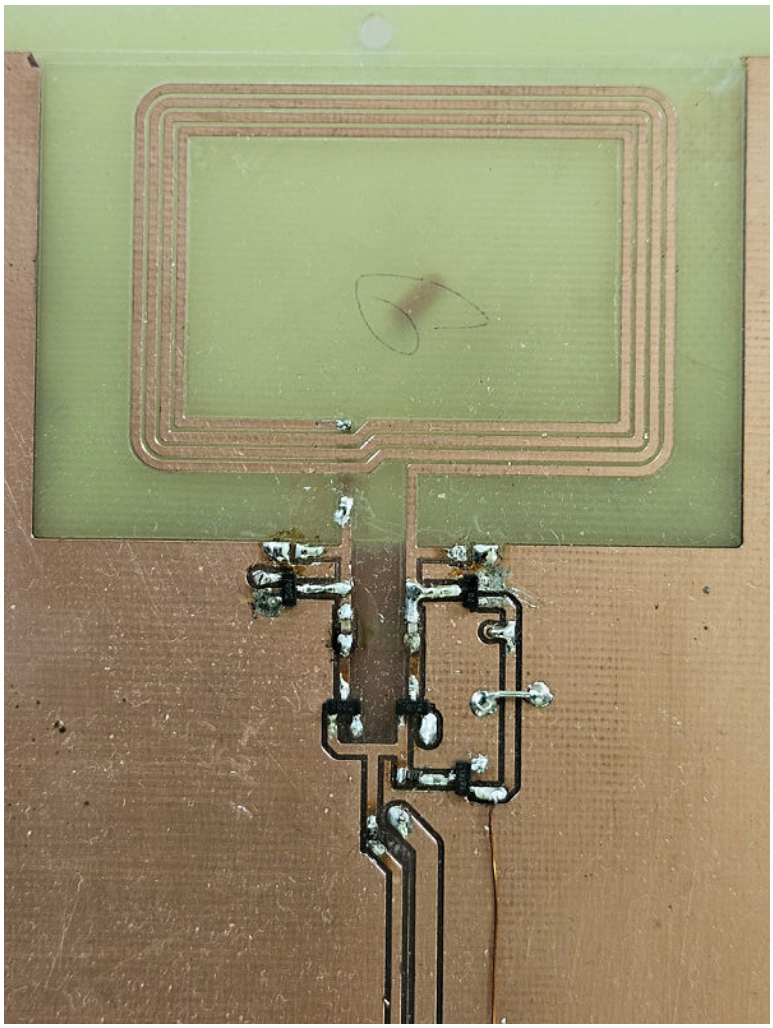
Figure 13. Continuous polling signal



7.2 Antenna matching

As shown in Figure 14, each antenna has its switching system close to the ports. This matching network is located directly on these ports. Each antenna should show approximately the same matching behavior under these conditions, which can be proved with the VNA. The path between the switching, matching network, and EMI filter should be equalized as much as possible.

Figure 14. Antenna with the switching block



DT79229V1

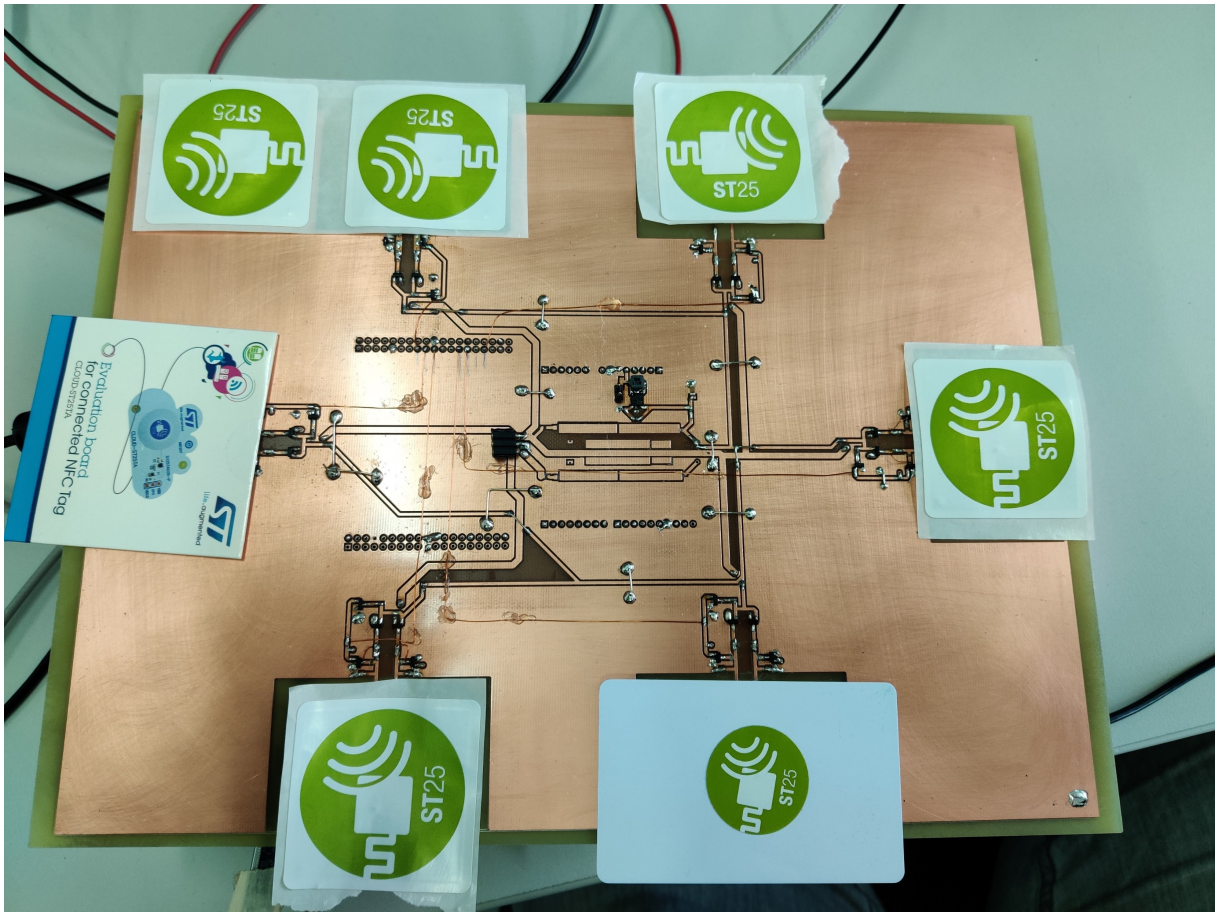
The parasitics of the capacitor manufacturer's accuracy of 5% causes a few Hz deviation.

7.3 Card reading

A card reading test is performed to verify that each antenna switch works.

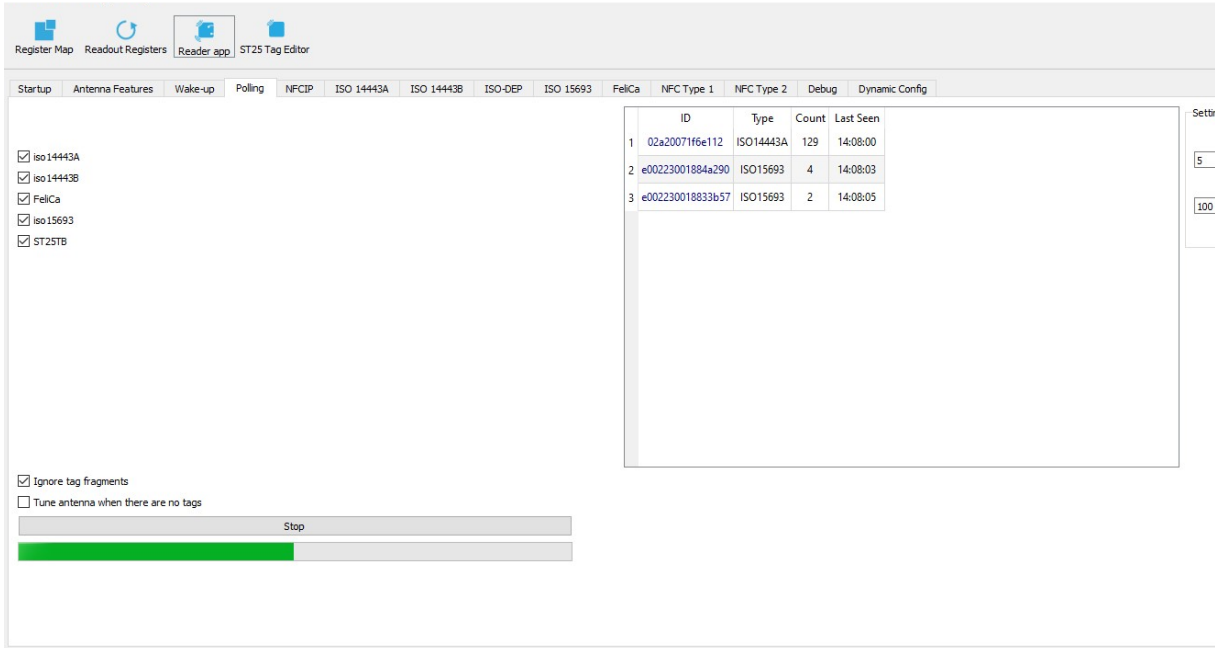
An NFC tag with a unique ID is placed on each antenna. Pressing the 'next' button on the Nucleo control panel turns off the active antenna and turns on the next antenna in the sequence.

Figure 15. **Setup for the sequential card reading test**



As shown in Figure 16, the GUI shows that the chip reads each card on the currently selected antenna.

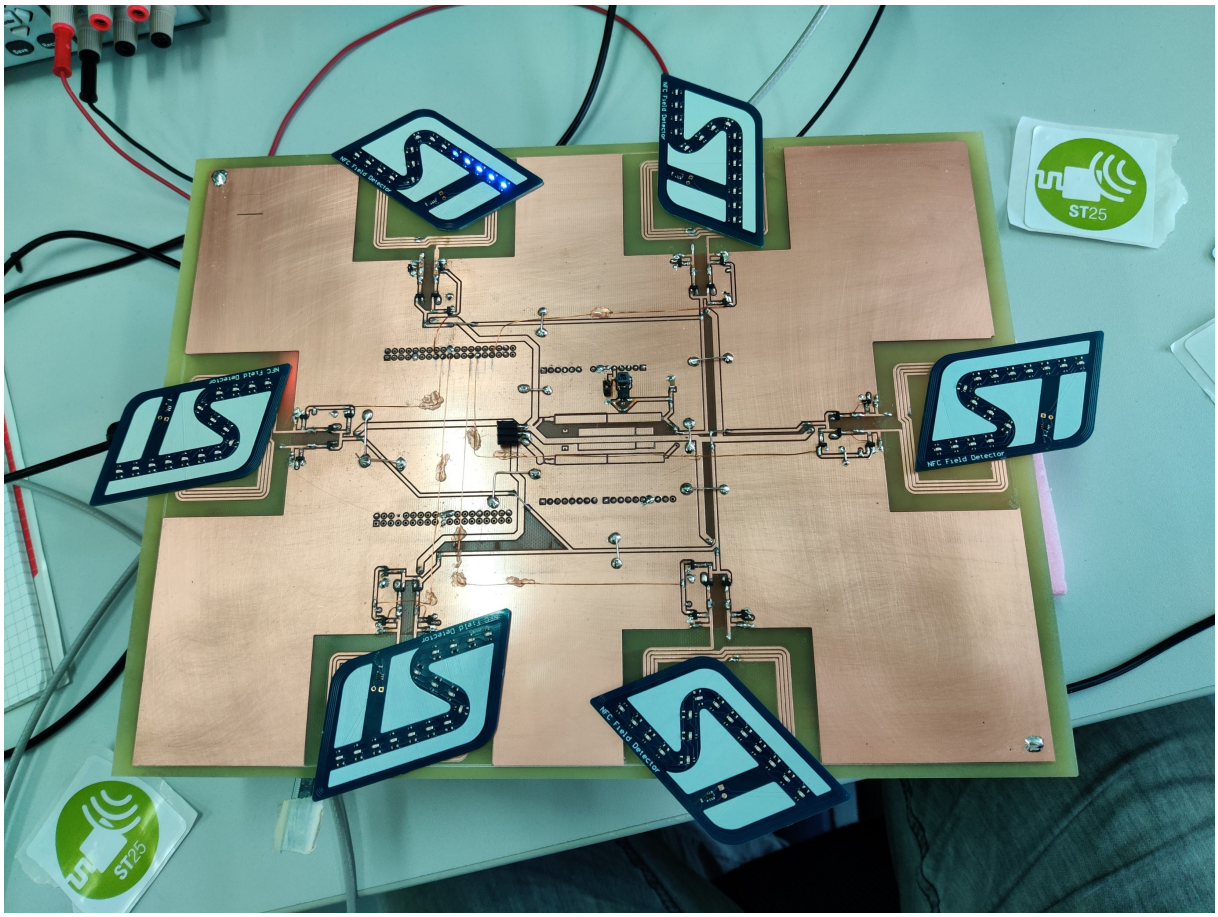
Figure 16. **Reading cards on discovery graphical user interface**



When reading, the system waits four seconds before moving to the next card. No crosstalk is visible. The card reads are recognized at the button press.

Pressing the enable button activates only the selected antenna. Figure 17 shows part of the polling sequence. The field detector is illuminated. All other detectors remain dark.

Figure 17. Lights on indicate the active module



8 Conclusion

This document has demonstrated the possibility of driving several antennas using applicable devices. Refer to Table 1.

The system is built with six antennas as a proof of concept, but it is possible to drive up to 84 antennas, depending on their dimensions.

This expands the possibilities for NFC applications in parallelized systems such as game boards, shelf-sorting tables or general sorting boards.

Revision history

Table 3. **Document revision history**

Date	Version	Changes
19-Sep-2025	1	Initial release.
03-Nov-2025	2	Updated: • Section 6: Schematics

Contents

List of tables

List of figures