life.augmented

AN6128

Application note

The STPMIC25 PCB layout guidelines

Introduction

This application note aims to provide some information about how to place the STPMIC25 on a 4-layer PCB (2s2p std JEDEC board JESD51-7), paying attention to the routing tracks and the switching part with a high current path.

Therefore, the correct PCB routing and component placement are key factors in a highly integrated power management, and the following topics must be considered:

- High frequency switching currents due to the intrinsic behavior of inductor-based DC-DC conversion
- Signal integrity of the digital interface
- Thermal management of dissipated power

This document shares some tips regarding the layout rules to follow to make the STPMIC25 evaluation board (the order code of the kit is "STEVAL-PMIC25V1", which includes the STPMIC25 evaluation board "STEVAL-PMIC25M1" and the I²C USB interface "STEVAL-USBDNGV1".

1 Power section layout considerations

A PCB layout that follows the tips in this document is key for the design of switching power supply, due to high switching currents and sensitive control signals in the surrounding area. Increased power losses, output ripple, EMI emissions, and the possibility of inaccurate regulation are direct consequences of an improper layout of the power section of any DC-DC converter. Less common effects are induced noise on digital lines, loop instability, and audible acoustic noise from passive components. In rare cases, stray inductance of long traces may cause abnormal voltage spikes which, in turn, may stress the STPMIC25 above its maximum voltage ratings (AMR). In the following sections, the root causes of the critical current paths and some recommendations about how to limit their effects on the STPMIC25 performance are provided.

1.1 General recommendations

- Always consider and determine where and how the return currents flow.
- As in all switching DC-DC converter configurations, the minimum length of critical traces is a key factor as well as the use of ground and power planes.
- Reduce the use of vias along the critical current paths.
- Route analog signals in the analog section of the board only.
- Do not route analog signals (voltage feedback signals) over ground plane gaps.
- In the case that a ground or power plane must be split (for mechanical and or electrical reasons), do not place any trace across the gap on an adjacent layer.
- Never underestimate the importance of decoupling capacitors. Decoupling is the process of placing a capacitor as close as possible to the STPMIC25 to provide the transient switching current. In a DC-DC converter, it is the process of placing an L-C network near the STPMIC25 to minimize the trace inductances causing overvoltage spikes. If the spikes exceed the value of AMR, the device may be damaged.
- A high-capacity value of the decoupling capacitors is important for low-frequency decoupling effectiveness, but it is less important at high frequencies, where the most important rule is to reduce the stray inductance in series with the decoupling capacitors.
- All passive components should be placed as close as possible to the STPMIC25 pins, but when this device packs many regulators into a small area, this can be difficult. A criterion for the passive components placement is to manage their distance from the STPMIC25 by following these priorities, the highest being the shortest distance:
  - Input capacitors of each buck converter
  - Input capacitors for each LDO and device power supply (VIN, INTLDO, etc.)
  - Inductors for each DC-DC converter
  - Output capacitors of each buck converter
  - Output capacitors for each LDO regulator
- Grouping and orientation of capacitors should be carried out so that the input capacitor and output capacitor of each DC-DC have their ground side very close to each other.
- The positive side of the output capacitor must be placed as close as possible to the inductor, and from its connection point. The voltage feedback trace should start towards the V_{OUT} pin.

1.2 Buck converter critical current paths

Figure 1 and Figure 2 show the simplified schematic of a buck converter. The green/orange lines show the critical paths of switching currents during the inductor charging/discharging phases.

Figure 1. Buck converter schematic (charging phase)

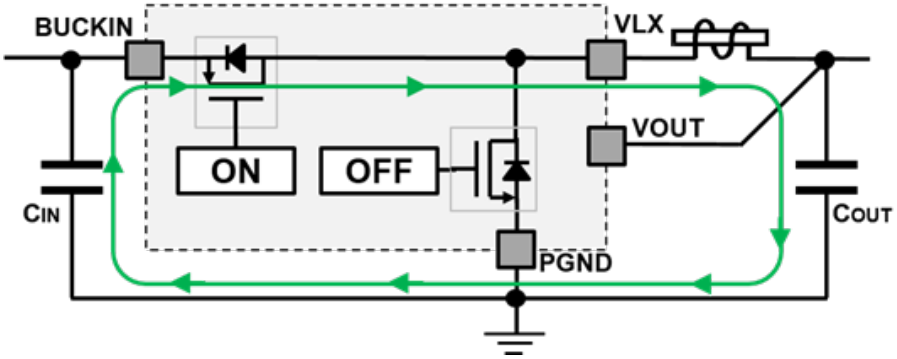
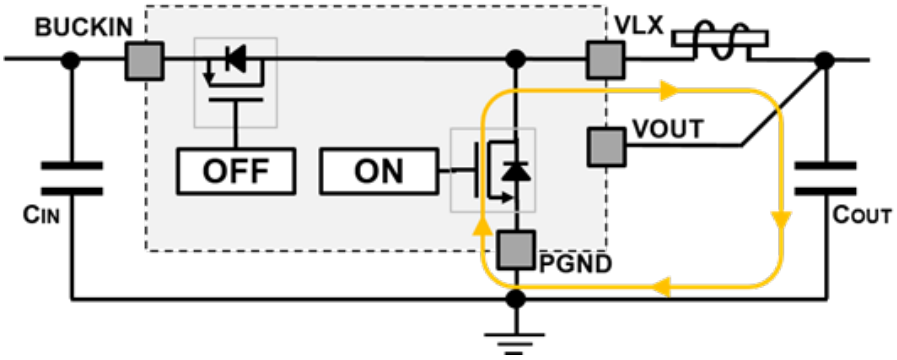


Figure 2. Buck converter schematic (discharging phase)



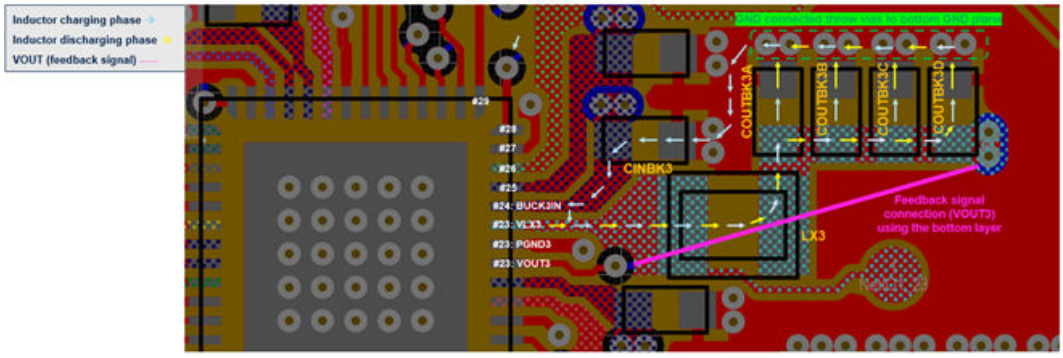
The capacitors and inductors should be placed as close as possible to the STPMIC25 device and routed with both wide and short traces. The input capacitor is the most critical component to be placed in the PCB layout. It must be placed as close as possible to the BUCKIN pin and the related PGND pin, to minimize GND loop. If properly routed, the input capacitor cuts the high voltage spikes produced by the switching activity of the device.

The output capacitor should be placed close to the inductor. It is recommended to connect at a single common point or immediately connect to the ground plane using the appropriate number of vias:

- The ground side of the output capacitor
- The ground side of the input capacitor
- The PGND pin of the device

The output voltage feedback signal should be picked exactly on the output capacitor and routed to the V_{OUT} pin (feedback signal), avoiding noisy nets. To minimize noise pick-up, its trace should be tiny, placed away from any switching trace, and it is better if routed in a separate layer, shielded from switching lines by the ground plane as shown in Figure 3 where the track for the feedback signal is in the bottom layer (purple trace).

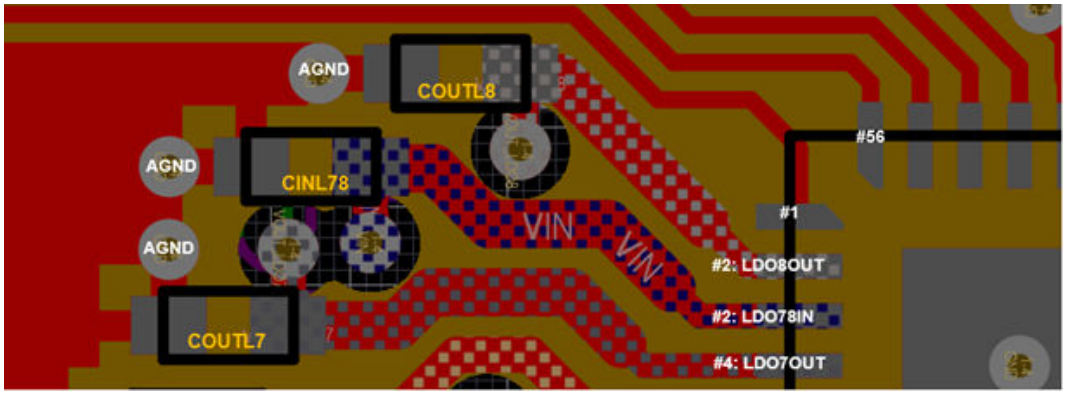
Figure 3. **Buck3 reference routing with critical paths**



1.3 LDOs

LDOs are not solely affected by the switching noise activity, but since they are physically very close to the active buck converters, the injected noise can be a problem. For this reason, each LDO supply should be filtered by a decoupling capacitor placed as close as possible to the input pin of the related LDO. Besides, to assure the best performance, the output capacitor should be placed close to the LDO output, possibly with its ground side far from any switching ground return, to avoid any noise injection.

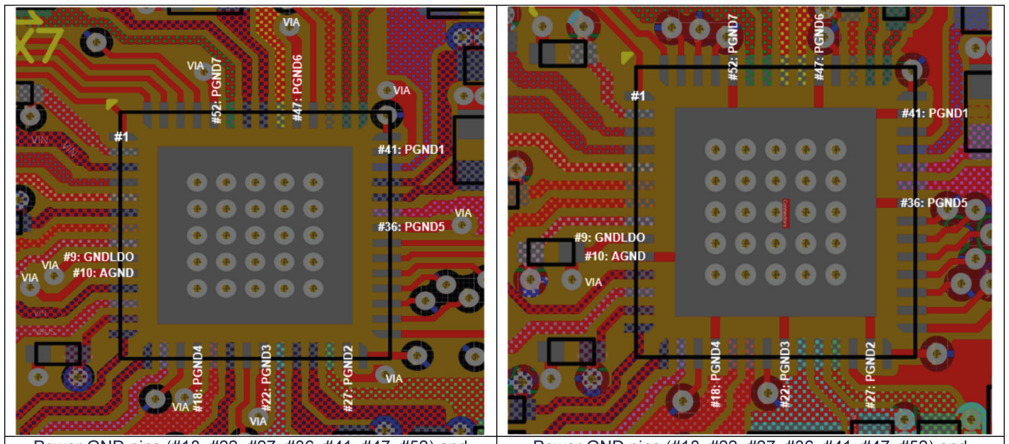
Figure 4. **LDO reference routing**



1.4 Connection between exposed pad and GND pins

Two different layouts, which have been tested, demonstrate the way how the exposed pad is connected to the power GND pins and AGND pin, as shown in the Figure 5:

Figure 5. Connection between exposed pad and power/analog GND pins: direct connections vs. VIA connections



Power GND pins (#18, #22, #27, #36, #41, #47, #52) and AGND pin (#10) connected to the exposed pad through vias in internal layer

Power GND pins (#18, #22, #27, #36, #41, #47, #52) and AGND pin (#10) connected to the exposed pad through direct tracks in the top layer.

Both layouts were tested at bench level with no significant difference in terms of dynamic performance of the buck converters, such as load and line transient measurements. So, at the end, the first approach was followed in the evaluation board layout of STPMIC25, and vias were used to connect the power GND and analog GND pins to the GND exposed pad.

1.5 Thermal considerations

The package of the STPMIC25 is a WFQFN 56L 6.5 x 6.5 x 0.9 mm with an exposed pad (ePad), which helps the thermal power dissipation of the device. In the PCB, a group of about a dozen thermal vias carry the heat away from the IC. It is strongly suggested that a minimum of 9 via holes (ground-fill) be put underneath the ePad of the device, since the PCB acts as a heat-sink by mainly using the ground plane for improved thermal power dissipation.

The exposed pad solder area can be segmented into a symmetric pad array, by applying the solder paste to approximately 50% to 75% of the area of the exposed pad.

Figure 6, Figure 7, Figure 8 and Figure 9 show the STPMIC25 package bottom, side, and top views and the recommended footprint outline.

Figure 6. **STPMIC25 package bottom view**

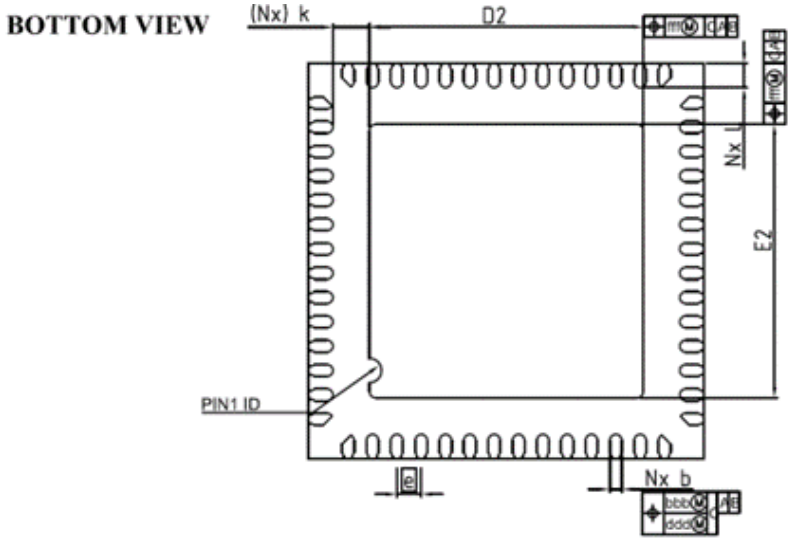


Figure 7. **STPMIC25 package side view**

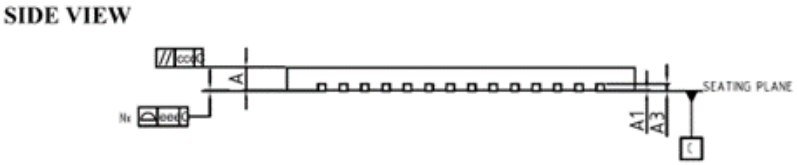


Figure 8. **STPMIC25 package top view**

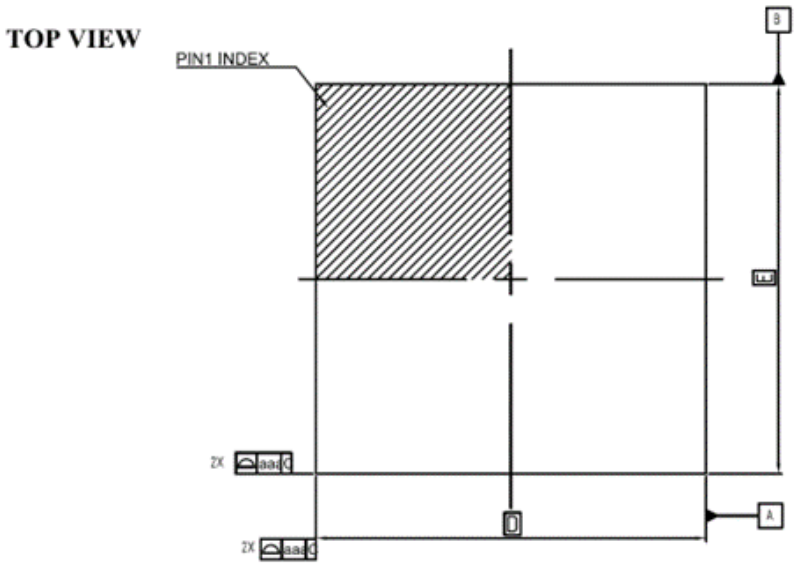


Figure 9. **STPMIC25 recommended footprint outline**

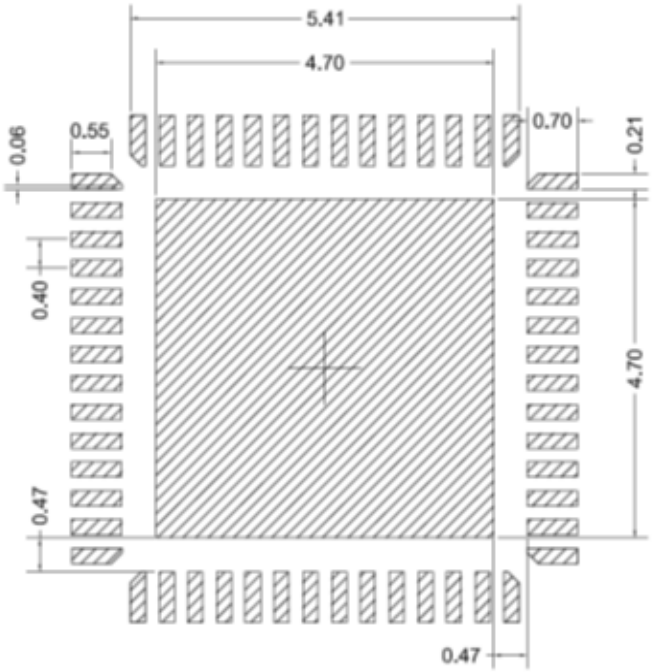
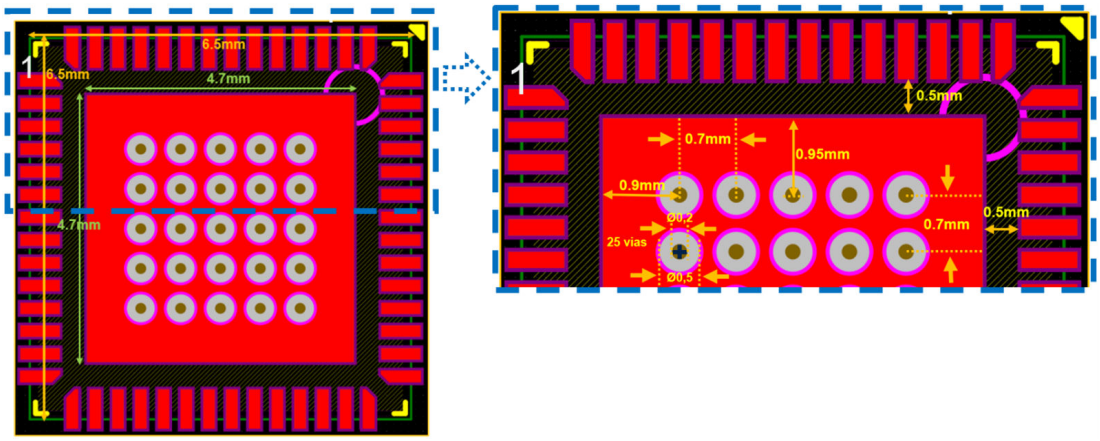


Figure 10 instead shows the footprint that was used in the STPMIC25 evaluation board for the QFN package 6.5 x 6.5 x 0.9 mm and the arrangement of the thermal pads over the exposed pad.

Figure 10. **Exposed pad and vias placement on the top layer of the STPMIC25 evaluation board layout**



As shown in Figure 10, ST suggests surrounding each pad with a 0.06 mm wide solder mask to prevent solder bridging.

For the thermal pads, a symmetric matrix of 5x5 vias was designed. It is strongly suggested that a minimum of 9 via holes (ground-fill) be put underneath the exposed ePad of the device, since the PCB acts as a heat-sink by mainly using the ground plane for the improved thermal power dissipation.

ST recommends placing thermal vias in the solder mask defined thermal pad to effectively transfer the heat from the top copper layer of the PCB to the inner or bottom copper layers. The recommended via external diameter is 0.5 mm or less, the internal hole diameter is 0.2 mm, and the recommended via spacing is 0.7 mm along the x and y axes.

2 Digital interface layout considerations

To avoid noise injection on the digital signals by the switching activity of the DC-DC converters, it is good practice to shield the digital traces by ground planes placed on adjacent layers. Other suggestions are to:

- Partition mixed-signal PCBs with separate analog and digital sections.
- Route digital signals only in the digital section of the board (I²C BUS).
- In the case that ground or power planes must be split for a specific reason (for mechanical and/or electrical causes), do not place any traces across the gap on an adjacent layer.
- The digital decoupling capacitor for the VIO pin should be connected directly to the digital ground if the VIO pin is supplied far from the STPMIC25.

3 PCB example: the STPMIC25 evaluation board layout

The STEVAL$PMIC25M1 evaluation board is based on a 4-layer PCB, 2s2p, to be compliant with the JEDEC JESD51-2 standard.

Figure 11 shows the PCB stack-up layer that was used for the STPMIC25 evaluation board.

Figure 11. STEVAL$PMIC25M1 evaluation board: PCB stack-up layers

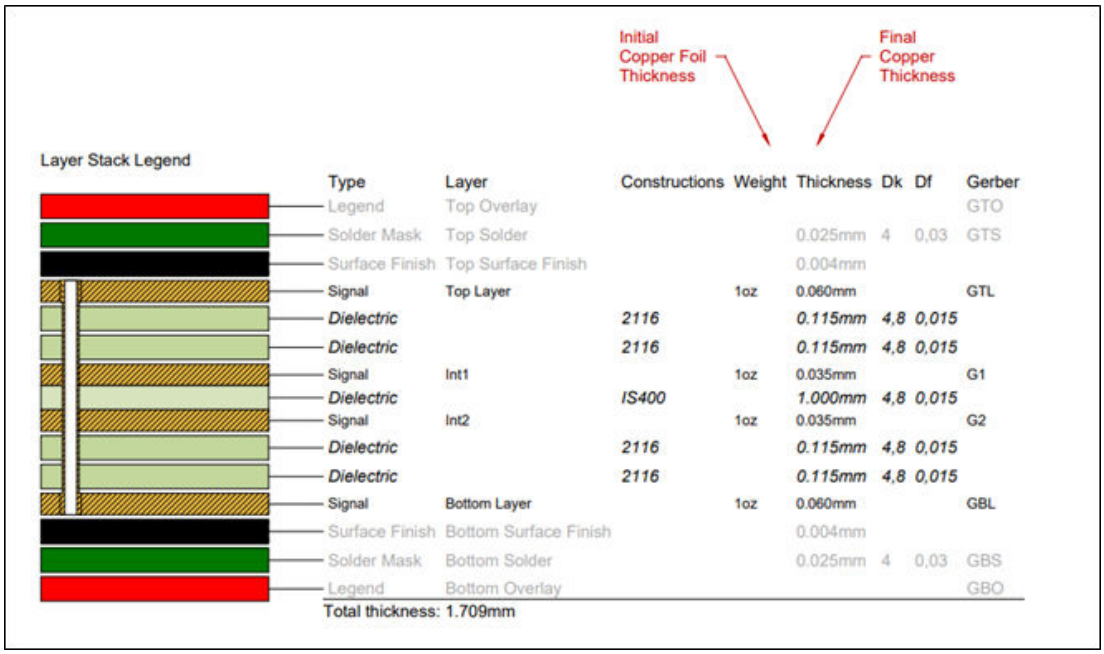


Table 1. STEVAL$PMIC25M1 evaluation board: stack-up layer details

Layer	Stack-up
Top	Component/power/signal
Mid signal 1	GND
Mid signal 2	Power/GND
Bottom	Power/GND

The following pictures show the board layout of the STPMIC25 evaluation board. All the guidelines described in the previous sections were applied to the drawing of the board to secure the STPMIC25 device's best performance.

Figure 12. **STEVAL$PMIC25M1 evaluation board: 3D layout**

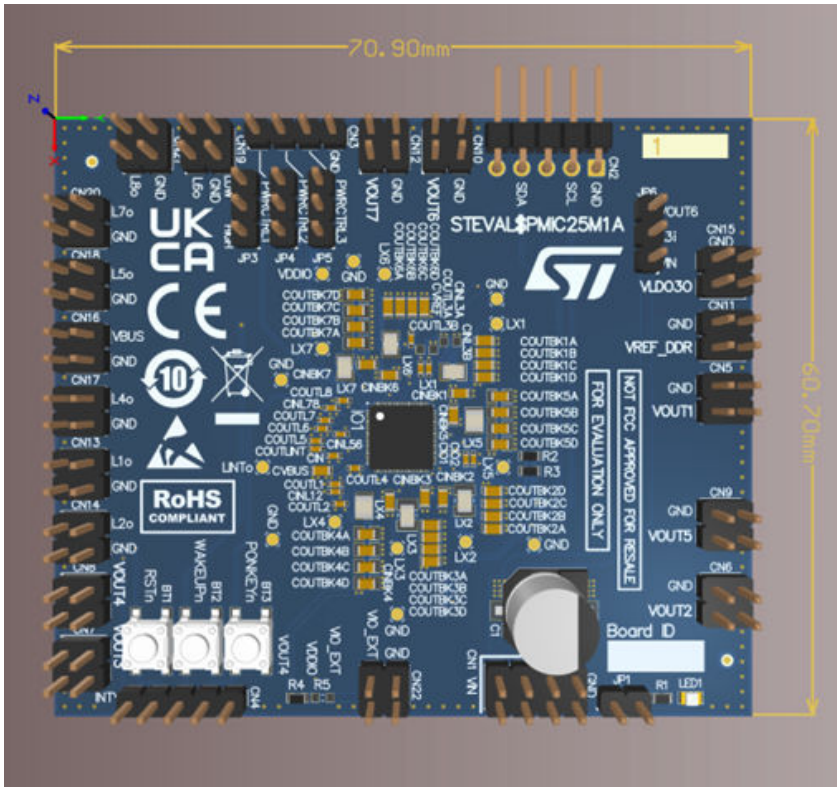


Figure 13. **STEVAL$PMIC25M1 evaluation board: top layer (components/power/signal)**

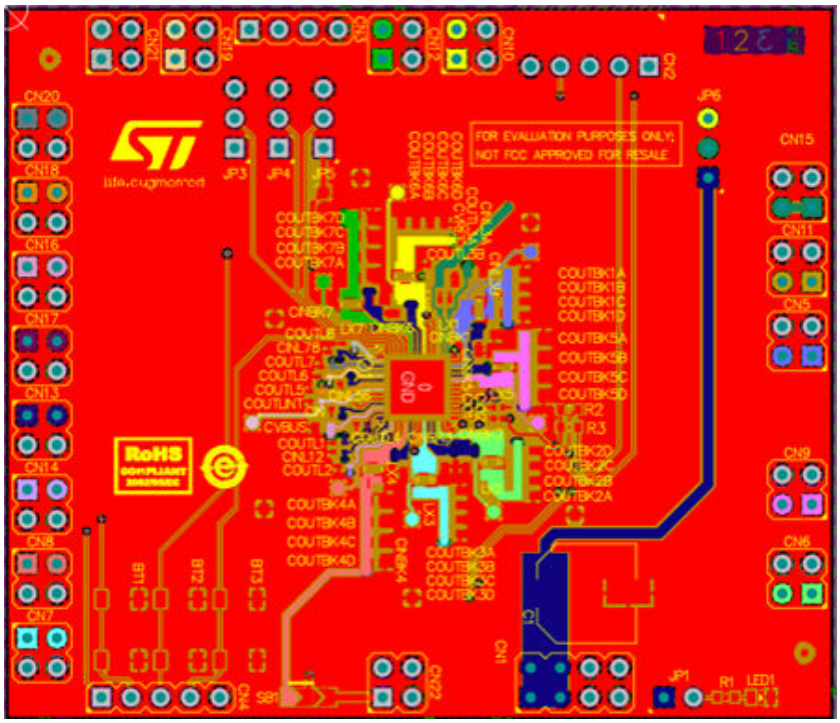


Figure 14. **STEVAL$PMIC25M1 evaluation board: mid layer 1 (GND)**

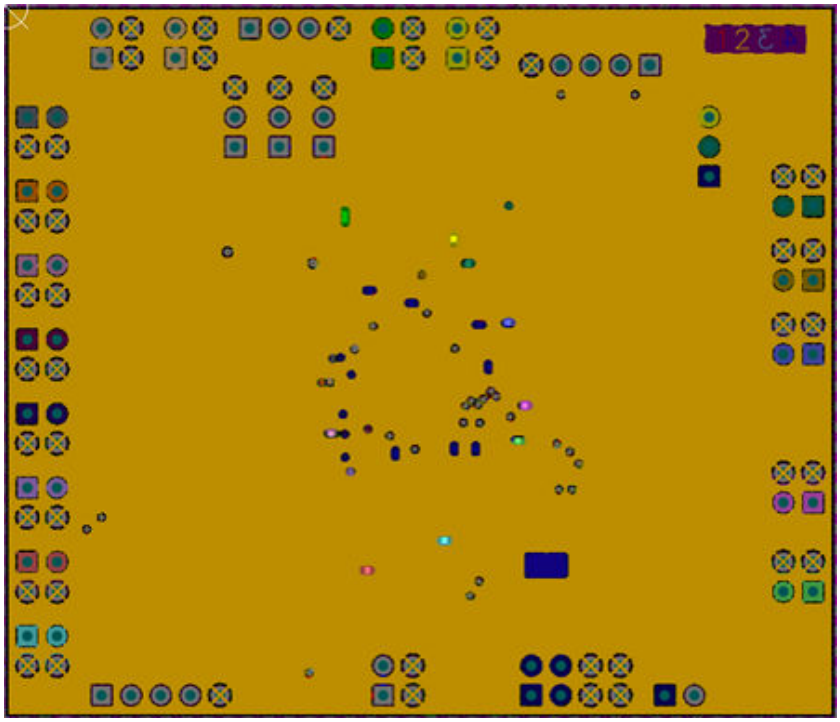


Figure 15. **STEVAL$PMIC25M1 evaluation board: mid layer 2 (power/GND)**

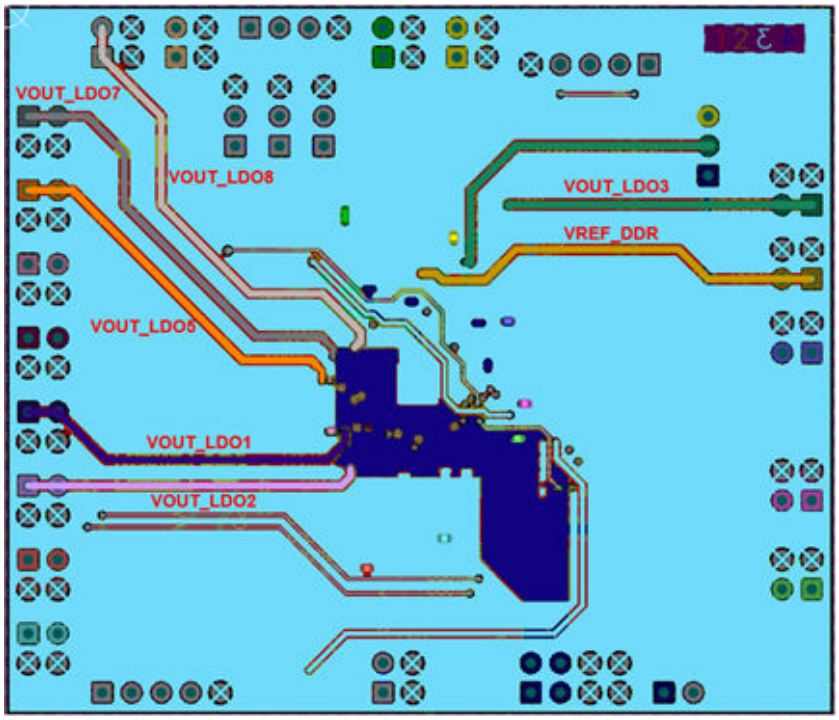
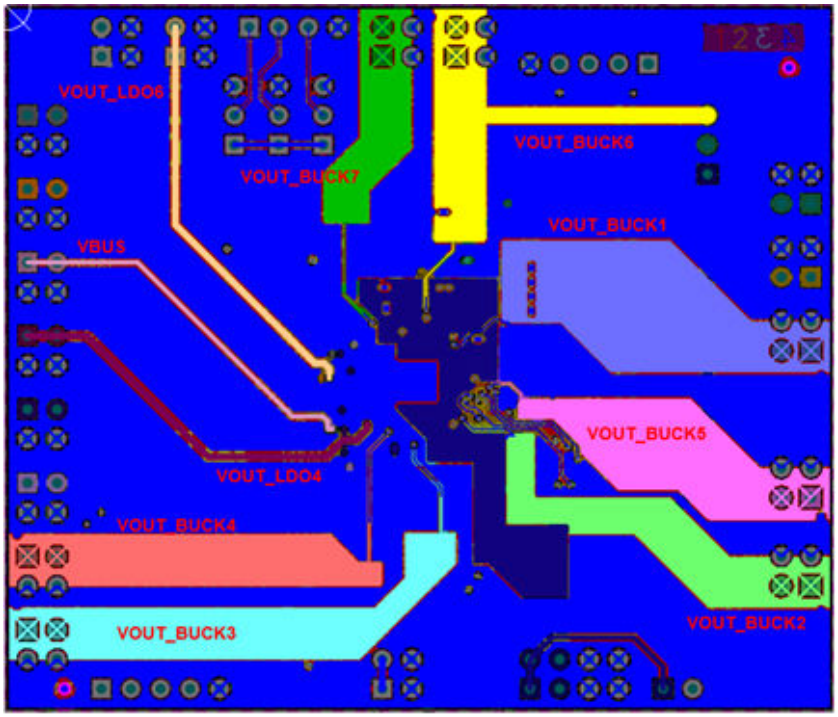


Figure 16. **STEVAL$PMIC25M1 evaluation board: bottom layer (power/GND)**

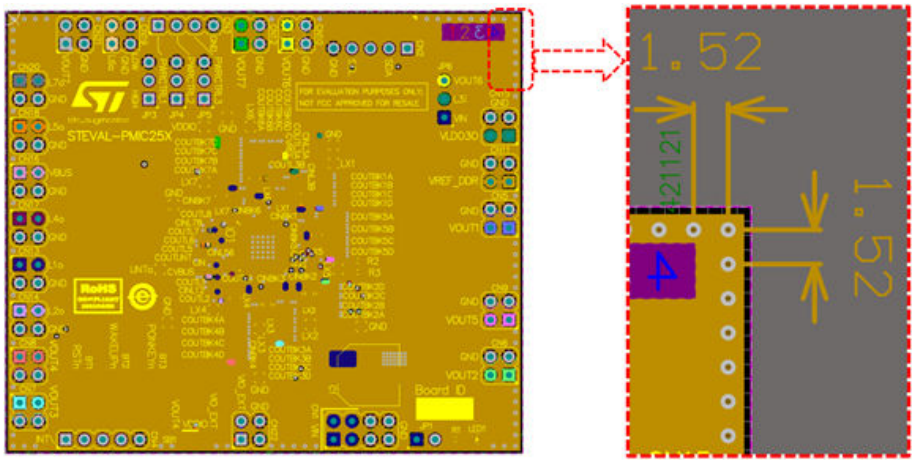


3.1 Power and ground planes

Since both POWER and GROUND are planes, inductive effects are minimized, providing a very low impedance path to the STPMIC25. The use of a continuous ground layer with multiple via holes is a good method to achieve low impedance ground returns. However, to keep low impedance over all areas of the PCB, the continuous ground layer should never be narrowed or partitioned.

Figure 17 shows the mid layer 1 of the STPMIC25 evaluation board layout, with the detail on GND vias placed all around the PCB edge with 2 mm spacing

Figure 17. **Mid layer 1 (GND plane)**



The usage of flat and large shapes, whether possible, is recommended for all high current power supplies such as V_{IN}, V_{OUT}, and V_{BUS}. This helps to reduce the power losses. When examining the ground and power planes, make sure that the plane continuity is not affected by too many vias.

Examples of power planes, vias placement, and plane shapes are shown in Figure 15 (mid-layer 2), in which they are used to route V_{IN} and all V_{OUT} of the regulators out to connector headers.

3.2 Via holes

Though the ground plane is a good ground reference, the presence of the vias along ground returns introduces some stray inductances at high frequency. Placing multiple via holes in a plane reduces this effect considering that the stray inductances are in parallel. Those via holes must be spaced in such a way that the power plane is not excessively cut up.

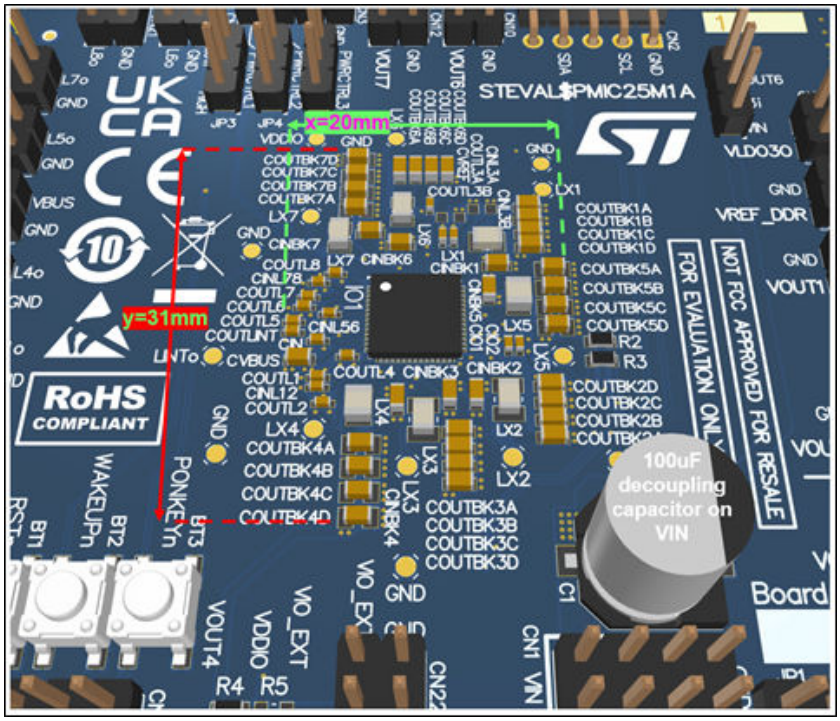
Table 2. Via size

Via type	Hole size	Pad size
Via holes	0.2 mm	0.5 mm

3.3 Passive components placement around STPMIC25 in the evaluation board

Figure 18 shows the STPMIC25 passive components arrangement (input and capacitors, output coils, and resistors) around the STPMIC25 in the evaluation board. The aim was to shrink all the BOM into the smallest area around the STPMIC25 device (20 x 31 mm).

Figure 18. STEVAL$PMIC25M1 evaluation board: bottom layer (power/GND)



All the suggestions described in this application note have been followed in the STPMIC25 evaluation board.

Moreover, it is good practice to put all passive components on top of the layout and to use the bottom side only if it is really needed by the application/board size.

A decoupling capacitor of 100 µF was placed on the input supply rail for two reasons:

- In case there is an input voltage drop, it provides adequate power to the STPMIC25 to maintain the voltage level.
- In case there is a voltage surge, it prevents the excess current from flowing through the STPMIC25 to keep the voltage stable.

Revision history

Table 3. **Document revision history**

Date	Version	Changes
11-June-2024	1	Initial release.

Contents

1 **Power section layout considerations** 2
1.1 General recommendations 2
1.2 Buck converter critical current paths 3
1.3 LDOs 4
1.4 Connection between exposed pad and GND pins 5
1.5 Thermal considerations 5
2 **Digital interface layout considerations** 8
3 **PCB example: the STPMIC25 evaluation board layout** 9
3.1 Power and ground planes 12
3.2 Via holes 13
3.3 Passive components placement around STPMIC25 in the evaluation board 13
Revision history 14

List of figures

Figure 1. Buck converter schematic (charging phase) . . . 3
Figure 2. Buck converter schematic (discharging phase) . . . 3
Figure 3. Buck3 reference routing with critical paths . . . 4
Figure 4. LDO reference routing . . . 4
Figure 5. Connection between exposed pad and power/analog GND pins: direct connections vs. VIA connections . . . 5
Figure 6. STPMIC25 package bottom view . . . 6
Figure 7. STPMIC25 package side view . . . 6
Figure 8. STPMIC25 package top view . . . 6
Figure 9. STPMIC25 recommended footprint outline . . . 7
Figure 10. Exposed pad and vias placement on the top layer of the STPMIC25 evaluation board layout . . . 7
Figure 11. STEVAL$PMIC25M1 evaluation board: PCB stack-up layers . . . 9
Figure 12. STEVAL$PMIC25M1 evaluation board: 3D layout . . . 10
Figure 13. STEVAL$PMIC25M1 evaluation board: top layer (components/power/signal) . . . 10
Figure 14. STEVAL$PMIC25M1 evaluation board: mid layer 1 (GND) . . . 11
Figure 15. STEVAL$PMIC25M1 evaluation board: mid layer 2 (power/GND) . . . 11
Figure 16. STEVAL$PMIC25M1 evaluation board: bottom layer (power/GND) . . . 12
Figure 17. Mid layer 1 (GND plane) . . . 12
Figure 18. STEVAL$PMIC25M1 evaluation board: bottom layer (power/GND) . . . 13