AN6188

Application note

Migrating from the STM32F427/437 or STM32F429/439 to the STM32H5Ex/5Fx MCUs

Introduction

The designers of STM32 microcontroller applications must be allowed to replace a microcontroller from a given family by another from the same or a different family easily. The reasons for migrating an application to a different microcontroller can be for example:

- To fulfill higher product requirements, extra demands on memory size, or an increased number of I/Os
- To meet cost reduction constraints that require switching to smaller components and shrinking the PCB area

This application note details the steps required to migrate a design based on the STM32F427/437 or STM32F429/439 MCUs to one based on the STM32H5Ex/5Fx MCUs.

This document provides the full set of features available for the STM32F427/437 and STM32F429/439 devices, and the equivalent features on the STM32H5Ex/5Fx product lines. This document also provides guidelines on both hardware and peripheral migration.

To ease the understanding of the information inside this application note, the user must be familiar with the STM32 microcontroller family.

This application note is a complement to the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx datasheets and reference manuals. For additional information, refer to the product datasheets and reference manuals.

1 General information

The STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices are 32-bit microcontrollers based on the Arm® Cortex® processor.

Note: Arm and Cortex are registered trademarks of Arm Limited (or its subsidiaries or affiliates) in the US and/or elsewhere.

Reference documents

[1] *STM32F405/415, STM32F407/417, STM32F427/437, and STM32F429/439 advanced Arm®-based 32-bit MCUs*, reference manual (RM0090)

[2] *STM32H5E4/H5F4 and STM32H5E5/H5F5 Arm®-based 32-bit MCUs*, reference manual (RM0517)

[3] STM32F427xx/STM32F429xx datasheet (DS9405)

[4] STM32F437xx/STM32F439xx datasheet (DS9484)

[5] STM32H5Fxxx datasheet (DS14972)

STM32H5Exxx datasheet (DS14971)

[6] *STM32 microcontroller system memory boot mode*, application note (AN2606)

2 Overview of the STM32H5Ex/5Fx line MCUs

2.1 Main features

The STM32H5Ex/5Fx cryptographic MCUs include a larger set of peripherals with more advanced features compared to the STM32F427/437 and STM32F429/439 MCUs.

Here is a list of some of the new STM32H5Ex/5Fx peripherals and improved features:

- Graphic peripherals:
  - Chrom-ART Accelerator (DMA2D)
  - JPEG compressor/decompressor
  - Graphic timer (GFXTIM)
  - LCD-TFT display controller (LTDC)
- Security peripherals:
  - TrustZone®-aware and securable peripherals
  - Active tamper, secure firmware installation, secure firmware upgrade support, secure data storage with a hardware-unique key
  - Preconfigured immutable root of trust (STiRoT)
  - Flexible life cycle scheme with secure debug authentication
  - Coupling and chaining bridge (CCB)
  - Up to eight configurable secure attribution unit (SAU) regions
  - Additional encryption accelerator engine:
    - Advanced encryption hardware accelerator (AES)
    - Public key accelerator (PKA)
    - Secure AES coprocessor (SAES)
    - On-the-fly decryption engine on OCTOSPI (OTFDEC)
- Performance features:
  - Frequency up to 250 MHz
  - Direct access to the flash memory interface through the instruction cache (ICACHE)
  - ICACHE for internal and external memories
  - Data cache (DCACHE) for external memories
- Power supply features:
  - Embedded regulator (LDO)
  - Switched-mode power supply (SMPS) step-down converter:
    - Depending on the package configuration (SMPS or LDO), the regulator is selected through hardware. The SMPS and the LDO regulator are selected exclusively.
    - Both regulators can provide four different voltages (voltage scaling) and can operate in stop modes.
- New peripherals:
  - Filter mathematical accelerator (FMAC)
  - Coordinate rotation digital computer (CORDIC) coprocessor
  - New communication interfaces: I3C, FDCAN, LPUART, USB Type-C® connector/USB power delivery interface (UCPD), and parallel synchronous slave interface (PSSI)
  - Programmable logic array (PLAY)
  - OCTOSPI
  - Comparator (COMP)
  - Operation amplifiers (OPAMP)
  - Audio digital filter (ADF)
  - Multi-function digital filter (MDF)

Note: This document only manages the differences between the features that the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx have in common. It does not cover the new features of the STM32H5Ex/5Fx devices, mainly linked to TrustZone® support. The detailed list of available features and packages for each product is available in the respective product datasheet.

The table below summarizes the memory availability of the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx MCUs.

Table 1. Memory availability

Products	Flash memory		RAM size (Kbytes)						Feature level
	Size	Bank	SRAM1	SRAM2	SRAM3	SRAM4	SRAM5	BKPSRAM	
STM32H5Fx	Up to 4 Mbytes	Dual	256	128	384	384	384	4	With hardware cryptography: AES, PKA, SAES, and on-the-fly decryption (OTFDEC)
STM32H5Ex	Up to 4 Mbytes	Dual	256	128	384	384	384	4	N/A(1)
STM32F427/437, STM32F429/439	2 Mbytes	Dual	112	16	64	N/A	N/A	4	N/A

1. *N/A stands for not applicable.*

2.2 System architecture

The STM32H5Ex/5Fx devices embed:

- High-speed memories (up to 4 Mbytes of dual-bank flash memory and 1536 Kbytes of SRAM)
- A flexible external memory controller (FMC)
- Two octo-SPI memory interfaces (at least one octo-SPI available on all packages)
- An extensive range of enhanced I/Os and peripherals connected to three APB buses
- Three AHB buses and a 32-bit multi-AHB bus matrix

The following table illustrates the bus matrix differences between the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Table 2. Bus matrix

Bus type	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
AHB bus matrix masters	**Up to 8 masters**: • CPU I-bus, D-bus, and S-bus • DMA1 memory bus, DMA2 memory bus, and DMA2 peripheral bus • Ethernet DMA bus • USB OTG HS DMA bus	**Up to 16 masters**: • Fast C-bus • Slow C-bus • CPU core S-bus (three masters connected to three internal SRAMs without latency) • CPU core S-bus connected to the external memories through the data cache • GPDMA1 and GPDMA2 (general-purpose DMAs, both featuring two master ports) • SDMMC1 and SDMMC2 • Ethernet MAC • USB OTG HS • DMA2D • LTDC
AHB bus matrix slaves	**Up to 7 slaves**: • Internal flash memory ICode and DCode buses • SRAM1 and SRAM2 • AHB1 peripherals (including AHB-to-APB bridges and APB peripherals) • AHB2 peripherals • FMC	**Up to 13 slaves**: • Internal flash memory • SRAM1, SRAM2, SRAM3, SRAM4, and SRAM5 • AHB1 peripherals (including APB1 and APB2) and backup RAM (BKPSRAM) • AHB2 peripherals • FMC (flexible memory controller) • OCTOSPI1 and OCTOSPI2 • AHB3 peripherals • AHB4 peripherals

The bus matrix provides access from a master to a slave. This enables concurrent access and efficient operation even when several high-speed peripherals work simultaneously.

Figure 1 and Figure 2 show the system architectures of the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Figure 1. System architecture of the STM32F427/437 and STM32F429/439 devices

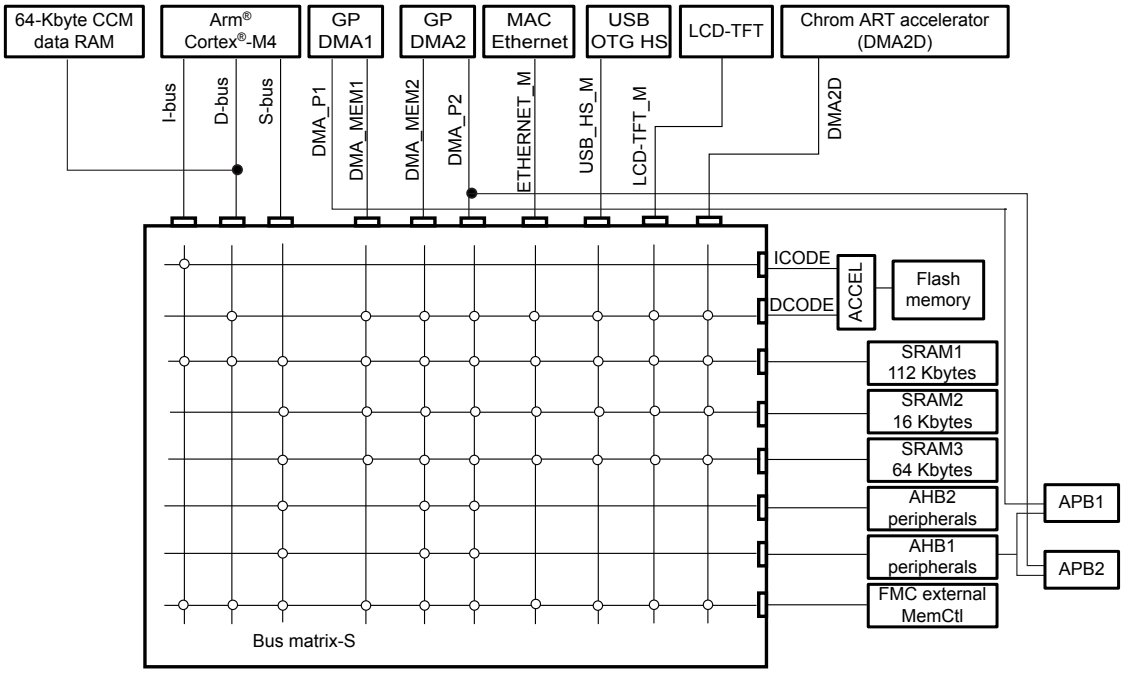
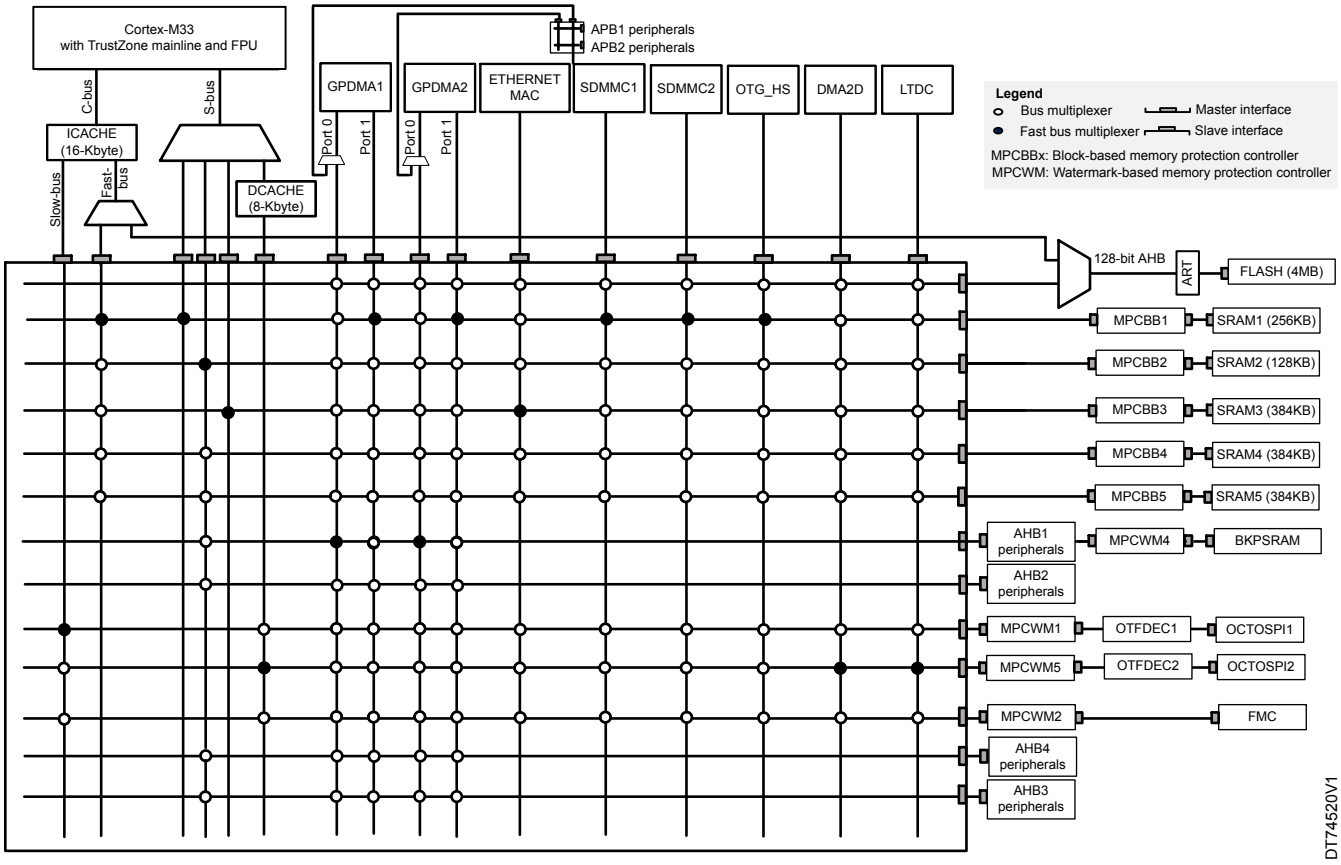


Figure 2. System architecture of the STM32H5Ex/5Fx devices



3 Hardware migration

This section details the package and pinout compatibility for the hardware migration.

3.1 Package availability

The STM32H5Ex/5Fx devices offer eight packages from 100 to 225 pins, and two options of pinout:

- LDO option, without an internal SMPS: most packages are partially compatible with the STM32F427/437 and STM32F429/439 devices.
- Internal SMPS option: versions with an internal SMPS, fully new packages. For this pinout version, the SMPS step-down converter and the LDO are embedded in parallel to provide the V_{CORE} supply.

All STM32H5Ex/5Fx packages are available with both options–LDO or SMPS supply for the V_{CORE}.

For more details on the pinout, refer to the product datasheets.

The table below lists the available packages on the STM32H5Ex/5Fx compared to STM32F427/437 and STM32F429/439 devices.

Table 3. Package availability

Package	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx (LDO version)		STM32H5Ex/5Fx (SMPS version)	
		LDO	LDO USBPHY	SMPS	SMPS USBPHY
LQFP100 (14 × 14 mm)	X	**X**	N/A(1)	**X**	N/A
LQFP144 (20 × 20 mm)	X	**X**	**X**	**X**	N/A
LQFP176 (24 × 24 mm)	X	**X**	N/A	**X**	**X**
LQFP208 (28 × 28 mm)	X(2)	N/A	N/A	N/A	N/A
UFBGA144 (10 × 10 mm)	N/A	**X**	N/A	**X**	N/A
UFBGA169 (7 × 7 mm)	X	**X**	N/A	**X**	N/A
UFBGA176 (10 × 10 mm)	X	**X**	N/A	**X**	**X**
TFBGA216 (13 × 13 mm)	X(2)	N/A	N/A	N/A	N/A
TFBGA225 (13 × 13 mm)	N/A	N/A	N/A	N/A	**X**
WLCSP	WLCSP143	N/A	N/A	N/A	WLCSP105

1. *N/A stands for not applicable.*
2. *Not available for STM32F437 devices.*

3.2 Pinout compatibility

The STM32F427/437 and STM32F429/439 devices are not identical to the STM32H5Ex/5Fx devices in terms of MCU port assignment to package terminals. They have different pinouts or ballouts. This holds for all the common types of package listed in Table 3. Package availability.

For the LQFP176 and UFBGA176 packages, the STM32H5Ex/5Fx features a VSS pin instead of the BYPASS_REG pin in the STM32F427/437 and STM32F429/439. In these devices, the BYPASS_REG pin connected to VDD is used to select the mode where the internal regulator is switched off and the core supply is provided externally.

For the STM32H5Ex/5Fx devices, there is no dedicated pin that defines if the regulator is in bypass mode or which regulator(s) is/are used. The hardware enables the LDO or SMPS regulator on power-on reset depending on the package configuration. To supply the V_{CORE} voltage from an external source, one can disable the regulator by setting the BYPASS bit.

In the STM32H5Ex/5Fx series, VCAP_1 and VCAP_2 pins are replaced by VSS and VDDUSB pins in the LQFP100 and LQFP144 packages.

The following subsections provide the package pinout figures and tables that show the package pinout differences.

3.2.1 LQFP100 package

Figure 3. **STM32H5Ex/5Fx LQFP100 pinout**

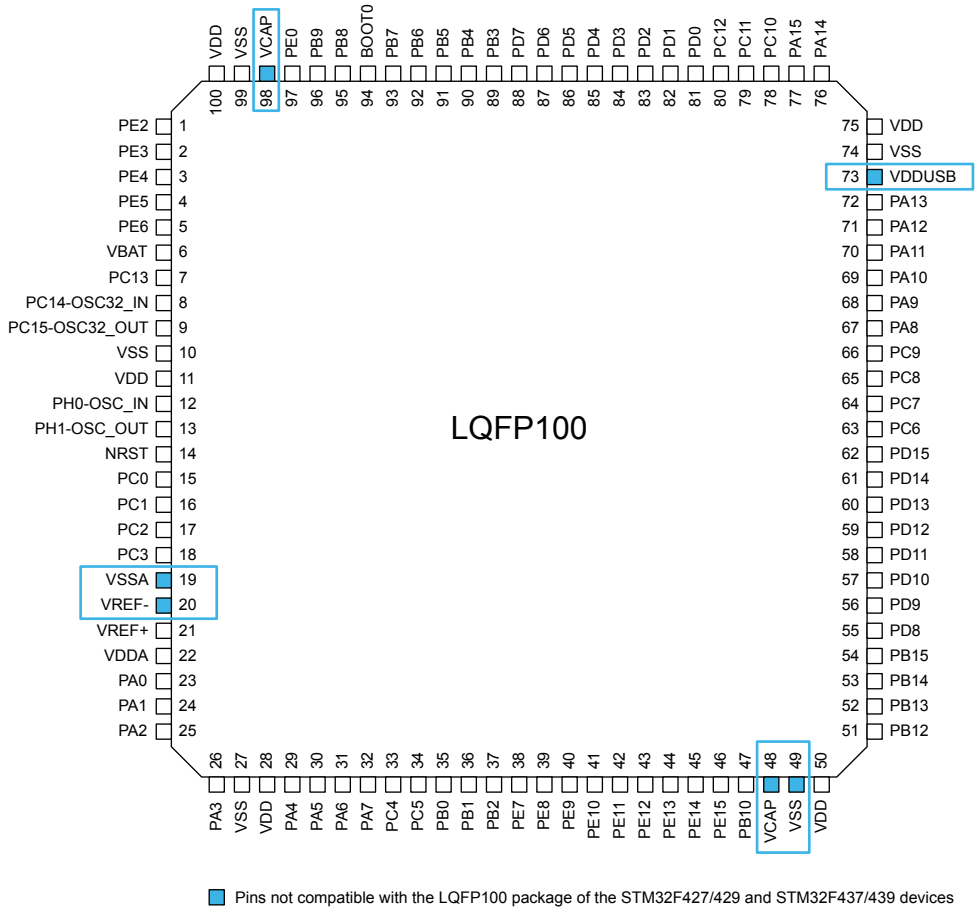


Table 4. **LQFP100 pinout differences**

LQFP100 pin number	STM32F427/437 pinout	STM32H5Ex/5Fx pinout
19	VDD	VSSA
20	VSSA	VREF-
48	PB11	VCAP
49	VCAP_1	VSS
73	VCAP_2	VDDUSB
98	PE1	VCAP

3.2.2 LQFP144 package

Figure 4. STM32H5Ex/5Fx LQFP144 pinout

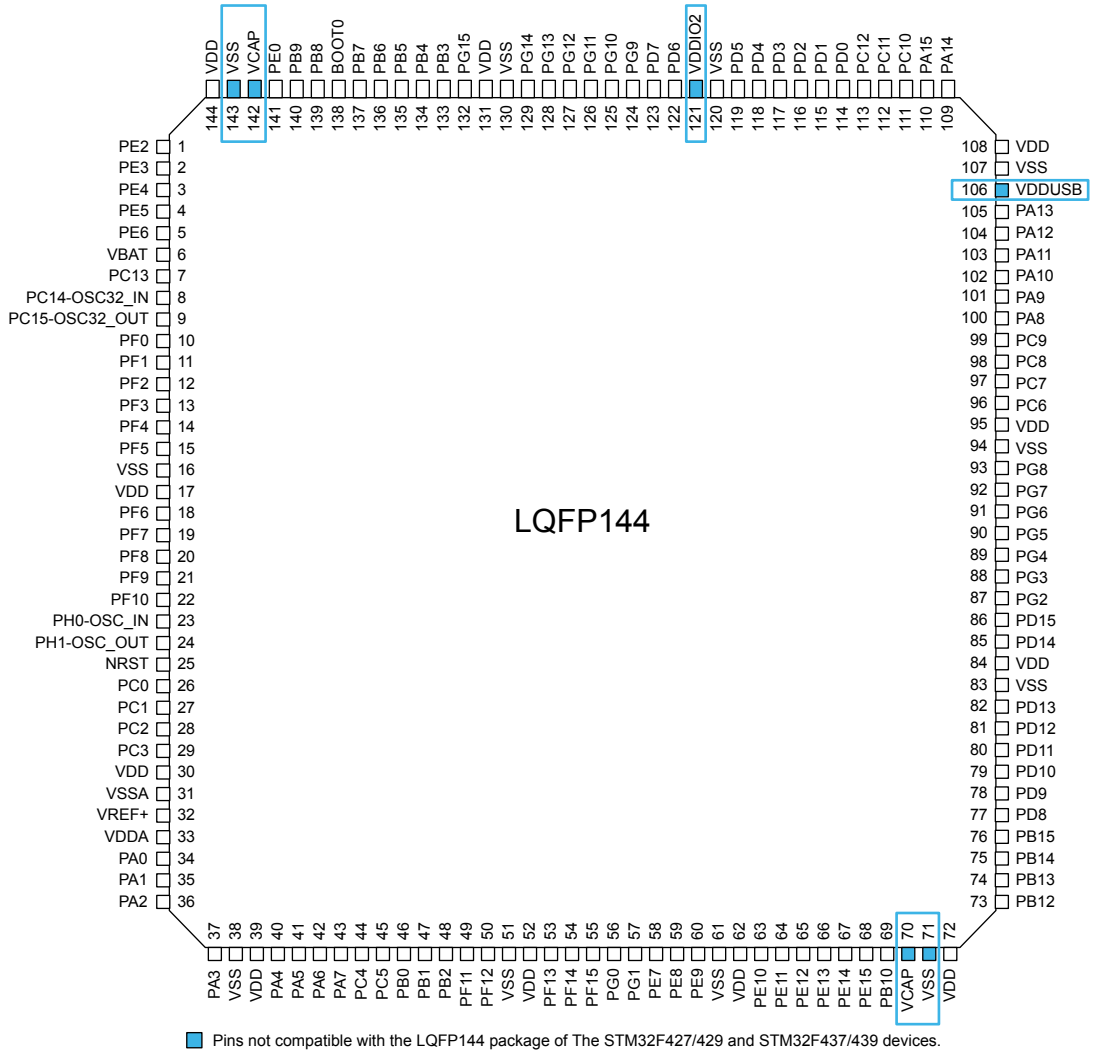


Table 5. LQFP144 pinout differences

LQFP144 pin number	STM32F427/437 and STM32F429/439 pinout	STM32H5Ex/5Fx pinout
70	PB11	VCAP
71	VCAP_1	VSS
106	VCAP_2	VDDUSB
121	VDD	VDDIO2
142	PE1	VCAP
143	PDR_ON	VSS

3.2.3 LQFP176 package

Figure 5. STM32H5Ex/5Fx LQFP176 pinout

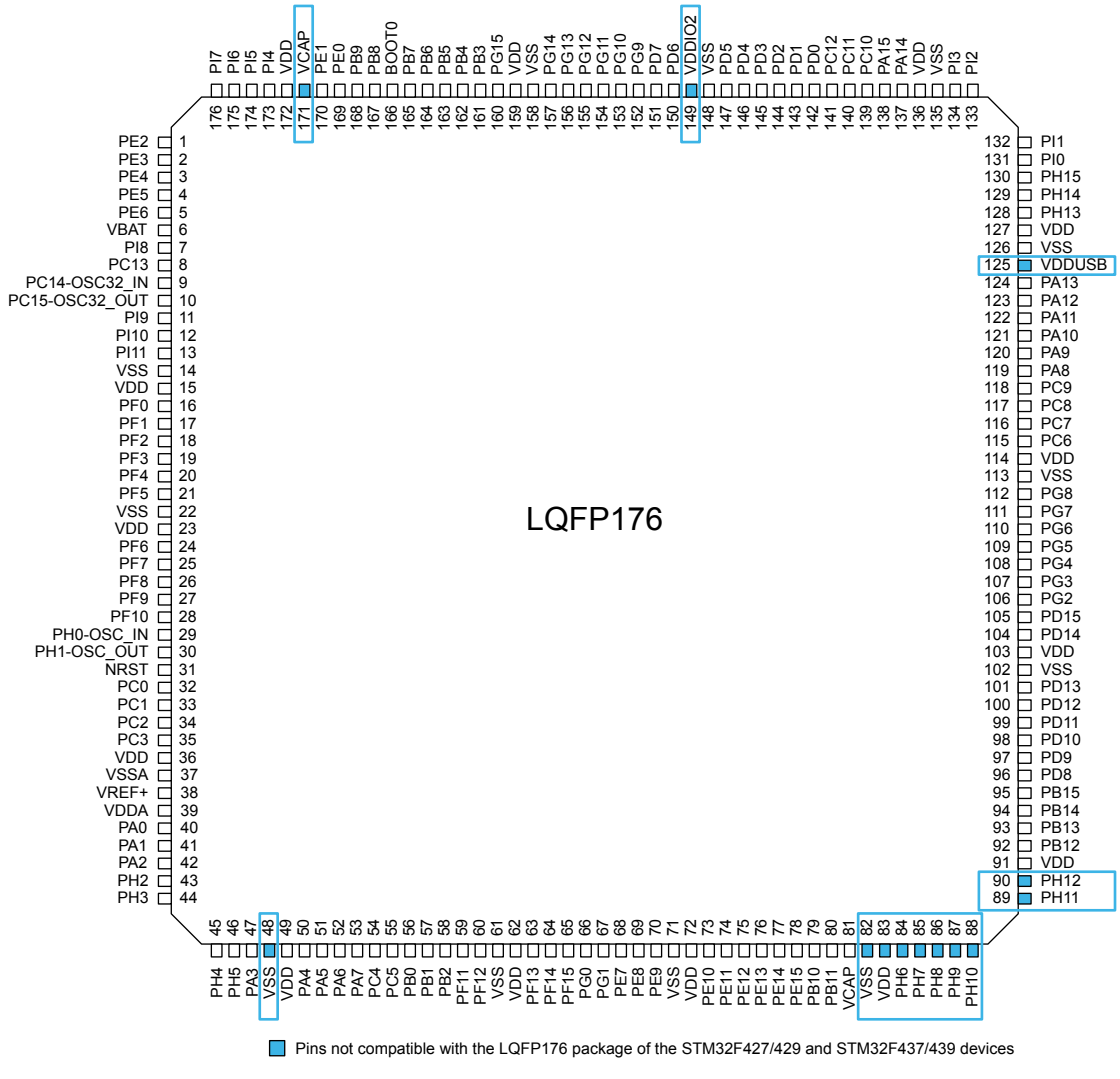


Table 6. **LQFP176 pinout differences**

LQFP176 pin number	STM32F427/437 and STM32F429/439 pinout	STM32H5Ex/5Fx pinout
48	BYPASS_REG	VSS
82	VDD	VSS
83	PH6	VDD
84	PH7	PH6
85	PH8	PH7
86	PH9	PH8
87	PH10	PH9
88	PH11	PH10
89	PH12	PH11
90	VSS	PH12
125	VCAP_2	VDDUSB
149	VDD	VDDIO2
171	PDR_ON	VCAP

3.2.4 UFBGA176 + 25 package

Figure 6. STM32H5Ex/5Fx UFBGA176 + 25 ballout

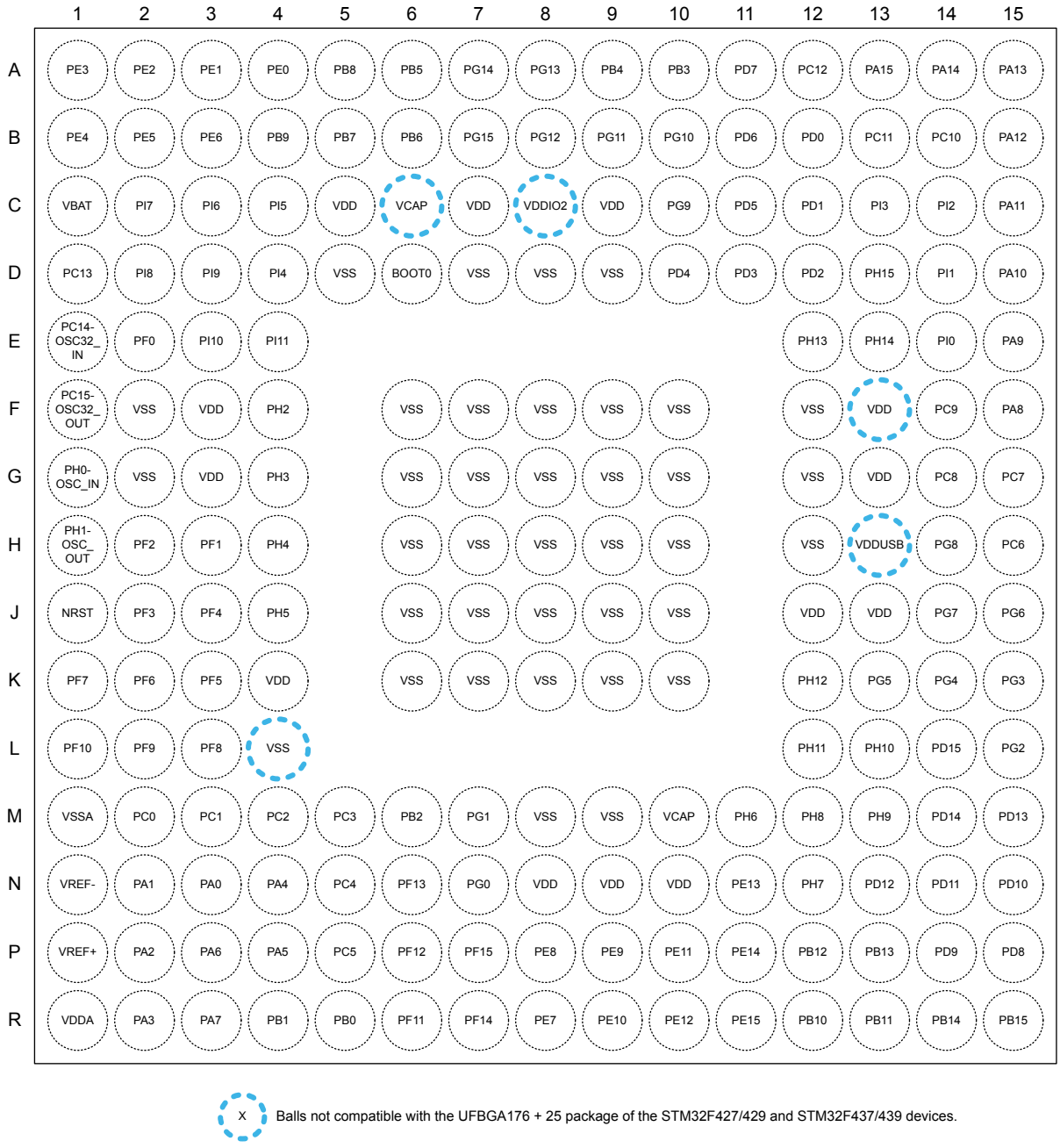


Table 7. UFBGA176 + 25 ballout differences

UFBGA176 + 25 ball number	STM32F427/437 and STM32F429/439 ballout	STM32H5Ex/5Fx ballout
C6	PDR_ON	VCAP
C8	VDD	VDDIO2
F13	VCAP_2	VDD
H13	VDD	VDDUSB
L4	BYPASS_REG	VSS

3.2.5 UFBGA169 package

For the UFBGA169 package, the STM32F427/437 and STM32F429/439 devices are not compatible with the STM32H5Ex/5Fx devices.

4 Boot mode compatibility

4.1 STM32F427/437 and STM32F429/439 boot modes

In the STM32F427/437 and STM32F429/439, three different boot modes can be selected through the BOOT[1:0] pins as shown in the table below.

Table 8. Boot modes for the STM32F427/437 and STM32F429/439 devices

Boot mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
X	0	Main flash memory	The main flash memory is selected as the boot space.
0	1	System memory	The system memory is selected as the boot space.
1	1	Embedded SRAM	The embedded SRAM is selected as the boot space.

4.2 STM32H5Ex/5Fx boot modes

The sections below present the STM32H5Ex/5Fx boot modes, when TrustZone® is disabled or enabled.

The STM32H5Ex/5Fx devices embed a secure boot system (SBS) peripheral that controls the boot and security features. For these devices, the main boot control actions are listed below:

1. Run the product with or without TrustZone® enabled.
2. Select between STiRoT or OEMiROT (refer to the reference manual for more details.)
3. Boot when launching a debug authentication sequence.
4. Select boot between the bootloader or the user flash memory boot.
5. Initialize the isolation level (HDPL) boot value.

For the STM32H5Ex/5Fx devices, the boot configurations are selected considering the product settings:

- BOOT0: to select booting on the user flash memory or RSS (root secure services).
- BOOT_UBE: option byte to select the iROT between STiRoT and OEMiROT.
- TZEN: option byte to activate/deactivate the TrustZone®.
- sbs_boot_addresses: list of addresses defined through the flash memory:
- NSBOOTADD: nonsecure boot address
- SECBOOTADD: secure boot address
- PRODUCT_STATE: option byte to activate the different security mechanisms depending on the product use.
- sbs_dbg_req: used to launch the debug authentication protocol when booting

4.2.1 STM32H5Ex boot modes

Table 9 provides the detail of the boot mode when the TrustZone® is disabled (TZEN = 0xC3), for the STM32H5Ex devices.

Table 9. STM32H5Ex boot modes when TrustZone® is disabled (TZEN = 0xC3)

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	N/A	NSBOOTADD [31:8]	Boot address defined by user option byte NSBOOTADD [31:8]	Flash : 0x0800 0000
	1	N/A	N/A	Bootloader	Bootloader
Provisioning	X	N/A	N/A	RSS	RSS

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Provisioned, Closed, Locked	X	N/A	NSBOOTADD [31:8]	Boot address defined by user option byte NSBOOTADD [31:8]	Flash : 0x0800 0000

Table 10 provides the detail of the boot mode when the TrustZone® is enabled (TZEN=0xB4), for the STM32H5Ex devices.

Table 10. STM32H5Ex boot modes when TrustZone® is enabled (TZEN = 0xB4)

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	N/A	NSBOOTADD [31:8]	Boot address defined by user option byte NSBOOTADD [31:8]	Flash : 0x0C00 0000
	1	N/A	N/A	Bootloader	Bootloader
Provisioning	X	N/A	N/A	RSS	RSS
Provisioned, TZ_Closed, Closed, Locked	X	N/A	NSBOOTADD [31:8]	Boot address defined by user option byte NSBOOTADD [31:8]	Flash : 0x0C00 0000

4.2.2 STM32H5Fx boot modes

Table 11 provides the detail of the boot mode when the TrustZone® is disabled (TZEN = 0xC3), for the STM32H5Fx products.

Table 11. STM32H5Fx boot modes when TrustZone® is disabled (TZEN = 0xC3)

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	N/A	NSBOOTADD [31:8]	Boot address defined by user option byte NSBOOTADD [31:8]	Flash : 0x0800 0000
	1	N/A	N/A	Bootloader	Bootloader
Provisioning	X	N/A	N/A	RSS	RSS
Provisioned, Closed, Locked	X	N/A	NSBOOTADD [31:8]	Boot address defined by user option byte NSBOOTADD [31:8]	Flash : 0x0800 0000

Table 12 provides the detail of the boot mode when the TrustZone® is enable (TZEN = 0xB4), for the STM32H5Fx products.

Table 12. STM32H5Fx boot modes when TrustZone® is enabled (TZEN = 0xB4)

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	X	SECBOOTADD [31:8]	Boot address defined by user option byte SECBOOTADD [31:8]	Flash : 0x0C00 0000
	1	0xB4	N/A	Bootloader	Bootloader

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Open	1	0xC3	N/A	STiRoT	STiRoT
Provisioning	X	N/A	N/A	RSS	RSS
Provisioned, TZ_Closed, Closed, Locked	X	0xC3	STiRoT	STiRoT	STiRoT
	X	0xB4	SECBOOTADD [31:8]	Boot address defined by user option byte SECBOOTADD [31:8]	Flash : 0x0C00 0000

4.3 System bootloader

The system bootloader is in the system memory. STMicroelectronics programs it during the production phase. It is used to reprogram the flash memory using one of the serial interfaces listed in the table below.

The following table shows the communication peripherals that the system bootloader supports. For more details, refer to the application note [6].

Table 13. Bootloader communication peripherals

System bootloader peripherals	STM32F427/437 and STM32F429/439 I/O pin	STM32H5Ex/5Fx I/O pin
DFU (1)	PA11/PA12	PA11/PA12 (OTG_FS)
	N/A(2)	OTG_HSDP / OTG_HSDM
USART1	PA9/PA10	
USART2	N/A	PA2/PA3
USART3	PB10 / PB11 and PC10 / PC11	PD8/PD9
CAN	CAN2 (PB5/PB13 PB8/PB9)	N/A
I2C3	N/A	PA8/PC9
I2C4	N/A	PD12/PD13
I3C1	N/A	PB6/PB7

1. *On the STM32H5Ex/5Fx, the USB DFU bootloader does not need an external quartz oscillator. It uses the internal HSI48.*
2. *N/A stands for not applicable.*

5 Peripheral migration

5.1 Cross-compatibility between STM32 products

The STM32 microcontrollers embed a set of peripherals that can be classified into the following groups:

- Group 1: peripherals, which are, by definition, common to all products.
  Those peripherals are identical. They have the same structure, registers, and control bits. There is no need to modify the firmware to ensure the same functionality at the application level after migration. All the features and the behavior remain the same.
- Group 2: peripherals shared by all products but with some minor differences (mainly, to allow them to support new features.)
  The migration from one product to another is very easy and does not need any significant development effort.
- Group 3: peripherals that change considerably from one product to another (new architecture or new features for example.)
  For this group of peripherals, the migration requires new development at the application level.

For the STM32H5Ex/5Fx, all the following can be configured as trusted or untrusted:

- Each GPIO or peripheral
- Each DMA channel
- Each clock configuration register
- Each ICACHE and DCACHE
- Every small part of flash memory or SRAM

The following table summarizes the available peripherals in the STM32F427/437 and STM32F429/439 compared to the STM32H5Ex/5Fx.

Table 14. STM32 peripheral compatibility between products

Peripherals		STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Core		Cortex®-M4	Cortex®-M33
Maximum CPU frequency		Up to 180 MHz	Up to 250 MHz
Flash memory		2 Mbytes	4 Mbytes
SRAMs	System	256 Kbytes (112+16+64+64)	1536 Kbytes (256+128+384+384+384)
	Backup	4 Kbytes	4 Kbytes
Timers	General-purpose	2 (32 bits) and 8 (16 bits)	2 (32 bits) and 8 (16 bits)
	Advanced control	2 (16 bits)	2 (16 bits)
	Basic	2 (16 bits)	2 (16 bits)
	Low-power(1)	No	6 (16 bits)
	SysTick timer	1	2
	Watchdog timers (independent, window)	2	2
Communications interfaces	SPI/I2S	Up to 6 SPIs, 2 with multiplexed full-duplex I2S	Up to 6 SPIs. Including three multiplexed with full-duplex I2S and up to 5 additional SPIs from 5 USARTs when configured in synchronous mode (one additional SPI with OCTOSPI)
	I2C	3 (Sm and Fm interfaces (SMBus/PMBus)	4 (Sm, Fm, and Fm+ interfaces (SMBus/PMBus)
	I3C (1)	No	2
	USART/UART	4/4	6/6

Peripherals		STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Communications interfaces	LPUART (1)	No	1
	USB	USB OTG FS and USB OTG HS	OTG FS and OTG HS
	UCPD (1)	No	Yes
Communication interfaces	CAN	2	x3 FDCAN
	SAI	1	2
	SDIO/SDMMC	1	2
	DCMI	Yes	Yes
	PSSI (1)	No	Yes
	Ethernet	Yes	Yes (1 Ethernet 10/100 Mbit/s)
Flexible memory controller (FMC)		Yes (8-, 16-, 32-bit data bus width)	Yes (8-, 16-, 32-bit data bus width with SDRAM)
OCTOSPI (1)		No	2
HDMI-CEC (1)		No	Yes
CRC		Yes	Yes
Graphic accelerators	LCD-TFT display controller (LTDC)	Yes	Yes
	JPEG (1)	No	Yes
	Chrom-ART Accelerator DMA2D	Yes	Yes
	GFXTIM (1)	No	Yes
DMA		2	2 GPDMA (featuring two master ports) TrustZone® support/linked list
CORDIC coprocessor (1)		No	Yes
Filter mathematical accelerator (FMAC) (1)		No	Yes
Real-time clock (RTC)		Yes	Yes
Random number generator (RNG)		Yes	Yes
SAES, AES (1)		No	Yes
Public key accelerator (PKA) (1)		No	Yes
HASH		Yes	Yes (SHA-1, SHA-2 family and SHA-3 family)
Cryptographic processor (CRYP)		Yes	No
On-the-fly decryption engine (OTFDEC)(1)		No	Yes
GPIOs		Up to 168	Up to 176
ADC (12 bits)	Count	3 (12-bit ADC 2.4 MSPS and 7.2 MSPS in triple interleaved mode)	3 (12-bit ADC with up to 5 MSPS)
	Number of channels	Up to 24	Up to 30
DAC (12 bits)	Count	1	1
	Number of channels	2	2
Comparator (COMP)(1)		No	2
Operation amplifier (OPAMP)(1)		No	1
CRC (1)		No	Yes

Peripherals	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Multifunction digital filter (MDF)(1)	No	Yes
Audio digital filter (ADF)(1)	No	Yes
Programmable logic array (PLAY)(1)	No	Yes
RCC	Yes	Yes
Operating temperatures	Ambient temperature: –40 to +85 °C or –40 to +105 °C Junction temperature: –40 to + 125 °C	Ambient operating temperature: –40°C to +85°C / – 40°C to +105°C VOS0 (up to 250 MHz): Tj from -40 to 105 °C VOS1 (up to 200 MHz): Tj from -40 to 130 °C
Operating voltage	1.7 to 3.6 V	1.71 to 3.6 V
Internal voltage reference buffer	No	Yes

1. *New versus STM32F427/437 and STM32F429/439.*

5.2 Migrating the system peripherals

5.2.1 Embedded flash memory (FLASH)

The following table compares the flash memory interface on the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Table 15. FLASH features

Flash memory	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Main/program memory	• Up to 2 Mbytes (dual bank) • 4 sectors of 16 Kbytes • 1 sector of 64 Kbytes • 6 sectors of 128 Kbytes	• Up to 4 Mbytes of nonvolatile memory (dual bank) • Flash memory read operations supporting multiple lengths: 128 bits, 64 bits, 32 bits, 16 bits, or one byte • Support for 8 Kbyte sector erase, bank erase, and dual-bank mass erase operations
Features	Read while write (RWW)	
Error code correction (ECC)	No	One error detection/correction or two error detections per 128-bit flash memory word using 9 ECC bits, on 16-bit words with 6 bits within the configurable high-cycle data area of the flash memory
Wait states	Up to 8 (depending on the supply voltage and frequency)	Up to 6 (depending on the supply voltage and frequency)
One-time programmable (OTP) memory	512 bytes (OTP) for user data	2 Kbyte (OTP) area
FLASH security and protections	• Read protection (RDP) • Write protections • Proprietary code readout protection (PCROP)	• TrustZone®-backed watermark and block security protection. • HDP protection providing temporal isolation • Configuration protection • Write protection • Nonvolatile security life cycle of the device and application boot state management

Flash memory	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
User option bytes [1]	nRST_STDBY nRST_STOP WDG_SW BOR_LEV BFB2 OPTSTRT OPTLOCK DB1M nWRP RDP USER SPRMOD	NRST_STBY NRST_STOP IWDG_SW WWDG_SW IWDG_STBY, IWDG_STOP BOR_LEV BORH_EN BOOT_UBE OPTSTRT OPTLOCK WRPSG PRODUCT_STATE IO_VDDIO2_HSLV SWAP_BANK

1. *Refer to [1] and [2], "Option-byte organization" table, which provides all user option bytes.*

5.2.2 SRAMs

In the STM32F427/437 and STM32F429/439, the control of the SRAM is integrated within the SYSCFG.

The RAMCFG controller, a new peripheral available on the STM32H5Ex/5Fx, is dedicated to control SRAM1, SRAM2, SRAM3, SRAM4, SRAM5, and BKPSRAM. Refer to [2], section *RAM configuration controller* for more details.

Table 16. SRAM features

Features	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Size	• Up to 256 Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM. • Main internal SRAM1 (112 KB) – Auxiliary internal SRAM2 (16 KB) – Auxiliary internal SRAM3 (64 KB) • 4 Kbytes of backup SRAM	Up to 1536 Kbytes: • 256-Kbyte SRAM1 • 128-Kbyte SRAM2 • 384-Kbyte SRAM3 • 384-Kbyte SRAM4 • 384-Kbyte SRAM5 • 4-Kbyte BKPSRAM
DMA and CPU access	BKPSRAM (system bus) Possible access types: bytes, half-words (16 bits), or full words (32 bits)	Possible access types: bytes, half-words (16 bits), or full words (32 bits)
CPU access bus	System bus or ICode/DCode buses BKPSRAM (system bus)	• System bus or C-bus • BKPSRAM (only system bus)
Retention	BKPSRAM: Optional retention in Standby mode Optional retention in VBAT mode	
Security	N/A[1]	• When the TrustZone® security is enabled, all SRAMs are secure after reset • The SRAMs can be programmed as nonsecure, using the MPCBB with a block granularity of 512 bytes

Features	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Hardware and software erase conditions	A tamper event does not mass-erase the backup SRAM. The backup SRAM is only erased when the RDP changes from level 1 to 0.	The tamper detection circuit protects the SRAM2 and BKSRAM. The hardware erases SRAM2 and BKSRAM in the case of a tamper detection. SRAM2 is deleted in the case of a regression.
System reset erase	N/A	A system reset can erase SRAM2 if the SRAM2_RST option bit is so configured in the user option bytes of the flash memory. SRAM1, SRAM3, SRAM4, and SRAM5 are erased when a system reset occurs if the SRAM1345_RST option bit is selected in the user option bytes of the flash memory.
Error detection and correction	N/A	• Single-error detection and correction with interrupt generation • Double-error detection with interrupt or NMI generation • SRAM2, SRAM3, and BKPSRAM support ECC when the feature is enabled with the SRAM2_ECC, SRAM3_ECC, and BKPRAM_ECC user option bits. • ECC: 7 bits are added per 32 bits • Interrupts are generated when single- and/or double-ECC errors are detected: – Two ECC RAMCFG interrupts – One ECC NMI interrupt
Write protection	N/A	SRAM2 can be write-protected with a page granularity of 1 Kbyte. Each 1-Kbyte page can be write-protected by setting its corresponding PxWP (x = 0 to 63) bit in the RAMCFG registers.
Read access latency	N/A	3-bit programmable wait states depending on the AHB clock frequency (HCLK) and voltage scaling range

1. *N/A stands for not applicable.*

5.2.3 System configuration controller

The table below presents the main differences in the system configuration controller (SYSCFG) between the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Note: For the STM32H5Ex/5Fx devices, the SYSCFG is integrated in the SBS (system configuration, boot, and security).

Table 17. System configuration features

STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
• Managing the I/O compensation cell • Selecting the Ethernet PHY interface	
• Remapping the memory accessible in the code area • Managing the external interrupt line connection to the GPIOs	N/A(1)
N/A	• Enabling/disabling the FMP high-drive mode of some I/Os and voltage booster for I/O analog switches • Configuring TrustZone® security register access • Tracking the PVT conditions to control the current slew rate and output impedance in the I/O buffer through compensations cells • Two compensation cells are embedded: – One for the I/Os supplied by the V_{DDIO} power rail – One for the I/Os supplied by the V_{DDIO2} power rail

1. *N/A stands for not applicable*

5.2.4 Instruction and data caches (ICACHE/DCACHE)

The STM32H5Ex/5Fx devices embed an ICACHE (16 Kbytes) and a DCACHE (8 Kbytes), which allow a more efficient use of the external memory through the OCTOSPI and FMC ports.

The STM32F427/437 and STM32F429/439 devices do not embed these caches.

5.2.5 Direct memory access controller (DMA)

The STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx have different DMA architectures and features.

All devices embed two DMA controllers:

- DMA1 (8 channels) and DMA2 (8 channels) for the STM32F427/437 and STM32F429/439
  Each channel is dedicated to managing the memory access requests from one or more peripherals. The devices also embed an arbiter for handling the priorities among the DMA requests.
- GPDMA1 (12 channels) and GPDMA2 (12 channels) for STM32H5Ex/5Fx
  Each GPDMA instance has the same channel-based implementation and is connected to the same requests and triggers.

The STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx also embed a Chrom-ART Accelerator (DMA2D) that is a specialized DMA dedicated to image manipulation. The following table illustrates the main differences between DMA requests in the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Table 18. DMA features

Peripherals	STM32F427/437 and STM32F429/439		STM32H5Ex/5Fx	
	DMA1	DMA2	GDMA1	GDMA2
Architecture	Each instance of DMA controllers can access memory and peripherals			
Number of instances	1	1	1	1
Number of masters	Dual AHB master bus	Dual AHB master bus	Dual bidirectional AHB master	
Number of channels	8	8	12	12
TrustZone® security	N/A(1)		Yes	
Privileged/unprivileged DMA				
Linked list				

1. *N/A stands for not applicable.*

5.2.6 Reset and clock control (RCC)

The table below presents the main differences related to the RCC (reset and clock controller) between the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Table 19. RCC features

RCC	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
HSI	16 MHz RC oscillator	64 MHz RC oscillator
CSI	N/A(1)	CSI: low-power RC oscillator that can be used directly as the system clock, peripheral clock, or PLL input. The CSI advantages are the following: • Low-cost clock source since no external crystal is required. • Faster startup time than HSE (a few microseconds). • Very-low power consumption. The CSI provides a clock frequency of about 4 MHz while the HSI is able to provide a clock up to 64 MHz.
HSI48	N/A	48 MHz RC oscillator HSI48 can drive USB and the RNG.
LSI	The clock frequency is around 32 kHz. Lower consumption and higher accuracy	
HSE	From 4 to 26 MHz	From 4 to 50 MHz
LSE	32.768 kHz	32.768 kHz Provide a low-power, highly accurate clock source to the real-time clock (RTC) for clock/calendar or other timing functions.

RCC	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
PLL	Three PLLs: • PLLI2S and PLLSAI generate an accurate clock. • A main PLL (PLL) clocked by the HSE or the HSI oscillator. It features two different output clocks: – One output generates the high-speed system clock (up to 180 MHz) – One output for the USB OTG_FS, RNG, and SDIO	Three PLLs: • The main PLL (PLL1) provides clocks for the CPU and some peripherals. • PLL2 and PLL3 generate the kernel clock for peripherals. Each PLL offers three outputs with postdividers. Input frequency range: • 2 to 16 MHz for the VCO in wide-range mode • 1 to 2 MHz for the VCO in low-range mode
AHB frequency	Up to 180 MHz	Up to 250 MHz
APB1 frequency	Up to 45 MHz	Up to 250 MHz
APB2 frequency	Up to 90 MHz	Up to 250 MHz
RTC clock source	LSE, LSI, or HSE/ 32	
Kernel clock	N/A	Independent kernel clock for each IP. It allows frequency scaling without any impact on the communication interfaces.
System clock source	HSI, HSE, or PLL	HSI, CSI, HSE, or PLL1
Clock security system	CSS on HSE	CSS on HSE CSS on LSE
MCO clock source	• MCO1 pin (PA8): HSI, LSE, HSE, or PLL • MCO2 pin (PC9): HSE, PLL, SYSCLK, or PLLI2S	• MCO1 pin (PA8): HSI, LSE, HSE, PLL1, or HSI48 • MCO2 pin (PC9): SYSCLK, PLL2, HSE, PLL1, CSI, or LSI

1. *N/A stands for not applicable.*

The peripherals presented below have a dedicated clock source that is used to generate the clock required for their operation. The table below presents the difference between the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices related to peripherals with different clock sources.

Table 20. Peripherals with different clock sources

Peripherals	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
SAI	PLLI2S_Q PLLSAI_Q External clock mapped on the I2S_CKIN pin	pll1_q_ck pll2_p_ck pll3_p_ck AUDIOCLK per_ck
U(S)ART	APB1 or APB2 clock (PCLK1 or PCLK2)	rcc_pclk1(1) rcc_pclk2(2) pll2_q_ck pll3_q_ck hsi_ker_ck csi_ker_ck

Peripherals	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
		lse_ck
I2C	APB1 clock (PCLK1)	rcc_pclk1(3) pll3_r_ck hsi_ker_ck csi_ker_ck
SPI	APB clock (PCLK)	rcc_pclk2(4) rcc_pclk3(5) pll2_q_ck(6) pll3_q_ck(6) hsi_ker_ck(6) hse_ck(6) csi_ker_ck(6) pll1_q_ck(7) pll2_p_ck(7) pll3_p_ck(7) AUDIOCLK(7) per_ck(7)
I2S	PLLI2S External clock mapped on the I2S_CKIN pin	pll1_q_ck pll2_p_ck pll3_p_ck AUDIOCLK per_ck
CAN	APB clock (PCLK)	hse_ck pll1_q_ck pll2_q_ck
ADC	APB2 clock (PCLK2)	rcc_hclk sys_ck pll2_r_ck hse_ck hsi_ker_ck csi_ker_ck
USB FS	PLL 48 MHz derived from main PLL VCO (PLLQ clock)	hsi48_ker_ck pll1_q_ck pll3_q_ck clk48mohci
OTG_HS	N/A(8)	-
RNG	No	hsi48_ker_ck pll1_q_ck lse_ck lsi_ker_ck
SDMMC	SDIO/SDMMC1: PLL48CLK	SDMMCx (x = 1, 2): pll1_q_ck pll2_r_ck
MDF and ADF	N/A	Pll1_q_ck

Peripherals	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
		Pll2_q_ck Pll3_q_ck per_ck
PLAY	N/A	rcc_pclk3 pll2_p_ck pll3_r_ck lse_ker_ck lsi_ker_ck per_ck
IWDG	LSI	

1. *Only for UARTx (x = 4, 5, 7, 8, 9, 12) and USARTx (x = 2, 3, 6, 10, 11).*
2. *Only for USART1.*
3. *Only for I2Cx (x = 1, 2).*
4. *Only for SPIx (x = 4, 6).*
5. *Only for SPI5.*
6. *Only for SPIx (x = 4, 5, 6).*
7. *Only for SPIx (x = 1, 2, 3).*
8. *N/A stands for not applicable.*

5.2.7 Power (PWR)

The table below presents the PWR controller differences between the STM32F427/437 and STM32F429/439 devices, and the STM32H5Ex/5Fx devices. Both the dynamic and static power consumptions were optimized for the STM32H5Ex/5Fx devices.

Table 21. PWR features

PWR	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Power supply	**V_{DD} = 1.7 to 3.6 V:** external power supply for I/Os and the internal regulator (when enabled). It is provided externally through the VDD pins.	**V_{DD} = 1.71 V to 3.6 V:** external power supply for the I/Os, the internal regulator, and the analog components of the system such as reset, power management, and internal clocks. It is provided externally through the VDD pins.
	V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for the ADC, DAC, reset blocks, RCs, and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.	**V_{DDA} = 1.62 V (ADCs)/1.8 V (DAC) or 2.0 V (op amp) or 2.1 V (VREFBUF) to 3.6 V:** external analog power supply for the A/D converters, D/A converters, and voltage reference buffer. The V_{DDA} voltage level is independent of the V_{DD} voltage.
	V12: voltage source through the VCAP_1 and VCAP_2 pins. It is around **1.2 V**.	**V_{CAP} = 1.0 V to 1.35 V:** power supply for the digital peripherals, SRAMs (except BKPSRAM), and embedded flash memory.
	V_{BAT} = 1.65 to 3.6 V When V_{DD} is not present, V_{BAT} is the power supply for the RTC, 32 kHz external clock oscillator, and backup registers.	**V_{BAT} = 1.2 V to 3.6 V** When V_{DD} is not present, V_{BAT} is the power supply for the RTC, 32 kHz external clock oscillator, backup registers, and optional backup SRAM (1)(2)
	N/A(3)	**V_{DDSMPS} = 1.71 V to 3.6 V:** external power supply for the SMPS step-down converter. It is provided externally through the VDDSMPS supply pin and must be connected to the same supply as the VDD pin. VLXSMPS is the switched SMPS step-down converter output. An external coil with a typical value of 2.2 µH must be connected between the dedicated VLXSMPS pin to VSSSMPS, via a capacitor of 10 µF. VSSSMPS is an isolated supply ground.
	N/A	**V_{DDUSB} = 3.0 V to 3.6 V:** external independent power supply for USB transceivers

PWR	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Power supply		The V_{DDUSB} voltage level is independent from the V_{DD} voltage.
	N/A	**$V_{DD11USB}$ = 0.95 V to 1.40 V**: the digital power supply for the OTG_HS transceiver. This supply is only available on specific packages and must be connected to V_{CAP} when used, and to GND when not used. Ist is only available on STM32H5Ex/5Fx devices.
	N/A	**V_{DDIO2} = 1.08 V to 3.6 V:** external power supply for 10 I/Os (PD6, PD7, PG9:14, PB8, and PB9). This voltage is independent of the V_{DD} voltage.
Battery backup domain	RTC with backup registers LSE Backup SRAM when the low-power backup regulator is enabled. PC13 to PC15 I/Os plus PI8 I/O (when available)	RTC with backup registers (128 bytes) LSE PC13 to PC15 I/Os plus PI8 I/O (when available)
Power supply supervisor	POR, PDR, BOR, PVD	
	N/A	AVD Backup domain voltage and temperature monitoring
Wake-up sources in Sleep mode	Any peripheral interrupt/wake-up event	
Wake-up sources in Standby mode	WKUP pin PA0 on the rising edge RTC event (RTC ALARM, Tamper event, timestamp event) IWDG reset External reset at the NRST pin	WKUPx pin edge, RTC event, external reset at the NRST pin, IWDG reset, and BOR reset
Wake-up sources in Stop mode	Any EXTI line (configured in the EXTI registers, internal and external lines)	Any EXTI line (configured in the EXTI registers) Specific peripherals events
Wake-up System clock	Stop: HSI RC oscillator	Stop: • CSI when STOPWUCK = 1 in the RCC_CFGR register • HSI with a frequency up to 64 Hz before entering Stop mode with STOPWUCK = 0 Standby: HSI clock at 64 MHz
Low-power modes	Sleep mode	Sleep mode
	Stop mode	Stop mode: To optimize the power consumption further, the unused RAMs can be totally or partially shut off.
	Standby mode	Standby mode

1. *Supply for the SMPS power stage (available on SMPS packages). The SMPS power supply pins are available only on a specific package with the SMPS step-down converter option.*
2. *VDDSMPS and VLXSMPS are only available in the STM32H5Ex/5Fx devices.*
3. *N/A stands for not applicable.*

The STM32H5Ex/5Fx devices embed two regulators: one LDO or one SMPS to provide the V_{CORE} supply for the digital peripherals, SRAMs (except BKPSRAM), and embedded flash memory. These regulators can provide four different voltages (voltage scaling) and operate in Stop mode. Depending on the package configuration (SMPS or LDO), the hardware selects the regulator. The selection of the SMPS or LDO is exclusive.

The following figures present the power supply for the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Figure 7. STM32H5Ex/5Fx power-supply overview with LDO

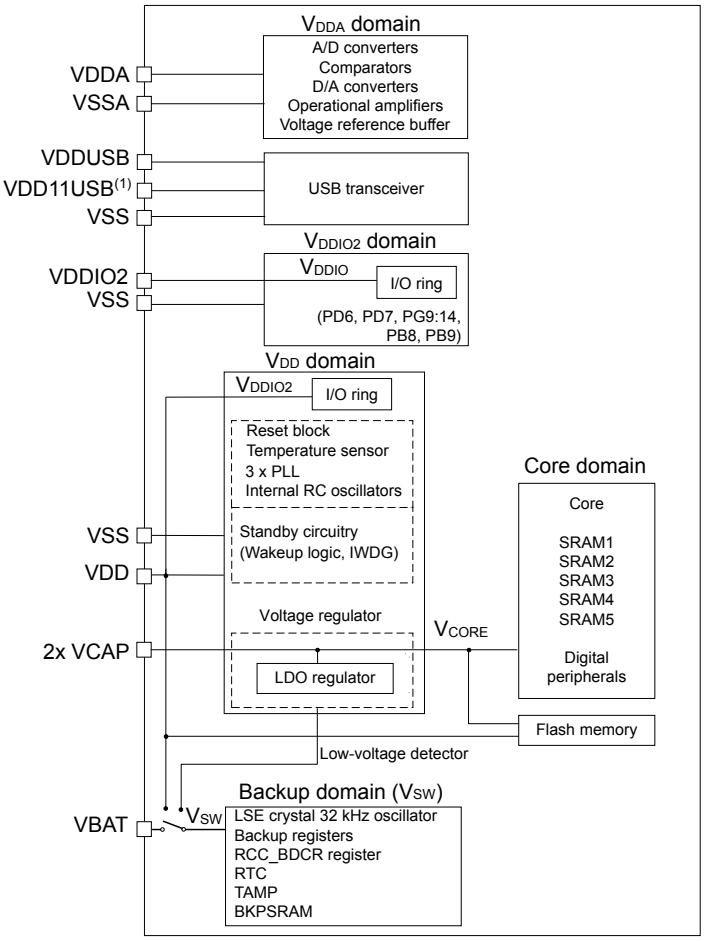


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Figure 8. STM32H5Ex/5Fx power-supply overview with SMPS

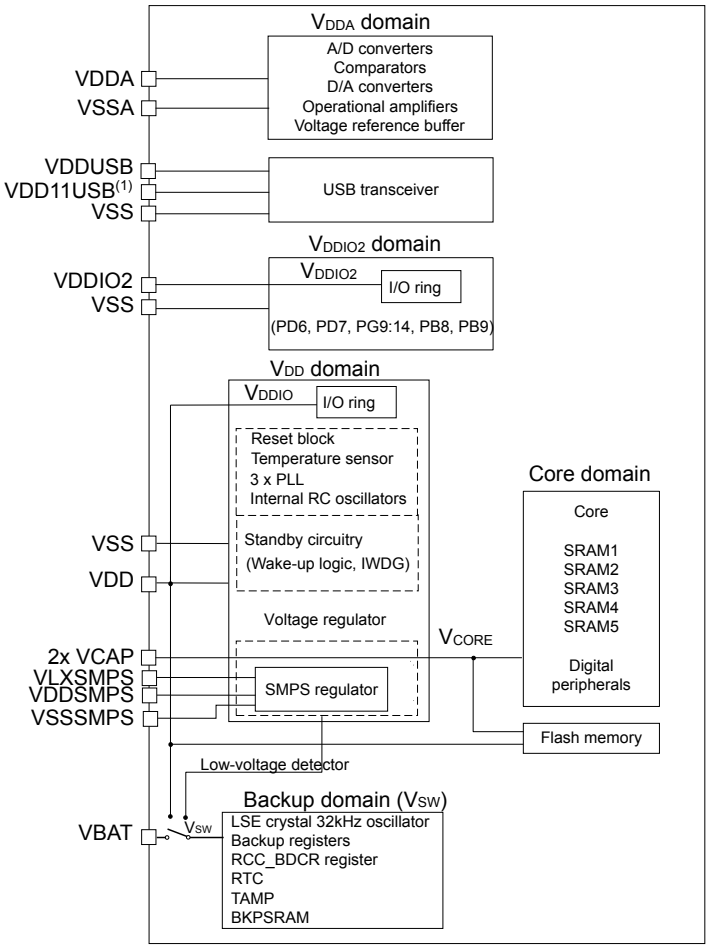

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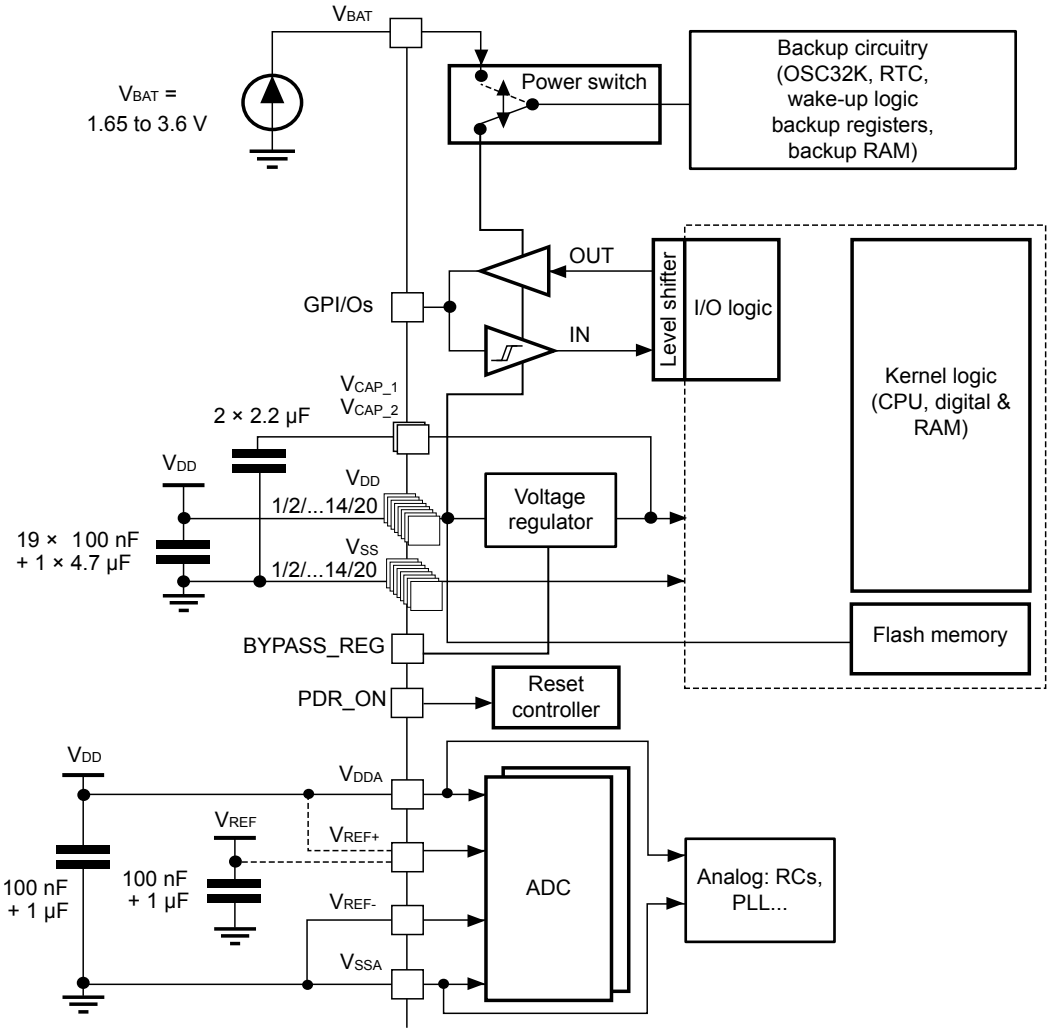
Figure 9. **Power supply overview of the STM32F427/437 and STM32F429/439 devices**



5.2.8 General-purpose I/Os (GPIO)

The STM32H5Ex/5Fx devices implement the same GPIO features as the STM32F427/437 and STM32F429/439 devices, but with main differences.

In the STM32H5Ex/5Fx devices, each GPIO port has a dedicated set of registers:

- Four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR, and GPIOx_PUPDR)
- Two 32-bit data registers (GPIOx_IDR and GPIOx_ODR)
- A 16-bit reset register (GPIOx_BRR)
- A 32-bit set/reset register (GPIOx_BSRR)

In addition, all the GPIOs have the following registers:

- A 32-bit locking register (GPIOx_LCKR)
- Two 32-bit alternate function selection registers (GPIOx_AFRH and GPIOx_AFRL)
- A secure configuration register (GPIOx_SECCFGR)
- A high-speed low-voltage register (GPIOx_HSLVR)

Each general-purpose I/O pin of the GPIO port in the STM32H5Ex/5Fx devices can be individually configured as secure through the GPIOx_SECCFGR register. After reset, all GPIO ports are secure.

All GPIO registers can be read and written through privileged and unprivileged access, whatever the security state: secure or nonsecure.

- Additional TrustZone® security support
  The TZEN option byte in the flash memory option byte register activates the TrustZone® security. When the TrustZone® is active (TZEN = 0xB4), each I/O pin of the GPIO port can be configured individually as secure through the GPIOx_SECCFGR register.
- I/O state retention during Standby mode
  In Standby mode, the I/Os in the STM32H5Ex/5Fx devices are in the floating state by default. If the IORETEN bit in the PWR_IORETR register is set, the I/Os state is sampled during Standby mode entry. The state of the I/Os is applied to the pin via pull-up and pull-down resistors. The pull-up and pull-down resistors remain applied after Standby wake-up until the software clears the IORETEN bit in the PWR_IORETR register.
- High-speed low-voltage mode (HSLV)
  Some I/Os can increase their maximum speed at a low voltage by configuring them to HSLV mode. The I/O HSLV bit controls whether the I/O output speed is optimized to operate at 3.3 V (default setting) or at 1.8 V (HSLV = 1).

For more information about the STM32H5Ex/5Fx GPIOs and TrustZone® security, refer to [2], *General-purpose I/Os (GPIO)* section and to [5] for a detailed description of the pinout and alternate function mapping.

5.2.9 Extended interrupt and event controller (EXTI)

5.2.9.1 *Main EXTI features in the STM32H5Ex/5Fx devices*

The extended interrupt and event controller (EXTI) manages the individual CPU and system wake-up through configurable event inputs. It provides wake-up requests to the power control. It also generates an interrupt request to the CPU NVIC, and events to the CPU event input. The CPU requires an additional event generation block (EVG) to generate the CPU event signal.

The STM32H5Ex/5Fx devices feature TrustZone® security and privileged/unprivileged mode selection. They do **not** feature direct event inputs.

EXTI security protection

When security is enabled for an input event, only secure access can modify and read the associated input event configuration and control bits. Nonsecure write access is discarded and read access returns 0.

EXTI privilege protection

When privilege is enabled for an input event, only privileged access can modify and read the associated input event configuration and control bits. Unprivileged write access is discarded and read access returns 0.

The table below describes the difference in EXTI features between the STM32F427/437 and STM32F429/439 devices, and the STM32H5Ex/5Fx devices.

Table 22. EXTI features

EXTI	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Features	Generation of up to 23 software event/interrupt requests	Supported features: • 67 input events • TrustZone® • Privileged/unprivileged modes

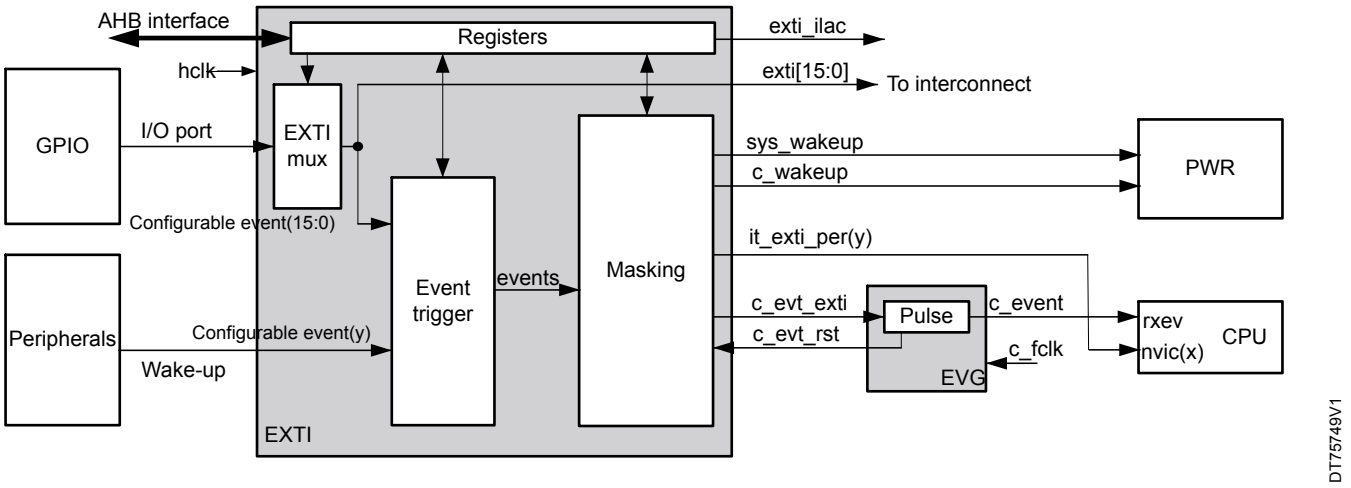
5.2.9.2 *Block diagram of the STM32H5Ex/5Fx EXTI*

As shown in the figure below, the EXTI consists of the following:

- A register block accessed via an AHB interface
- An event input trigger block
- A masking block, and an EXTI multiplexer (mux)

The register block contains all the EXTI registers. The event input trigger block provides an event input edge trigger logic.

Figure 10. **EXTI block diagram of the STM32H5Ex/5Fx**



The table below presents the EXTI line differences between STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Table 23. **EXTI line differences**

EXTI line	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
0-15	16 external interrupt lines	GPIO
16	PVD output	PVD/AVD output
17	RTC alarm event	RTC nonsecure
18	USB OTG FS wake-up event	RTC secure
19	Ethernet wake-up event	TAMP nonsecure
20	USB OTG HS (configured in FS) wake-up event	TAMP secure
21	RTC tamper and timestamp events	I2C1 wake-up
22	RTC wake-up event	I2C2 wake-up
23	N/A[(1)]	I2C3 wake-up
24		I3C wake-up
25		USART1 wake-up
26		USART2 wake-up
27		USART3 wake-up
28		UART4 wake-up
29		UART5 wake-up
30		USART6 wake-up
31		UART7 wake-up
32		UART8 wake-up
33		UART9 wake-up
34		USART10 wake-up
35		USART11 wake-up
36		UART12 wake-up
37		LPUART1 wake-up
38		LPTIM1

EXTI line	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
39	N/A[1]	LPTIM2
40		SPI1 wake-up
41		SPI2 wake-up
42		SPI3 wake-up
43		SPI4 wake-up
44		SPI5 wake-up
45		SPI6 wake-up
46		ETH wake-up
47		USB FS wake-up
48		USBPD1 wake-up
49		LPTIM2 CH1
50		DTS wake-up
51		HDMI-CEC wake-up
52		I2C4 wake-up
53		UVM output
54		LPTIM3
55		LPTIM4
56		LPTIM5
57		LPTIM6
58		COMP1 output
59		COMP2 output
60		OTGHS wake-up
61		I3C2 wake-up
62		ADF1
63		MDF1
64		Play_out14
65		IWDG
66		Vddio2 voltage monitor

1. *N/A stands for not applicable.*

5.2.10 CRC calculation unit

The table below presents the CRC differences between the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Table 24. CRC features

CRC	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Features	• Uses the CRC-32 (Ethernet) polynomial • Single input/output 32-bit data register • CRC computed in 4 AHB clock cycles (HCLK) for the 32-bit data size • General-purpose 8-bit register (can be used for temporary storage)	
	Handles the 32-bit data size	• Handles the 8-, 16-, and 32-bit data size, fully programmable polynomial with programmable size (7, 8, 16, 32 bits) • Programmable initial CRC value • Input buffer to avoid bus stalling during calculation • Reversibility option on I/O data • 32-bit word access only through the AHB slave peripheral. **Exception:** word access, right-aligned half-word access, and right-aligned byte access allowed for the CRC_DR register only.
CRC registers	CRC data register (CRC_DR) CRC independent data register (CRC_IDR) CRC control register (CRC_CR) CRC register map	
	-	Initial CRC value (CRC_INIT) CRC polynomial (CRC_POL)

5.3 Migrating the security peripherals

5.3.1 Random number generator (RNG)

The STM32H5Ex/5Fx, STM32F427/437, and STM32F429/439 devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit. The table below presents the RNG features of these devices.

Table 25. RNG features

RNG	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Features	• The RNG delivers 32-bit random numbers. • There are 40 periods of the RNG_CLK clock signal between two consecutive random numbers. • The RNG passed the FIPS PUB 140-2 tests with a success ratio of 99%. • The RNG entropy is monitored to flag abnormal behaviors.	• The RNG delivers 32-bit true random numbers. • It can be used as an entropy source to construct a nondeterministic random bit generator (NDRBG). • It was tested using the German BSI statistical tests of AIS-31 (T0 to T8). • It embeds startup and NIST SP800-90B-approved continuous health tests. • The AHB slave peripheral is accessible through 32-bit word single accesses only. • The RNG outputs an internal tamper event signal to the TAMP peripheral. • It can be enabled with an automatic low-power mode (default configuration).
	It can be disabled to reduce the power consumption.	

In the STM32H5Ex/5Fx devices, SAES and PKA use the RNG transparently.

When the RNG finds an unexpected error, an internal tamper event is triggered in the TAMP peripheral, and the RNG stops delivering random data. When this event occurs, the secure application needs to reset the RNG peripheral using either the central reset management or the global SoC reset. Then, a proper initialization of the RNG is required.

5.3.2 Hash processor (HASH)

The following table illustrates the differences in HASH features between the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Table 26. HASH features

HASH	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Features	• Secure HASH algorithm (SHA-1, SHA-224, and SHA-256) • MD5 (message-digest algorithm 5) hash algorithm • HMAC (keyed-hash message authentication code)	• Secure HASH algorithm (SHA-1, SHA-2, and SHA-3 families) • HMAC (keyed-hash message authentication code) algorithm
	• FIPS PUB 180-2 • Secure HASH standard specifications (SHA-1, SHA-224, and SHA-256) • IETF RFC 1321 (internet engineering task force request for comments number 1321) specifications (MD5)	• FIPS PUB 180-4 • Secure HASH standard (SHA-1, SHA-2, and SHA-3 families) • FIPS PUB 186-4, digital signature standard (DSS) • Internet engineering task force (IETF) request for comments RFC 2104
	Fast computation of SHA-1, SHA-224, and SHA-256, and MD5 (SHA-224 and SHA-256 are available on the STM32F43xxx only)	Fast computation of SHA-1, SHA2-224, SHA2-256, SHA2-384, SHA2-512, SHA3-224, SHA3-256, SHA3-384, and SHA3-512
	8× 32-bit words (H0 to H7) on the STM32F43xxx for the output message digest	50 × 32-bit words (HR0 to HR41) for output message digest and general purpose SHA-3 outputs
	32-bit data words for input data, supporting word, halfword, byte, and bit bit-string representations, with little-endian data representation only	A single 32-bit, write-only, input register associated with an internal input FIFO that can receive a single data block of size depending on the selected algorithm
	Automatic data flow control supporting direct memory access (DMA)	• Automatic data flow control supporting DMA • Support for both single and fixed DMA burst transfers of four words
	• AHB target peripheral • The corresponding 32-bit words of the digest from consecutive message blocks are added up to form the digest of the whole message. • Automatic padding to complete the input bit string	

5.3.3 On-the-fly decryption engine (OTFDEC)

The OTFDEC decrypts the encrypted content stored in the external OCTOSPI memories used in memory-mapped mode. The OTFDEC uses the AES-128 algorithm in counter mode (CTR).

The STM32H5Ex/5Fx devices embed one OTFDEC peripheral. The STM32F427/437 and STM32F429/439 devices do not support this peripheral.

5.3.4 Public key accelerator (PKA)

The STM32H5Ex/5Fx devices embed one PKA peripheral intended for the computation of cryptographic public key primitives within the Montgomery domain.

All needed computations are performed within the accelerator. No further hardware/software elaboration is needed to process the inputs or the outputs.

The STM32F427/437 and STM32F429/439 devices do not support a PKA peripheral.

5.3.5 AES and SAES hardware accelerators

The STM32H5Ex/5Fx devices embed two AES accelerators: a secure AES (SAES) and a faster AES. The SAES is a new feature in the STM32H5Ex/5Fx. The AES replaces the cryptographic processor (CRYP) that is available in the STM32F427/437 and STM32F429/439 devices.

In the STM32H5Ex/5Fx devices, the SAES with a hardware-unique key embeds protection against differential power analysis (DPA) and related side-channel attacks.

When an unexpected hardware fault occurs, an output tamper event is triggered, and the AES automatically clears the key registers. A reset is required for the AES to be usable again.

The AES peripheral can use the SAES peripheral as a security coprocessor. In this case, the secure application performs two actions:

- It prepares the key in the robust SAES peripheral.
- When they key is ready, the AES can load this prepared key through a dedicated hardware key bus.

5.3.6 Coupling and chaining bridge (CCB)

The STM32H5Ex/5Fx devices embed the Coupling and Chaining Bridge (CCB) that can be programmed to implement special coupling and chaining operations, required to protect private keys used in PKA protected operations.

These coupling and chaining operations involve the Public Key Accelerator (PKA), Secure AES (SAES), and the Random Number Generator (RNG).

5.3.7 Global TrustZone® controller (GTZC)

The security architecture of the STM32H5Ex/5Fx devices is based on the Arm® TrustZone® with the Armv8-M mainline extension.

Note: Arm and TrustZone are registered trademarks of Arm Limited (or its subsidiaries or affiliates) in the US and/or elsewhere.

The following components can be configured as trusted or untrusted:

- Each GPIO
- Each peripheral
- Each DMA channel
- Each clock configuration register
- Each DCACHE/ICACHE
- A small part of the flash memory or SRAM

The GTZC embedded in the STM32H5Ex/5Fx devices is used to configure secure TrustZone® and privileged attributes within the full system. Refer to [2] for a detailed description of the GTZC.

This controller is a new feature of the STM32H5Ex/5Fx devices and is not embedded in the STM32F427/437 and STM32F429/439 devices.

5.4 Migrating the communication peripherals

5.4.1 Serial peripheral interface (SPI)

This section highlights the SPI features implemented on the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Table 27. SPI features

SPI	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Instances	×6 SPIs	×6 SPIs
Speed	Up to 45 Mbit/s	Up to 50 Mbps
Features	SPI + I2S	
	2 SPIs muxed with full-duplex I2S	Including 3 SPIs multiplexed with full-duplex I2S

SPI	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Full-duplex synchronous transfer on three lines	X(1)	X
Half-duplex	X	X
Simplex synchronous transfer on two lines	With or without a bidirectional data line	With a unidirectional data line
Data size	Frame format selection: 8-bit or 16-bit	Data size selection: • From 4 bits up to 32 bits • Fixed to a multiple of 8 bits
Multimaster mode capability	X	X
Baud rate prescalers	8 baud rate prescalers in master mode ($f_{PCLK/2}$ max.)	Baud rate prescaler up to kernel frequency/2 or bypass from the RCC in master mode
Protection of configuration and settings	N/A(2)	X
Chip select (SS) management	NSS management through hardware or software for both master and slave: dynamic change of master/slave operations	Hardware or software management of SS for both master and slave
Configurable SS signal polarity and timing	N/A	Configurable SS signal polarity and timing, MISO x MOSI swap capability
Programmable transaction data	N/A	Programmable number of data items within a transaction to control SS and CRC
Programmable data order with MSB-first or LSB-first shifting	X	X
Programmable clock polarity and phase	X	X
Dedicated transmission and reception flags with interrupt capability	X	X
SPI Motorola and TI format support	X	X
Hardware CRC feature for reliable communications: • The CRC value can be transmitted as the last byte in Tx mode. • Automatic CRC error check for the last-received byte	X	X
Interrupt events and error detection with interrupt capability	Interrupts: • Transmit buffer empty flag • Receive buffer not empty flag • Master mode fault event • Overrun error • CRC error flag • TI frame format error	Interrupts: • Tx FIFO ready to be loaded • Data received in the Rx FIFO • Both TXP and RXP are active. • Transmission transfer filled. • Overrun error • Underrun error • TI frame format error • CRC error • Mode fault • End of transfer • Master mode suspended • Tx FIFO transmission complete All the interrupt events can wake up the system from Sleep mode at each instance.

SPI	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Configurable behavior at slave underrun condition	N/A	X (support of cascaded circular buffers)
FIFOs	N/A	Two 8-bit-multiple embedded Rx and Tx FIFOs (the FIFO size depends on the instance) Configurable FIFO thresholds (data packing)
RDY status pin	N/A	Optional status pin RDY signaling that the slave device is ready to handle the data flow

1. *X= supported*
2. *N/A stands for not applicable.*

5.4.2 Inter-integrated circuit (I2C)

The STM32H5Ex/5Fx devices implement the same I2C features as the STM32F427/437 and STM32F429/439 devices but with some enhancements. The table below provides the main differences.

Table 28. I2C differences

I2C	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Instances	×3 (I2C1, I2C2, I2C3)	×4 (I2C1, I2C2, I2C3, and I2C4)
Features	• 7-bit and 10-bit addressing mode • SMBus/PMBus • Standard mode (up to 100 kbit/s) • Fast mode (up to 400 kbit/s)	
	Single clock source	Fast-mode plus (up to 1 MHz) I2C bus Wake-up from Stop mode only (no autonomous mode) Independent clock

5.4.3 Improved inter-integrated circuit (I3C)

The STM32H5Ex/5Fx devices implement a new feature compared to the STM32F427/437 and STM32F429/439 devices, which is the I3C peripherals.

5.4.4 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32H5Ex/5Fx devices implement several new features on the U(S)ART compared to the STM32F427/437 and STM32F429/439 devices. The following table shows the U(S)ART differences.

Table 29. U(S)ART features

USART	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Instances	• 4 USARTs • 4 UARTs	• 6 USARTs • 6 UARTs • LPUART
Baud rate	Up to 4× 11.25 Mbit/s	Depends on the frequency (oversampling: by 16 or 8) (1)
Clock	Single clock domain	Dual clock domain and wake-up from low-power mode
Data	Word length: programmable (8 or 9 bits)	• Word length: programmable (7, 8, or 9 bits) • Programmable data order with MSB-first or LSB-first shifting
Interrupt	10 interrupt sources with flags	23 interrupt sources with flags
Other features	Hardware flow control (CTS/RTS)	• RS-232 hardware flow control • RS-485 hardware control mode

USART	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Other features	• LIN mode • IrDA SIR encoder block • Continuous communication using DMA • Multiprocessor communications • Single-wire half-duplex communication	
	N/A	• Modbus communication: timeout feature, CR/LF character recognition Two internal FIFOs for transmit and receive data Receiver timeout interrupt (except LPUART) Automatic baud rate detection (except LPUART) • Driver enable • Swappable Tx/Rx pin configuration • Wake-up from Stop mode
	• Smartcard mode: the software must implement it. • Number of stop bits: 0.5, 1, 1.5, and 2	• Smartcard mode: support the T=0 and T=1 asynchronous protocols • Number of stop bits: 0.5, 1, 1.5, and 2

1. *Refer to the USART section in [2].*

5.4.5 Serial audio interface (SAI)

The SAI offers a wide set of audio protocols due to its flexibility and wide range of configurations. It allows many stereo or mono audio applications to be targeted (such as the I2S standards: LSB- or MSB-justified; the PCM/DSP, TDM, and AC'97 protocols.)

Table 30. SAI features

SAI	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Instances	SAI1	SAI1 and SAI2
I2S, LSB or MSB-justified; PCM/DSP, TDM, or AC'97	Same features on all available instances	
Mute mode		
Stereo/mono audio frame capability		
16 slots with configurable size		
Data-size-configurable: 8-, 10-, 16-, 20-, 24-, or 32-bit		
FIFO size	8 words	
SPDIF	-(1)	X(2)
PDM	-	Available only on SAI1

1. *'-' = not supported.*
2. *X = supported*

5.4.6 Digital camera interface (DCMI)

The DCMI is available on the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

The DCMI main features are the following:

- 8-, 10-, 12-, or 14-bit parallel interface
- Embedded/external line and frame synchronization
- Continuous or snapshot mode
- Crop feature

Supported data formats:

- 8-, 10-, 12-, and 14-bit progressive video (either monochrome or raw Bayer)
- YCbCr 4:2:2 progressive video
- RGB 565 progressive video
- Compressed data JPEG

5.4.7 Parallel synchronous slave interface (PSSI)

The PSSI is only available on the STM32H5Ex/5Fx devices.

The DCMI and PSSI use the same circuitry. So, when they are both implemented on a device, they cannot be used at the same time. When the PSSI is used, the DCMI registers cannot be accessed, and vice versa. In addition, the PSSI and DCMI share the same alternate functions and interrupt vector.

The main features of the PSSI peripheral are listed below:

- Slave mode operation
- 8- or 16-bit parallel data input or output
- 8 words (32 bytes)
- Data enable (PSSI_DE) alternate function input and ready (PSSI_RDY) alternate function output.

5.4.8 Controller area network (CAN)

The table below presents the main differences related to CAN between the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices

Table 31. CAN features

CAN	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Instances	×2	×3 FDCAN
Features	• They support the CAN protocol version 2.0 A, B active. • Bit rates up to 1 Mbit/s • Tx: – 3 transmit mailboxes – Configurable transmit priority – Timestamp on SOF transmission • Rx: – 2 receive FIFOs with three stages – Scalable filter banks – Identifier list feature – Configurable FIFO overrun – Timestamp on SOF reception • They support the time-triggered communication option: – Disable automatic retransmission mode – 16-bit free running timer – Timestamp sent in the last two data bytes Management: • Maskable interrupts • Software-efficient mailbox mapping onto a unique address space Dual CAN: • CAN1: master bxCAN for managing the communication between a slave bxCAN and the 512-byte SRAM memory • CAN2: slave bxCAN, with no direct access to the SRAM	• They are compliant with the CAN protocol version 2.0-part A, B, and ISO 11898-1: 2015, -4 • CAN FD with maximum 64 data bytes supported • CAN error logging • AUTOSAR and J1939 support • Improved acceptance filtering • Two receive FIFOs of three payloads each (up to 64 bytes per payload) • Separate signaling on reception of high priority messages • Configurable transmit FIFO/queue of three payloads (up to 64 bytes per payload) • Transmit event FIFO • Programmable loopback test mode • Maskable module interrupts • Two clock domains: APB bus interface and CAN core kernel clock • Power-down support

5.4.9 Universal serial bus interface (USB)

The STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices have different USB peripherals:

- The STM32F427/437, STM32F429/439 devices implement an USB FS only instead of an USB OTG FS.
- The STM32H5Ex/5Fx devices implement an OTG FS, OTG HS, and USB Type-C® connector/USB power delivery interface (UCPD).

The STM32H5Ex/5Fx devices support most of the features supported by the STM32F427/437 and STM32F429/439 devices.

The table below lists the main differences in USB between the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Table 32. USB differences

USB	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
General	Full support for USB on-the-go (USB OTG FS)	Full support for USB on-the-go (OTG FS and OTG HS)
	FS mode: • One bidirectional control endpoint • 3 IN endpoints (bulk, interrupt, isochronous) • 3 OUT endpoints (bulk, interrupt, isochronous) **HS mode:** • 6 bidirectional endpoints (including EP0) • 12 host mode channels	**FS mode:** • One bidirectional control endpoint • 5 IN endpoints (bulk, interrupt, isochronous) • 5 OUT endpoints (bulk, interrupt, isochronous) **HS mode:** • 1 bidirectional endpoint (including EP0) • 8 IN endpoints (bulk, interrupt, isochronous) • 8 OUT endpoints (bulk, interrupt, isochronous) • 16 host mode channels
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D + (USB_DP) line	USB connect/disconnect capability (controllable embedded pull-up resistor on the USB_DP line)
	N/A(1)	Battery charging detection (BCD) support for device
		Independent V_{DDUSB} power supply
Buffer memory	**FS mode:** • 1.25-Kbyte data FIFOs • Management of up to 4 Tx FIFOs (one for each IN endpoint) + one Rx FIFO **HS mode:** • 4 Kbytes of total RAM	**FS mode:** • 1.25-Kbyte data FIFOs • Management of up to 6 Tx FIFOs (one for each IN end point) + shared Rx FIFO • 1.2 Kbytes of total RAM **HS mode:** • 1.25-Kbyte data FIFOs • Management of up to 9 Tx FIFOs (one for each IN end point) + shared Rx FIFO • 4 Kbytes of total RAM
Low-power modes	**FS mode:** • USB suspend and resume **HS mode:** • No LPM supported	USB revision 2.0 including link power management (LPM) support

1. *N/A stands for not applicable.*

5.5 Migrating the analog peripherals

5.5.1 Analog-to-digital converter (ADC)

The STM32F427/437 and STM32F429/439 devices embed three ADCs: ADC1, ADC2, and ADC3 (12-bit resolution.)

The STM32H5Ex/5Fx devices embed three ADCs:

- ADC1 and ADC2 are tightly coupled and can operate in dual mode (ADC1 is the master)
- ADC3 is controlled independently

Table 33. ADC differences between devices

ADC	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Instances	×3	×3
Resolution	12-bit	
Number of channels	16/24	30/30
Configurable resolution	12-bit, 10-bit, 8-bit, or 6-bit	
Maximum sampling speed	2.4 MSPS 7.2 MSPS in triple interleaved mode	5 MSPS
Conversion modes	• Single • Continuous • Scan • Discontinuous • Dual mode	
DMA support	Yes	
Data register	16-bit data register	
Analog watchdog feature	This feature allows the application to detect if the input voltage exceeds the user-defined upper or lower thresholds.	
ADC input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$	$V_{SSA} \leq V_{IN} \leq V_{REF+}$
New features	N/A(1)	• ADC conversion time independent of the AHB bus clock frequency • Single-ended or differential input management • Low-power features • Three analog watchdogs per ADC • Self-calibration • Oversampling ratio adjustable from 2 to 256 • Programmable data shift up to 8 bits • Parallel data output to ADF/MDF

1. *N/A stands for not applicable.*

5.5.2 Digital-to-analog converter (DAC)

The STM32H5Ex/5Fx devices implement some enhanced DAC compared to the STM32F427/437 and STM32F429/439 devices. Refer to the table below for the main DAC differences between them.

Table 34. DAC differences

DAC	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Instances	×2 with one output channel each	×1 with a maximum of two output channels
Resolution	12 bits	
Output buffer	Yes	
Dual DAC channel	For independent or simultaneous conversions	
New features	N/A(1)	• Double-data DMA • Buffer offset calibration • Sample and hold modes for low-power operation in Stop mode

1. *N/A stands for not applicable.*

5.6 Migrating the timer peripherals

The STM32H5Ex/5Fx, STM32F427/437, and STM32F429/439 devices include the following timers:

- Two advanced-control timers
- Up to 10 general-purpose timers
- Two basic timers
- Two watchdog timers
- Two SysTick timers (one for the STM32F427/437 and STM32F429/439 devices)

Furthermore, the STM32H5Ex/5Fx devices include six low-power timers.

The following subsections compare the features of the above listed timers and the RTC in the STM32H5Ex/5Fx, STM32F427/437, and STM32F429/439 devices.

5.6.1 Advanced-control timers (TIM1/TIM8)

The STM32H5Ex/5Fx, STM32F427/437, and STM32F429/439 devices include two advanced-control timers, TIM1 and TIM8, with almost identical features detailed in the table below.

Table 35. Advanced-control timer (TIM1/8) features

Feature	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Counter resolution and type	16-bit up, down, or up/down autoreload counter	
Prescaler factor	16-bit programmable prescaler, which allows the counter clock frequency to be divided (also “on the fly”) by any factor between 1 and 65536	
Channels	Up to four independent channels for: • Input capture • Output compare • PWM generation (edge and center-aligned mode) • One-pulse mode output	Up to six independent channels for: • Input capture (channels 5 and 6) • Output compare • PWM generation (edge and center-aligned mode) • One-pulse mode output
Complementary outputs	Complementary outputs with programmable dead time	
Synchronization with external signals and general-purpose timers	• The synchronization circuit controls the timer with the external signals and interconnects several timers together. • The advanced-control (TIM1/TIM8) and general-purpose (TIMy) timers are completely independent, and do not share any resources.	
Repetition counter	Repetition counter to update the timer registers only after a given number of cycles of the counter	
Break inputs	One break input to put the timer output signals in the reset state or in a known state	Two break inputs to put the timer output signals in the reset state or in a known state
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow and counter initialization (through the software or an internal/external trigger) • Trigger event (counter start, stop, initialization, or count through an internal/external trigger) • Input capture • Output compare	
Encoders and sensors	Supports incremental (quadrature) encoders and hall-sensor circuitries for positioning purposes	
Trigger input	Trigger input for external clock or cycle-by-cycle current management	
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM, and complementary PWM with dead-time insertion)	

5.6.2 General-purpose timers with up, down, up-down autoreload counter (TIM2/3/4/5)

The general-purpose timers consist of a 16-bit or 32-bit autoreload counter driven by a programmable prescaler.

The STM32H5Ex/5Fx, STM32F427/437, and STM32F429/439 devices include general-purpose timers with an up, down, or up/down autoreload counter (TIM2, TIM3, TIM4, and TIM5). These timers have identical features.

Table 36. General-purpose timer (TIM2/3/4/5) features

Feature	STM32H5Ex/5Fx, STM32F427/437, and STM32F429/439
32-bit resolution	TIM2 and TIM5
16-bit resolution	TIM3 and TIM4
Counter resolution and type	16-bit or 32-bit up, down, or up/down autoreload counter
Prescaler factor	16-bit programmable prescaler used to divide the counter clock frequency (also “on the fly”) by any factor between 1 and 65535
Channels	Up to four independent channels for: • Input capture • Output compare • PWM generation (edge- and center-aligned modes) • One-pulse mode output
Synchronization with external signals and other timers	Synchronization circuit to control the timer with external signals and to interconnect several timers
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow and counter initialization (through software or internal/external trigger) • Trigger event (counter start, stop, initialization, or count through internal/external trigger) • Input capture • Output compare
Encoders and sensors	Supports incremental (quadrature) encoders and hall-sensor circuitries for positioning purposes
Trigger input	Trigger input for external clock or cycle-by-cycle current management
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare and PWM)

5.6.3 General-purpose timers with autoreload upcounter

The STM32H5Ex/5Fx, STM32F427/437, and STM32F429/439 devices include 16-bit resolution general-purpose timers with a 16-bit autoreload upcounter:

- TIM12/TIM13/TIM14 and TIM15/TIM16/TIM17 for the STM32H5Ex/5Fx devices
- TIM9 to TIM14 for the STM32F427/437 and STM32F429/439 devices

Table 37. General-purpose timer (with autoreload upcounter) features

Feature	STM32F427/437 and STM32F429/439		STM32H5Ex/5Fx			
16-bit resolution	TIM10/TIM11 and TIM13/TIM14	TIM9/TIM12	TIM12	TIM13/14	TIM15	TIM16/TIM17
Counter resolution and type	16-bit autoreload upcounter					
Prescaler factor	16-bit programmable prescaler used to divide the counter clock frequency by any factor between 1 and 65535					
Channels	Independent channel for:	Up to two independent channels for:		Independent channel for:	Up to two independent channels for:	One channel for:
	• Input capture • Output compare • PWM generation (edge-aligned mode) • One-pulse mode output					
Complementary outputs	N/A(1)				Complementary outputs with programmable dead time (for channel 1 only)	Complementary outputs with programmable dead time
Break input	N/A				Break input to put the timer output signals in the reset state or a known state	
Synchronization with external circuits and other timers	N/A	Synchronization circuit to control the timer with external signals and to interconnect several timers together		N/A	Synchronization circuit to control the timer with external signals and to interconnect several timers together	N/A
Repetition counter	N/A				Repetition counter to update the timer registers only after a given number of cycles of the counter	
Interrupt generation	Interrupt generation on the following events:				Interrupt/DMA generation on the following events:	

Feature	STM32F427/437 and STM32F429/439		STM32H5Ex/5Fx			
Interrupt generation	• Update: counter overflow and counter initialization (through software) • Input capture • Output compare	• Update: counter overflow and counter initialization (through software or internal trigger) • Trigger event (counter start, stop, initialization, or count through internal trigger) • Input capture • Output compare	• Update: counter overflow and counter initialization (through software or internal trigger) • Trigger event (counter start, stop, initialization, or count through internal trigger) • Input capture • Output compare	• Update: counter overflow • Input capture • Output compare	• Update: counter overflow and counter initialization (through software or internal/ external trigger) • Trigger event (counter start, stop, initialization, or count through internal/external trigger) • Input capture • Output compare • Break input (interrupt request)	• Update: counter overflow • Input capture • Output compare • Break input
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare and PWM)					

1. *N/A stands for not applicable.*

5.6.4 Basic timers (TIM6/7)

The basic timers TIM6 and TIM7 consist of a 16-bit autoreload counter driven by a programmable prescaler.

These timers are completely independent, and do not share any resources.

The STM32H5Ex/5Fx, STM32F427/437, and STM32F429/439 devices have basic timers with identical features.

Table 38. Basic timers

Feature	STM32H5Ex/5Fx, STM32F427/437, and STM32F429/439
Counter resolution and type	16-bit autoreload upcounter
Prescaler factor	16-bit programmable prescaler used to divide the counter clock frequency (also “on the fly”) by any factor between 1 and 65535
Synchronization signals	Synchronization circuit to trigger the DAC
Interrupt/DMA generation	Interrupt/DMA generation on the update event: counter overflow

5.6.5 Low-power timers (LPTIM1/2/3/4/5/6)

The LPTIM is a 16-bit timer that benefits from the ultimate developments in power-consumption reduction. This is a new feature in the STM32H5Ex/5Fx devices that is not available in the STM32F427/437 and STM32F429/439 devices. The table below describes the LPTIM features in the STM32H5Ex/5Fx devices.

Table 39. LPTIM features

Feature	STM32H5Ex/5Fx
LPTIMx	LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5, and LPTIM6
Counter resolution and type	16-bit upcounter
Prescaler factor	3-bit prescaler with 8 possible dividing factors (1, 2, 4, 8, 16, 32, 64, and 128)
Selectable clock	• Internal clock sources: configurable internal clock source (see Section 5.2.6: Reset and clock control (RCC)) • External clock source over the LPTIM input (working with no LP oscillator running, used by the pulse counter application)
Autoreload	16-bit ARR auto reload register
Capture/compare	16-bit capture/compare register
Continuous mode	Continuous/one-shot mode
Trigger mode	Selectable software/hardware input trigger
Glitch filter	Programmable digital glitch filter
Configurable output	Configurable output: pulse or PWM
Polarity	Configurable I/O polarity
Encoder mode	Yes
Repetition counter	Yes
Input capture, PWM, and one-pulse channels	Up to two independent channels for: • Input capture • PWM generation (edge-aligned mode) • One-pulse mode output
DMA requests	DMA request generation on the following events: • Update event • Input capture

5.6.6 Watchdogs (WWDG/IWDG)

The STM32H5Ex/5Fx, STM32F427/437, and STM32F429/439 devices embed two watchdogs:

- A system window watchdog (WWDG) with the same features
- An independent watchdog (IWDG) with the same differences

Table 40. IDWG features

Feature	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Clock	Clocked from an independent RC oscillator	• Independent clock • LSI used as the IWDG kernel clock (iwdg_ker_ck)
Window option	-(1)	X(2)
Early wake-up interrupt generation	-	X
Reset generation	X	

1. *"-" = not supported*
2. *X = supported*

5.6.7 Real-time clock (RTC)

The following table describes the difference in RTC features between the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices. For more information about the RTC, refer to the RTC section in the product reference manual ([1] or [2]).

Table 41. RTC features

RTC	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Feature	Calendar with subseconds, seconds, minutes, hours (12 or 24 format), weekday, date, month, and year	
	Two programmable alarms	
	Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision	
	Timestamp function	
	Daylight saving time	
	Automatic wake-up	
	Digital calibration circuit with 0.95 ppm resolution	
	Alarm A, alarm B, wake-up interrupt, timestamp, and tamper detection	Alarm A, alarm B, wake-up timer, and timestamp individual privilege protection
	N/A(1)	• Binary mode with a 32-bit free-running counter • On-the-fly correction from 1 to 32767 RTC clock pulses • RTC TrustZone® support
Tamper and backup registers	• 20× 32-bit backup registers • 2× tamper pins/2 events • Edge or level detection with configurable filtering	• 32× 32-bit backup registers • Up to 11 tamper pins for 8 external tamper detection events • 13 internal tamper events • TrustZone® support

1. *N/A stands for not applicable.*

5.6.8 SysTick timer

The SysTick timer is dedicated to real-time operating systems but can also be used as a standard down-counter.

The STM32H5Ex/5Fx Cortex®-M33 with TrustZone® embeds two SysTick timers.

When TrustZone® is activated, the two SysTick timers are available:

- SysTick, secure instance
- SysTick, nonsecure instance

But when TrustZone® is disabled, only one SysTick timer is available.

The STM32F427/437 and STM32F429/439 devices embed a Cortex®-M4 with just one SysTick timer.

5.7 Migrating external memory interface peripherals

5.7.1 Flexible memory controller (FMC)

The following table presents the FMC interface differences between the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Table 42. FMC features

FMC		STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
External memory interfaces		• SRAM • NOR flash memory/one NAND flash memory • PSRAM • 16-bit PC card-compatible devices • Two banks of NAND flash memory with ECC hardware to check up to 8 Kbytes of data	• SRAM • NOR flash memory/one NAND flash memory • PSRAM • Ferroelectric RAM (FRAM) • NAND flash memory with ECC • Hardware to check up to 8 Kbytes of data
Data bus width		8, 16, or 32-bit	8- or 16-, or 32-bit
FMC bank memory mapping	Bank 1 4× 64-Mbyte	NOR/PSRAM/SRAM	NOR/PSRAM/SRAM
	Bank 2 4× 64-Mbyte	NAND flash memory	Not used
	Bank 3 4× 64-Mbyte		NAND flash memory
	Bank 4 4× 64-Mbyte	PC card	Not used
	SDRAM Bank 1 4× 64-Mbyte	SDRAM	SDRAM
	SDRAM Bank 2 4× 64 Mbyte		

For the STM32H5Ex/5Fx devices, the FMC registers can be configured as secure through the TZSC controller (refer to [2] for more details.)

5.7.2 Octo-SPI interface (OCTOSPI)

The OCTOSPI peripheral provides a serial interface that enables communication with external serial memories such as flash memory, PSRAM, HyperRAM™, and HyperFlash™.

The specialized octo-SPI communication interface targets single-, dual-, quad-, or octo-SPI memories. It can be configured into three modes: indirect, status-polling, and memory-mapped.

The OCTOSPI peripheral is available on the STM32H5Ex/5Fx devices, with the following features:

- Functional modes: indirect, automatic status-polling, and memory-mapped
- Read and write support in memory-mapped mode
- Dual-quad configuration
- SDR (single-data rate) and DTR (double-transfer rate)
- Data strobe (DS and DQS)
- GPDMA interface
- 8-, 16-, and 32-bit data access allowed
- Integrated FIFO for reception and transmission
- Possibility to disable the automatic prefetch
- OCTOSPIM: the extended-SPI I/O manager is a low-level interface that enables an efficient OCTOSPI pin assignment with a full I/O matrix

Note: The STM32F427/437 and STM32F429/439 devices do not support the OCTOSPI interface.

5.8 Migrating graphic peripherals

5.8.1 Graphic timer (GFXTIM)

The graphic timer (GFXTIM) is available only in the STM32H5Ex/5Fx devices. It is a graphic-oriented timer, which allows the smart management of graphical events for frame or line counting.

The GFXTIM supports:

- Integrated frame and line clock generation
- One absolute frame counter with one compare channel
- Two autoreload relative frame counters
- One line timer with two compare channels
- External tearing-effect line management and synchronization
- Four programmable event generators with external trigger generation
- One watchdog counter

5.8.2 LCD-TFT display controller (LTDC)

The LTDC peripheral is available in the STM32H5Ex/5Fx, STM32F427/437, and STM32F429/439 devices. To interface directly to a variety of LCD and TFT panels, it provides the following:

- Parallel digital RGB (red, green, blue) signals for horizontal and vertical synchronization
- A pixel clock
- A data enable output

The LTDC supports the following:

- A 24-bit RGB parallel pixel output
- Two display layers with a dedicated FIFO (64x32-bit)
- A color lookup table (CLUT) with up to 256 color (256x24-bit) per layer

5.8.3 Chrom-ART Accelerator (DMA2D)

The Chrom-ART Accelerator (DMA2D) is a graphic-dedicated peripheral, which allows image manipulation without using the CPU. The DMA2D is a hardware accelerator for graphical operations (such as plane blending, pixel format conversions, or antialiasing fonts with specific modes.) The DMA2D is built around a graphic 2D DMA for fast data copy operations.

The following table presents the DMA2D interface differences between the STM32F427/437, STM32F429/439, and STM32H5Ex/5Fx devices.

Table 43. DMA2D features

Feature	STM32F427/437 and STM32F429/439	STM32H5Ex/5Fx
Bus architecture	Single AHB master	Single AHB master
Color formats	Up to 11 color formats from 4 bits up to 32 bits per pixel	Up to 11 color formats from 1 bit up to 32 bits per pixel
Operating modes	4 operating modes: • Register-to-memory • Memory-to-memory • Memory-to-memory with pixel format conversion • Memory-to-memory with pixel format conversion and blending	6 operating modes: • Register-to-memory • Memory-to-memory • Memory-to-memory with pixel format conversion • Memory-to-memory with pixel format conversion and blending • Memory-to-memory with pixel format conversion, blending, and fixed color foreground • Memory-to-memory with pixel format conversion, blending, and fixed color background

5.8.4 JPEG CODEC

The JPEG CODEC peripheral is available only in the STM32H5Ex/5Fx devices.

The hardware 8-bit JPEG CODEC encodes uncompressed image data streams and decodes JPEG-compressed image data streams. It also fully manages JPEG headers. The main JPEG CODEC features are:

- High-speed fully synchronous operation
- Configurable as an encoder or decoder
- Single-clock-per-pixel encoding/decoding
- Support for RGB, YCbCr, YCMK, and BW (gray scale) image color space
- 8-bit depth per image component for encoding/decoding
- JPEG header generator/parser with enable/disable function
- Four programmable quantization tables
- Single-clock Huffman coding and decoding
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit
- Interface with concurrent input and output data streams

5.9 Migrating signal/image processing accelerators

5.9.1 Digital filters

The STM32H5Ex/5Fx devices embed two hardware digital filters:

- Multifunction digital filter (MDF)
- Audio digital filter (ADF)

These filters are not available in the STM32F429/439 and STM32H5Ex/5Fx devices. The table below shows the differences between the embedded filters.

Table 44. Digital filters in the STM32H5Ex/5Fx devices

Features	STM32H5Ex/5Fx	
Digital filter type	ADF	MDF
Number of filters	1	6
Number of trigger inputs	N/A	14
Sound activity detection (SAD)	Yes	No
Rx FIFO depth (number of 24-bit words)	4	4
Input from the internal ADC	ADC3	ADC1/ADC2

5.9.2 CORDIC coprocessor

The CORDIC coprocessor is a new peripheral embedded only in the STM32H5Ex/5Fx devices. It provides hardware acceleration of certain mathematical functions (mainly trigonometric ones) commonly used in motor control, metering, signal processing, and many other applications.

The CORDIC speeds up the calculation of these functions compared to a software implementation, making it possible to use a lower operating frequency, or to free up processor cycles to perform other tasks.

The main CORDIC features are the following:

- 24-bit CORDIC rotation engine
- Circular and hyperbolic modes
- Rotation and vectoring modes
- Functions: sine, cosine, sinh, cosh, atan, atan2, atanh, modulus, square root, and natural logarithm
- Programmable precision
- Low-latency AHB slave interface
- Results readable as soon as ready, without polling or interrupt
- DMA read and write channels
- Multiple register read/write operations through DMA

5.9.3 Filter math accelerator (FMAC)

The FMAC is only implemented in the STM32H5Ex/5Fx devices. This peripheral performs arithmetic operations on vectors. It comprises a multiplier/accumulator (MAC) unit and an address generation logic that allows the FMAC to index vector elements stored in local memory.

The main FMAC features are the following:

- 16 × 16-bit multiplier
- 24 + 2-bit accumulator with addition and subtraction
- 16-bit input and output data
- 256 × 16-bit local memory
- Up to three areas in memory for data buffers (two inputs, one output) definable by programmable base address pointers and associated size registers.
- Circular input and output buffer
- Filter functions: FIR, IIR (direct form 1)
- Vector functions: dot product, convolution, and correlation
- AHB slave interface
- DMA read and write data channels

Revision history

Table 45. **Document revision history**

Date	Revision	Changes
18-Feb-2026	1	Initial release.

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