How to optimize power consumption on STM32U3 MCUs

Introduction

The STM32U3 series microcontrollers (MCUs) are based on the high-performance Arm® 32-bit Cortex®-M33 CPU with Arm® TrustZone® and FPU. These MCUs use an innovative architecture to reach best-in-class, ultra-low-power figures owing to their high flexibility and advanced set of peripherals. They outperform the competition in the ultra-low-power world by providing the best energy efficiency for applications.

The STM32U3 series are the first STM32 series based on near-threshold voltage technology to deliver breakthrough improvement in battery life. With near-threshold technology, the STM32U3 series devices reduce the active consumption down to 10 µA/MHz, resulting in far longer battery life for any application.

With the integration of the ART Accelerator 8-Kbyte instruction cache, the STM32U3 series MCUs can operate at frequencies up to 96 MHz and achieve 144 DMIPS performance, while maintaining extremely low dynamic power consumption and best-in-class low-power modes.

This application note provides qualitative and quantitative information to be able to configure different parameters, such as frequency, range, and low-power mode, before starting the implementation and optimization. All computations are performed with typical data from the product datasheet and at ambient temperature, unless otherwise specified.

This application note uses the industry-standard ULPMark™ benchmark from EEMBC® as a reference case to correlate the computations and simulations with the measurements.

1 General information

This application note applies to the STM32U3 series microcontrollers that are Arm® Cortex® core-based devices.

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Reference documents

[1] *STM32U3 series Arm®-based 32-bit MCUs*, reference manual (RM0487)

[2] *STM32U3 series* datasheets

[3] *STM32U3 series* erratasheets

[4] *STM32 microcontroller GPIO configuration for hardware settings and low-power consumption*, application note (AN4899)

[5] EEMBC® documentation on www.eembc.org

2 Energy efficiency processing

The high processing performance in Run mode (expressed in DMIPS/MHz) is achieved by using a Cortex®-M33 core associated with the interfaces of its memories. To ensure full performance operation at maximum operating frequency, the STM32U3 series devices embed the ART accelerator instruction cache (ICACHE), which masks the flash memory access wait state. The processing performance can then achieve 1.5 DMIPS/MHz, regardless of the system clock frequency.

The consumption is even lower on STM32U3 series thanks to the adaptive voltage scaling (AVS) technique. The V_{CORE} is tuned individually on each device to achieve the target frequency of every voltage range and have the lowest consumption at the same time

All consumption data used in this application note are based on typical specifications extracted from device datasheets at T_A = 25°C and V_{DD} = 3.0 V, unless otherwise specified.

2.1 Internal regulator efficiency

The STM32U3 series devices embed two internal regulators depending on the application's performance and consumption requirements:

- A step-down SMPS, which provides superior efficiency, especially at higher V_{DD} levels.
- A linear regulator (LDO), which offers simpler behavior but higher consumption.

Each regulator supports two operating modes:

- Main regulator mode, used during performance-oriented operation
- Low-power regulator mode, used to minimize consumption

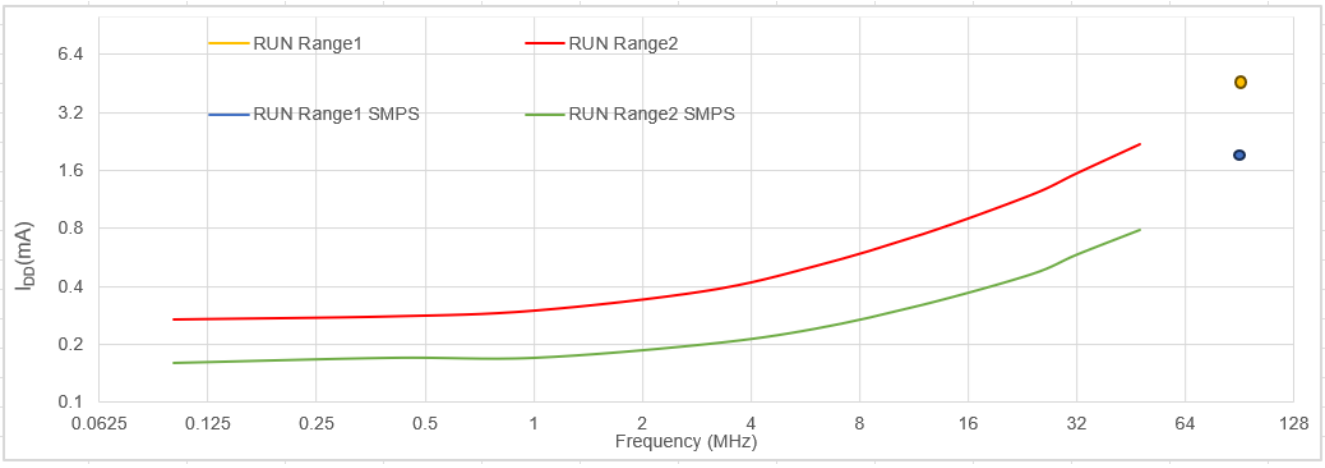
Both regulators can be used in all voltage scaling ranges, and can operate in all Stop modes.

Table 1. Power distribution of the internal regulators

Voltage regulator mode	Device mode
Main regulator (Range 1, 2)	Run, Sleep, Stop 0
Low-power regulator (SMPS or LDO)	Stop 1, Stop 2, Stop 3, (Standby with 8-Kbyte or full SRAM2)

Figure 1 shows the typical current consumption of an STM32U375/385 microcontroller in Run mode, as a function of system frequency, for both SMPS and LDO configurations with F_{HCLK} = F_{HSE} bypass mode, all peripherals disabled, flash memory Bank 2 in power down, and all SRAMs enabled.

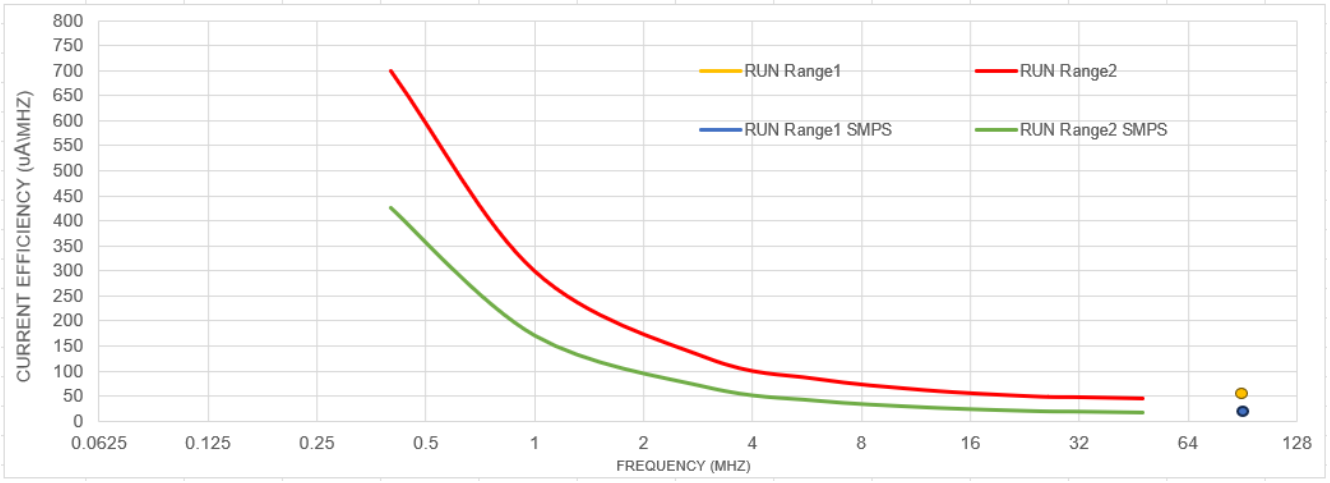
Figure 1. Current consumption for STM32U375/385 in Run mode with ICACHE ON, 1-way, prefetch ON, SMPS versus LDO



The lowest power consumption is achieved when running from the internal flash memory with cache 1-way. The instruction cache tends to reduce the number of accesses to the memory, thus reducing the overall current consumption. The current consumption from the internal SRAM is similar to the flash memory when the ICACHE is used.

Figure 2 shows the same curve translated into power efficiency by dividing the current consumption (µA) by the CPU frequency.

Figure 2. Power efficiency for STM32U375/385 with ICACHE ON, 1-way, prefetch ON, SMPS versus LDO



Using the SMPS improves power efficiency by up to 65 %, depending on the frequency. Its flatter µA/MHz profile demonstrates more stable and efficient operation across the entire clock-frequency range.

2.2 Dynamic voltage scaling management

The STM32U3 series devices support dynamic voltage scaling, which is a power management technique that allows the voltage (V_{CORE}) and frequency to be dynamically adjusted based on processing requirements to optimize power consumption.

Dynamic voltage scaling to increase V_{CORE} is known as overvolting. It allows the device to improve its performance. It is performed to save power, particularly in laptops and other mobile devices where the energy comes from a battery and is thus limited.

The regulator operates in the following ranges:

- Range 1: high performance. It provides a typical output voltage of 0.9 V. It is used when the system clock frequency is up to 96 MHz.
- Range 2: low-power range. It provides a typical output voltage of 0.75 V. The system clock frequency can be up to 48 MHz.

The EPOD (embedded power distribution) must be enabled above 24 MHz in both ranges to ensure proper regulation margins (refer to document [1] for sequences to switch between voltage scaling ranges).

Table 2. Bus maximum frequency

Product voltage range		AHB1/AHB2/APB1/APB2/APB3
Range 1	EPOD booster enabled	96 MHz
	EPOD booster disabled	24 MHz
Range 2	EPOD booster enabled	48 MHz
	EPOD booster disabled	24 MHz

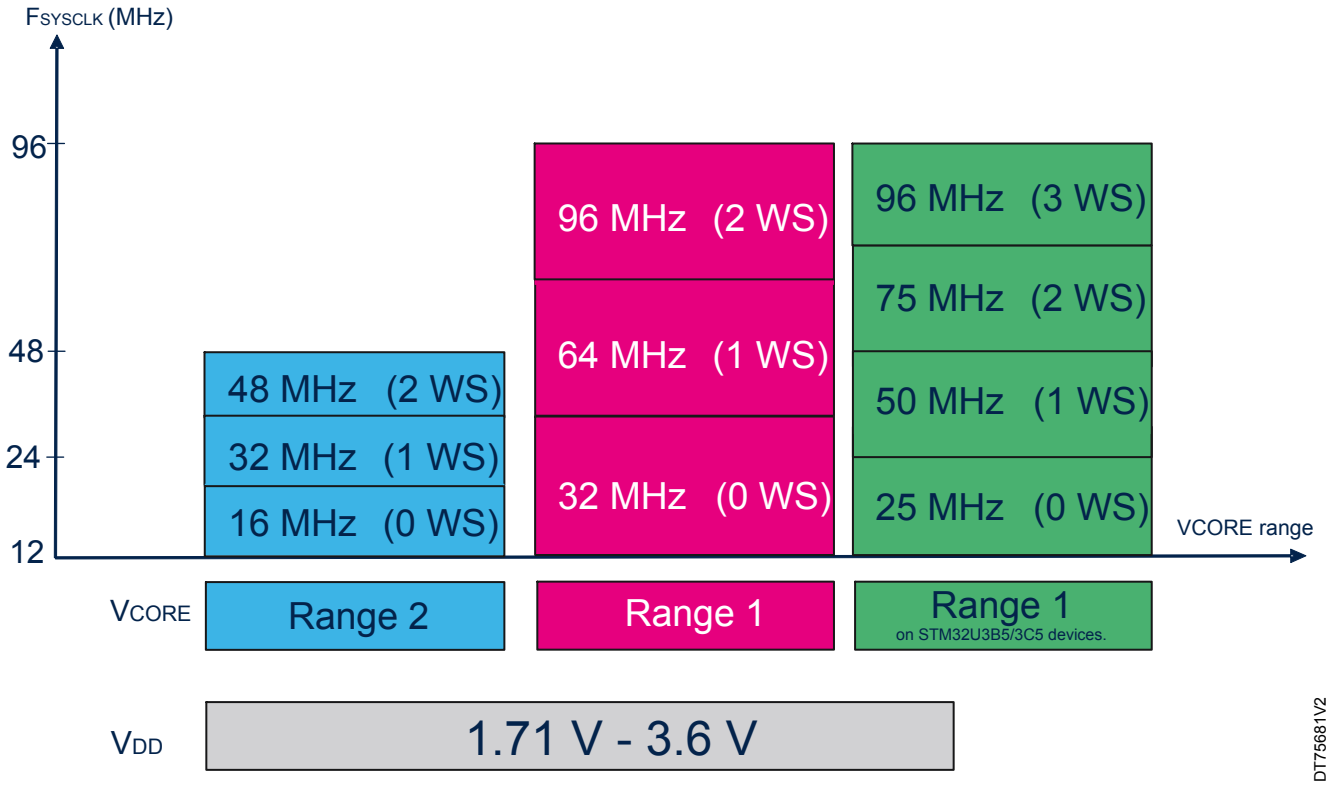
Reducing Run-mode power consumption therefore requires aligning VCORE scaling with the application's processing needs rather than keeping the device at its highest performance level.

2.3 Flash memory and ICACHE efficiency

2.3.1 Flash memory efficiency

Figure 3 shows the flash memory latency (number of wait states to be programmed in the flash memory access control register), depending on the STM32U3 series regulator voltage scaling range and system clock frequency.

Figure 3. Flash memory latency versus V_{CORE} range (V_{DD} = 1.71 to 3.6 V, LPM = 0)



The flash memory supports a low-power read mode (LPM). The number of wait states (WS) depends on the LPM value:

- Up to 3 WS when LPM = 0 (depending on the supply voltage and the frequency)
- Up to 4 WS when LPM = 1 (depending on the supply voltage and the frequency)

Table 3. Current consumption for STM32U375/385 in Run mode versus LPM

Symbol	Conditions	Current consumption (mA)	
		LPM = 1	LPM = 0
$I_{DD(RUN)}$	SMPS, prefetch ON, SecureMark™ code, V_{DD} = 1.8 V, 24 MHz Range 2, FLASH power-down Bank 2	0.58	0.61

In Range 2, it is particularly beneficial to reduce dynamic consumption by enabling LPM in FLASH_ACR. Using LPM is therefore encouraged whenever timing constraints permit, especially in low-voltage, low-frequency scenarios.

2.3.2 ICACHE efficiency

The STM32U3 series devices embed an 8-Kbyte instruction cache (ICACHE) that allows boosted code execution from the internal flash memory or external octo-SPI memories. This cache can be configured in either a 2-way associative mode or a more power-efficient direct-mapped mode.

Table 4. Current consumption for STM32U375/385 in Run mode with ICACHE ON (1-way) versus prefetch

SecureMark™ benchmark with SMPS and V_{DD} = 1.8 V and FLASH power-down Bank 2.

Frequency (MHz)	Current consumption (mA)	
	Prefetch ON	Prefetch OFF
96 (Range 1)	2.74	2.73
48 (Range 2)	1.1	1.09
24 (Range 2)	0.61 (0.58 if LPM = 1)	0.61

Prefetch tends to increase code execution performance at the cost of extra flash memory accesses, resulting in a moderate rise in current consumption up to 1 % when LPM = 0. Setting the LPM bit at 24 MHz in Range 2 leads to a 5 % reduction in power consumption when prefetch is activated and ICACHE is set to 1-way.

Table 5. Current consumption for STM32U375/385 in Run mode with prefetch ON versus ICACHE configurations

SecureMark™ benchmark with SMPS and V_{DD} = 1.8 V and FLASH power-down Bank 2.

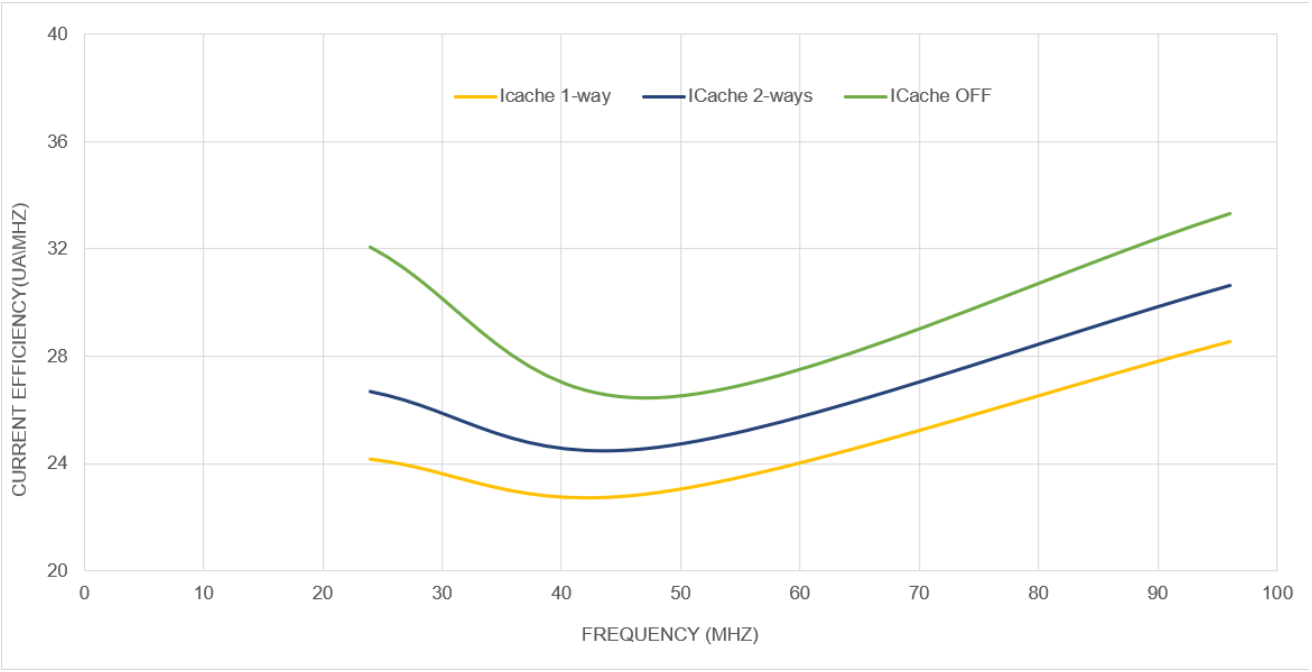
Frequency (MHz)	Current consumption (mA)		
	ICACHE ON (1-way)	ICACHE ON (2-way)	ICACHE OFF
96 (Range 1)	2.74	2.94	3.2
48 (Range 2)	1.1	1.18	1.27
24 (Range 2)	0.61 (0.58 if LPM = 1)	0.64	0.77

Configuring the ICACHE in 1-way mode provides the best energy efficiency, reducing current consumption by up to 10 % versus 2-way mode and up to 26 % versus ICACHE OFF. Combining 1-way ICACHE with LPM delivers additional gains at low frequencies.

ICACHE should therefore remain enabled, preferably in 1-way mode, for all applications targeting low-power operation.

Figure 4 shows the power efficiency of an STM32U375/385 microcontroller in Run mode on a SecureMark™ for benchmark for different ICACHE configurations, as a function of system frequency, with SMPS and V_{DD} = 1.8 V.

Figure 4. Power efficiency for various ICACHE configurations (SecureMark™, SMPS, prefetch ON, V_{DD} = 1.8 V)



2.4 ULPMark™ CoreMark® performance comparison (CoreMark/mW with different IDEs)

2.4.1 ULPMark™ CoreMark® description

The ULPMark™ CoreMark® benchmark provides a unified method to evaluate both the processing performance (CoreMark) and energy efficiency (ULPMark) of a microcontroller.

The ULPMark™ CoreMark® score is the number of CoreMark iterations a device can execute per millijoule. This number, when presented with the CoreMark iterations-per-second score, illustrates how the two opposing metrics are related.

The benchmark defines three operating-point configurations:

1. Performance mode (PERF), optimized for maximum CPU throughput.
2. Energy-Efficiency mode (EE), using the lowest possible supply voltage.
3. Energy-Efficiency at 3 V (EE3V), allowing comparisons across products at a common voltage point.

For more information on ULPMark™ CoreMark®, refer to document [5].

2.4.2 ULPMark™ CoreMark® results on STM32U3 series devices

Table 6 and Table 7 show the ULPMark™ CoreMark® results on STM32U375/385 with the following configuration:

- System clock at 48 MHz Range 2 (optimum configuration) for energy efficiency and 96 MHz Range 1 for performance
- ICACHE configured to 1-way
- Code in FLASH Bank 1 and data, stack/seap in SRAM1 page 1
- FLASH Bank 2 powered down with low-power mode set to 1

Table 6. ULPMark™ CoreMark® score on STM32U375/385 with IAR™ 9.40

Data and stack/heap in SRAM1			
Metric	**Performance Run**	**Energy efficiency Run**	**Energy efficiency Run at 3 V**
CoreMark	382.68	191.34	191.34
CoreMark/MHz	3.99	3.99	3.99
Power (uW)	4302.20	1734.60	1947.11
Voltage (V)	1.8	1.8	3
Frequency (MHz)	96	48	48
Estimated freq. (MHz)	96.30	48.20	48.28
Library	libcmM33i9040	libcmM33i9040	libcmM33i9040
Iterations	4500	2000	2000
Temperature (°C)	22	22	22
ULPMark-CM	89.23	110.77	98.84

Table 6 shows the best performance on the STM32U3 series with IAR™ 9.40.1 is 3.99 CM/MHz, using high-speed, no-size-constraint optimization. The best energy efficiency on the STM32U3 series obtained with IAR™ is 110.77 Coremark/mW at 1.8 V and system clock at 48 MHz.

Table 7. ULPMark™ CoreMark® score on STM32U375/385 with Keil® 5.36 (arm compiler V6.16)

Data and stack/heap in SRAM1			
Metric	**Performance Run**	**Energy efficiency Run**	**Energy efficiency Run at 3 V**
CoreMark	387.3	196.14	196.14
CoreMark/MHz	4.03	4.09	4.09
Power (uW)	4217.40	1682.19	1839.16
Voltage (V)	1.8	1.8	3
Frequency (MHz)	96	48	48
Estimated freq. (MHz)	96.33	48.21	48.28
Library	libcmM33k536	libcmM33k536	libcmM33k536
Iterations	4500	2000	2000
Temperature (°C)	22	22	22
ULPMark-CM	92.15	117.10	107.27

Table 7 shows the best performance on the STM32U375/385 with Keil® 5.36 is 4.09 CM/MHz, using Omax and LTO optimization. The best energy efficiency on the STM32U3 series obtained with Keil® is 117.10 Coremark/mW at 1.8 V and system clock at 48 MHz.

The ULPMark™ CoreMark® score is a quantitative measure that indicates the energy efficiency of the microcontroller in continuous monitoring tasks. A higher ULPMark™ CoreMark® score signifies better energy efficiency and lower power consumption in such scenarios.

The STM32U3 series achieves a strong balance of high processing efficiency and low energy consumption. The combination of Range 2 operation, SMPS regulation, ICACHE 1-way mode, and Flash power-down allows the devices to reach CoreMark/mW scores among the best in the ultra-low-power microcontroller category.

Note: The ULPMark™ CoreMark® score (Performance: CoreMark/MHz or energy efficiency: CoreMark/mW) varies based on the chosen IDEs and their respective versions.

3 STM32U3 series low-power modes

The STM32U3 series microcontrollers offer a range of low-power modes to optimize energy efficiency and extend battery life in embedded application when the CPU does not need to be kept running, for example when waiting for an external event. It is up to the user to select the mode that gives the best compromise between low-power consumption, short startup time, and available wake-up sources. Refer to document [1] for more details.

3.1 Low-power overview

After any system or power reset, the device operates in Run mode. From there, software can transition into several low-power modes depending on the required trade-off between power consumption, available functionality, memory retention, and wake-up latency.

Below is an overview of each mode with typical consumption values measured at 3 V.

Sleep mode

CPU clock off, all peripherals including Cortex®-M33 core such as NVIC and SysTick can run and wake up the CPU when an interrupt or an event occurs.

The typical average power consumption of the system in Sleep mode is 150 µA at 3 V, on STM32U375/385 devices.

Stop 0, Stop 1, Stop 2, and Stop 3 modes

Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. The SRAMs can be totally or partially switched off to further reduce consumption. All clocks in the core domain are stopped. The MSI (MSIS and MSIK) RC, the HSI16 RC, and the HSE crystal oscillators are disabled while the low-speed ones (LSE, LSI) can be kept active.

In Stop 0 mode, the regulator remains in main regulator mode, allowing a very fast wake-up time but with much higher consumption.

In Stop 1 mode, the regulator is in low-power mode, and the whole core domain is fully powered. All autonomous peripherals are functional. The typical average power consumption of the system in Stop 1 mode is 50 µA at 3 V.

In Stop 2 mode, most of the core domain (D1 domain) is put in a lower leakage mode, keeping register retention but without any possible functionality. The D2 domain, embedding APB3 peripherals, is kept fully powered, so those peripherals can be kept functional. The typical average power consumption of the system in Stop 2 mode with 8-Kbyte SRAM is 3.1 µA at 3 V.

Stop 3 is the lowest power mode with full retention, but the functional peripherals and sources of wake-up are reduced to the same ones as in Standby mode. The typical average power consumption of the system in Stop 3 mode with 8-Kbyte SRAM is 1.15 µA at 3 V.

The system clock when exiting from Stop mode can be either MSIS up to 48 MHz or HSI16, depending on software configuration.

Standby mode

The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the core domain is powered off. The MSI (MSIS and MSIK) RC, the HSI16 RC, and the HSE crystal oscillators are also switched off. The system clock after wake-up is MSIS up to 12 MHz.

The typical average power consumption of the system in Standby mode is 0.22 µA at 3 V, on STM32U375/385 devices.

Shutdown mode

The Shutdown mode allows the lowest power consumption. The internal regulator is switched off so that the core domain is powered off. The HSI16, the MSI (MSIS and MSIK), the LSI, and the HSE oscillators are also switched off.

The system clock after wake-up is MSIS at 12 MHz.

The typical average power consumption of the system in Shutdown mode is 0.19 µA at 3 V, on STM32U375/385 devices.

3.2 Power consumption optimization

3.2.1 ICACHE in low-power mode

ICACHE reduces power consumption by fetching instructions from the internal ICACHE most of the time, rather than from the larger and more power-consuming main memories. This reduction is even higher if the cached main memories are external. Applications with a lower-performance profile and stringent low-power consumption constraints may benefit from the lower power consumption of an ICACHE configured as direct mapped (ICACHE_1-way). This single-way cache configuration is obtained by programming WAYSEL = 0 in ICACHE_CR.

Note: The hit and miss monitors are disabled (stopped) by default to reduce power consumption.

3.2.2 FLSAH in low-power mode

After reset, Bank 1 and Bank 2 are in normal mode. To reduce power consumption in Run and Sleep modes, each bank can be independently put in power-down mode by setting the PDREQx bit in FLASH_ACR. The flash memory supports a low-power read mode (LPM) to reduce power consumption, which can be enabled by setting LPM = 1 in FLASH_ACR. When the LPM bit is set, the flash latency must be configured according to the CPU (HCLK) frequency. For more details, refer to document [1].

Note: Prefetch tends to increase code execution performance at the cost of extra flash memory accesses. It must be used carefully in low-power applications.

3.2.3 Power control optimization

After reset, the regulator is the LDO in Range 2. Switching to SMPS provides lower consumption, particularly at high V_{DD} voltage in Run, Sleep, or any other low-power mode. When exiting the Stop or Standby mode, the regulator is the same as when entering low-power modes. The voltage range is Range 2 (low-power range), except when exiting Stop 0 mode.

During Standby mode, and if BOR level 0 is selected, it is possible to set the BOR in ultra-low-power mode to further reduce current consumption by setting the ULPMEN bit in PWR_CR1.

3.2.4 RCC in low-power mode

To reduce the power consumption, it is recommended to select MSIRC1 as an oscillator source and lower the speeds of SYSCLK, HCLK, and PCLK clocks.

After a reset or when exiting Shutdown mode, the CPU clock frequency is 12 MHz, generated from MSIRC1. When exiting Standby mode, the selected oscillator is always MSIRC1 (from 3 to 12 MHz). When exiting Stop modes, the system clock can be either MSIS (up to 48 MHz) or HSI16, depending on the STOPWUCK bit in the RCC_CR.

By default, the MSI bias (for both MSIS and MSIK) is in continuous mode to maintain the output clock accuracy. Setting the MSIBIAS bit in RCC_ICSCR1 reduces MSI consumption when the device is in Stop 1 or Stop 2 mode, or when the regulator is in Range 2, but it decreases MSI accuracy.

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

3.2.5 GPIO in low-power mode

Refer to document [4] for more details.

Configure unused GPIO input as analog input

A GPIO always has an input channel, which can be either digital or analog. If it is not necessary to read the GPIO data, prefer the analog input configuration. This saves the input Schmitt trigger consumption.

Note: To further reduce power consumption, it is recommended to put all unused I/Os in the analog state.

Disable GPIO register clock

If a GPIO bank is not needed for a long time, disable its clock by using the `HAL_RCC_GPIOx_CLK_DISABLE()` function.

Configure GPIO when entering low-power modes

In Sleep, Stop 0, and Stop 1 modes, all I/O pins keep the same state as in Run mode. For outputs, set the level required by the external component. In Stop 2 mode, all I/O pins also keep the same state as in Run mode, except for I3C-specific pull-up. In Stop 3, Standby, or Shutdown mode, the I/Os are in a floating state by default.

Apply an internal pull-up or pull-down by software, depending on the level required by the external component.

Note: This software internal pull-up/pull-down is not applied when exiting Shutdown mode until the firmware configures the GPIO.

Refer to document [1] for more details.

3.2.6 SRAMs in low-power mode

In Run mode, SRAMs can be permanently turned off by configuring bits in the PWR_CR1 register. Once SRAM is set to power-down, it cannot be used again until the next power-on reset.

In Stop 1, Stop 2, and Stop 3 modes, the SRAMs (Sub-blocks of SRAMx, ICACHE, FDCAN, PKA SRAM) can be powered down to further reduce power consumption by setting the corresponding bit to 1 in PWR_CR2.

Note: Refer to the device datasheet for SRAM associated peripheral.

In Standby mode, the SRAMs and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, the SRAM2 content can be partially (8 Kbytes or 24 Kbytes or 32 Kbytes) or fully (64 Kbytes) preserved depending on RRSB1, RRSB2, and RRSB3 bits configuration in PWR_CR1. In this case, the low-power regulator is on and provides the supply to SRAM2 only.

In Shutdown mode, the SRAMs and register contents are lost except for registers in the Backup domain.

Refer to document [1] for more details.

3.2.7 Debug in low-power mode

In Standby and Stop modes, it is possible to maintain the core supply and keep all the clocks and oscillators active to enable full debugging capability for low-power applications.

This can be achieved by setting DBG_STANDBY or DBG_STOP bits in DBGMCU_CR register.

Note: Using this feature in low-power mode increases power consumption and simulates the entry into low-power mode.

By default, all clocks are disabled and the core is powered down automatically in Stop and Standby modes if the power is switched off or if the core is not clocked.

Note: For the NUCLEO-U385RG-Q board, PA13 and PA14 are SWDIO/SWDCLK. If they are kept active in stop modes for debugging purposes, an extra consumption of up to 200 µA can be added in Stop modes. To further reduce power consumption when entering Stop modes, it is recommended to disable the debug by resetting the DBG_STANDBY or DBG_STOP bits in the DBGMCU_CR register and putting PA13/PA14 in Analog mode.

Refer to document [1] for more details.

3.3 Peripherals clock gating and autonomous mode

Clock gating in Sleep mode

When a peripheral is enabled, its clock can be automatically gated off when the device is in Sleep mode, by clearing the peripheral SLPEN bit in RCC_AHBxSLPENR and RCC_APBxSLPENR.

To keep the clock on in Sleep mode, both the EN and SLPEN bits of the peripheral must be set.

Clock gating in Stop 0, Stop 1, and Stop 2 modes

When a peripheral is enabled, its clock can be automatically gated off when the device is in Stop mode, by clearing the peripheral STPEN bit in RCC_AHBxSTPENR and RCC_APBxSTPENR.

To keep the clock on in Stop mode, all the EN, SLPEN, and STPEN bits of the peripheral must be set.

Autonomous peripherals

Several peripherals support the Autonomous mode and can operate in Stop mode by requesting their Kernel clock and their bus (APB or AHB) when needed, in order to transfer data with GPDMA1 depending on peripherals and power mode.

Refer to document [1] for more details.

The table below lists all STM32U3 series peripherals that support the autonomous mode.

Table 8. Peripherals supporting Autonomous mode

Low-power mode	Peripherals
Stop 0 and Stop 1	• DAC1 (2 channels) • LPTIMx (x = 1 to 4) • U(S)ARTx (x = 1 to 5)(1) • LPUART1 • SPIx (x = 1 to 4)(1) • I2Cx (x = 1 to 4)(1) • I3Cx (x = 1 to 2) • ADF1 and GPDMA1
Stop 2	• LPTIM1 • LPTIM3 • LPTIM4 • LPUART1 • I2C3

1. *Refer to the device datasheet for availability of its associated peripheral.*

In Stop 2 mode, if one of the autonomous peripherals requests the AHB/APB clocks for a DMA transfer, the whole core domain is switched to Stop 1 higher leakage mode, and the clock is distributed to GPDMA1, enabled SRAMs, and peripherals to perform the autonomous peripheral DMA transfer. Then the core domain automatically returns to Stop 2 lower leakage mode.

Note: GPDMA1 transfers are functional and autonomous in Stop 0 and 1 modes.

In Stop 2 mode, GPDMA1 supports only LPUART1, I2C3, LPTIM1, LPTIM3, and LPTIM4 requests. None of GPDMA1 triggers are supported. Interrupts wake up from Stop 2 modes.

The COMPs, the PVM, and the PVD can be used in Stop 2 mode. If they are not needed, they must be disabled by software to save their power consumptions.

All the peripherals that cannot be functional in Stop 2 mode must be either disabled by clearing the enable bit in the peripheral itself or put under reset state by configuring RCC_AHBxENR and RCC_APBxENR.

4 Energy saving in ultra-low-power application (different duty cycle) using STM32U3, STM32L4, and STM32U5

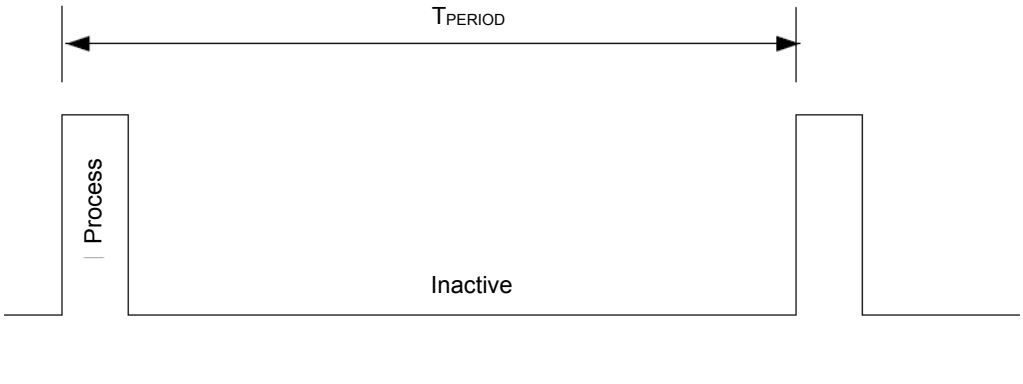
The next section delves into a comparative analysis of energy efficiency versus duty cycle runtime across distinct STM32 products. This investigation aims to provide a comprehensive understanding of how different STM32 microcontrollers handle energy consumption in relation to varying duty cycle runtime.

4.1 Low-power application profile

In applications where the battery lifetime is a concern, the system must be optimized to provide maximum performance and reactivity with the minimal power consumption. This type of application generally contains two different phases:

- Active phase (processing) executes a defined set of instructions within a fixed time frame.
- Inactive phase waits for the next wake-up event while maintaining necessary context (registers, selected SRAM blocks, RTC) and keeping the power consumption as low as possible.

Figure 5. Application profile



Two parameters need to be selected to optimize the average power consumption:

- Run mode and clock frequency to be used during the active phase
- Low-power mode to be used during the inactive phase

4.2 Application profile overview

This section demonstrates the benefits of using the STM32U3 series in ultra-low-power applications with various application profiles. These applications execute the CoreMark® algorithm during the processing phase in each frame time. Afterward, the system transitions to Stop mode and waits for an RTC interrupt to wake it up.

The three application profiles outlined below are executed with different duty cycles, combining the CoreMark® code with extended inactivity periods to simulate various application domains such as consumer, metering, and industrial.

Human activity recognition (HAR)

Human activity recognition (HAR) focuses on the automatic identification and classification of human activities based on data collected from various sensors. HAR systems can recognize and categorize different activities or gestures performed by individuals, such as walking, running, sitting, or specific exercises.

Figure 6. HAR application

DT75684V1

This application simulates a consumer scenario with a 3% duty cycle, consisting of a 3 ms runtime and 97 ms inactive period, with a wake-up frequency of 10 Hz over a duration of 100 ms. It measures over one second consisting in 30 ms runtime and 970 ms inactive period.

Metering (flow meter)

A metering system is designed to measure, monitor, and record the consumption of utilities such as electricity, water, gas, or heat. Metering applications are commonly used in residential, commercial, and industrial settings to track and manage resource usage for billing, analysis, and conservation purposes.

Figure 7. Flow meter application

DT75685V1

This application simulates a metering scenario with a 0.1% duty cycle, consisting of a 3 ms runtime and a 2997 ms inactive period, with a wake-up frequency of 0.3 Hz over a duration of 3 seconds.

Industrial GPS tracker

An industrial GPS tracker is used in industrial settings to track and monitor the location and movement of assets, vehicles, or equipment. These applications are tailored to meet the specific needs of industrial operations, such as fleet management, logistics, asset tracking, and supply chain management.

Figure 8. **GPS tracker application**

DT75686V1

This application simulates an industrial GPS tracker scenario with a 0.04% duty cycle, consisting of a 11 ms runtime and a 29989 ms inactive period, with a wake-up frequency of 0.03 Hz over a duration of 30 seconds.

4.3 Energy consumption for the three different application profiles

Table 9, Table 10, and Table 11 show the dynamic(mW) and static(µW) energy consumption of the different three application profiles on STM32U3, STM32L4, and STM32U5. The measurements are taken at 1.8 V for the HAR application and at 3.3 V for the metering and tracker applications, with 128-kbyte SRAM retention during the inactive phase.

Table 9. **STM32U385 energy consumption with system clock at 48 MHz**

STM32U385 at 48 MHz (R2) 128-KB RAM retention				
-	Application	HAR (3%) Consumer	Metering (0.1%)	Tracker (0.04%) Industrial
Dynamic energy	Voltage (V)	1.8	3.3	3.3
	Time (s)	0.03	0.003	0.011
	Current (mA)	1.1	0.685	0.683
	mW	1.98	2.26	2.25
	µJoule	59.40	6.78	24.79
	Energy % for Run mode	92.72	24.79	10.75
Static energy	Voltage (V)	1.8	3.3	3.3
	Time (s)	0.97	2.997	29.989
	Current (µA)	2.67	2.08	2.08
	µW	4.81	6.86	6.86
	µJoule	4.66	20.57	205.84
	Energy % for Stop mode	7.28	75.21	89.25
-	**Total (µJ)**	**64.06**	**27.35**	**230.64**

Note: For STM32U385, 128-kbyte SRAM is retained in Stop mode, while the full RAM is available in Run mode.

Table 10. STM32U545 energy consumption with system clock at 48 MHz

STM32U545 at 48 MHz (R3) 128-KB RAM retention				
-	Application	HAR (3%) Consumer	Metering (0.1%)	Tracker (0.04%) Industrial
Dynamic energy	Voltage (V)	1.8	3.3	3.3
	Time (s)	0.03	0.003	0.011
	Current (mA)	2.53	1.81	1.81
	mW	4.55	5.97	5.97
	µJoule	136.62	17.92	65.70
	Energy % for Run mode	97.05	46.67	24.28
Static energy	Voltage (V)	1.8	3.3	3.3
	Time (s)	0.97	2.997	29.989
	Current (µA)	2.38	2.07	2.07
	µW	4.28	6.83	6.83
	µJoule	4.16	20.47	204.85
	Energy % for Stop mode	2.95	53.33	75.72
-	**Total (µJ)**	**140.78**	**38.39**	**270.56**

Table 11. STM32L476 energy consumption with system clock at 48 MHz

STM32L476 at 48 MHz (R1) 128-KB RAM retention				
-	Application	HAR (3%) Consumer	Metering (0.1%)	Tracker (0.04%) Industrial
Dynamic energy	Voltage (V)	1.8	3.3	3.3
	Time (s)	0.035	0.0035	0.013
	Current (mA)	7.54	7.66	7.66
	mW	13.57	25.28	25.28
	µJoule	475.02	88.47	328.61
	Energy % for Run mode	99.44	82.48	63.61
Static energy	Voltage (V)	1.8	3.3	3.3
	Time (s)	0.965	2.9965	29.987
	Current (µA)	1.55	1.90	1.90
	µW	2.79	6.27	6.27
	µJoule	2.69	18.79	188.02
	Energy % for Stop mode	0.56	17.52	36.39
-	**Total (µJ)**	**477.71**	**107.26**	**516.63**

Table 12 shows the energy consumption gains on STM32U3 compared to STM32L4 and STM32U5 for different application profiles.

Table 12. Comparison between STM32U3, STM32L4, and STM32U5

Application at 48 MHz		Consumer HAR 3% Run	Metering (flow meter) 0.1% Run	Industrial GPS tracker 0.04% Run
STM32L476 Run (136 µA/MHz) Stop (1.5 µA)	Run	99.44%	82.48%	63.61%
	Stop	0.56%	17.52%	36.39%
STM32U545 Run (39 µA/MHz) Stop (2 µA)	Run	97.05%	46.67%	24.28%
	Stop	2.95%	53.33%	75.72%
	Gain versus L476	3.4x	2.8x	1.9x
STM32U385 Run (14.2 µA/MHz) Stop (2.0 µA)	Run	93.42%	25.86%	11.33%
	Stop	6.58%	74.14%	88.67%
	Gain versus L476	7.4x	3.9x	2.2x
	Gain versus U545	2.2x	1.4x	1.2x

The energy-consumption figures highlighted in Table 12 clearly show that the STM32U3 series achieves substantial gains in both active and low-duty-cycle scenarios. These improvements come from the combination of near-threshold voltage operation, efficient Stop mode architecture, and optimized memory and regulator behavior. As a result:

- Applications with frequent active periods benefit from a lower energy cost per instruction, extending battery life without compromising responsiveness.
- Applications dominated by long inactive periods leverage the extremely low Stop-mode currents to reduce average power consumption, enabling multi-year operation on small batteries.

In practice, this means that designers can meet aggressive autonomy goals without sacrificing processing capability or system reactivity, making the STM32U3 family a strong fit for modern, battery-powered embedded systems.

5 Conclusion

This application note has presented the main ultra-low-power features of the STM32U3 series microcontrollers and how they contribute to reducing power consumption in embedded systems. These devices provide a wide range of configuration options to optimize both performance and energy usage, allowing designers to adapt the system behavior to any application scenario.

The guidelines summarized in this document, supported by experimental data and quantitative measurements, help developers quickly identify the most suitable Run mode and low-power configurations for their use case. By applying these techniques, end-user applications can achieve significantly longer battery life while maintaining the required level of responsiveness and functionality.

Revision history

Table 13. **Document revision history**

Date	Version	Changes
13-Feb-2025	1	Initial release.
28-Feb-2025	2	Updated Section Introduction.
25-Feb-2026	3	Updated: • Section 1: General information • Section 2: Energy efficiency processing and related topics • Section 3.1: Low-power overview • Section 3.2.6: SRAMs in low-power mode • Table 8. Peripherals supporting Autonomous mode • Section 4.1: Low-power application profile • Section 5: Conclusion

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