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## Getting started with STM32C5 MCU hardware development

### Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features. Examples of these features are power supply, clock management, reset control, boot mode settings and debug management.

This document details how to use the STM32C5 series microcontrollers (MCUs) and describes the minimum hardware resources required to develop an application using these MCUs. Detailed reference design schematics are given in this document with the description of the main components, interfaces and modes.

For additional information, refer to the product datasheets and reference manuals available on [www.st.com](http://www.st.com).

## 1 General information

This document applies to the STM32C5 series Arm® Cortex®-based microcontrollers.



Note:

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## 2 Power supply management

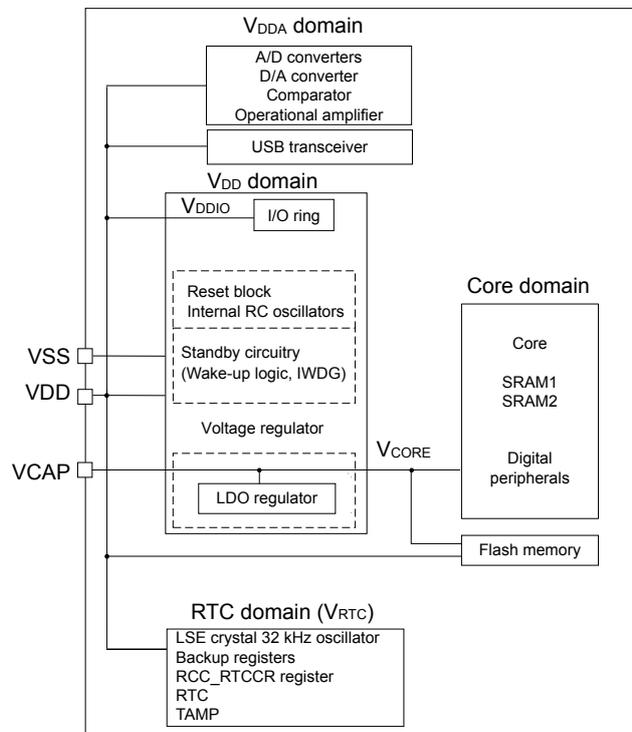
### 2.1 Power supplies

The STM32C5 series requires a 2.7 V to 3.6 V operating voltage supply  $V_{DD}$ .

Several independent supplies can be provided for specific peripherals. Those supplies must not be provided without a valid operating supply on the VDD pin.

- $V_{DD} = 2.7$  to  $3.6$  V**  
 $V_{DD}$  is the external power supply for the I/Os, the internal regulator, and the system analog (such as reset, power management, and internal clocks). It is provided externally through the VDD pins.
- $V_{DDA} = 2.7$  V (ADCs, DAC, COMP, OPAMP) to  $3.6$  V**  
 $V_{DDA}$  is the external analog power supply for A/D converters, D/A converters, and the analog comparator. The  $V_{DDA}$  voltage domain is physically connected to the  $V_{DD}$  voltage.
- $V_{CAP} = 0.9$  to  $1.15$  V: digital core domain supply**  
 This power supply is independent from all the other power supplies:
- $V_{RTC} = 2.7$  to  $3.6$  V**  
 $V_{RTC}$  is the power supply for RTC, external clock 32 kHz oscillator, and backup registers. The  $V_{RTC}$  voltage level is physically connected to the  $V_{DD}$  voltage.
- $V_{REF-}$ ,  $V_{REF+}$**   
 $V_{REF+}$  is the input reference voltage for ADCs, DAC, and COMP.  
 $V_{REF+}$  can be grounded when ADC and DAC are not active.  
 $V_{REF-}$  and  $V_{REF+}$  pins are not available on all packages. When not available, they are bonded to VSS and VDD, respectively.  
 $V_{REF-}$  must always be equal to  $V_{SSA}$ .  
 Figure 1 shows the power-supply overview of STM32C5 devices.

**Figure 1. STM32C5 power-supply overview**



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### 2.1.1 Analog peripherals supply

The  $V_{DDA}$  and  $V_{SSA}$  analog supply, providing power to ADC, DAC, OPAMP, and COMP, are connected internally to digital supply  $V_{DD}$  and  $V_{SS}$  offering extra GPIOs to user.

#### ADC and DAC reference voltage

To ensure a better accuracy on low-voltage inputs and outputs, the user can connect to VREF+, a separate reference voltage lower than  $V_{DDA}$ .

$V_{REF+}$  is the highest voltage, represented by the full-scale value, for an analog input (ADC) or output (DAC) signal.

For more details, refer to the device datasheet and to the reference manual.

*Note: The VREF+ and VREF- pins are not available on all packages (connected internally respectively to VDDA and VSSA). Do not enable the internal voltage reference buffer when an external power supply is applied to the VREF+ pin.*

### 2.1.2 RTC domain

To retain the content of the backup registers and to supply the RTC function when the device enters Standby mode.

The RTC domain powers the RTC unit and the LSE oscillator, allowing the RTC to operate even when the core supply domain is switched off.

#### RTC domain access

After a system reset, the RTC domain (RCC RTC domain control register RCC\_RTCCR, RTC registers, TAMP registers, and backup registers) is protected against possible unwanted write accesses. To enable access to the RTC domain, set the DBP bit in the PWR disable backup domain control register (PWR\_DBPR) to enable access to the RTC domain.

### 2.1.3 Voltage regulator

Linear voltage regulator (LDO) is enabled on power-on reset. It supplies digital parts of the STM32C5 in the  $V_{CORE}$  domain and is stabilized thanks to the 2.2  $\mu\text{F}$  capacitor positioned on VCAP pad.

#### Embedded voltage regulator operating modes

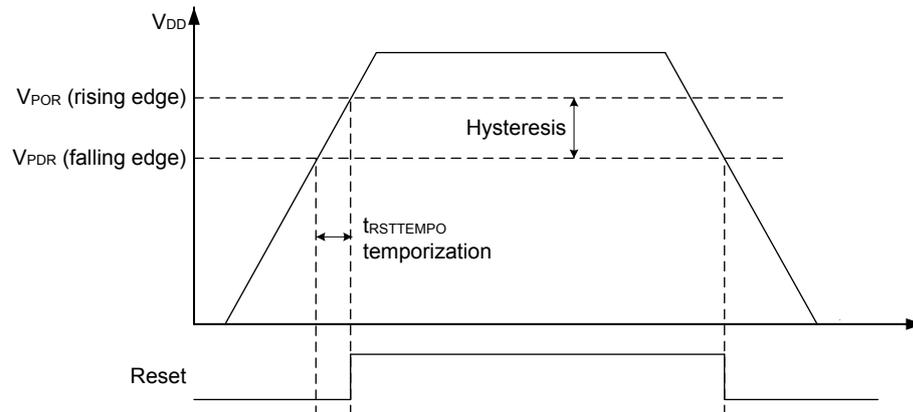
There are three different power modes:

- **Run mode**  
The voltage regulator provides full power to the  $V_{CORE}$  domain (core, memories, and digital peripherals). The regulator output voltage is in range of 1.2 V in Run and Sleep mode.
- **Stop mode**  
The voltage regulator supplies the  $V_{CORE}$  domain to retain the content of registers and internal memories. The regulator output voltage is decreased to 0.95 V under Stop modes.
- **Standby mode**  
The regulator is OFF and the  $V_{CORE}$  domains are powered down. The content of the registers and memories is lost except for the Standby circuitry and the RTC domain.

## 2.2 Power supply scheme

The following figure shows the power supply scheme for STM32C5 devices.



**Figure 3. POR/PDR reset waveform**


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### 2.3.2 Programmable voltage detector (PVD)

The PVD can be used to monitor the  $V_{DD}$  power supply by comparing it to a threshold in range of 3 V (refer to product datasheet for more details). The PVD is enabled by setting the PVDE bit in PWR voltage monitor control register (PWR\_VMCR).

A PVDO flag is available in the PWR voltage monitor status register (PWR\_VMSR) to indicate if  $V_{DD}$  voltage is higher or lower than the PVD threshold. This event is internally connected to the EXTI and can generate an interrupt, provided it has been enabled through the EXTI registers.

The rising/falling edge sensitivity of the EXTI line must be configured according to PVD output behavior that is, if the EXTI line is configured to rising edge sensitivity, the interrupt is generated when  $V_{DD}$  voltage drops below the PVD threshold. As an example, the service routine could perform an emergency shutdown.

### 2.3.3 System reset

A system reset sets all registers to their reset values except the reset flags in RCC reset status register (RCC\_RSR) and the registers in the backup domain.

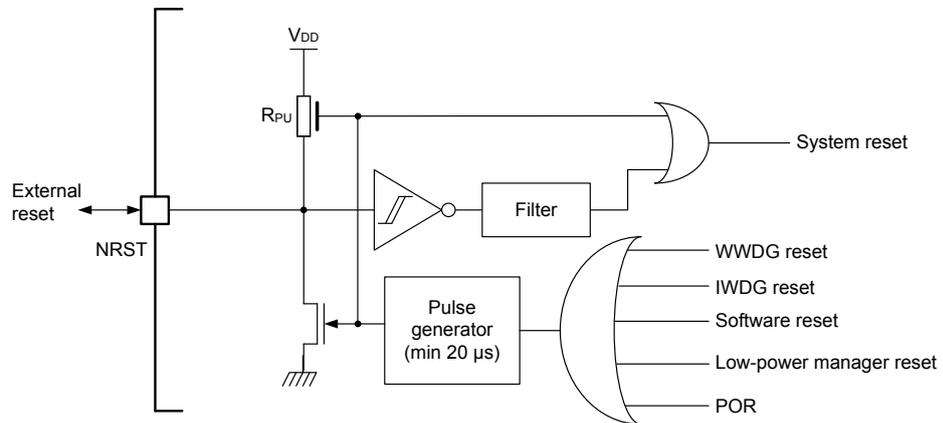
A system reset is generated when one of the following events occurs:

- A low level on the NRST pin (external reset)
- A window watchdog event (WWDG reset)
- An independent watchdog event (IWDG reset)
- A software reset (SW reset)
- A low-power mode security reset

These sources act on the NRST pin and this pin is always kept low during the delay phase. The reset service routine vector is selected depending on the RPD level, on Boot option bytes or on both.

The system reset signal provided to the device is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20  $\mu\text{s}$  for each internal reset source. In case of an external reset, the reset pulse is generated while the NRST pin is asserted low. In case on an internal reset, the internal pull-up RPU is deactivated in order to save the power consumption through the pull-up resistor.

**Figure 4. Simplified diagram of the reset circuit**



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### 2.3.4 RTC domain reset

An RTC domain reset is generated when one of the following events occurs:

- A software reset, triggered by setting the RTCDRST bit in the RCC\_RTCCR register
- A  $V_{DD}$  power-on

An RTC domain reset affects the LSE oscillator, the RTC, the backup registers all secrets protected by tamper and the RCC\_RTCCR register.

### 3 RCC clocks functional description

Four different clock sources can be used to drive the system clock (SYSCLK):

- HSIS: high-speed internal clock at 144 MHz  
→ and HSIDIV3: high-speed internal clock is divided by 3; at 48 MHz
- PSIS: precise speed internal clock up to 160 MHz (max SYSCLK is 144 MHz)
- HSE: high-speed external crystal or clock, from 4 to 50 MHz

The HSIDIV3 is used as a the system clock source after startup from reset, at 48 MHz.

*Note: If HSE or PSIS with HSE as reference are used as SYSCLK and the HSE CSS detect a failure, HSIDIV3 is automatically set as SYSCLK. Adequate wait state supporting both frequencies must be configured in this case.*

The device has the following additional clock sources:

- HSIK: high-speed internal clock divided by 1;1.5; 2;...; 7.5; 8
- PSIDIV3: precise speed internal clock divided by 3
- PSIK: precise speed internal clock divided by 1;1.5; 2;...; 7.5; 8
- LSI: 32 kHz low-speed internal RC that drives the independent watchdog and optionally the RTC used for auto-wake-up from Stop and Standby modes
- LSE: 32.768 kHz low-speed external crystal or clock that optionally drives the real-time clock (rtc\_ck)

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

Several prescalers can be used to configure the AHB and APB frequencies. The maximum frequency of the AHB and APB domains is 144 MHz.

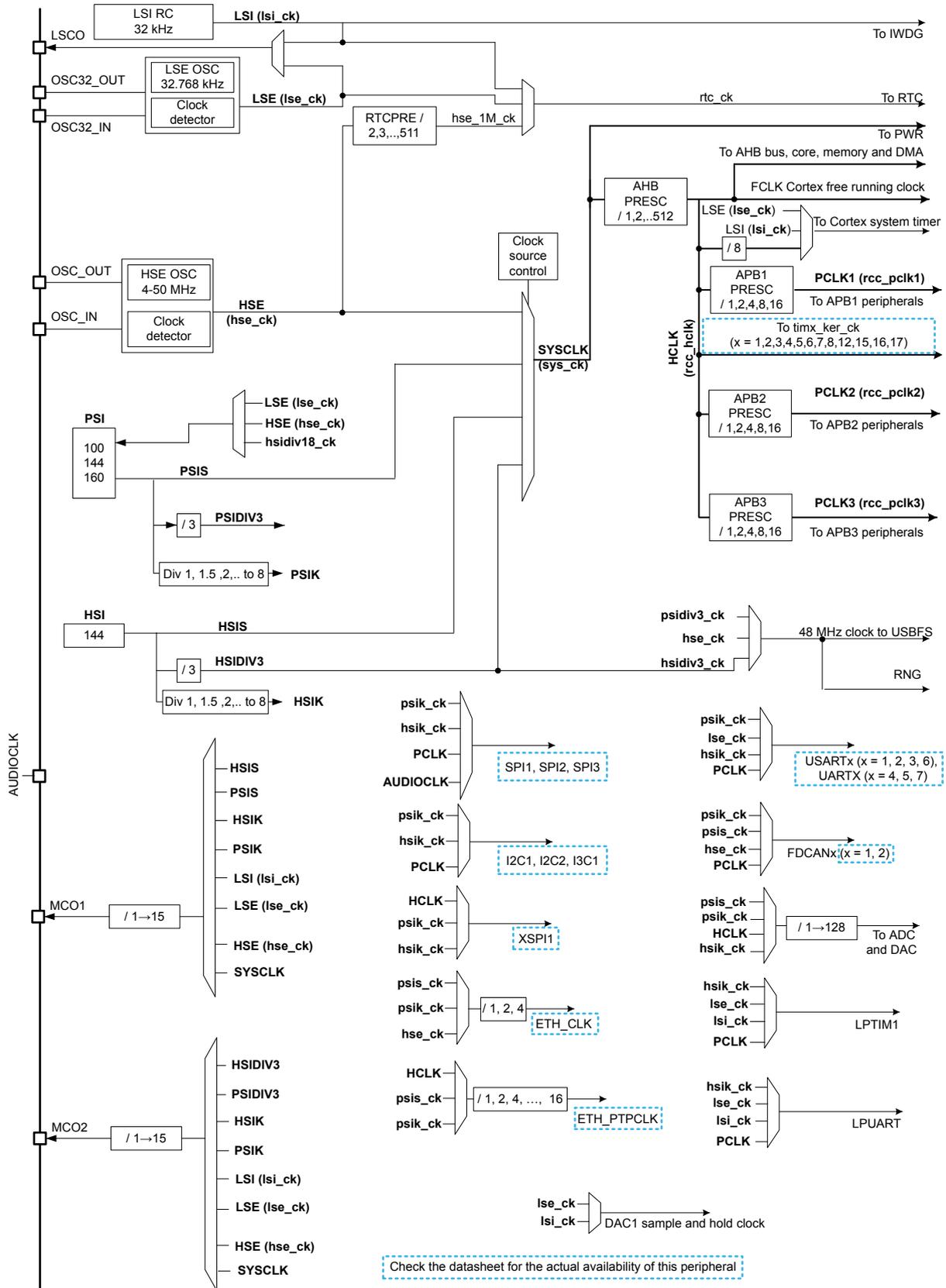
The peripheral clocks are derived from their bus clock (HCLK, PCLK1, PCLK2 or PCLK3), except those that receive an independent kernel clock. This kernel clock can be selected by software between several sources thanks to RCC\_CCIPRx registers (x = 1,2).

*Note: All timers (except LPTIM) are clocked by HCLK, independently of their respective PCLK.*

In addition, the RTC kernel clock is selected by software in RCC\_RTCCR. The IWDG clock is always the LSI 32 kHz clock.

The RCC feeds the Cortex system timer (SysTick) external clock with the AHB clock (HCLK) divided by eight, or LSE or LSI. The SysTick can work either with this clock or directly with the Cortex clock (HCLK), configurable in the SysTick control and status register.

FCLK acts as a Cortex-M33 free-running clock.

**Figure 5. Clock tree**


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## 4 Packages

### 4.1 Package summary

The package selection must consider the constraints that are strongly dependent upon the application. The list below summarizes the most frequent ones:

- Number of interfaces required: some interfaces may not be available on some packages. Some interfaces combination may not be possible on some packages.
- PCB technology constrains: small pitch and high-ball density may require more PCB layers and higher-class PCB.
- Package height.
- PCB available area.
- Noise emission or signal integrity of high-speed interfaces.
- Smaller packages usually provide better signal integrity. This is further enhanced as small-pitch and high-ball density requires multilayer PCBs that allow better supply/ground distribution.
- Compatibility with other devices.

**Table 1. Package summary for STM32C5 devices**

Package	Size (mm)	Height (mm)	Pitch (mm)	STM32C53x/C54x	STM32C55x/C56x	STM32C59x/C5Ax
LQFP144	20 × 20	1.6	0.5	-	-	X
LQFP100	14 × 14	1.6	0.5	-	X	X
LQFP80	12 × 12	1.6	0.5	-	X	X
LQFP64	10 × 10	1.6	0.5	X	X	X
LQFP48	7 × 7	1.6	0.5	X	X	X
UFQFPN48	7 × 7	0.6	0.5	X	X	X
LQFP32	7 × 7	1.6	0.8	X	X	X
UFQFPN32	5 × 5	0.6	0.5	X	X	X
UFQFPN24	4 × 4	0.6	0.5	X	-	-
TSSOP20	6.5 × 4.4	1.2	0.65	X	-	-
UFQFPN20	3 × 3	0.6	0.5	X	-	-

## 4.2 Pinout summary

**Table 2. Pinout summary for STM32C5 devices**

Pin name	Package options										
	UFQFPN20	TSSOP20	UFQFPN24	UFQFPN32	LQFP32	UFQFPN48	LQFP48	LQFP64	LQFP80	LQFP100	LQFP144
<b>Specific I/Os</b>											
PC14-OSC32_IN	-	-	-	X <sup>(1)</sup>	X <sup>(1)</sup>	X	X	X	X	X	X
PC15-OSC32_OUT	-	-	-	-	-	X	X	X	X	X	X
PH0-OSC_IN	X	X	X	X	X	X	X	X	X	X	X
PH1-OSC_OUT	X	X	X	X	X	X	X	X	X	X	X
<b>System pins</b>											
NRST	X	X	X	X	X	X	X	X	X	X	X
PH2-BOOT0	-	-	-	X	-	X	X	X	X	X	X
PB8-BOOT0	X	X	X	-	X	-	-	-	-	-	-
<b>Power pins</b>											
VREF+	X	X	X	X	X	X	X	X	X	X	X
VREF-	X	X	-	-	-	X	X	X	X	X	X
VCAP	X	X	X	X	X	X	X	X	X	X	X
Number of VDD	1	1	1	2	2	3	3	4	5	5	11
Number of VSS	1	1	0 <sup>(2)</sup>	0 <sup>(2)</sup>	2	3 <sup>(2)</sup>	3	4	5	5	11
<b>Max GPIOs</b>											
GPIOs	14	14	20	27	25	38	38	52	66	86	118

1. On these packages PC14-OSC32\_IN is double bonded to PH0-OSCIN, it can not be used with an external crystal as OSC32OUT is not available but can be used in bypass mode for LSE if HSE is not used.

2. Plus VSS connection through exposed pad.

## 5 Boot configuration

### 5.1 Boot mode selection

At startup, the BOOT0 pin or option bit (based on the value of the BOOT\_SEL option bit) and BOOTADD[31:8] option bytes are used to select the boot memory address that includes:

- Boot from any address in user flash memory
- Boot from system memory  
→ Bootloader

When boot from user flash is selected, the boot address is defined by BOOTADD. This address can be locked thanks to BOOT\_LOCK.

#### Embedded bootloader

The embedded bootloader is located in the system memory and is programmed by ST during production. It is used to reprogram the flash memory using USART, SPI, FDCAN, or USB in device mode through the DFU (device firmware upgrade).

Refer to the application note STM32 microcontroller system memory boot mode (AN2606).

#### 5.1.1 STM32C5 boot modes

The following table provides the details of the boot modes for the STM32C5 devices.

**Table 3. STM32C5 boot modes**

RPD_STATE	BOOT_SEL option bit	BOOT0 option bit	BOOT0 pin	EMPTY flag value <sup>(1)</sup>	Boot area
Level 0	1	X	0	X	Boot address defined by user option byte BOOTADD[31:8]
			1		Bootloader
	0	0	X	0	Boot address defined by user option byte BOOTADD[31:8]
				1	Bootloader
Level 2 with boundary scan and level 2	X	X	X	0	Bootloader
				X	Boot address defined by user option byte BOOTADD[31:8]

1. The boot address, defined by BOOTADD option byte, is considered empty only if the FLASH word is equal to 0xFFFF FFFF. In this case, at option byte loading, the EMPTY bit is set in FLASH\_CR.

#### Empty check

During the option byte loading phase, after loading all options, the flash memory interface checks whether the boot location in the main memory, indicated by BOOTADD[31:8], is programmed. The result of this check, with the boot0 information, is used to determine where the system should boot from. It prevents the system from booting from the main flash memory area when, for instance, no user code has been programmed.

The main flash memory empty check status can be read from the EMPTY bit in the FLASH access control register (FLASH\_ACR). Software can modify it by writing an appropriate value to the EMPTY bit.

The BOOT\_LOCK, which locks modifications of option bytes involved in BOOT selection, has no impact on this empty check mechanism.

### Embedded bootloader

The embedded bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the flash memory by using USART, SPI, FDCAN, or USB in device mode through the DFU (device firmware upgrade).

For further information, refer to the application note STM32 microcontroller system memory boot mode (AN2606).

## 5.2 System bootloader

The system bootloader is located in the system memory, programmed by ST during the production. It is used to reprogram the flash memory using one of the following serial interfaces.

**Table 4. Bootloader summary**

Interface name	Package options										
	UFQFPN 20	TSSOP20	UFQFPN 24	UFQFPN 32	LQFP32	UFQFPN 48	LQFP48	LQFP64	LQFP80	LQFP100	LQFP144
USART1	-	-	-	-	-	PA9/PA10	PA9/PA10	PA9/PA10	PA9/PA10	PA9/PA10	PA9/PA10
USART2	PA2/PA3	PA2/PA3	PA2/PA3	PA2/PA3	PA2/PA3	PA2/PA3	PA2/PA3	PA2/PA3	PA2/PA3	PA2/PA3	PA2/PA3
USART3	-	-	-	-	-	-	-	-	-	PD8/PD9	PD8/PD9
UART4	PA0/PA1	PA0/PA1	PA0/PA1	PA0/PA1	PA0/PA1	PA0/PA1	PA0/PA1	PA0/PA1	PA0/PA1	PA0/PA1	PA0/PA1
SPI1	PA4/PA5/ PA6/PA7	PA4/PA5/ PA6/PA7	PA4/PA5/ PA6/PA7	PA4/PA5/ PA6/PA7	PA4/PA5/ PA6/PA7	PA4/PA5/ PA6/PA7	PA4/PA5/ PA6/PA7	PA4/PA5/ PA6/PA7	PA4/PA5/ PA6/PA7	PA4/PA5/ PA6/PA7	PA4/PA5/ PA6/PA7
SPI2	-	-	-	-	-	PB12/ PB13/ PB14/ PB15	PB12/ PB13/ PB14/ PB15	PB12/ PB13/ PB14/ PB15	PB12/ PB13/ PB14/ PB15	PB12/ PB13/ PB14/ PB15	PB12/ PB13/ PB14/ PB15
SPI3 <sup>(1)</sup>	-	-	-	-	-	PB0/PB1/ PB2/PB8	PB0/PB1/ PB2/PB8	PB0/PB1/ PB2/PB8	PB0/PB1/ PB2/PB8	PB0/PB1/ PB2/PB8	PB0/PB1/ PB2/PB8
FDCAN <sup>(2)</sup>	-	-	-	PB5/PB6	PB5/PB6	PB5/PB6	PB5/PB6	PB5/PB6	PB5/PB6	PB5/PB6	PB5/PB6
USB DFU	PA11/ PA12	PA11/ PA12	PA11/ PA12	PA11/ PA12	PA11/ PA12	PA11/ PA12	PA11/ PA12	PA11/ PA12	PA11/ PA12	PA11/ PA12	PA11/ PA12

1. Not supported on STM32C53x/C54x.

2. FDCAN1 on STM32C55x/C56x and FDCAN2 on STM32C53x/C54x/C59x/C5Ax.

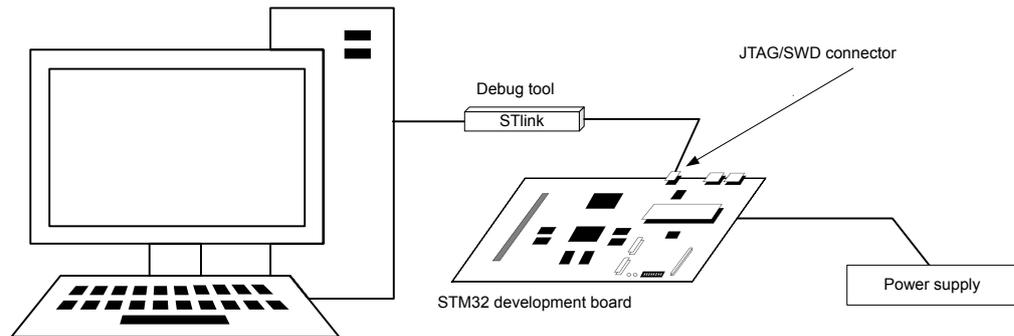
For more details refer to the application note STM32 microcontroller system memory boot mode (AN2606).

## 6 Debug management

The Host/Target interface is the hardware equipment that connects the host to the application board. This interface is made of three components, a hardware debug tool, a JTAG or a serial-wire connector and a cable connecting the host to the debug tool.

The figure below shows the connection of the host to a development board.

Figure 6. Host-to-board connection



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### 6.1 SWJ-DP (serial-wire and JTAG debug port)

The core of the STM32C5 microcontrollers integrates the serial wire / JTAG debug port (SWJ-DP). It is an Arm® standard CoreSight™ debug port that combines a 5-pin JTAG-DP interface and a 2-pin SW-DP interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port.
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port.

In the SWJ-DP, the two JTAG pins of the SW-DP are multiplexed with some of the five JTAG pins of the JTAG-DP.

*Note:* All SWJ port IOs can be reconfigured to other functions by software, but debugging is no longer possible. All SWJ port IOs can be reconfigured to other functions by software, but debugging is no longer possible.

For more details on the SWJ debug port, refer to the reference manual of the product.

The NRST pin is needed to run debug authentication.

### 6.2 Pinout and debug port pins

The devices are available in various packages with different numbers of available pins. As a result, some functionality related to the pin availability may differ from one package to another.

#### 6.2.1 SWJ-DP pins

Five pins are used as outputs for the SWJ-DP, as alternate functions of the GPIOs (general-purpose I/Os). These pins are available on all packages and detailed in the table below.

**Table 5. JTAG/Serial-wire debug port pins**

Pin name	JTAG debug port		Serial-wire debug port		Pin assignment
	Type	Description	Type	Description	
JTMS/SWDIO	Input	JTAG test mode select	Input/Output	Serial-wire data in/out	PA13
JTCK/SWCLK	Input	JTAG test clock	Input	Serial-wire clock	PA14
JTDI <sup>(1)</sup>	Input	JTAG test data input	-	-	PA15
JTDO	Output	JTAG test data output	-	-	PB3
nJTRST	Input	JTAG test reset	-	-	PB4

1. TDI is hosted on the same IO as a USBPD-CC line. To avoid pull-up/down conflict, a user option can help to decide whether the pad is used as TDI or as CC.

### 6.2.2 Flexible SWJ-DP pin assignment

After reset (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins that are immediately usable by the debugger host.

*Note:* The trace outputs are not assigned except if explicitly programmed by the debugger host.

The table below shows the different possibilities for releasing some pins.

**Table 6. SWJ-DP I/O pin availability**

Available debug ports	SWJ-DP I/O pin assigned				
	PA13 /JTMS/ SWDIO	PA14 /JTCK/ SWCLK	PA15 /JTDI	PB3 /JTDO	PB4/nJTRST
Full SWJ-DP (JTAG-DP + SW-DP) Reset state	x	x	x	x	x
Full SWJ-DP (JTAG-DP + SW-DP) but without nJTRST	x	x	x	x	-
JTAG-DP disabled and SW-DP enabled	x	x	-	-	
JTAG-DP disabled and SW-DP disabled	Released				

### 6.2.3 Internal pull-up and pull-down resistors on JTAG pins

The JTAG input pins must not be floating since they are directly connected to flip-flops that control the debug mode features. Special care must be taken with the SWCLK/TCK pin that is directly connected to the clock of some of these flip-flops.

To avoid any uncontrolled I/O levels, the devices embed the following internal resistors on the JTAG input pins:

- JNTRST: internal pull-up
- JTDI: internal pull-up
- JTMS/SWDIO: internal pull-up
- TCK/SWCLK: internal pull-down

Once a JTAG I/O is released by the user software, the GPIO controller takes the control again, and the software can then use these I/Os as standard GPIOs. The reset states of the GPIO control registers put the I/Os in the following equivalent states:

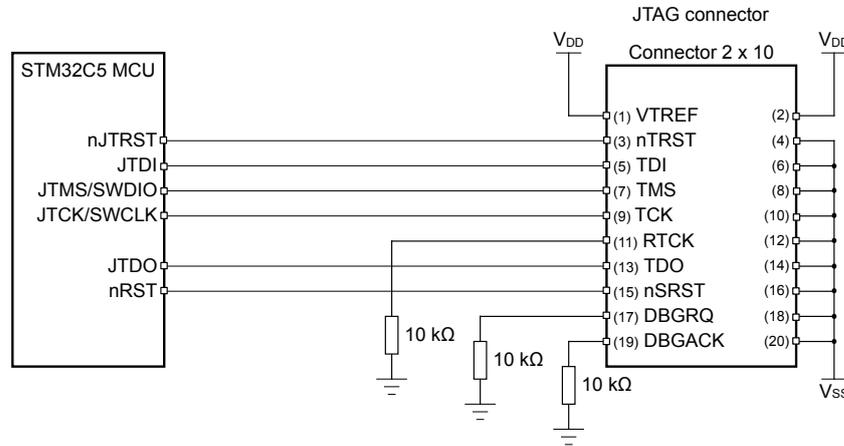
- JNTRST: input pull-up
- JTDI: input pull-up
- JTMS/SWDIO: input pull-up
- JTCK/SWCLK: input pull-down
- JTDO: input floating

*Note:* The JTAG IEEE standard recommends adding pull-up resistors on TDI, TMS, and nTRST, but there is no special recommendation for TCK. However, for the devices, an integrated pull-down resistor is used for JTCK. Having embedded pull-up and pull-down resistors removes the need to add external resistors.

### 6.2.4 SWJ-DP connection with standard JTAG connector

The figure below shows the connection between the device and a standard JTAG connector.

Figure 7. JTAG connector implementation



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### 6.3 Serial wire debug (SWD) pin assignment

The same SWD pin assignment, detailed in the table below, is available on all packages.

Table 7. SWD port pins

SWD pin	SWD port		Pin assignment
	Type	Debug assignment	
SWDIO	Input/Output	Serial-wire data input/output	PA13
SWCLK	Input	Serial-wire clock	PA14

#### 6.3.1 SWD pin assignment

After reset, the pins used for the SWD are assigned as dedicated pins that can be immediately used by the debugger host. However, the MCU offers the possibility to disable the SWD, therefore releasing the associated pins for GPIO use.

For more details on how to disable SWD port, refer to the section 'I/O pin alternate function multiplexer and mapping section of the reference manual.

#### 6.3.2 Internal pull-up and pull-down on SWD pins

Once the SWD I/O is released by the user software, the GPIO controller takes control of it. The reset states of the GPIO control registers put the I/Os in the equivalent states:

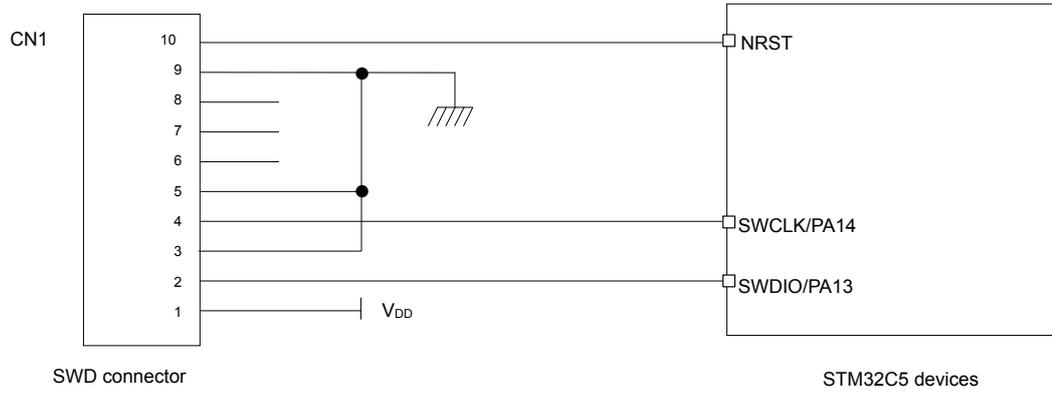
- SWDIO: alternate function pull-up
- SWCLK: alternate function pull-down

The embedded pull-up and pull-down resistors remove the need to add external resistors.

### 6.3.3 SWD port connection with standard SWD connector

The figure below shows the connection between the device and a standard SWD connector.

Figure 8. SWD connector implementation



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## 7 Recommendations

### 7.1 PCB (printed circuit board)

For technical reasons, it is best to use a multilayer printed circuit board PCB, with a separate layer dedicated to the ground ( $V_{SS}$ ) and another dedicated to the  $V_{DD}$  supply.

This provides both good decoupling and good shielding effect. For many applications, cost reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for the ground and the power supply.

### 7.2 Component position

A preliminary layout of the PCB must separate circuits into different blocks:

- High-current circuits
- Low-voltage circuits
- Digital component circuits
- Circuits separated according to their EMI contribution, in order to reduce noise due to cross-coupling on the PCB.

### 7.3 Ground and power supply

The following rules related to grounding must be respected:

- Ground every block (noisy, low-level sensitive, digital, or others) individually.
- Return all grounds to a single point.
- Avoid loops or ensure they have a minimum area.

In order to improve analog performance, the user must use separate supply sources for  $V_{DD}$  and  $V_{DDA}$ , and place the decoupling capacitors as close as possible to the device.

The power supplies must be implemented close to the ground line to minimize the area of the supplies loop. This is because the supply loop acts as an antenna, and acts as the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

### 7.4 Decoupling

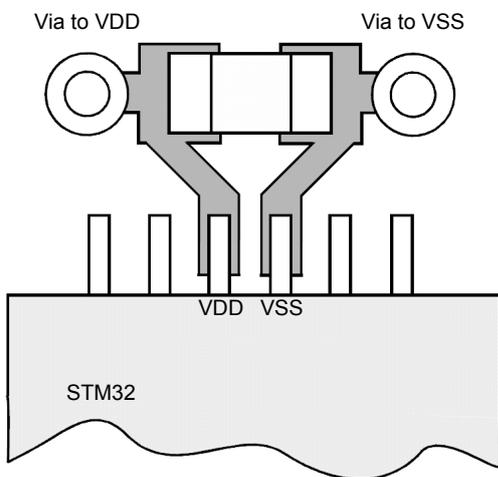
All power-supply and ground pins must be properly connected to the power supplies. These connections (including pads, tracks, and vias) must have the lowest possible impedance. This is typically achieved with thick track widths and, preferably, the use of dedicated power-supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering ceramic capacitors (100 nF) and one single ceramic capacitor (minimum 4.7  $\mu$ F) connected in parallel.

Some packages use a common VSS for several VDD instead of a pair of power pins (one VSS for each VDD), in that case the capacitors must be between each VDD and the common VSS. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but exact values depend on the application requirements.

The figure below shows the typical layout of such a VDD/VSS pair.

**Figure 9. Typical layout for VDD/VSS pin pair**



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## 7.5 Other signals

When designing an application, the EMC performance can be improved by closely studying the following:

- Signals for which a temporary disturbance affects the running process permanently (which is the case for interrupts and handshaking strobe signals but, not the case for LED commands). For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance. For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (example, clock)
- Sensitive signals (example: high impedance)

## 7.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase the EMC performance and avoid extra power consumption, the unused features of the device must be disabled and disconnected from the clock tree, as follows:

- The unused clock source must be disabled.
- The unused I/Os must not be left floating.
- The unused I/O pins must be configured as analog input by software, and must be connected to a fixed logic level 0 or 1 by an external or internal pull-up or pull-down, or configured as output mode using software.

## 8 Reference design

### 8.1 Description

The reference design shown in the following figures is based on the NUCLEO C562 in the LQFP64 package. This reference design can be tailored to any STM32C5 device with a different package, using the pin correspondence given in [Section 8.2](#).

#### Clock

Two clock sources are used for the MCU:

- LSE: X1– 32.768 kHz crystal for the embedded RTC
- HSE: X2– crystal for the MCU

See [Section 3](#) for more details.

#### Reset

The reset signal is active low in the reference design figures shown in [Section 8.2](#).

The reset sources include:

- The reset button (B1)
- Debugging tools via the connector CN1

See [Section 2.3](#) for more details.

#### Boot mode

The user can add a switch on the board to change the boot option but this is optional. On virgin samples the boot address is defined by option bytes (and empty check) and the pads PH2-BOOT0/PB8-BOOT0 are used as GPIO by default.

See [Section 5](#) for more details.

*Note:* When waking up from Standby mode, the BOOT pin is sampled, and the user must pay attention to its value.

#### SWD interface

The reference design shows the connection between the devices and a standard SWD connector.

See [Section 6](#) for more details.

*Note:* It is recommended to connect the RESET pins, so as to be able to reset the application from the tools and also to run RDP regression for debug opening.

#### Power supply

See [Section 2](#) for more details.

### 8.2 Component references

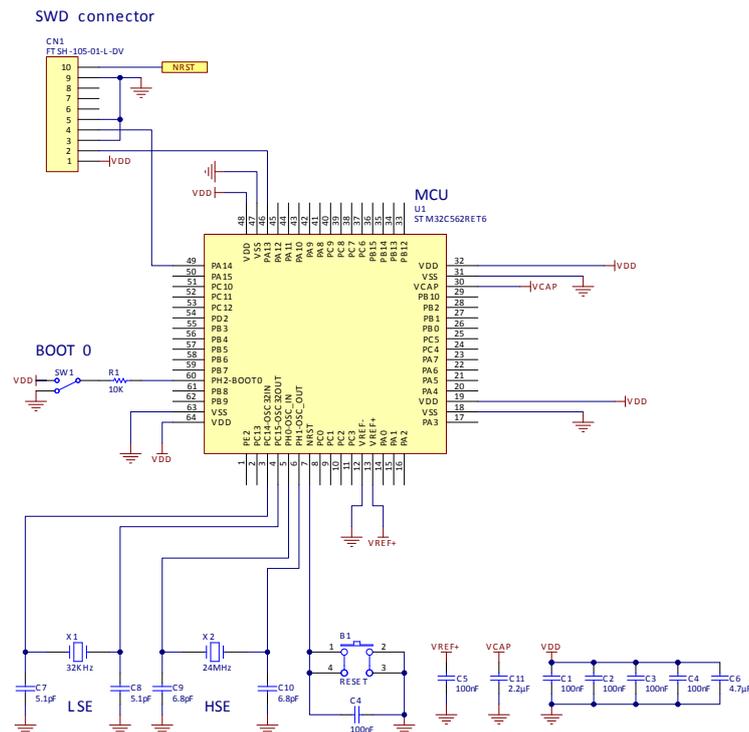
The following table lists the components in the STM32C5 Nucleo-64 boards (reference design MB2213).

The components list is based on:

- STM32C562 device (see [Figure 10](#))

**Table 8. Components of STM32C5 Nucleo-64 boards**

Reference	Type	Value	Quantity	Comments
B1	Push-button	-	1	-
C6	Tantalum or ceramic capacitor	4.7 $\mu$ F	1	Decoupling capacitor required for the package
C1, C2, C3, C4	Ceramic capacitor	100 nF	7	For each external power pin
C5		2.2 $\mu$ F	1	Required by the internal LDO regulator
C7, C8		5.1 pF	2	Used for LSE, HSE: values depend on crystal characteristics
C9, C10		6.8 pF	2	
X1	Quartz	32.768 kHz	1	Used for LSE
X2		24 MHz	1	Used for HSE
R1	Resistor	10 k $\Omega$	1	Maintains BOOT0 pin at a logic low or high level
SW1	Switch	-	1	Used to select the right boot mode

**Figure 10. STM32C562 reference design**


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**Note:** It is recommended to connect the 2.2  $\mu$ F ceramic capacitor as close as possible to VCAP pin.

## 9 PCB routing guidelines for STM32C5 devices

### 9.1 Crystal oscillator

Use the application note: Oscillator design guide for STM8S, STM8A and STM32 microcontrollers (AN2867), for further guidance on how to layout and route crystal oscillator circuits.

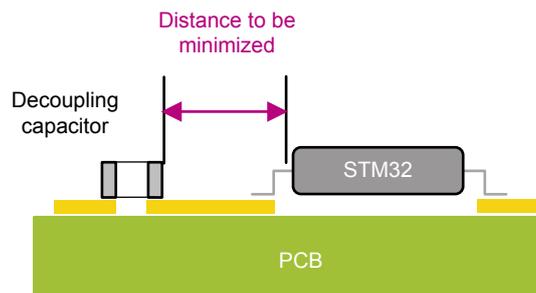
### 9.2 Power supply decoupling

An adequate power decoupling for STM32C5 devices is necessary to prevent an excessive power noise and ground bounce noise. Refer to [Section 2.2: Power supply scheme](#).

Then follow the recommendations:

- Place the decoupling capacitors as close as possible to the power and ground pins of the MCU.
- Add the recommended decoupling capacitors for each VDD/GND pair.
- Connect the decoupling capacitor pad to the power and ground plane with a wider, short trace/via. This allows reducing the series inductance, maximizing the current flow and minimizing the transient voltage drops from the power plane which also reduces the possibility of ground bounce.

**Figure 11. Decoupling capacitor placement depending on package type**



Decoupling capacitor and STM32 MCU on the same side of the package (all packages except BGA)

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### 9.3 High speed signal layout

#### 9.3.1 Embedded trace macrocell (ETM)

##### Interface connectivity

The ETM enables the reconstruction of the program execution. The data are traced using the data watchpoint and trace (DWT) component or the instruction trace macrocell (ITM) whereas instructions are traced using the embedded trace macrocell (ETM). The ETM interface is synchronous with the data bus of 4 lines D[0:3] and the clock signal CLK.

**Interface signals layout guidelines**

- Reference the plane using GND or PWR (if PWR, add 10 nf stitching cap between PWR and GND).
- Trace the impedance:  $50 \Omega \pm 10\%$
- All the data trace should be as short as possible ( $\leq 25$  mm).
- Trace the lines which should run on the same layer with a solid ground plane underneath it without a via.
- Trace the clock which should have only point-to-point connection. Any stubs should be avoided.
- It is strongly recommended also for other (data) lines to be point-to-point only. If any stubs are needed, they should be as short as possible. If longer are required, there should be a possibility to optionally disconnect them (for example, by jumpers).

## Revision history

**Table 9. Document revision history**

Date	Version	Changes
16-Feb-2026	1	Initial release.

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