EVLVIPGAN65WF: 24 V/65 W isolated flyback with VIPerGaN65W

Introduction

This document describes the evaluation board EVLVIPGAN65WF, a 24 V/65 W SMPS in a wide input voltage range (90 V_{AC} – 265 V_{AC}), set in isolated Quasi-Resonant (QR) flyback topology with secondary side regulation (SSR), and with the following characteristics:

- 4-point average active mode efficiency at full load: > 92% (compliant with European CoC ver. 5)
- input power consumption in no-load condition: < 55 mW (@ 230 V_{AC})
- Compliant with IEC55022 Class B conducted EMI, even with reduced EMI filter
- RoHS compliant

The evaluation board has been developed using VIPerGaN65W, a new advanced offline switcher by STMicroelectronics, featuring the following characteristics:

- 700 V power GaN with embedded senseFET (Si) and HV startup
- QR operation with dynamic blanking time and adjustable valley synchronization delay functions, to maximize efficiency at any input line and load condition
- Valley–lock to ensure constant valley skipping
- Input voltage feedforward compensation for mains-independent OPP intervention
- Adaptive burst mode for advanced power management in light-load conditions
- Frequency jittering for EMI suppression

Enhanced system reliability is ensured by the built-in soft start function and by the following set of protections:

- Input OVP (settable)
- Brown-in and brown-out (settable)
- Output OVP (settable)
- Output overload
- OCP LEB
- Embedded thermal shutdown

Figure 1. **EVLVIPGAN65WF evaluation board top**

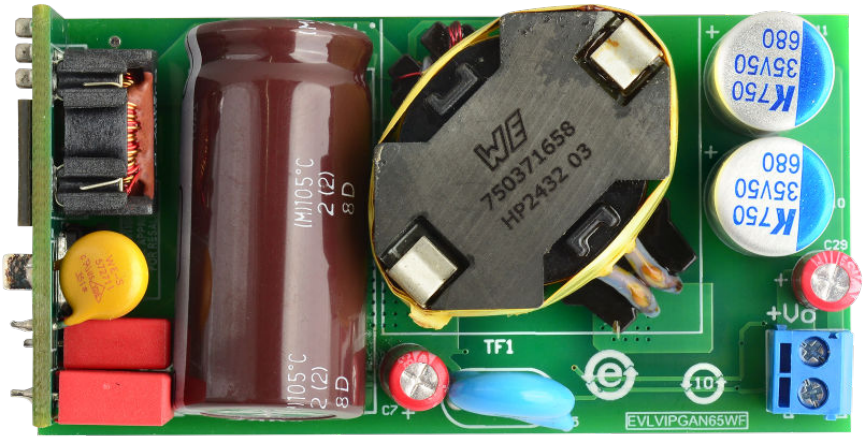
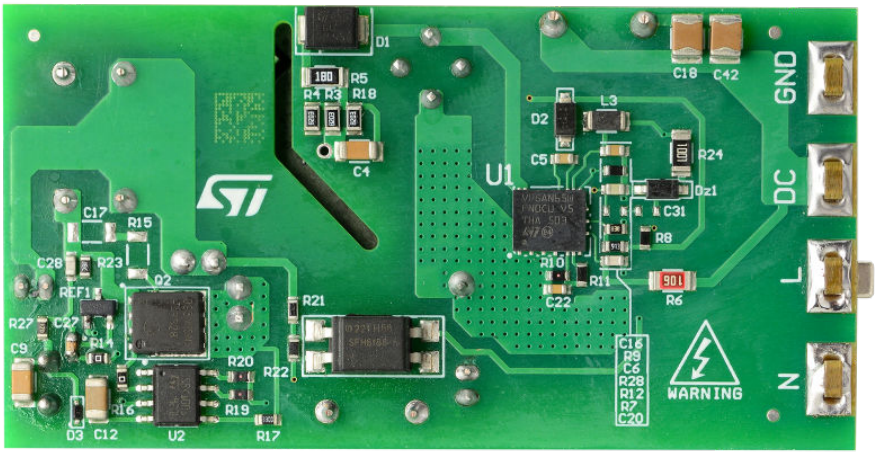


Figure 2. **EVLVIPGAN65WF evaluation board bottom**



1 Adapter features

The electrical specifications of the evaluation board are listed in Table 1

Table 1. EVLVIPGAN65WF electrical specifications

Parameter	Min.	Typ.	Max.	Unit
AC main input voltage	90		265	V_{AC}
Main frequency (f_L)	50		60	Hz
Output voltage	22.8	24	25.2	V
Output current			2.7	A
Rated output power		65		W
Output ripple voltage			50	mV
Standby input power @230 V_{AC}			55	mW
Brown in		120		V
Input OVP		395		V
Output OVP		29		V
Ambient operating temperature			60	°C

2 Circuit description

The EVLVIPGAN65WF is composed of a main board and an input board, whose schematics are shown in Figure 3 and Figure 4 respectively.

The main board contains, on the primary side: the input bulk capacitor; the VIPerGaN65W with all the related components needed for polarization and feature setting (described in detail later); and on the secondary side: the voltage reference; the voltage divider for output voltage setting; the compensation network; the output capacitors; the output rectifier, realized by a Power MOSFET driven by a synchronous rectifier for efficiency optimization; and the output connectors. An opto-coupler brings the voltage reference error signal to the primary side, to adjust the FB pin voltage level (and thus the DRAIN peak current) to the value required by the control loop for output voltage regulation.

The resistor R6, from rectified mains to the HV pin, is used to activate the internal high-voltage current source, which charges the capacitor connected between V_{DD} and GND at startup. As V_{DD} reaches V_{DD-ON} (15 V typ.), the high-voltage current source is turned off and the VIPerGaN65W starts switching. To minimize residual consumption from the mains, R6 is selected in the range of tens of MΩ.

In case of V_{DD} reduction below V_{DD-OFF} (for instance, during a fault managed in auto-restart), switching activity is immediately stopped and the high-voltage current source is activated again until the V_{DD} capacitor is recharged back to V_{DD-ON}.

When the high-voltage current source is turned off, HV is internally connected to iOVP. This allows the use of R6 also as the high-side resistor of a voltage divider sensing the rectified mains to set input overvoltage protection (low-side resistor is R11 + R10 between iOVP and GND) and brownout protection (low-side resistor is R10 between BR and GND), as described later.

QR operation is realized through the ZCD pin, connected to the transformer auxiliary winding, also used to supply the IC through the voltage divider made up by R8 and R9. When the transformer completes the energy transfer to the output, the auxiliary winding voltage decreases, and as the ZCD voltage falls below 60 mV, the GaN is enabled to switch, after some delay. The optimum value of this delay is the one for which turn-on occurs exactly at the valley of the resonance following the demagnetization, which minimizes switching losses. This delay can be determined experimentally and is easily set through the selection of R7 and R12, which form a voltage divider between auxiliary winding and TB.

The input board contains fuse, varistor, common-mode choke, diode bridges, and a π filter for rectification and EMI. It is soldered orthogonally to the main board.

3 Schematic and bill of materials

Figure 3. **EVLVIPGAN65W schematic (Main board)**

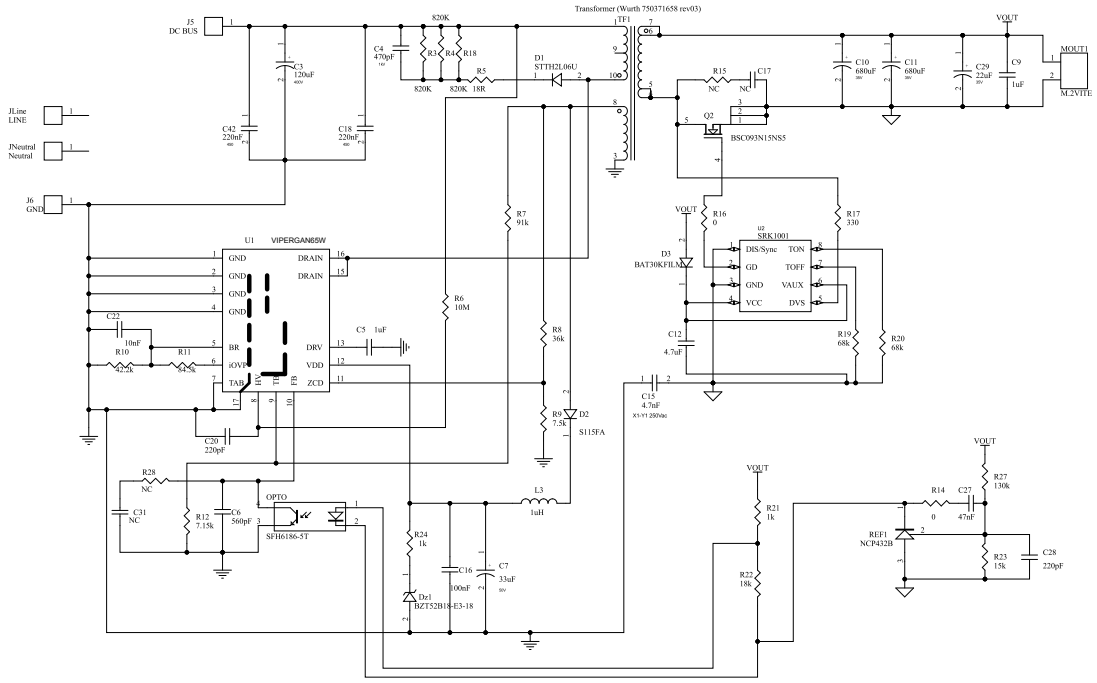


Figure 4. **EVLVIPGAN65WF schematic (Input board)**

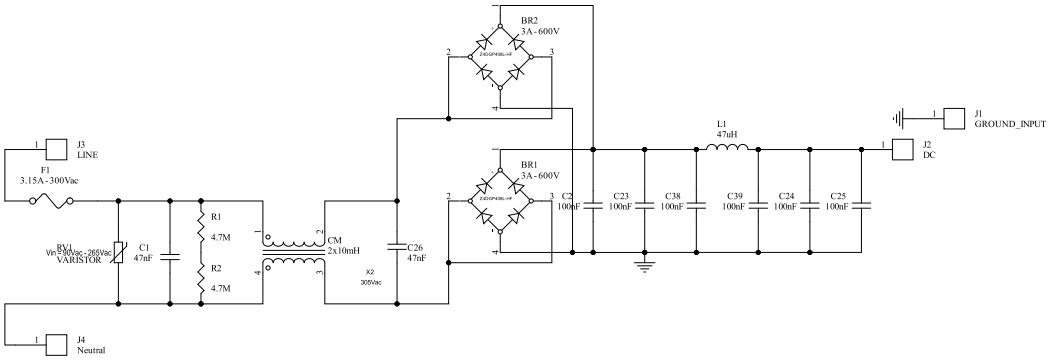


Table 2. EVLVIPGAN65WF Main Board – Bill of Materials

Ref.	Description	Part number	Package	Supplier
R3	820 kΩ ± 1% - 0.5 W – 400 V	ERJ-P06F8203V	0805	Panasonic
R4	820 kΩ ± 1% - 0.5 W – 400 V	ERJ-P06F8203V	0805	Panasonic
R5	18 Ω ± 5% - 0.66 W – 500 V	ERJP08J180V	1206	Panasonic
R6	10 MΩ ± 5% - 0.25 W – 800 V	CHV1206-JW-106ELF	1206	Bourns
R7	91 kΩ ± 1% - 0.1 W	560112116138	0603	Wurth Electronik
R8	36 kΩ ± 1% - 0.1 W	CRCW060336K0FKEA	0603	Vishay
R9	7.5 kΩ ± 1% - 0.25 W	ERJPA3F7501V	0603	Panasonic
R10	42.2 kΩ ± 1% - 0.25 W	ERJ-UP3F4222V	0603	Panasonic
R11	84.5 kΩ ± 1% - 0.33 W	ERJ-PA3F8452V	0603	Panasonic
R12	7.15 kΩ ± 1% - 0.1 W	CR0603FX-7151ELF	0603	Bourns
R14	0 Ω	RC0603FR-070RL	0603	Yageo
R15	Not mounted		1206	
R16	0 Ω	RC0603FR-070RL	0603	Yageo
R17	330 Ω ± 1% - 0.1 W	CRCW0603330RFKEA	0603	Vishay
R18	820 kΩ ± 1% - 0.5 W – 400 V	ERJ-P06F8203V	0805	Panasonic
R19	68 kΩ ± 1% - 0.25 W	ERJ-UP3F6802V	0603	Panasonic
R20	68 kΩ ± 1% - 0.25 W	ERJ-UP3F6802V	0603	Panasonic
R21	1 kΩ ± 1% - 0.1 W	ERJ-3EKF1001V	0603	Panasonic
R22	18 kΩ ± 1% - 0.1 W	CRCW060318K0FKEA	0603	Vishay
R23	15 kΩ ± 1% - 0.1 W	CR0603-FX-1502ELF	0603	Bourns
R24	1 kΩ ± 1% - 0.25 W	RC1206FR-071KL	1206	Yageo
R27	130 kΩ ± 1% - 0.1 W	CR0603-FX-1303ELF	0603	Bourns
D1	STTH2L06U 2 A/600 V Fast switching diode	STTH2L06U	DO-214AA (SMB)	STMicroelectronics
D2	S115FA 1 A/150 V Schottky diode	S115FA	SOD123FA2	ONSemiconductor
D3	BAT30KFILM 300 mA/30 V Small signal Schottky diode	BAT30KFILM	SOD-523	STMicroelectronics
Dz1	BZT52B18-E3-18 18 V/500 mW Zener diode	BZT52B18-E3-18	SOD-123	Vishay
L3	1 µH ± 10% - 100 mA	7447915	1206	Wurth Electronik
TF1	500 µH Flyback transformer	750371658 rev03	RM10	Wurth Electronik
C3	120 µF - 400 V Electrolytic capacitor	EKHF401ELL121MLN3S	t. h.	Chemi-con
C4	470 pF – 1000 V MLCC capacitor	885342208017	1206	Wurth Electronik
C5	1 µF – 25 V MLCC capacitor	885012106022	0603	Wurth Electronik
C6	560 pF ± 5% - 50 V MLCC capacitor	VJ0603A561JXAAC	0603	Vishay
C7	33 µF – 50 V Electrolytic capacitor	860010672011	t. h.	Wurth Electronik
C9	1 µF – 50 V MLCC capacitor	885012208093	1206	Wurth Electronik
C10	680 µF ± 20% - 35 V AL Electrolytic capacitor	A750MW687M1VAAE018	t. h.	Kemet
C11	680 µF ± 20% - 35 V AL Electrolytic capacitor	A750MW687M1VAAE018	t. h.	Kemet
C12	4.7 µF ± 10% - 50 V MLCC capacitor	885012208094	1206	Wurth Electronik
C15	4.7 nF – 250 Vac Y1 capacitor	DE1E3RA472MA4BN01F	t. h.	Murata

Ref.	Description	Part number	Package	Supplier
C16	100 nF – 50 V MLCC capacitor	885012206095	0603	Wurth Electronik
C17	Not mounted		1206	
C18	220 nF – 450 V MLCC capacitor	CGA6M4X7T2W224K200AE	1210	TDK
C20	220 pF – 250 V MLCC capacitor	885342006004	0603	Wurth Electronik
C22	10 nF – 100 V MLCC capacitor	885012206114R	0603	Wurth Elektronik
C27	47 nF – 50 V MLCC capacitor	885012206093	0603	Wurth Elektronik
C28	220 pF ± 5% - 50 V MLCC capacitor	885012006059	0603	Wurth Elektronik
C29	22 µF ± 20% - 35 V Electrolytic capacitor	860010572003	t. h.	Wurth Elektronik
C42	220 nF – 450 V MLCC capacitor	CGA6M4X7T2W224K200AE	1210	TDK
Q2	150 V - 9.3 mΩ, V_{GS_th} = 3 V Nchannel Power Mosfet	BSC093N15NS5ATMA1	PowerFLAT-5x6-8	Infineon
OPTO	SFH6186-5T optocoupler	SFH6186-5T	SMD-4	Vishay
U1	VIPerGaN65W HV switcher	VIPerGaN65W	QFN 5x6	STMicroelectronics
U2	SRK1001 Synchronous rectification controller	SRK1001	SO8	STMicroelectronics
REF1	NCP432BVSNT1G voltage reference	NCP432BVSNT1G	SOT23-3	ONSemiconductor
MOUT1	Output connector	1776275-2	t. h.	TE Connectivity

Table 3. EVLVIPGAN65WF Input Board – Bill of Materials

Ref.	Description	Part number	Package	Supplier
BR1	800 V – 4 A Bridge rectifier	Z4DGP408L-HF	Z4-D-4	Comchip Technology
BR2	800 V – 4 A Bridge rectifier	Z4DGP408L-HF	Z4-D-4	Comchip Technology
C1	47 nF – 310 Vac X2 capacitor	890334023015	t. h.	Wurth Elektronik
C2	100 nF ±10% - 450 V MLCC capacitor	C3216X7T2W104K160AE	1206	TDK
C23	100 nF ±10% - 450 V MLCC capacitor	C3216X7T2W104K160AE	1206	TDK
C24	100 nF ±10% - 450 V MLCC capacitor	C3216X7T2W104K160AE	1206	TDK
C25	100 nF ±10% - 450 V MLCC capacitor	C3216X7T2W104K160AE	1206	TDK
C26	47 nF – 310 Vac X2 cap	890334023015	t. h.	Wurth Elektronik
C38	100 nF ±10% - 450 V MLCC capacitor	C3216X7T2W104K160AE	1206	TDK
C39	100 nF ±10% - 450 V MLCC capacitor	C3216X7T2W104K160AE	1206	TDK
CM	10 mH - 1.2 A Common Mode Choke	CJ5094-CLD	SMT	Coilcraft
F1	3 A – 250 Vac Fuse	0443003.DR	SMT	Littelfuse
L1	47 µH Power choke	SRN8040TA-470M	SMT	Burns
R1	4.7 MΩ ± 5% - 0.25 W	CRCW12064M70JNEA	1206	Vishay Dale
R2	4.7 MΩ ± 5% - 0.25 W	CRCW12064M70JNEA	1206	Vishay Dale
RV1	275 Vac Disk varistor	820572711	t. h.	Wurth Elektronik

4 Transformer

Transformers' electric and mechanical characteristics are shown in the table and figures below

Table 4. Transformer characteristics

Parameter	Value	Test conditions
Manufacturer	WURTH	
Part number	750371658 rev03	
Primary inductance (10 – 1)	0.5 mH ±10%	10 kHz, 100 mV, Ls
Leakage inductance (10 – 1)	7.5 µH typ, 9.5 µH max	tie (3+8+4+5+6+7),100 kHz, 100 mV, Ls
Primary to aux turn ratio	10:1	(10-1):(8-3)
Primary to sec turn ratio	5:1	(10-1):(6-4), tie (6+7, 4+5)
Saturation current (10 – 1)	4 A typ.	20% roll-off from initial
Operating current (10 – 1)	3.5 A max	
DC-DC resistance (10 – 1)	0.407 Ω ± 10%	@20°C
DC-DC resistance (6 – 4)	0.027 Ω ± 20%	tie (6+7, 4+5), @20°C
DC-DC resistance (8 – 3)	0.109 Ω ± 10%	@20°C
Dielectric (10 – 6)	3650 V_{AC}, 1 minute	tie (1+8, 6+7, 4+5)

Figure 5. Transformer electrical schematic (on the left); pin diagram bottom view (on the right)

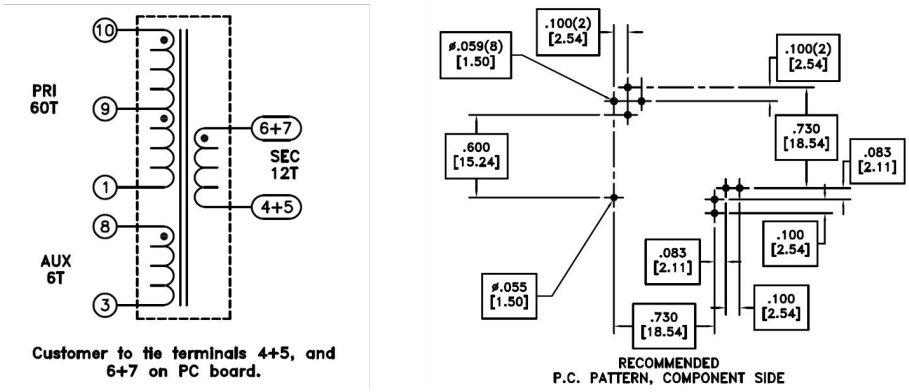
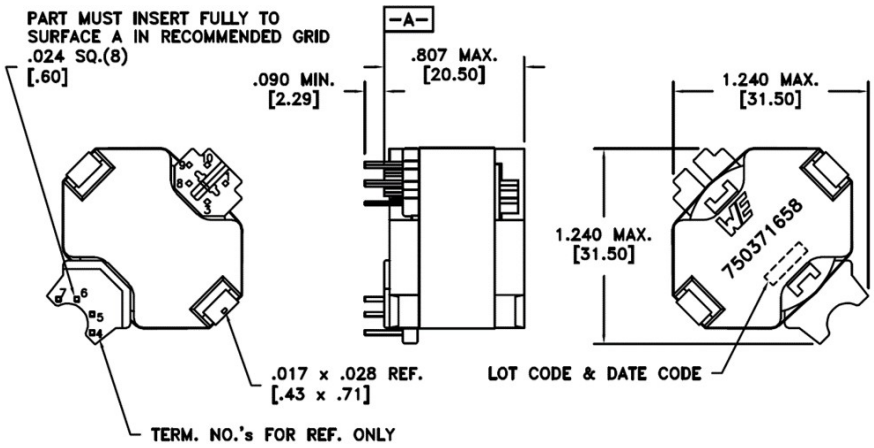


Figure 6. **Transformer size**



5 Testing the board

5.1 Efficiency

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75%, and 100% of maximum load, at nominal input voltages (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}).

External power supplies (the power supplies contained in a separate housing from the end-use devices they are powering) must comply with the Code of Conduct, version 5 "Active mode efficiency" criterion, which states that an SMPS with a power throughput of 65 W should have an active mode efficiency higher than 89.16%.

Another standard to be applied is the DOE (Department of energy) recommendation, whose active mode efficiency requirement for the same power throughput is 87.50%.

As shown in the following tables, the SMPS is compliant with both standards.

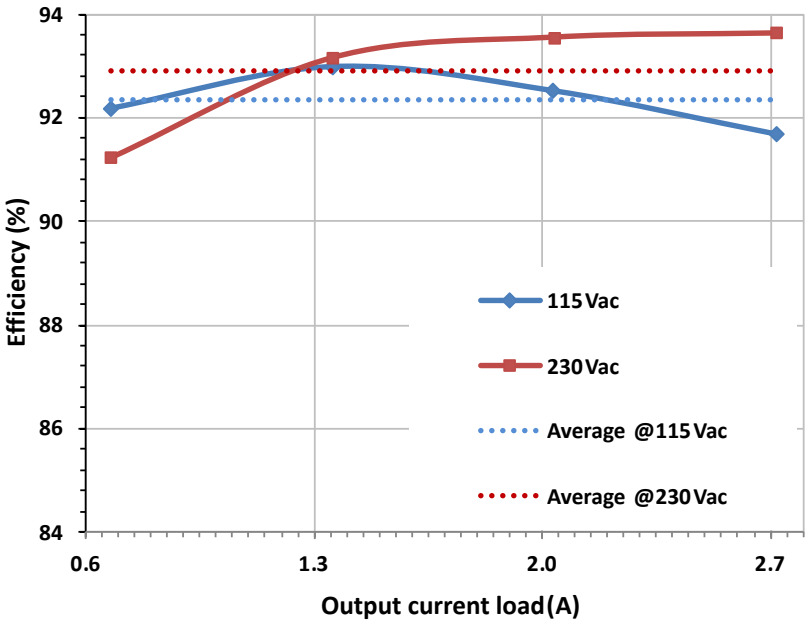
Table 5. Average efficiency at 115 V_{AC}

%Load	I_{OUT} (A)	V_{OUT} (V)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
25%	0.676	24.032	17.616	16.246	92.22
50%	1.356	24.003	34.995	32.548	93.01
75%	2.035	23.968	52.722	48.775	92.51
100%	2.717	23.934	70.911	65.029	91.71
Average efficiency					**92.36**

Table 6. Average efficiency at 230 V_{AC}

%Load	I_{OUT} (A)	V_{OUT} (V)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
25%	0.678	23.971	17.818	16.252	91.21
50%	1.358	23.957	34.929	32.534	93.14
75%	2.038	23.924	52.110	48.757	93.57
100%	2.719	23.900	69.412	64.984	93.62
Average efficiency					**92.89**

Figure 7. **Efficiency vs. Output current load**



5.2 Light-load performances

Figure 8. No load consumption vs. V_{IN}

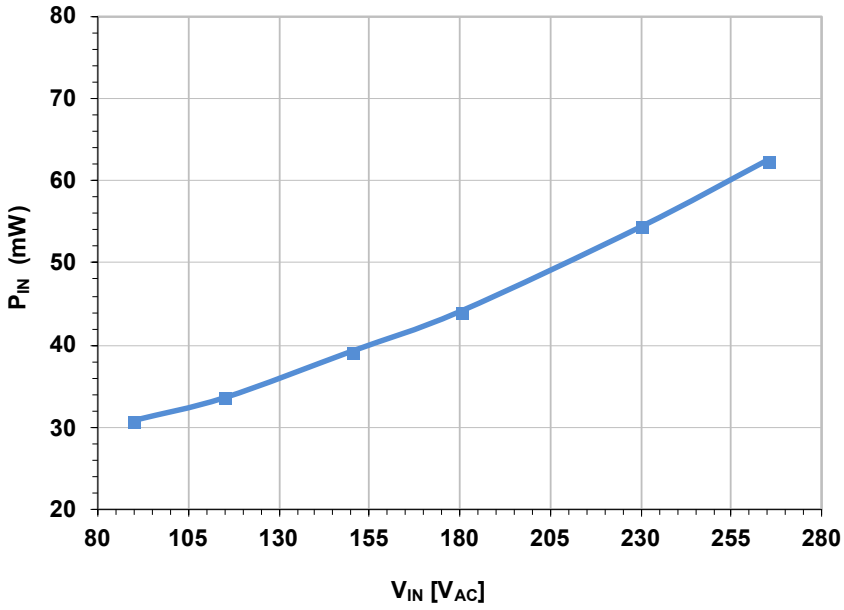
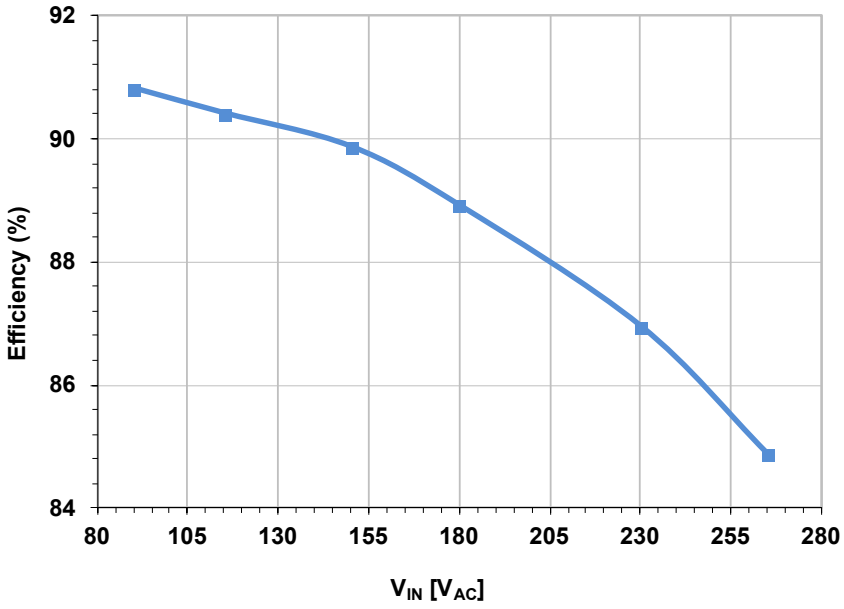


Figure 9. Efficiency @ 10% output load vs. V_{IN}



For a 65W SMPS, the CoC5 requirement at 10% of output load is 79%.

5.3 Typical waveforms

Drain voltage waveforms under full-load condition for the two nominal input voltages are shown in Figure 10 and Figure 11, while the corresponding waveforms for minimum and maximum input voltage are shown in Figure 12 and Figure 13, respectively.

Figure 10. 115 V_{AC} full load V_{DRAIN} & I_{DRAIN}

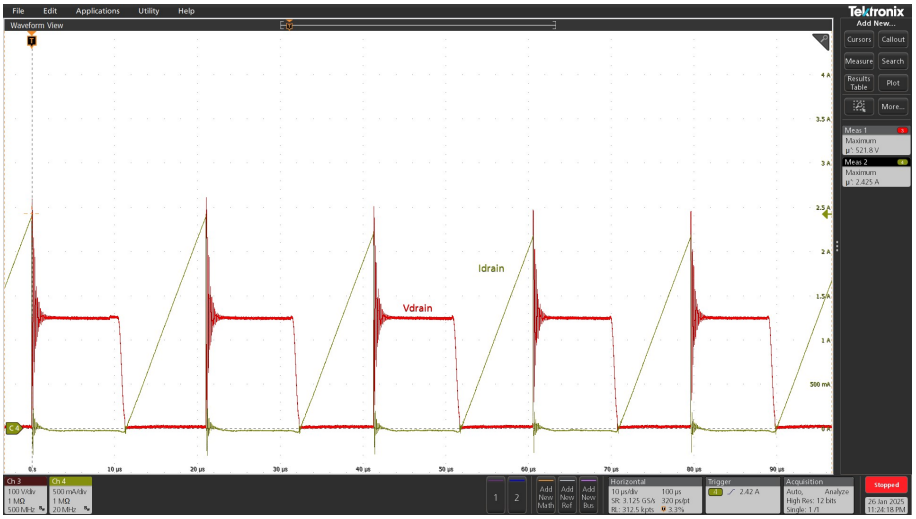


Figure 11. 230 V_{AC} full load V_{DRAIN} & I_{DRAIN}

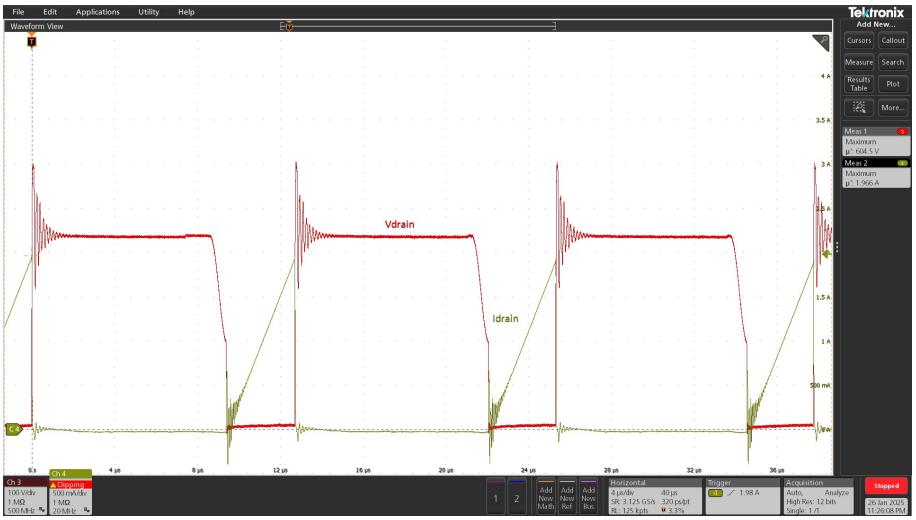


Figure 12. 90 V_{AC} full load V_{DRAIN} & I_{DRAIN}

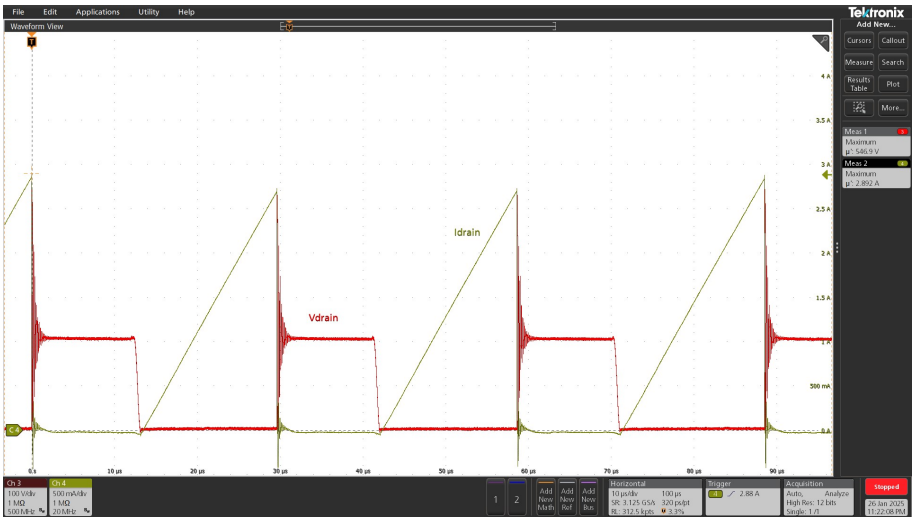
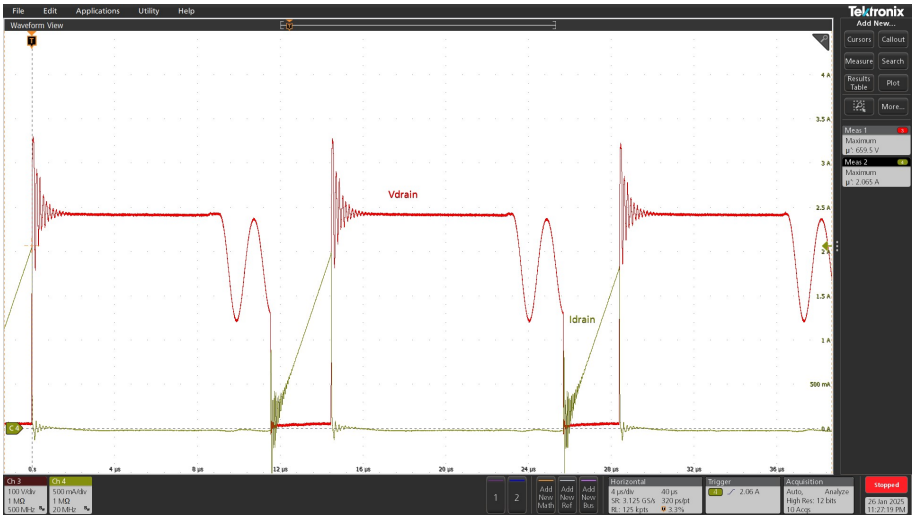


Figure 13. 265 V_{AC} full load V_{DRAIN} & I_{DRAIN}



6 ICs features

6.1 Turn-on delay (TB)

In VIPerGaN65W, transformer demagnetization sensing for QR or valley skipping operation is carried out by monitoring V_{ZCD}, which is a replica of the auxiliary winding voltage.

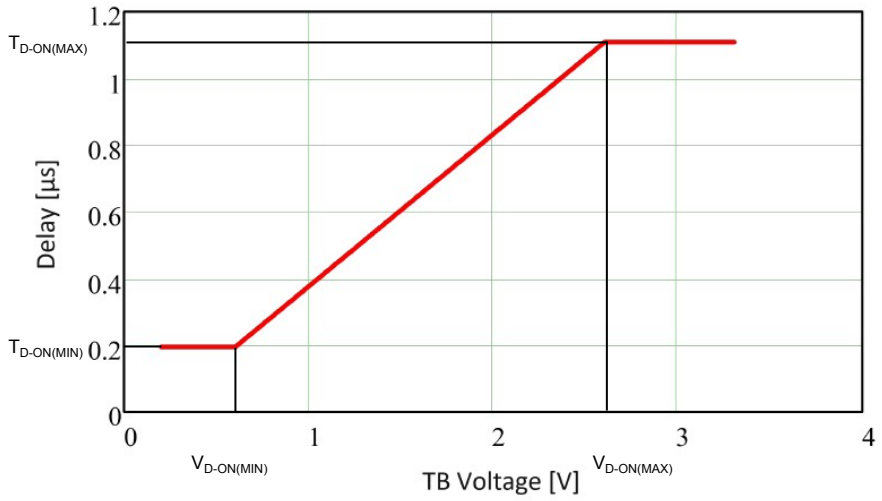
In particular, the GaN turn-on is enabled when V_{ZCD} falls below the internal triggering threshold V_{ZCDT} (60 mV, typ.), with a certain delay T_{DELAY}, to allow V_{DRAIN} to reach the oscillation valley in the meantime.

Since the frequency of the DRAIN oscillation after demagnetization depends on the transformer's parasitics, the value T_{DELAY_OPT}, which synchronizes the GaN turn-on exactly with the valley of V_{DRAIN} (thus minimizing switching losses), can vary between designs. For this reason, VIPerGaN65W provides the possibility to set this value externally.

If TB is connected to GND (or V_{TB}< 0.6 V), T_{DELAY} is set to the default $T_{D\text{-}ON(MIN)}$ (197 ns typ.)

If TB is connected to a voltage divider, T_{DELAY} depends on the V_{TB} measured at the end of the precedent turn-off, ranging from $T_{D\text{-}ON(MIN)}$ (at V_{TB} = 0.6 V) to $T_{D\text{-}ON(MAX)}$ = 1.1 µs (at V_{TB} = 2.5 V), as shown in the figure below.

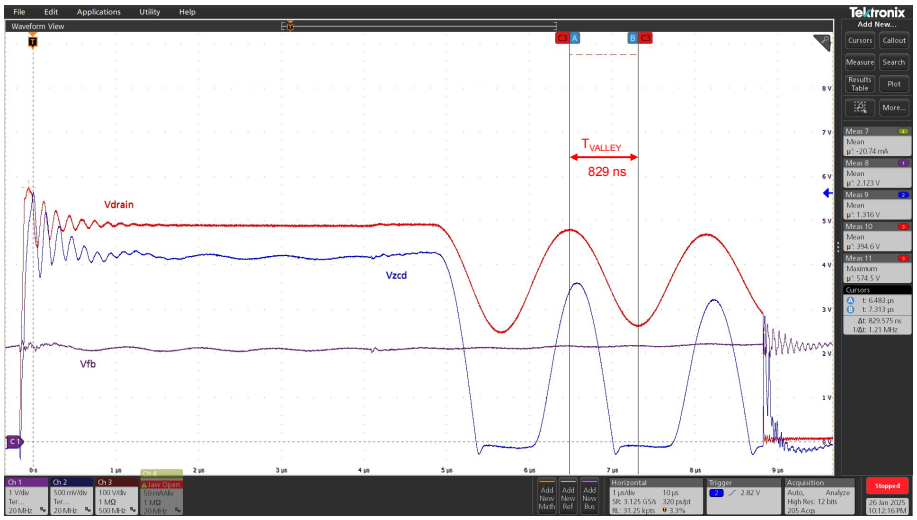
Figure 14. Typical turn-on delay after triggering as a function of the voltage on the TB pin



The optimum value of T_{DELAY} can be found experimentally as follows:

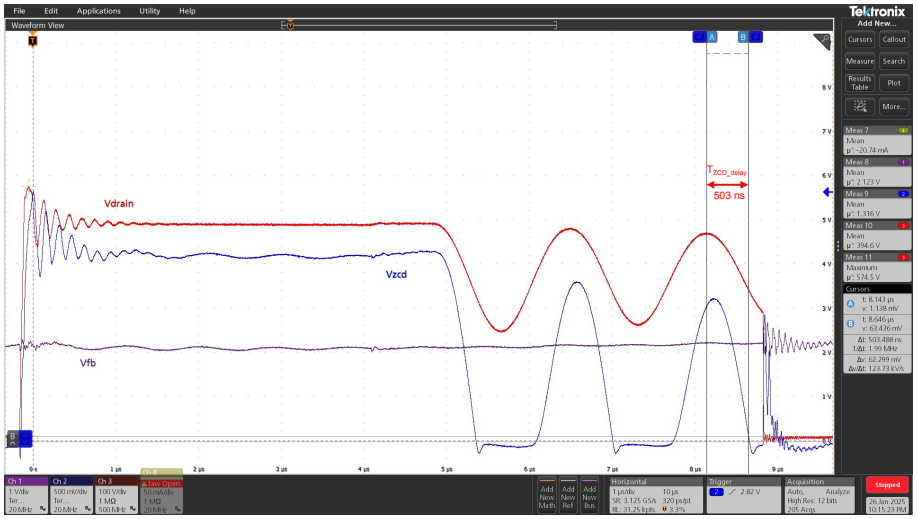
- TB is connected to GND; input voltage and output load are set so that the converter is operated in valley-skipping mode.
- T_{VALLEY} is measured as the time interval between a peak and the next valley of the DRAIN ringing after demagnetization (see Figure 15).

Figure 15. **Measure of T_{VALLEY} with TB connected to GND**



- T_{ZCD_delay} is measured as the time interval between the peak of the DRAIN ringing after demagnetization and the moment when the falling V_{ZCD} crosses the triggering threshold V_{ZCDT} with a negative slope (see Figure 16).

Figure 16. **Measure of T_{ZCD_delay} with TB connected to GND**



T_{DELAY_OPT} is the value of T_{DELAY} which satisfies the following equation:

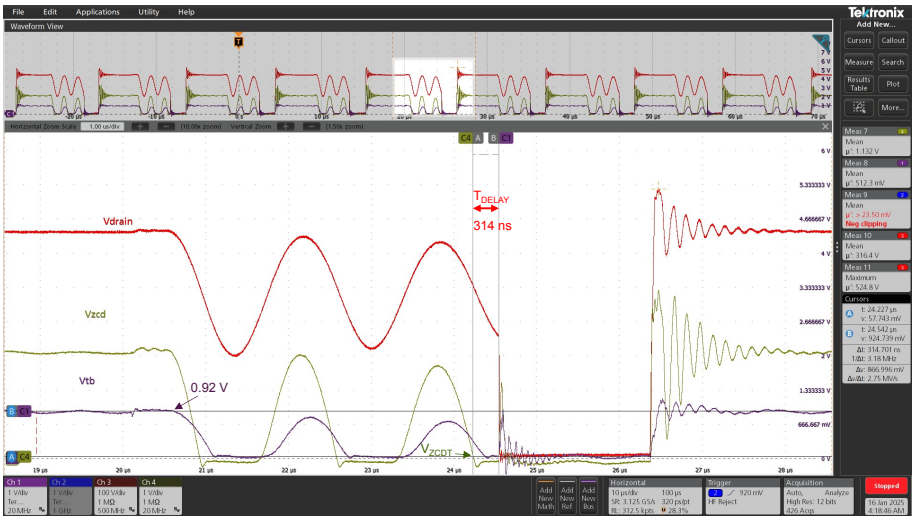
$$T_{DELAY\_OPT} = T_{VALLEY} - T_{ZCD\_delay} \quad (1)$$

From the above measurements: T_{VALLEY} = 829 ns and T_{ZCD_delay} = 503 ns → from Eq. (1) T_{DELAY_OPT} = 326 ns.
From Figure 14, T_{DELAY_OPT} = 326 ns corresponds to V_{TB_OPT} = 0.9 V, which, inserted in Eq. (2), allows calculation of the low-side resistor R_{delay_OPT} = R12 to get T_{DELAY_OPT}:

$$R_{delay\_OPT} = \frac{R_{TB}}{\frac{N_{AUX}}{N_{SEC}} \bullet \frac{V_{OUT}}{V_{TB\_OPT}} - 1} \quad (2)$$

Considering that N_{AUX}/N_{SEC} = 0.5; V_{OUT} = 24 V; R_{TB} = R7 = 91 kΩ, the result is R_{delay_OPT} = 7.5 kΩ.
The commercial value of 7.15 kΩ has been used, resulting in the actual value T_{DELAY_OPT} = 315 ns.
Figure 17 shows that, with this selection (V_{TB} = 0.92 V), turn-on occurs exactly at the valley of the DRAIN voltage ringing after demagnetization.

Figure 17. Valley switching with R_{DELAY} = 7.15 kΩ, V_{TB} = 0.92 V



6.2 Line Voltage feedforward

In QR operation, the switching frequency increases with the input voltage, and since the overcurrent setpoint is fixed, the deliverable output power can vary significantly from minimum to maximum input voltage, reaching a difference of more than twice in the case of wide-range mains applications.

In wide-range mains applications, the deliverable power at high line can be more than twice than at minimum voltage. This is problematic because the power supply must be designed to safely sustain the maximum power during overload events, although the maximum output load cannot exceed the power capability at low line.

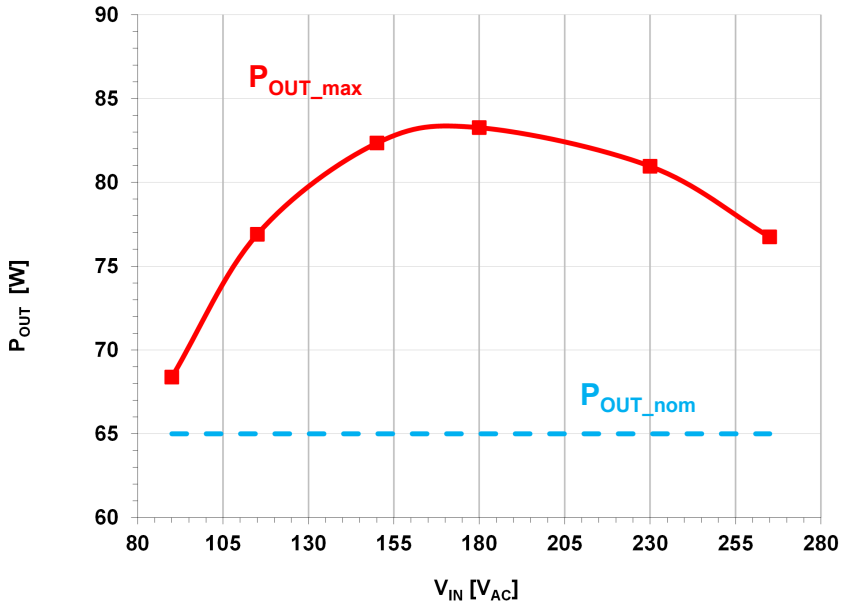
To solve this issue, the current sourced from the ZCD pin through the R8 resistor during GaN's ON-time, given by the following formula:

$$I_{FF} = \frac{N_{AUX}}{N_{PRI}} \bullet \frac{V_{IN}}{R_8} \quad (3)$$

is internally mirrored and used to reduce the overcurrent setpoint, in proportion to the input voltage. The optimum R8 value is that for which the maximum deliverable output power remains the same at both extremes of the input voltage range.

After bench tests, the value of 36 kΩ has been found, resulting in the power throughput shown in the figure below.

Figure 18. Max deliverable output power vs V_{IN} with feedforward compensation



6.3 Step load response

The undershoot/overshoot of the output voltage following a step load from no load to 2.7 A (max load), and vice versa, remains within 2% of the nominal value.

Figure 19. **Dynamic step load (I_{OUT} from 0 to 2.7 A) at 115 V_{AC}**

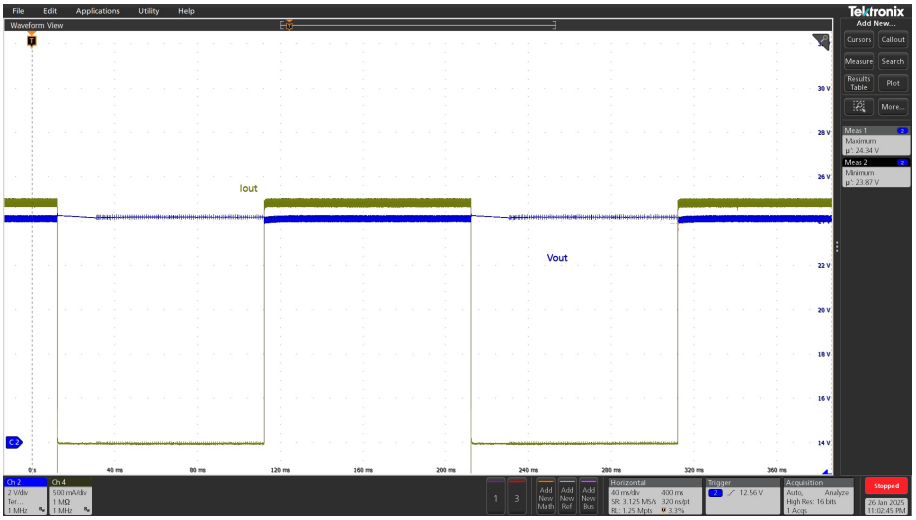
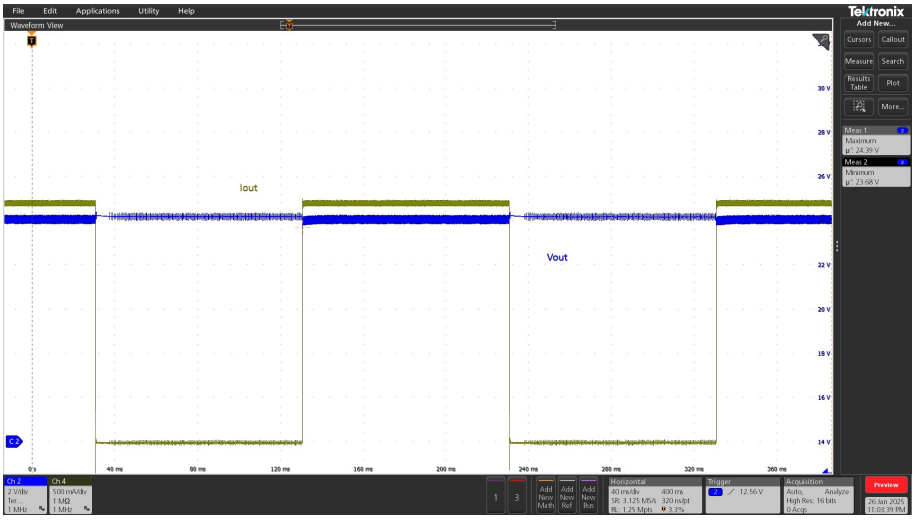


Figure 20. **Dynamic step load (I_{OUT} from 0 to 2.7 A) at 230 V_{AC}**



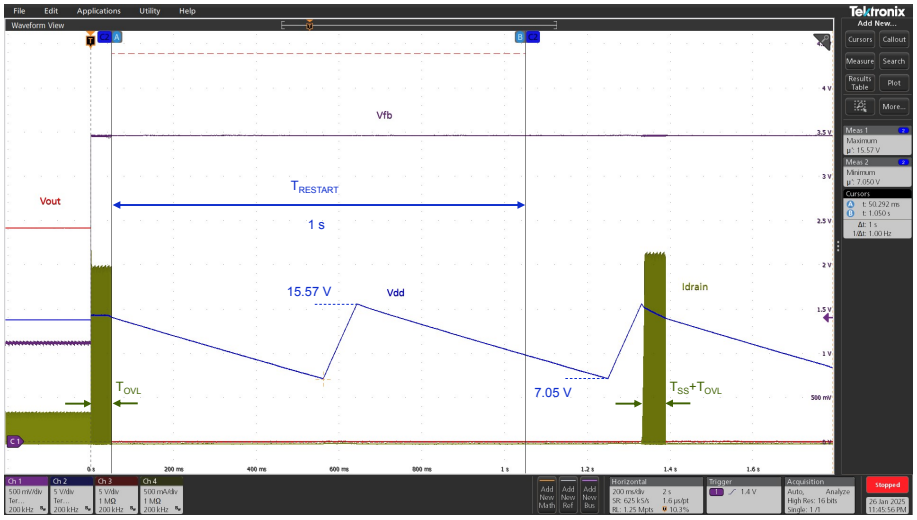
6.4 Overload Protection

To manage an overload or short-circuit condition, an internal up/down counter is incremented or decremented with an internal clock, depending on whether V_{FB} is above or below the upper saturation limit V_{FBH}.

In case of a permanent overload or short-circuit event, the protection is tripped after a delay time equal to T_{OVL} (50 ms typical value). The IC is then shut down and maintained off for a time equal to $T_{RESTART}$ (1 s typical value). During overload condition, V_{DD} is maintained between V_{DD-ON} and $V_{DD-RESTART}$ (15 V and 7 V typ. values, respectively) by the periodical activation of the internal HV current source.

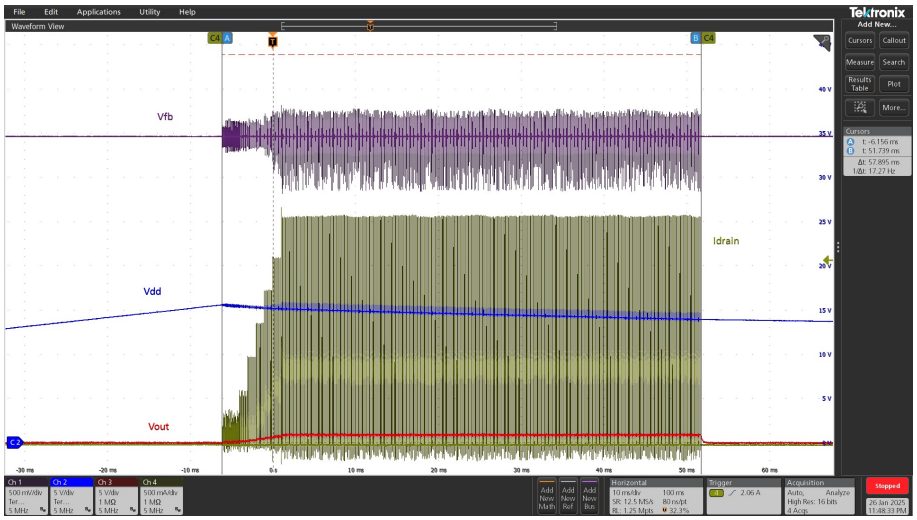
After $T_{RESTART}$, the device waits for the first V_{DD-ON} crossing, then restarts. If the fault persists, the protection remains active indefinitely in the same way, as shown in Figure 21. This ensures a low repetition rate of restart attempts, allowing the converter to operate safely with very low power throughput and preventing the IC overheating in case of repeated overload events.

Figure 21. Output short circuit applied



At any restart attempt, soft start is invoked (see Figure 22).

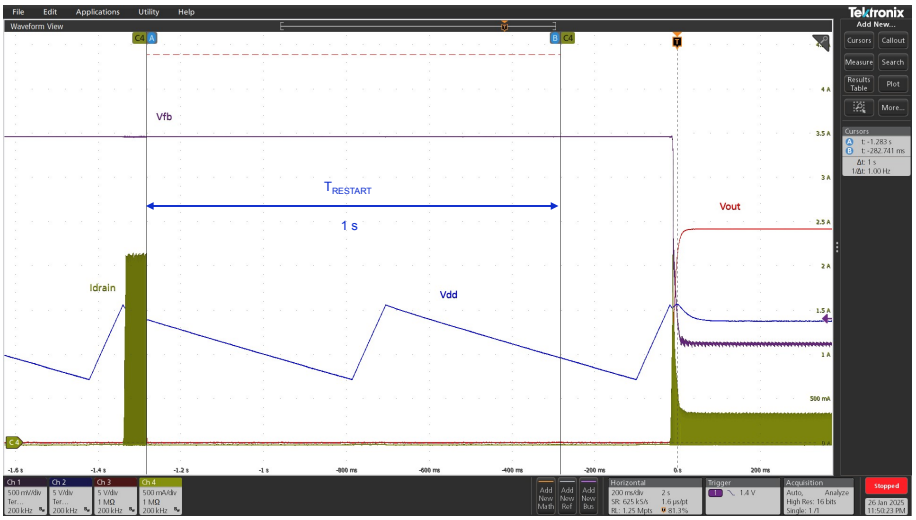
Figure 22. Output short circuit steady state, restart attempts with soft start



After the fault removal, the IC resumes normal operation (Figure 23). If the fault is removed during T_{SS} or T_{OVL} (that is, before the protection is triggered), the counter is decremented on a cycle-by-cycle basis down to zero, and the protection is not tripped.

If the short-circuit is removed during $T_{RESTART}$, the IC waits until $T_{RESTART}$ has elapsed and V_{DD} has recharged to V_{DD-ON} before resuming switching.

Figure 23. Output short circuit removed and IC restart



6.5 Input overvoltage protection

To avoid exceeding the GaN's breakdown voltage due to an overvoltage on the main line, an input overvoltage protection circuit is implemented. It connects the rectified input voltage mains to iOVP and GND through a voltage divider.

The input overvoltage level is set considering that:

- after startup, an internal switch connects iOVP to HV, which senses the rectified input voltage mains;
- when V_{iOVP} exceeds the internal threshold V_{iOVP_th} (5 V, typ.) for more than T_{iOVP} (250 µs, typ.), switching activity is inhibited and resumes only when V_{iOVP} falls below V_{iOVP_th}. The delay time T_{iOVP} is intended to filter out possible disturbances that may be coupled during operation and is implemented through an up/down counter. During protection, V_{DD} is recycled between $V_{DD-RESTART}$ and V_{DD-ON} by the periodic activation of the internal HV current source.

In this evaluation board, the input OVP level is set at about 400 V_{DC}. Triggering, steady-state, and restart after fault removal are shown in the following figures, where V_{BULK} is the DC voltage appearing across the input bulk capacitor C3.

Figure 24. Input OVP triggered

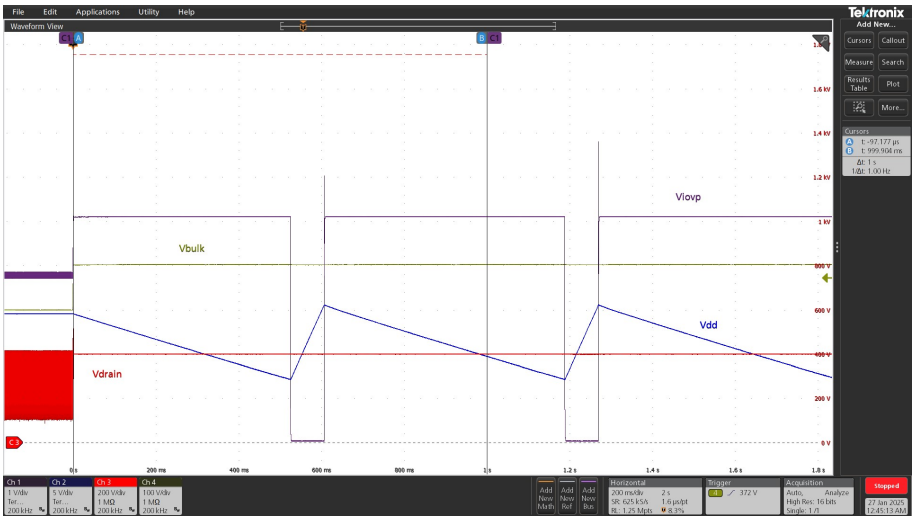


Figure 25. Input OVP triggered, T_{iOVP}

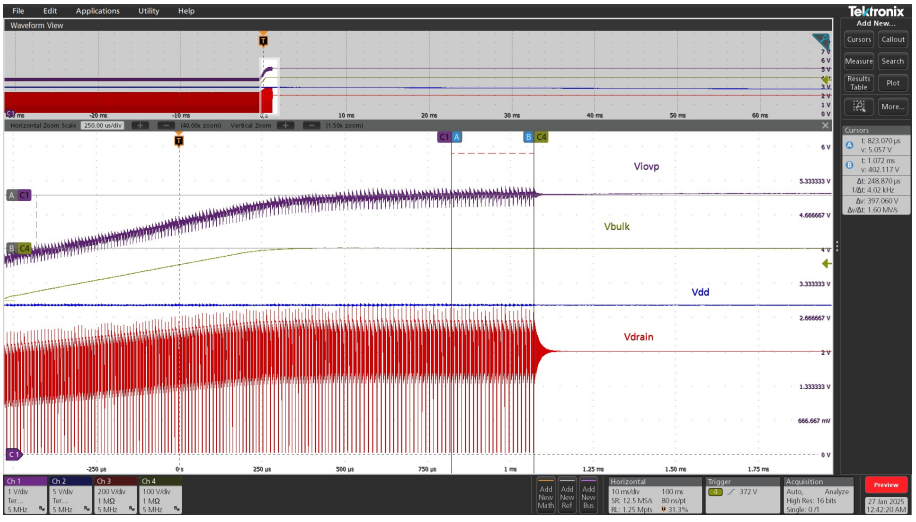


Figure 26. **Input OVP steady state**

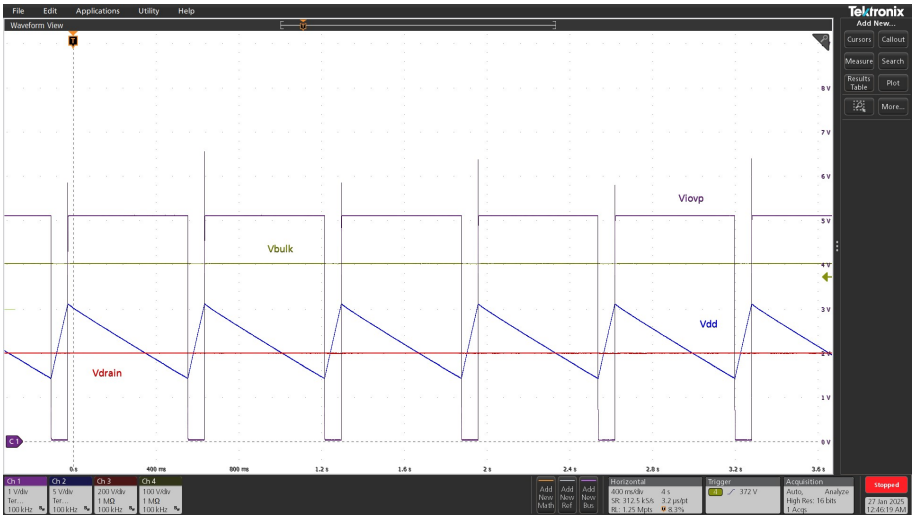
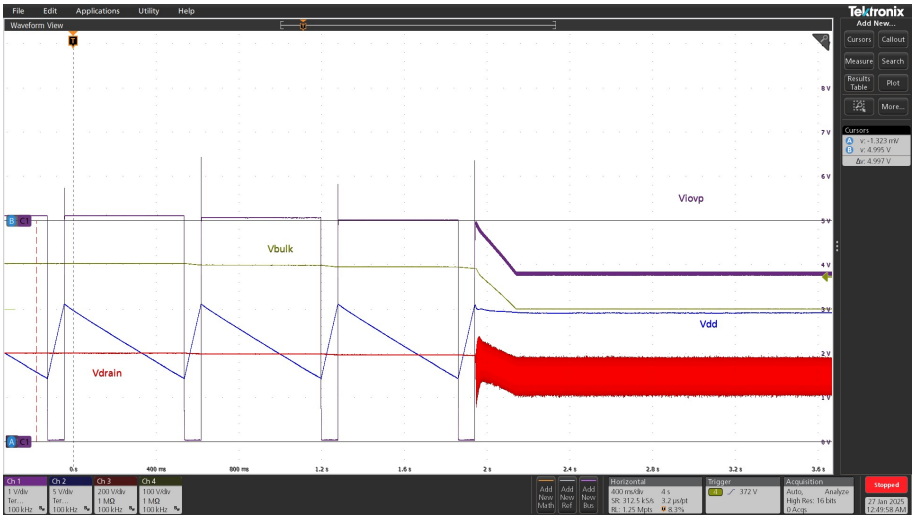
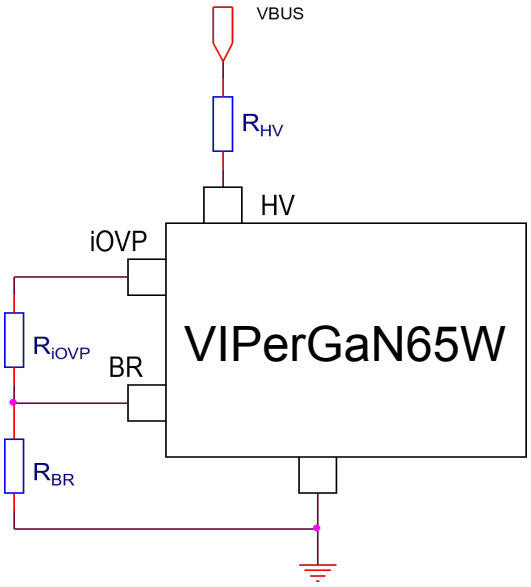


Figure 27. **Input OVP removed and normal operation restored**



To get minimal component count, the high-side resistor of the HV/iOVP voltage divider, R_{HV} (=R6 in the schematic of Figure 3), is also used for brown-in/brown-out protection setting, with the connection shown in the figure below.

Figure 28. Setting for input OVP, brown in and brown out setting (R_{HV} = R6, R_{iOVP} = R11, R_{BR} = R10)



The formulas to calculate R_{iOVP} and R_{BR} (= R11 and R10 of the BOM, respectively) taking both protections into account are given in Eq. (4) and Eq. (5).

To disable input overvoltage protection, iOVP should be connected to BR.

6.6 Brown-out and brown-in

The minimum input voltage from which the converter starts operating (brown-in), and the minimum input voltage below which the converter stops operating (brown-out), are set through the voltage divider sensing the rectified input voltage mains to BR.

In fact, if V_{BR} falls below the internal threshold $V_{BR\text{-}OUT}$ (0.4 V typ.) for more than $T_{BR\text{-}OUT}$ (30 ms, typ.), the VIPerGaN65W stops switching. If V_{BR} exceeds the internal threshold $V_{BR\text{-}IN}$ (0.5 V typ.) for more than $T_{BR\text{-}IN}$ (250 µs, typ.), the VIPerGaN65W resumes switching.

The delay times are implemented through up/down counters to reject temporary disturbances across the line. $T_{BR\text{-}OUT}$ is also intended to avoid false protection triggering due to input capacitor voltage ripple and to guarantee some hold-up in case of a missing cycle on the input line.

The resistor values are selected according to the equations below:

$$R_{iOVP} = R_{HV} \bullet \left(\frac{V_{iOVP\_th}}{V_{IN-OVP}} - \frac{V_{BR-IN}}{V_{IN-ON}} \right) \quad (4)$$

$$R_{BR} = R_{HV} \bullet \frac{V_{BR-IN}}{V_{IN-ON} - V_{BR-IN}} \quad (5)$$

where $V_{IN\text{-}ON}$ and $V_{IN\text{-}OVP}$ are the DC input voltages triggering brown-in and input overvoltage protection, respectively. The DC input voltage triggering brown-out, $V_{IN\text{-}OFF}$, is directly linked to $V_{IN\text{-}ON}$ according to Eq. (6):

$$V_{IN-OFF} = V_{IN-ON} \bullet \frac{V_{BR-OUT}}{V_{BR-IN}} \quad (6)$$

The resistor R_{HV}, used to start up the converter and also as part of the iOVP and BR voltage divider, is arbitrary. It is recommended to be a few tens of MΩ at least, to minimize residual consumption from the input mains.

Brown-in and input overvoltage specs values (see Table 1) inserted in Eq. (4) give R_{iOVP} = 84.9 kΩ (= R11 of the BOM). Input overvoltage spec inserted in Eq. (5) gives R_{BR} = 41.84 kΩ (= R10 of the BOM).

The commercial values R11 = 84.5 kΩ and R10 = 42.2 kΩ are selected, and the actual values $V_{IN\text{-}ON\text{-}act}$ = 119 V and $V_{IN\text{-}OVP\text{-}act}$ = 396 V are calculated. From Eq. (6), $V_{IN\text{-}OFF\text{-}act}$ is calculated as 95 V.

The bench check gives: $V_{IN\text{-}OVP}$ = 402 V, $V_{IN\text{-}OFF}$ = 94 V and $V_{IN\text{-}ON}$ = 119 V (see Figure 25, Figure 29 and Figure 31 respectively), which are quite in line with expectations.

Figure 29. Brown-out triggered and IC stop

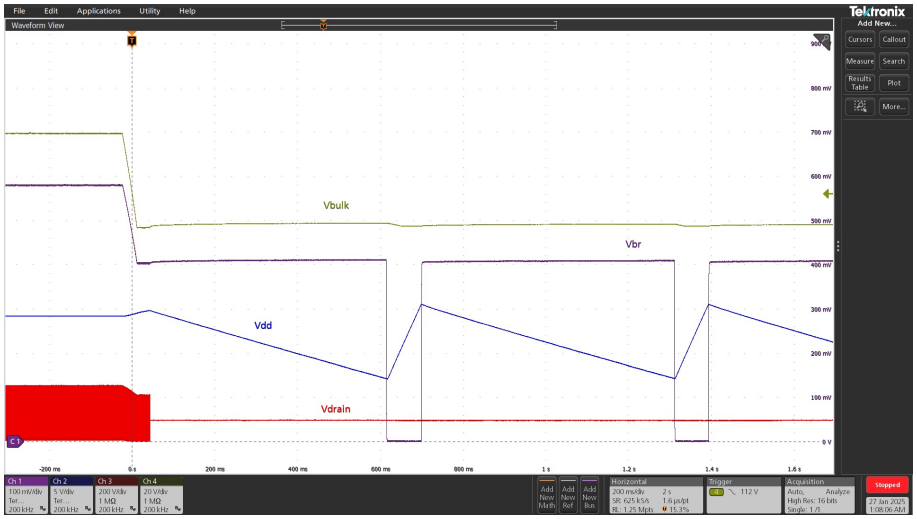


Figure 30. **Brown-out triggered and IC stop, T_{BR-OUT} detail**

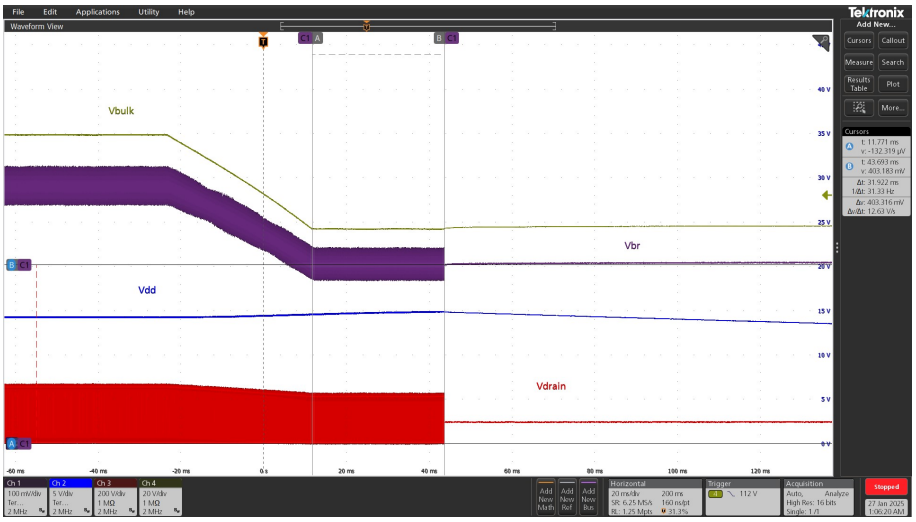


Figure 31. **Brown-in triggered and IC restart**

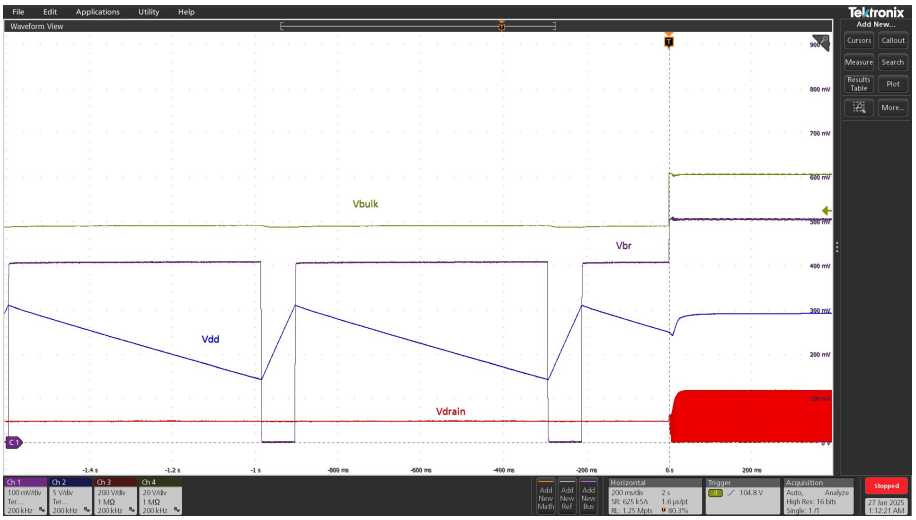
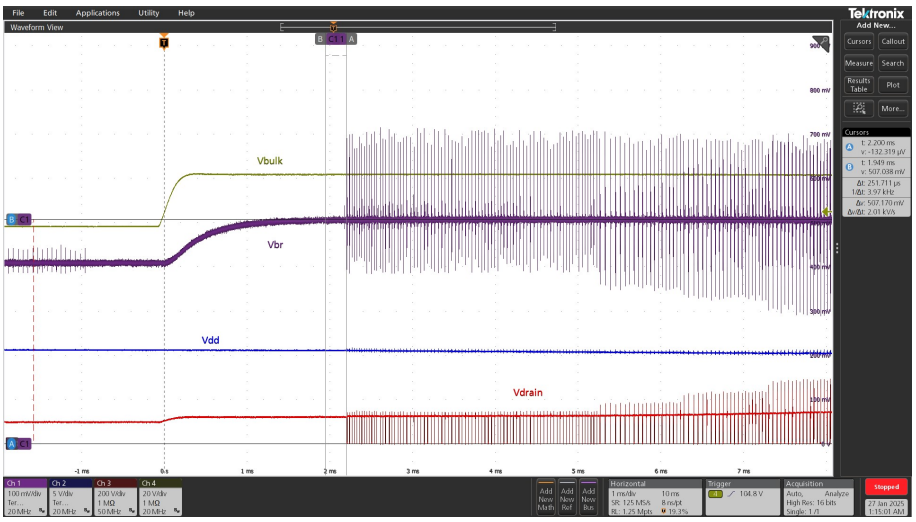


Figure 32. **Brown-in triggered and IC restart, T_{BR-IN} detail**



A 10 nF filter capacitor placed between BR pin and GND is necessary to avoid misbehavior of the brown-out logic when the high-voltage startup unit is activated.

The power consumption of the input overvoltage/brown-in/brown-out network can be calculated as:

$$Pin_{iOVP-BRin-BRout} = \frac{V^2{}_{IN}}{(R_{HV} + R_{OVP} + R_{BR})} \quad (7)$$

which results in about 10 mW consumption at 230 V_{AC} (~325 V_{DC}).

To disable input overvoltage protection, BR should be connected to GND.

6.7 Output overvoltage protection

The voltage on the ZCD pin is monitored at the end of the transformer's demagnetization, when the auxiliary winding accurately tracks the converter output voltage, and is compared with an internal reference. If the sampled voltage exceeds the internal OVP reference V_{OVP} (2.5 V typ.), an overvoltage condition is assumed. In this case, switching is inhibited for $T_{RESTART}$, and V_{DD} is recycled between $V_{DD\text{-}RESTART}$ and $V_{DD\text{-}ON}$ by the periodical activation of the HV current source.

The value of the low-side resistor of the ZCD voltage divider, R9, required to activate the OVP protection at a certain output voltage level $V_{OUT\text{-}OVP}$, can be found through the following formula:

$$R_9 = \frac{V_{OVP}}{\frac{N_{AUX}}{N_{SEC}} \bullet (V_{OUT-OVP} + V_{DSEC}) - V_{OVP}} \bullet R_8 \quad (8)$$

where R8 is the high-side resistor of the ZCD voltage divider (already selected based on feedforward considerations), and V_{DSEC} is the forward voltage of the secondary rectifier.

In this evaluation board: V_{OUT} = 24 V, R8 = 36 kΩ, and $V_{OUT\text{-}OVP}$ has been set to 30 V, which results in R8 = 7.25 kΩ. The commercial value of 7.5 kΩ has been selected, giving an actual value of 29.3 V.

This is confirmed by the bench test shown in the following figures, where the output overvoltage has been produced by shorting the low-side resistor of the output voltage divider, R23, to the secondary ground.

After $T_{RESTART}$, switching is enabled at the first V_{DD} recharge to $V_{DD\text{-}ON}$, and since the overvoltage is still present, the protection is triggered again in the same way, resulting in low-frequency intermittent operation. If the short is removed, the IC resumes normal operation.

Figure 33. OVP triggered

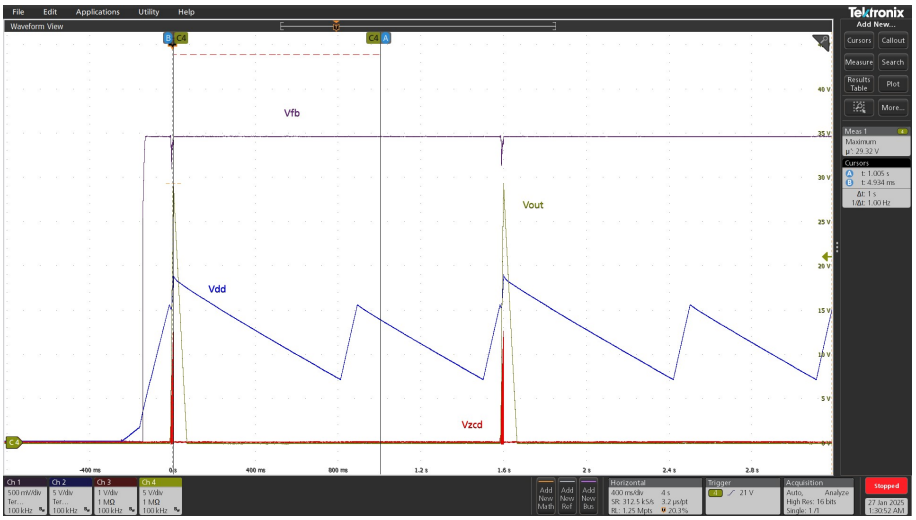
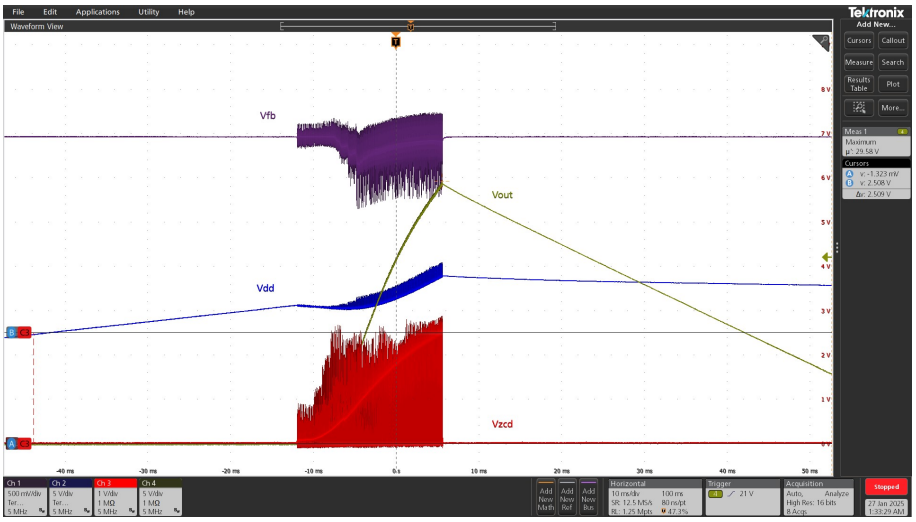
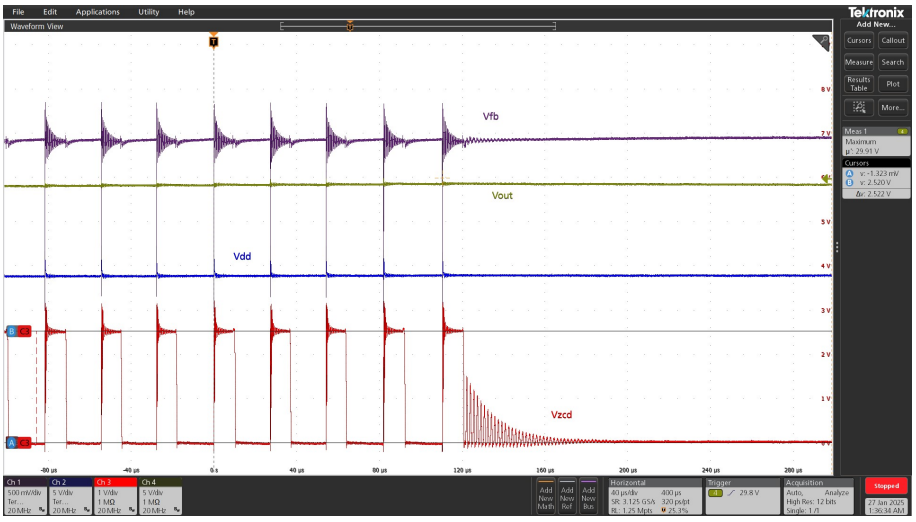


Figure 34. **OVP steady-state, $V_{OUT-OVP}$**



To reduce sensitivity to external noise and avoid false triggering, the protection is activated only if the OVP comparator is triggered for four consecutive oscillator cycles. A counter is implemented for this purpose, and it is reset each time the OVP comparator is not triggered during an oscillator cycle.

Figure 35. **OVP steady-state, V_{ZCD}**



6.8 OCP LEB

When the secondary rectifier fails short, the transformer's inductance reduces to leakage inductance, and the current could reach dangerously high values in a very short time. To avoid component damage, if I_{DRAIN} exceeds I_{OCP_LEB} at the end of T_{LEB} for two consecutive switching cycles, OCP LEB stops the switching of the IC for $T_{SD-REST}$ (2 s, typ.). During fault condition, V_{DD} is maintained between V_{DD-ON} and $V_{DD-RESTART}$ by the periodical activation of the internal HV current source. At the end of $T_{SD-REST}$, the device must wait for the first V_{DD-ON} crossing before restarting. If the fault is still present, the protection remains active indefinitely in the same way, otherwise the IC resumes normal operation.

To test this protection, the secondary rectifier has been shorted, and an input voltage of 110 V_{AC} has been applied.

Figure 36. OCP LEB @ 110 V_{AC}, $T_{SD-REST}$

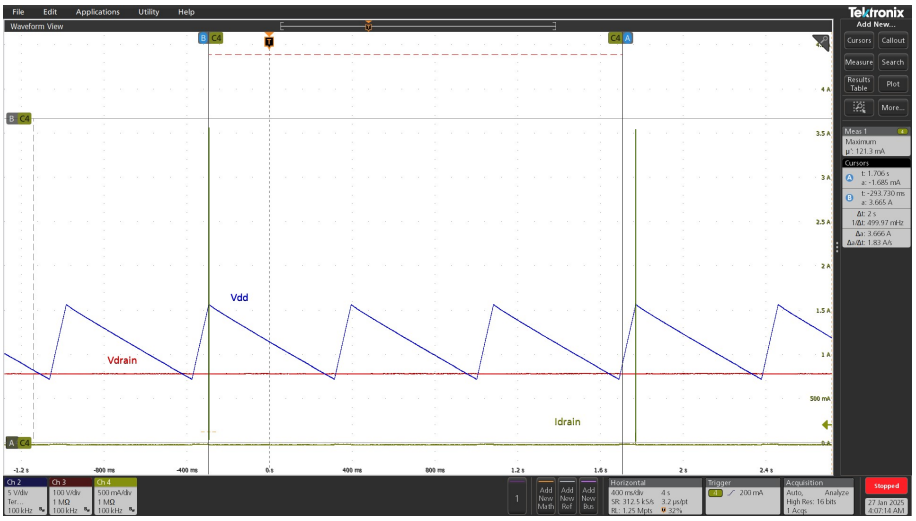


Figure 37. OCP LEB @ 110 V_{AC}, 2 switching cycles for protection triggering

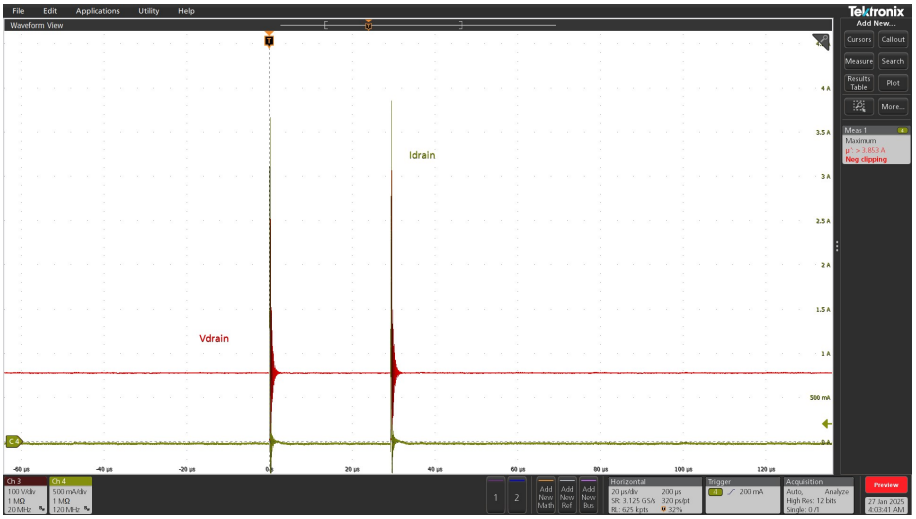
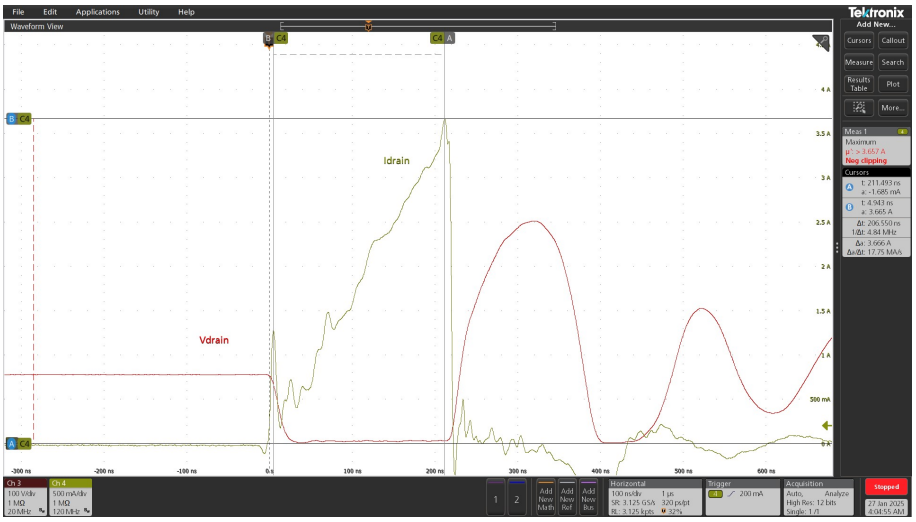


Figure 38. OCP LEB @ 110 V_{AC}



6.9 Thermal measurements

A thermal analysis of the board at T_{AMB} = 25 °C has been performed at 90 V_{AC}, 115 V_{AC}, 230 V_{AC}, and 265 V_{AC} mains input, under full-load condition, using an IR camera. The results are shown in the following figures.

Figure 39. Thermal measurement @ 90 V_{AC}, full load - main board, bottom

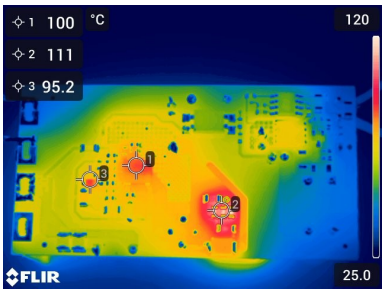


Figure 40. Thermal measurement @ 90 V_{AC}, full load - main board, top

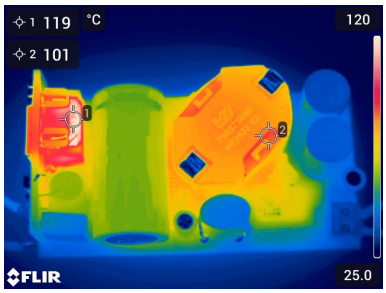


Figure 41. Thermal measurement @ 90 V_{AC}, full load - input board, bottom

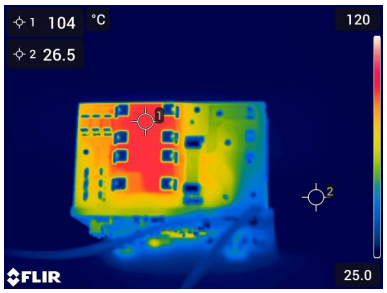


Figure 42. Thermal measurement @ 115 V_{AC}, full load - main board, bottom

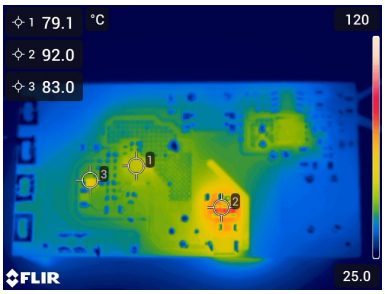


Figure 43. Thermal measurement @ 115 V_{AC}, full load - main board, top

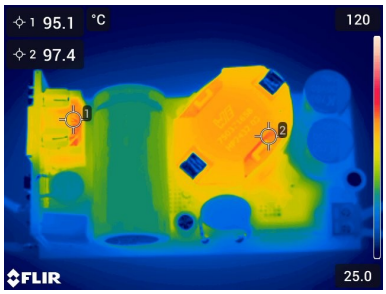


Figure 44. Thermal measurement @ 115 V_{AC}, full load - input board, bottom

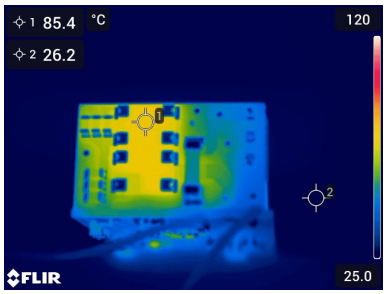


Figure 45. Thermal measurement @ 230 V_{AC}, full load - main board, bottom

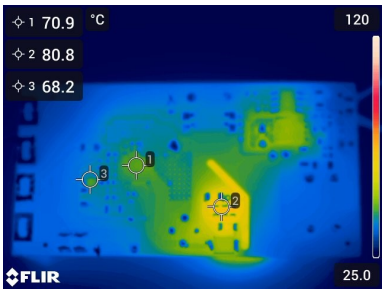


Figure 46. Thermal measurement @ 230 V_{AC}, full load - main board, top

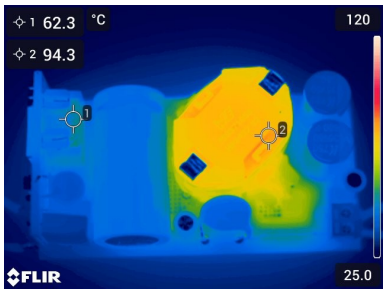


Figure 47. Thermal measurement @ 230 V_{AC}, full load - input board, bottom

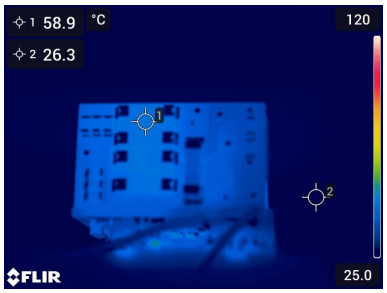


Figure 48. Thermal measurement @ 265 V_{AC}, full load - main board, bottom

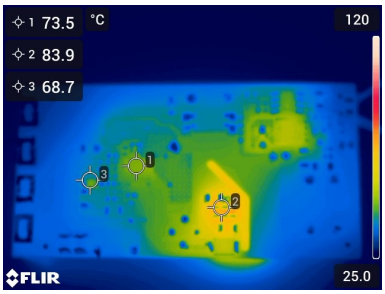


Figure 49. Thermal measurement @ 265 V_{AC}, full load - main board, top

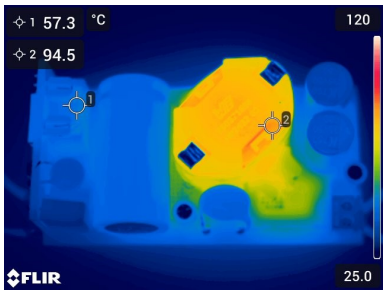


Figure 50. Thermal measurement @ 265 V_{AC}, full load - input board, bottom

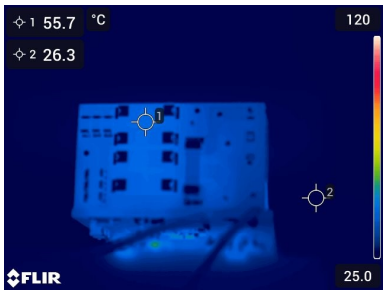


Table 7. Temperature of key components (T_{AMB} = 25 °C, emissivity = 0.95 for all points)

Point	Temp (°C)				Reference
	90 V_{AC}	115 V_{AC}	230 V_{AC}	265 V_{AC}	
Main board, bottom - 1	100	79.1	70.9	73.5	VIPerGaN65W
Main board, bottom - 2	111	92	80.8	83.9	Drain snubber
Main board, bottom - 3	95.2	83	68.2	68.7	R24
Main board, top - 1	119	95.1	62.3	57.3	Choke
Main board, top - 2	101	97.4	94.3	94.5	Transformer
Input board, bottom - 1	104	85.4	58.9	55.7	Bridge diode

6.10 EMI measurements

A pre-compliance tests to EN55022 (Class B) European normative with average detector has been performed using an EMC analyzer and a LISN. Results are reported in the figures below.

Figure 51. **Average measurements @ 115 V_{AC}, full load**

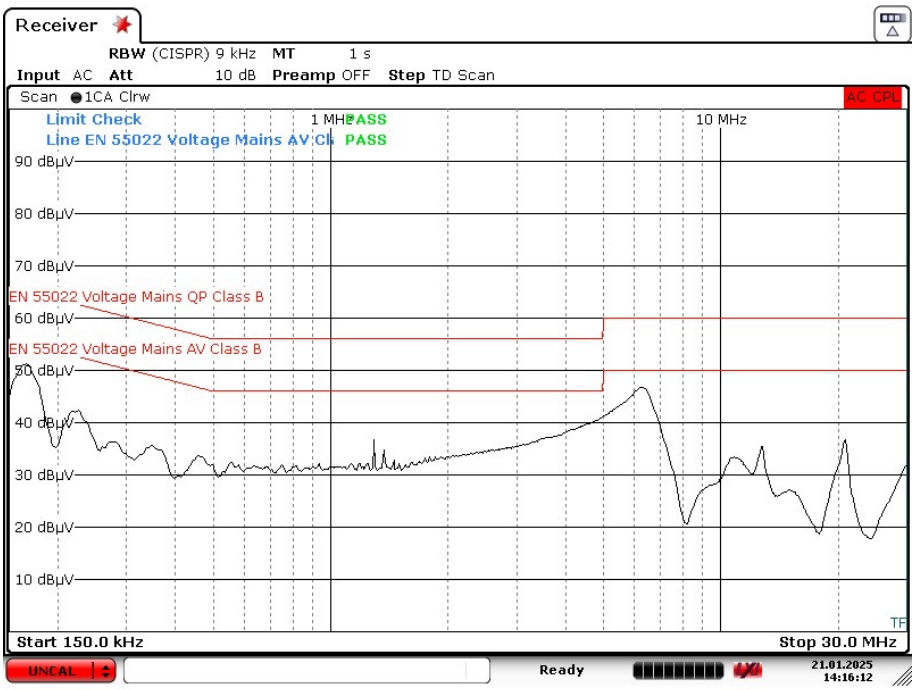


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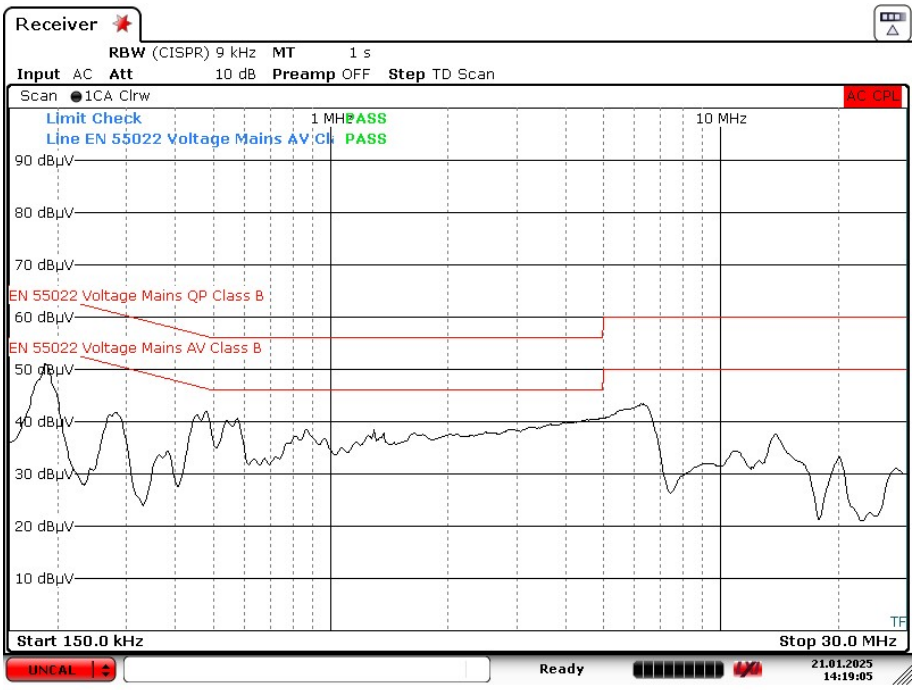
Figure 52. **Average measurements @ 230 V_{AC}, full load**



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7 Conclusions

In this document, the EVLVIPGAN65WF, a single output 24 V/65 W evaluation board in flyback isolated topology, has been described and characterized. The results demonstrate that VIPerGaN65W enables the design of an SMPS converter compliant with the most stringent energy regulations, achieving average efficiency higher than 92% both at 115 V_{AC} and at 230 V_{AC} nominal input voltage.

The VIPerGaN65W is an offline quasi-resonant (valley switching at switch turn-on) flyback converter. Depending on the converter's load condition, the device is able to operate in different modes. Based on the quasi-resonant principle, primary switching losses are minimized. Secondary losses are minimized by using the highly efficient and optimized synchronous rectification controller.

Users no longer need to manage GaN driving complexity to benefit from GaN technology, thanks to the highly integrated VIPerGaN65W IC, which enhances the robustness of the application.

Revision history

Table 8. **Document revision history**

Date	Version	Changes
30-Sep-2025	1	Initial release.

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