How to optimize the PCB layout for ST67W611M1 and STM32U575AI

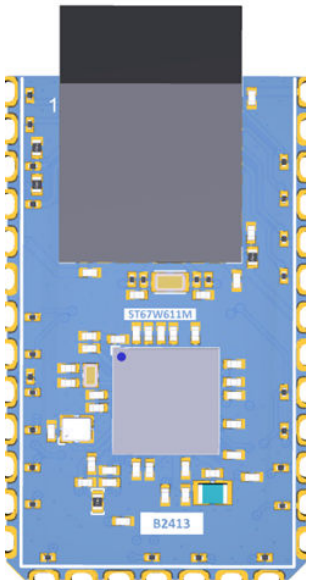
Introduction

The STDES-67W61BU-U5, based on the reference boards B2413, B2414, and B2415 integrates the microcontroller STM32U575AI (which is used as the host for the ST67W611M1 module), and is compatible with the PCB antenna and the UFL connector versions.

To respect the coexistence between the module and the host and reach the best performance, some recommendations must be followed concerning the board technology, including, the placement of the components, the signal routing, and the power supply strategy.

This design guide is based on a four-layer board with FR4 material in an optimized STAMP form factor.

Figure 1. B2413 top view



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1 Board description

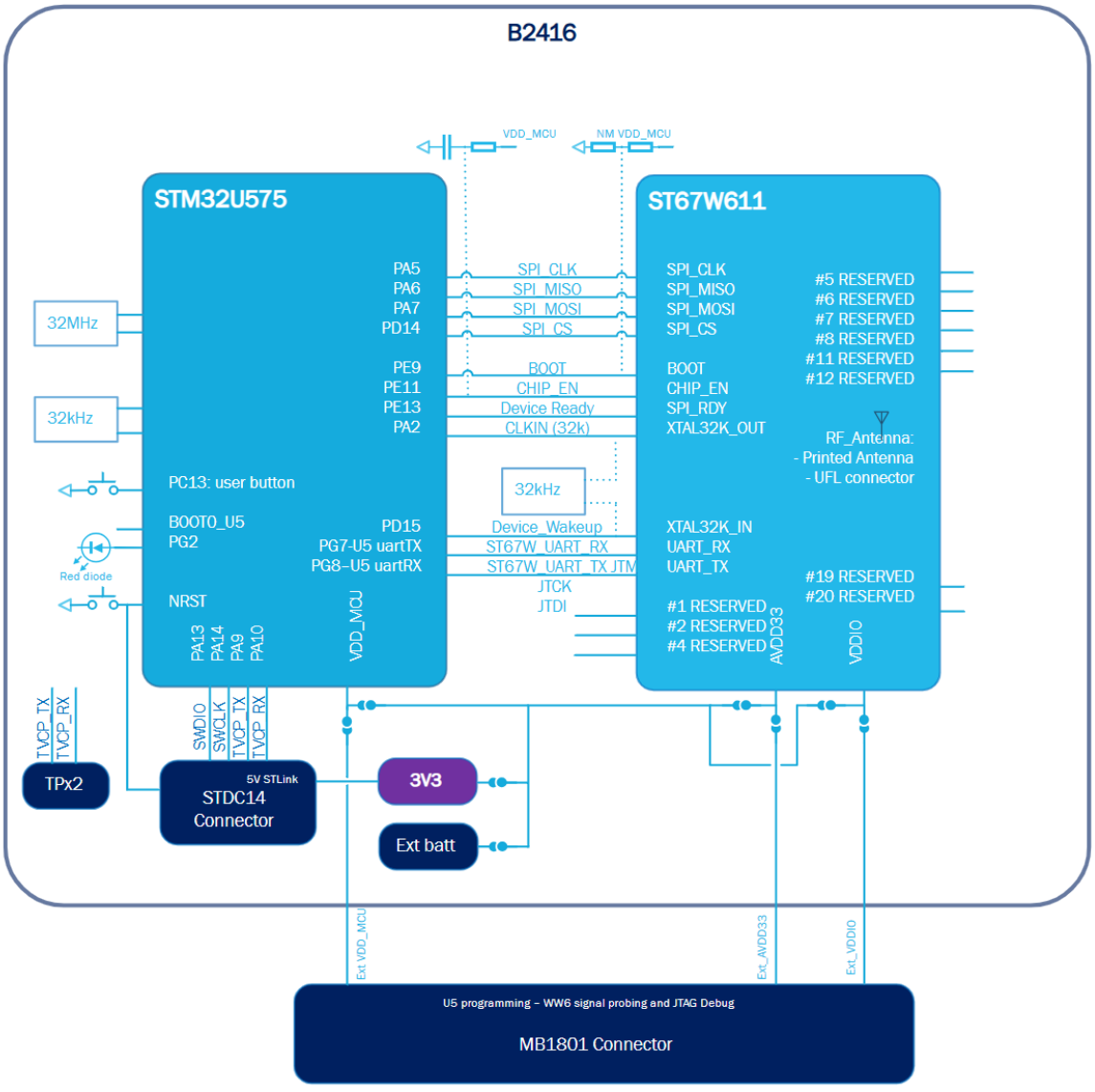
The aim of this reference design is to provide an optimum layout using the STM32U575AI in a BGA package. For test purposes, these boards are soldered on an interface board B2416 that embeds:

- STDC14 connector for the STLINK-V3
- U5 reset and user buttons
- UART link
- LDOs and connectors for different power supply strategies

1.1 B2413/B2414/B2415 and B2416 signals description

Signal description on the reference board is shown in Figure 2.

Figure 2. B2413/B2416 block diagram



This document only focuses on the B2413, B2414, and B2415 boards. For details on the B2416 configuration, refer to the wiki page of the ST67W611M1.

2 PCB specification

The selection of a small BGA 169 (7 x 7 mm) for the STM32U575AI means that micro vias are used, and consequently, a PCB with four layers.

Common features

- Type: FR4 - ε_r = 4.5
- PCB size: 34 x 20.32 mm
- Four-layer board
- PCB thickness: 0.7 mm
- Cu: 35 µm
- Finish: ENIG
- Solder mask color: blue
- Silkscreen: Yes (white)
- Min hole size: 0.2 mm
- µVias, no buried vias

Layer stack

Table 1. B2413 PCB stack-up

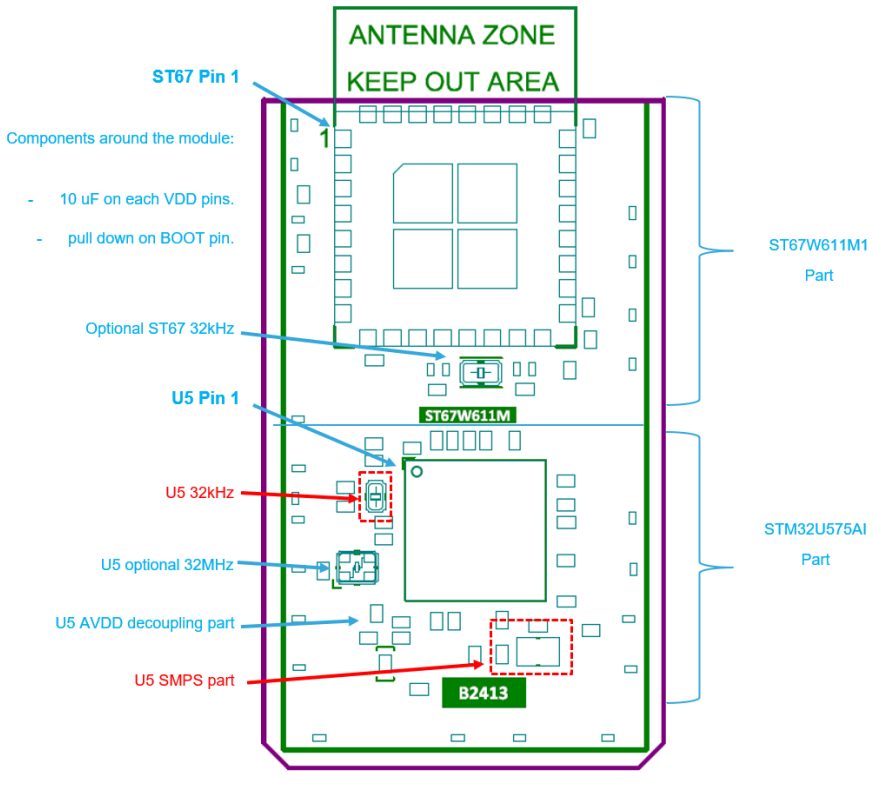
Number	Name	Material	Type	Weight (oz)	Thickness (mm)	Dk
-	Top overlay	-	Overlay	-	-	-
-	Top solder	Solder resist	Solder mask	-	0.02	3.2
1	Top layer	-	Signal	1	0.035	-
-	Dielectric 1	FR-4	Core	-	0.0762	3.7
2	Internal 1	-	Signal	1	0.035	-
-	Dielectric 3	FR-4	Prepreg	-	0.335	4.5
3	Internal 2	-	Signal	1	0.035	-
-	Dielectric 2	FR-4	Core	-	0.0762	3.7
4	Bottom layer	-	Signal	1	0.035	-
-	Bottom solder	Solder resist	Solder mask	-	0.02	4.2
-	Bottom overlay	-	Overlay	-	-	-

3 Component placement

3.1 Overview

All the components are located on the TOP side. The orientation of the U5 is determined by the SMPS component, which must be located on the U5 side opposite to the ST67W611M1 module. The SMPS is a noisy source that can affect RF performances.

Figure 3. B2413 component placement



In this configuration, the distance between the two chips is equal to 5.8 mm (~230 mil).

3.2 I/O connections

The signal connections to the STM32U575AI and ST67W611M1 pins are shown in Figure 4 and Table 2.

Figure 4. **B2413 pinout**

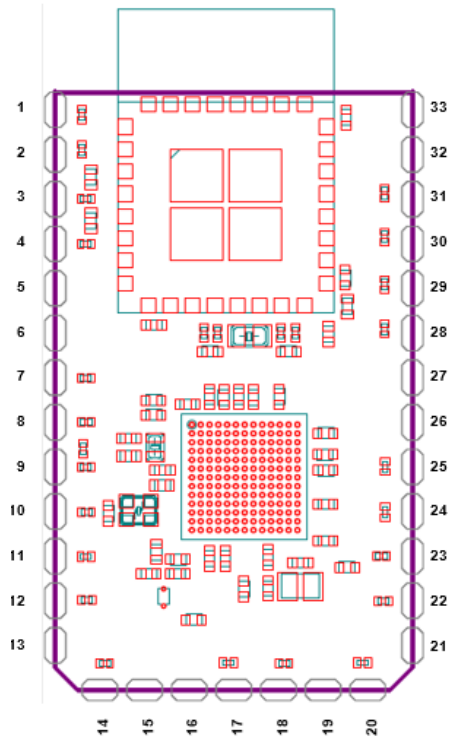


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Table 2. **Pinout table**

Pin number	Signal name	ST67W611M1 pin name	STM32U575AI
1	JTMS	RESERVED	NC
2	JTCK	RESERVED	NC
3	BOOT ST676/JTDO	BOOT	PE9
4	JTDI	RESERVED	NC
5	VDD_IO1	VDDIO	NC
6	GND	GND	GND
7	SWDIO	NC	PA13
8	SWCLK	NC	PA14
9	BOOT0_U5	NC	PH3-BOOT0
10	User_Button_U5	NC	PC13
11	TVCP_RX	NC	PA10
12	TVCP_TX	NC	PA9
13	GND	GND	GND
14	Reset_N	NC	RSTN
15	GND	GND	GND
16	VDD_MCU	NC	VDD
17	Ext_32K	XTAL32K_OUT	PA2
18	Red_LED_U5	NC	PG2
19	GND	GND	GND
20	Device wake-up	XTAL_32K_IN	PD15

Pin number	Signal name	ST67W611M1 pin name	STM32U575AI
21	GND	GND	GND
22	SPI_MOSI	SPI_MOSI	PA7
23	SPI_CLK	SPI_CLK	PA5
24	SPI_MISO/JTDO	SPI_MISO	PA6
25	CHIP_EN	CHIP_EN	PE11
26	GND	GND	GND
27	VDD33	VDD33	NC
28	Device ready	SPI_RDY	PE13
29	LPUART_TX/Host wake-up	UART_TX	PG7
30	LPUART_RX	UART_RX	PG8
31	LP WAKEUP	SPI_CS	PD14
32	GND	GND	GND
33	VDD_IO2	VDDIO	NC

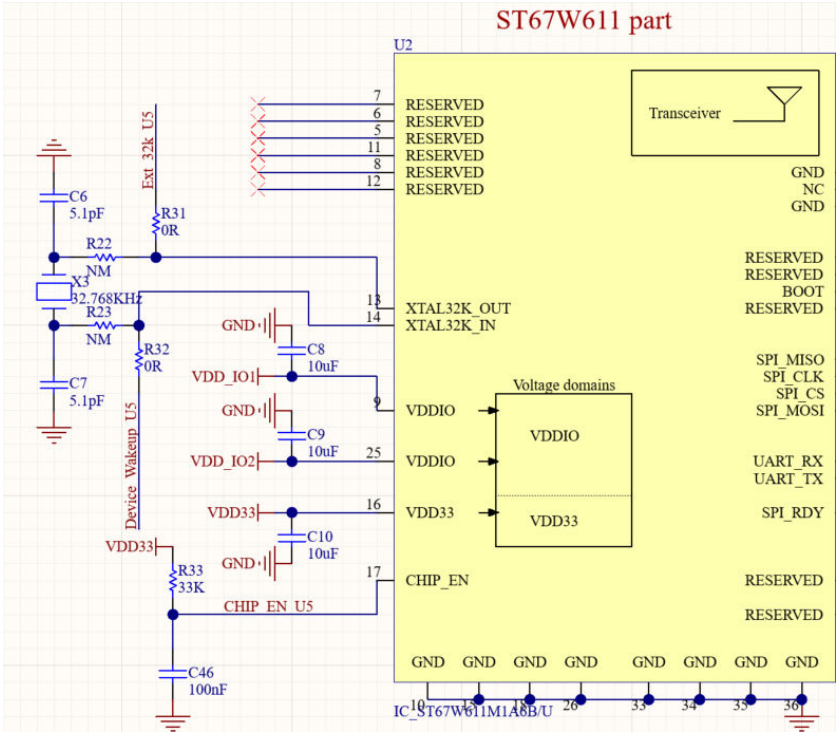
Most of the signals can be disconnected from the board pins because serial resistors are used.

3.3 ST67W611M1 use cases for 32 kHz

The module can operate with different 32 kHz sources:

- Internal RC 32 kHz: X3, R22, R23, R31, and R32 are not populated (in that case pins 13 and 14 can be left unconnected).
- External 32 kHz from MCU: the clock is provided by the STM32U575AI (pin PA2) and the external input clock is pin 13 (XTAL32K_OUT). In that configuration, R31 has to be populated and R22, R23, R32, and X3 are not populated (pin 14 can be left unconnected).
- XO 32 kHz: X3, R22, and R23 are populated. R31 and R32 are not populated.

Figure 5. 32 kHz configuration



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4 Layout considerations

4.1 ST67W611M1 footprint and GND via stitching

The recommendation is to have the maximum number of vias under the QFN PAD to ensure acceptable current return path (including RF) and an optimal power dissipation.

The amount of vias depends on the class of the PCB. In this design, five standard vias are placed under each Exposed PAD. If bigger vias are used, then a smaller amount is allowed

Figure 6. ST67W611M1 Bottom view

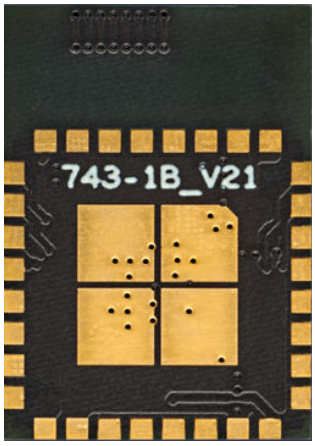

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Figure 7. ST67W611M1 footprint

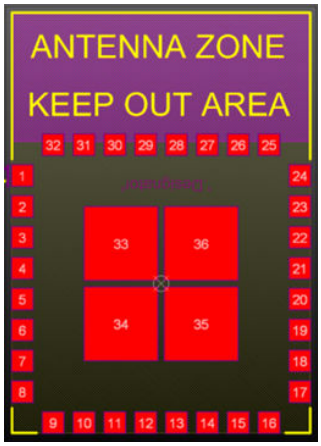

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Figure 8. ST67W611M1 VIAs GND PAD

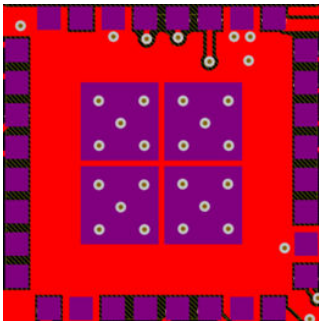

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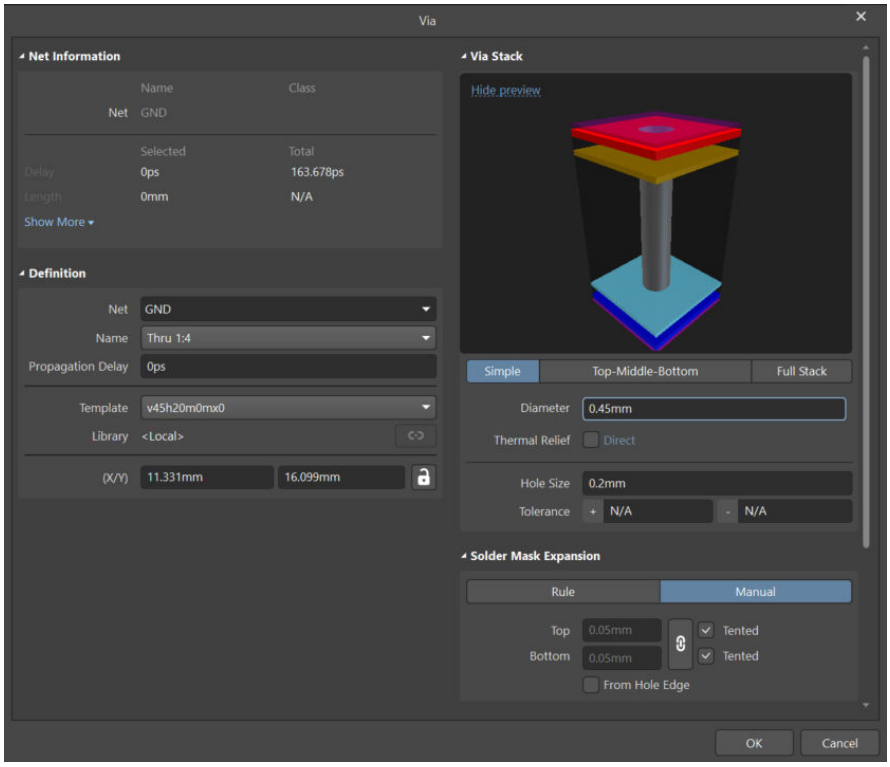
Figure 9. **Thru hole standard type**



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The thru hole type, shown in Figure 9, is standard for all the boards except for the BGA package, for which micro vias are used.

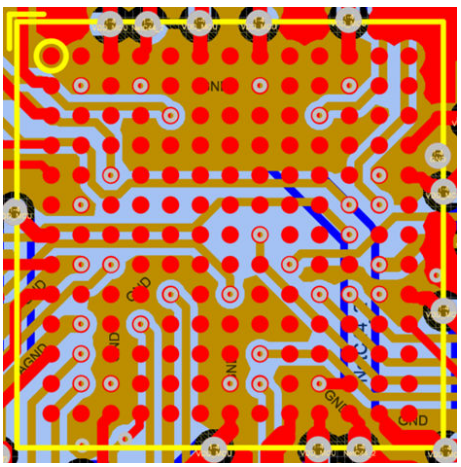
4.2 STM32U575AI footprint and micro-VIA placement

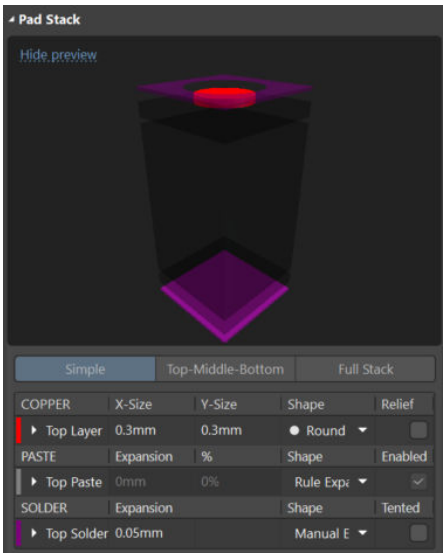
Micro vias are used to route the signals from the top of the BGA pads to the first inner layer.

Figure 10. **BGA balls footprint**

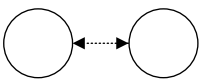
BGA 169 footprint:

PADs diameters = 300 µm
Top solder expansion = 50 µm





Distance between 2 PADS = 200 µm:



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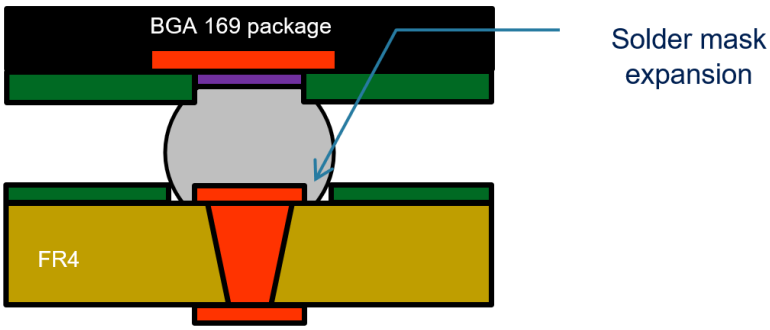
The micro vias are filled and the surface is flat so they can be placed just under the BGA balls. Their diameter is equal to 250 µm and the hole size is equal to 100 µm.

Figure 11. BGA micro via



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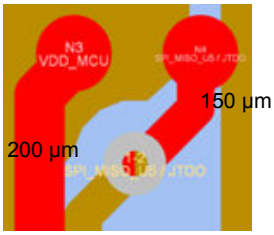
Other design rules

- Clearance between nets is equal to 120 µm.
- Maximum track width connected to the balls or micro vias:
  - Power signals (V_{DD}) max width = 200 µm
  - Signals max width = 150 µm

Figure 12. BGA line width



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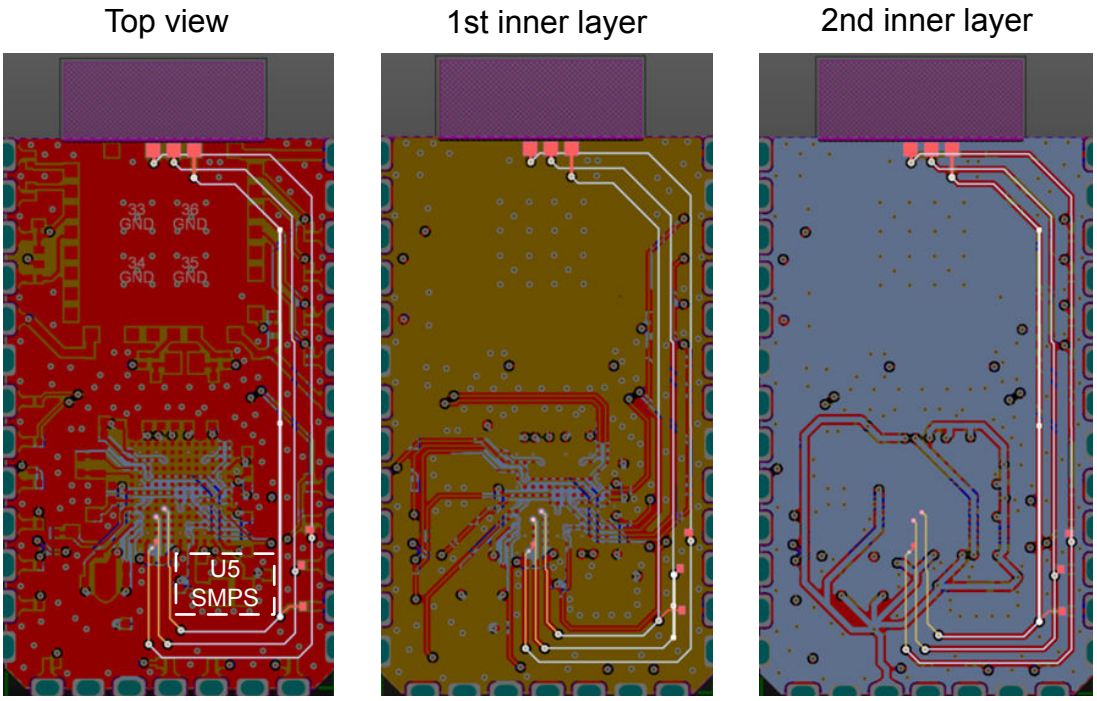
4.3 SPI routing signals

Recommendations for the SPI routing signals are as follows:

- Coplanar line routing (ground between signals)
- Avoid placing the SPI routing toward U5 across the SMPS area
- Internally route signals (in the first or second inner layer) to prevent SPI_CLK radiation

Figure 13. **PCB views**



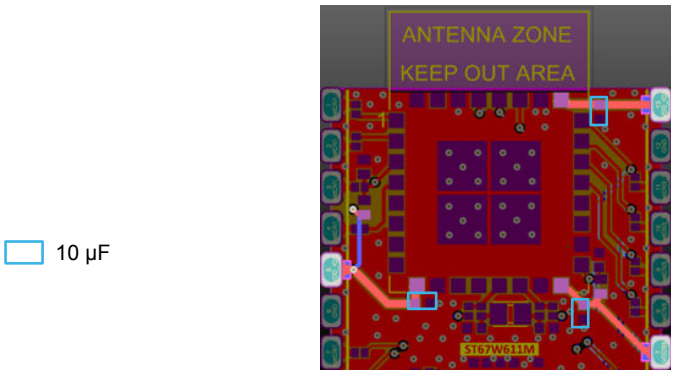
- Track length must be as short as possible to limit propagation delays between the host and the module. In this reference design, the total length is about 45 mm that represents a delay of 300 ps.
- There is no impedance control, but it should be as close to 50 Ω as possible (the main constraint is the thickness of the first dielectric, which is 76 µm due to the via). In that layer stack, the impedance of the lines is equal to 38 Ω.

4.4 Power supply distribution and decoupling

4.4.1 ST67W611M1 part

For certain 10 µF-0402, the placement is near to the VDD PADs: VDD_IO1, VDD_IO2, and VDD33. The connection to the board PAD is as short as possible, as shown in Figure 14.

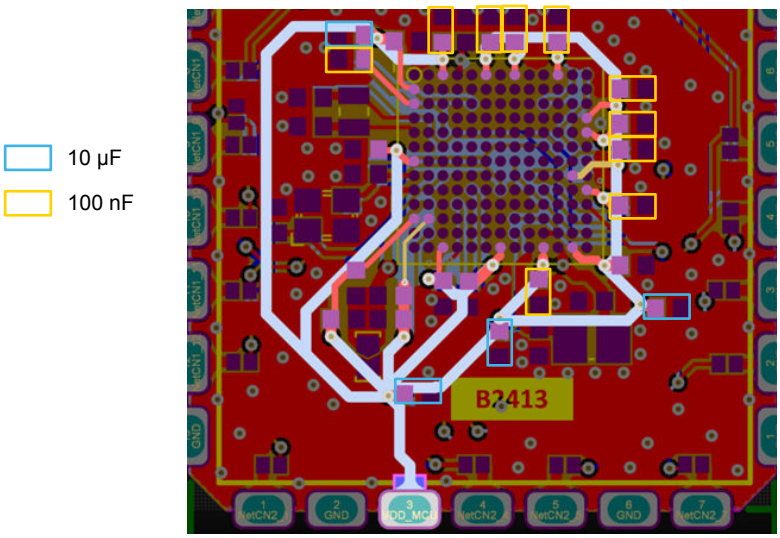
Figure 14. **ST67W611M1 power supply decoupling**



4.4.2 STM32U575AI part

All VDDs of the chip are regrouped in one single VDD MCU in a star distribution:

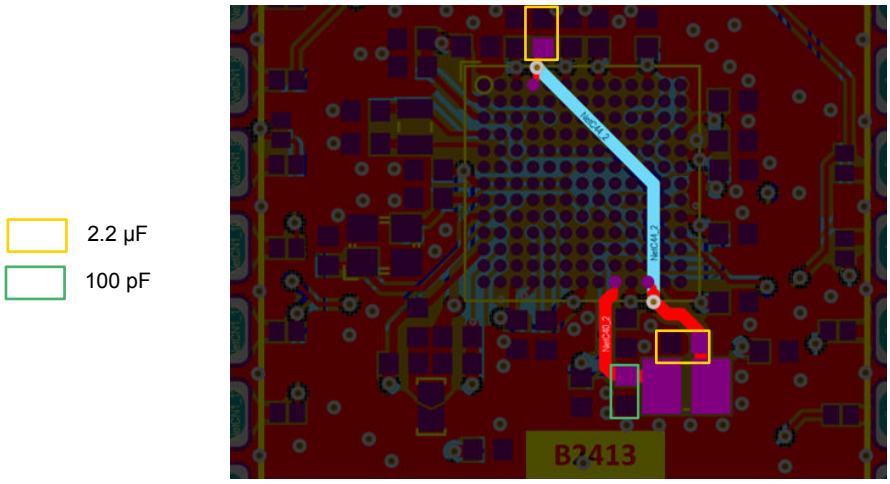
Figure 15. **STM32U575AI power supply decoupling**



Power supply track width = 400 µm.

The SMPS provides the 1.2 V reference for the input PADs of the two LDOs which are decoupled by 2 x 2.2 µF:

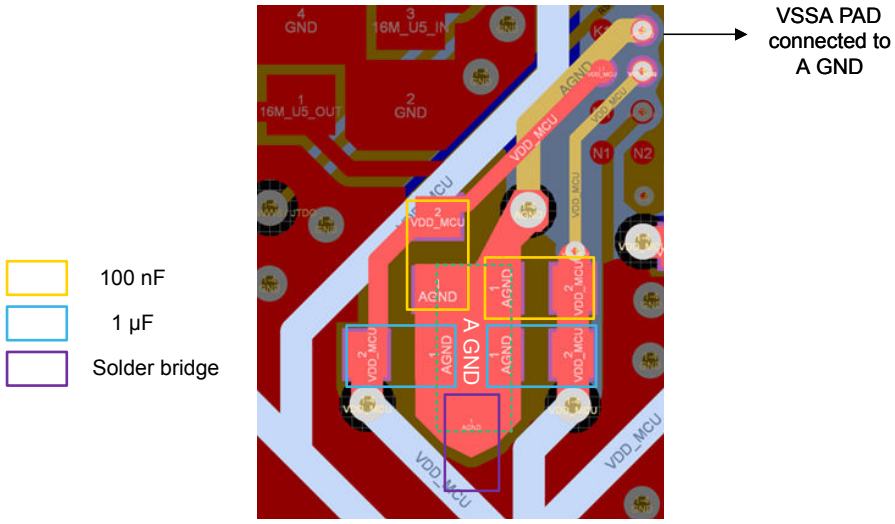
Figure 16. **STM32U575AI SMPS component**



Analog power supply:

V_{DDA} and V_{REFP} are analog power supplies which must be decoupled by two capacitors, 1 µF and 100 nF, connected directly to the analog ground pin VSSA. This analog ground pin is connected to the main ground by a soldering bridge (SB38), as shown in Figure 17.

Figure 17. **STM32U575AI analog VDD component**



Note: Refer to this wiki link concerning the STM32 MCU power supply design guide.

4.5 RF part characteristics

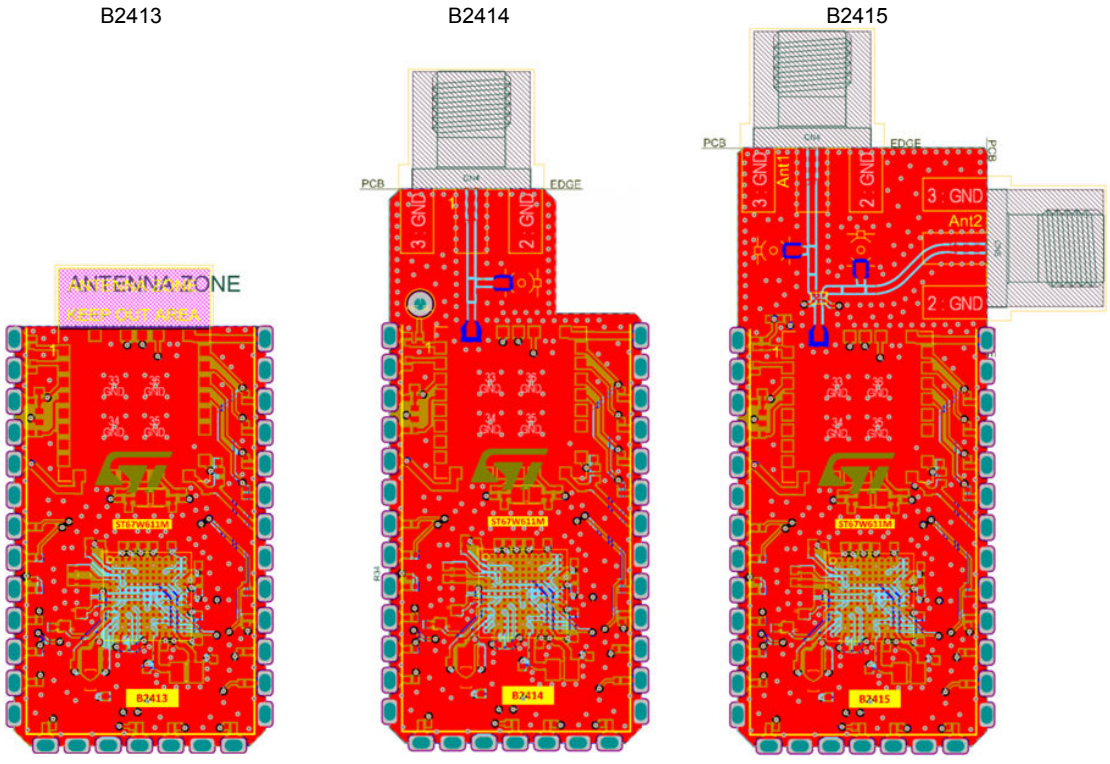
4.5.1 RF part overview

This section concerns only the boards B2414 and B2415 which embed the ST67W611M1A6P.

On the module ST67W611M1A6B and ST67W611M1A6U, the pin 31 is not connected. For the -P version, this pin is used as RF input and output.

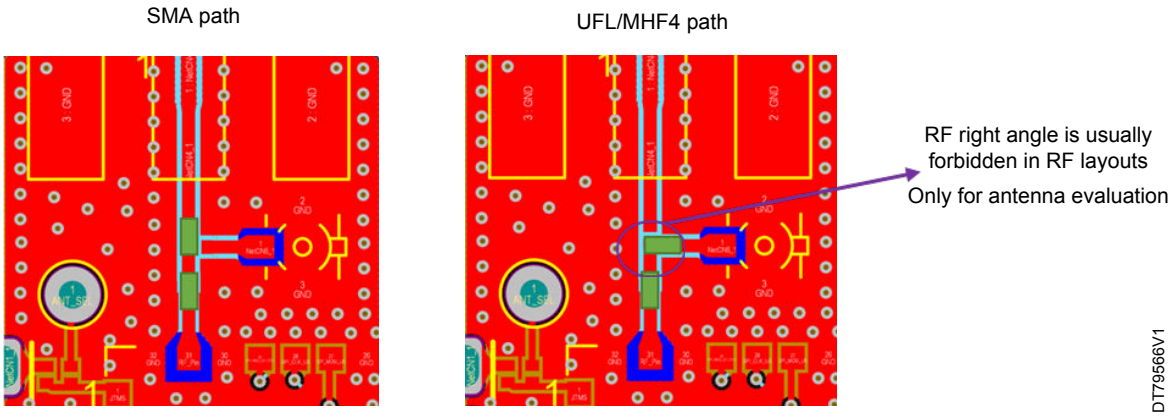
The boards B2414 and B2415 are similar to the board B2413 except the RF part:

Figure 18. **Boards B2413, B2414, and B2415**



For evaluation purposes, two RF paths are possible to connect either an UFL/MHF4 or an SMA antenna.
The path is chosen following 0 Ohm resistor placement, components are overlapped to avoid impedance mismatch due to larger width:

Figure 19. SMA and UFL/MHF4 paths

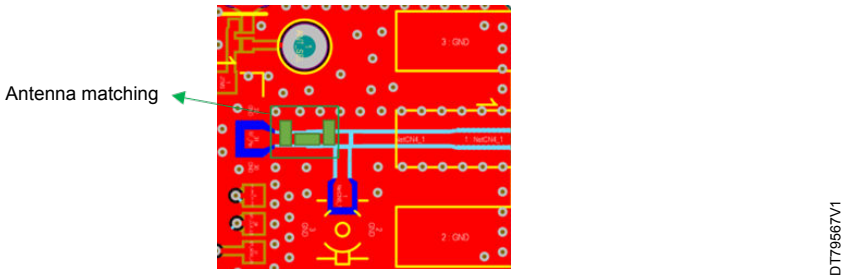


4.5.2 Design rules for the RF part management

RF part management should follow the guidelines:

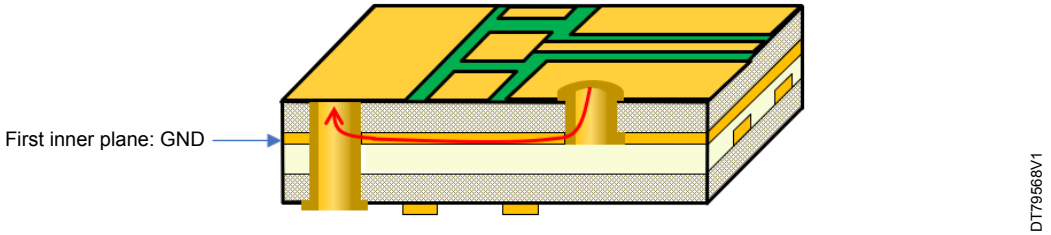
- Minimize the length from the pin to the antenna to allow fewer losses and reflections
- Antenna matching:
  - If an antenna presents a bad impedance, a PI cell allows different antenna matching possibilities (LC/CL/CLC)

Figure 20. Antenna matching possibilities



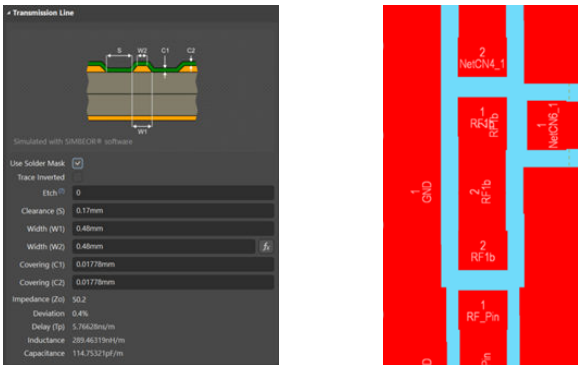
- RF current feedback to the main ground of the module:
  The impedance of the RF common mode current must be as low as possible, this is why the first inner layer is preferentially dedicated for the GND signal.

Figure 21. RF current feedback



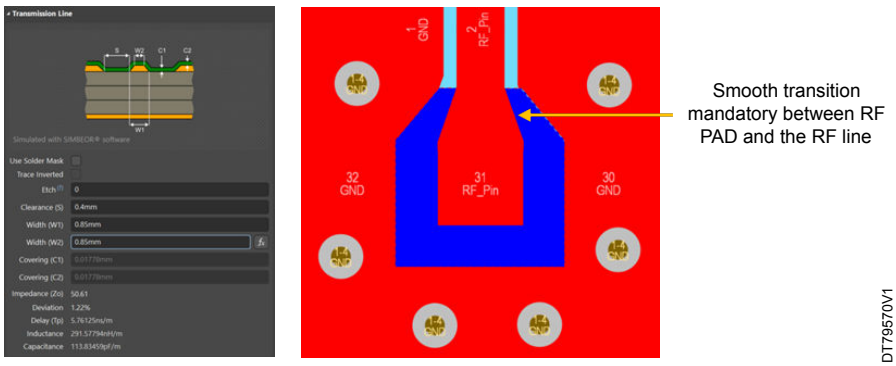
- Line width and impedance:
  - Pads of the component or the module can partially set the line width if the characteristics of the layer stack of the boards allow it.
  - In this case, the RF PAD width of the module is equal to 0.85 mm. It is not possible to reach 50 ohms considering the height of the board = 0.6 mm. The PAD width of the 0402 components is equal to 0.5 mm.
  - Considering the layer stack, line width is set to 0.48 mm and the RF GND reference is taken on the second inner layer. Line clearance is equal to 0.17 mm.

Figure 22. RF line characteristics



- PAD impedance and transition to RF tracks:
  - **RF PAD of the module:** PAD width = 0.85 mm, the RF GND reference is set to the bottom layer and the clearance is set to 0.4 mm to present 50 ohms to the module.

Figure 23. RF PAD module characteristics



  - **RF PAD of the UFL/MHF4 connector:** PAD width = 0.85 mm, the same footprint characteristics as the RF PADs of the module
  - **RF PAD of the SMA connector:** PAD width = 0.55 mm, the GND reference is the second inner layer. The clearance is slightly increased to 0.2 mm

FEM simulation of the RF path gives the following results:

Figure 24. SMA path (at F = 2443 MHz, losses = 0.09 dB, S11 (module plane) = -23.4 dB)

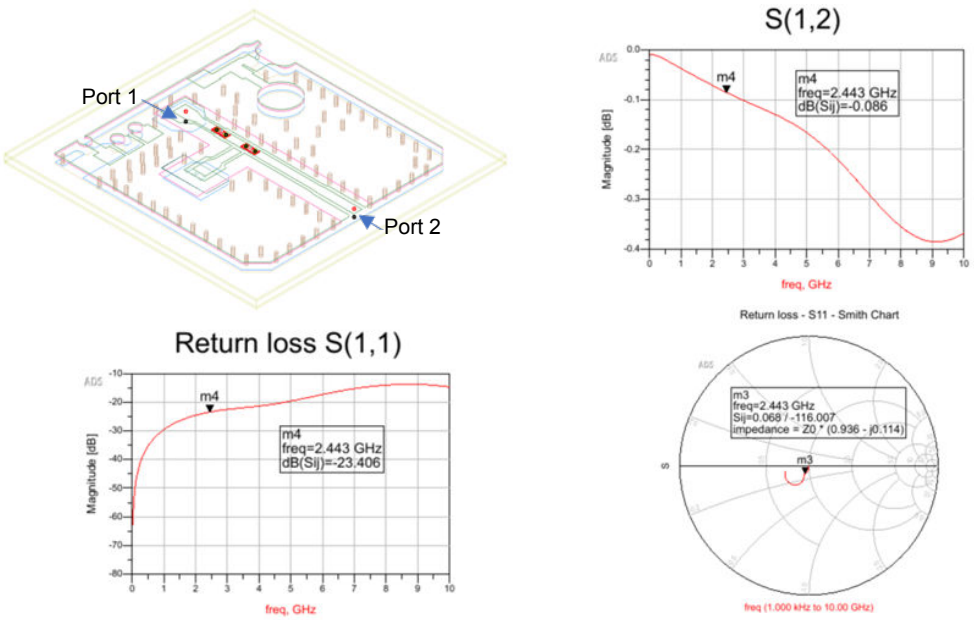


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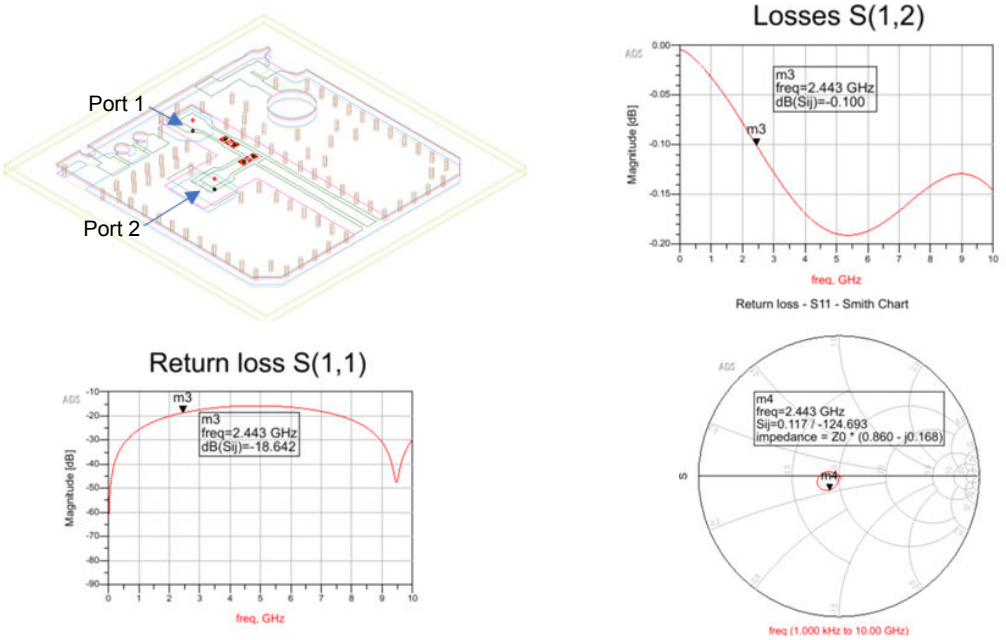
Figure 25. UFL path (at F = 2443 MHz, losses = 0.1 dB, S11 (module plane) = -18.6 dB



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5 Antenna placement

The placement of the module must be in the middle-edge of the board with respect to where the antenna is placed, irrespective of the dimensions of the board.

No copper or metallic plane should be placed under or close to the antenna:

Figure 26. ST67W611M1 recommended antenna placement

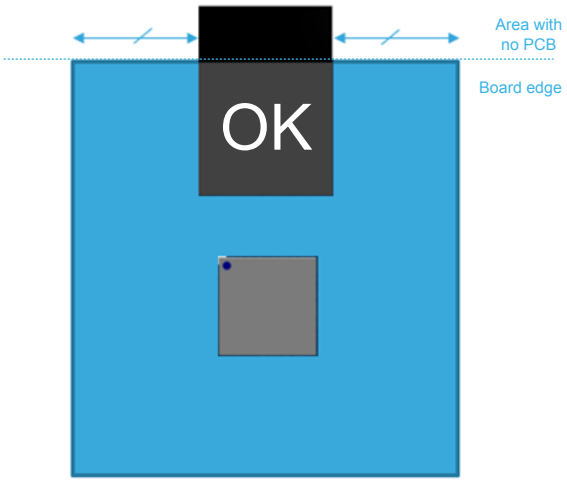

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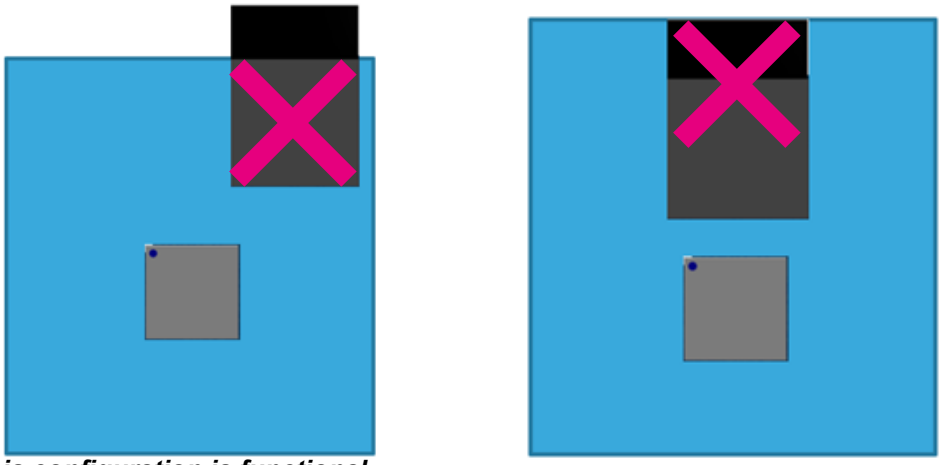
Figure 27. ST67W611M1 not recommended antenna placement



This configuration is functional, but not optimum

This configuration is not functional

Revision history

Table 3. **Document revision history**

Date	Version	Changes
28-May-2025	1	Initial release.
11-Sep-2025	2	Added: • Reference boards B2414 and B2415 • Section 4.5: RF part characteristics Updated: • Section 2: PCB specification • Section 3.2: I/O connections • Section 3.3: ST67W611M1 use cases for 32 kHz
21-Oct-2025	3	Updated: • Section 1.1: B2413/B2414/B2415 and B2416 signals description • Section 2: PCB specification • Section 4.1: ST67W611M1 footprint and GND via stitching • Figure 15. STM32U575AI power supply decoupling

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