Application note

Guidelines for understanding I2C EEPROM usage on the I3C Bus

Introduction

This application note explains the usage of STMicroelectronics I2C EEPROM memory on an I3C bus. It applies to all standard I2C EEPROM memory and provides guidelines for understanding the behavior, compatibility, and impact of I2C EEPROM devices when integrated into an I3C bus environment. The document outlines key considerations, configuration steps, and best practices to ensure seamless operation and optimal performance in mixed I2C/I3C systems.

1 General information

Table 1. Referenced documents

N°	Document
[1]	MIPI I3C Basic™ v1.1.1 (july 2021)
[2]	I2C-bus specification and user manual (UM10204)
[3]	I3C Characteristics Registers

Table 2. Acronyms

Acronym	Definition
BCR	Bus configuration register
DCR	Device configuration register
I3C	Improved inter-integrated circuit
LVR	Legacy virtual register
SCL	Serial clock
SDA	Serial data address
SDR	Single Data Rate
HDR-DDR	High Data Rate Double Data Rate

2 What is I3C

I3C is an evolution of the I2C bus. It aims to provide more efficiency to the I2C bus speed, with a clock that can go up to 12.5 MHz, and more flexibility, managing component addresses and more. I3C allows communication between integrated circuits using only two wires and can have several host and target components. A key feature is its backward compatibility with I2C. This note focuses on using ST I2C EEPROM memory on an I3C bus. It relies on the MIPI I3C Basic™ v1.1.1 specification, explaining I3C backward compatibility with I2C. The document covers I2C restrictions for I3C compatibility, different I3C bus configurations, hardware and software concerns, and concludes with bench demonstrations.

3 I2C compatibility with an I3C bus

The I3C protocol is backward compatible with I2C, but not with the full I2C specification. To operate on an I3C bus, I2C components must adhere to specific rules outlined in the MIPI I3C Basic™ v1.1.1 specification.

To function on an I3C bus, an I2C component must meet the requirements described in the following subsections of this chapter.

3.1 No clock stretching

The I3C host drives the SCL pad at all times during I3C communication. On an I2C bus, the external pull-up on the SCL pad allows the target to hold the SCL line low, even if the host attempts to drive it high. In I3C, this behavior may cause a bus conflict. Therefore, the clock stretching mechanism is not permitted for I2C components introduced into an I3C bus.

Note: ST I2C EEPROMs do not use the clock stretching mechanism.

3.2 50 ns spike filter

To enable I2C and I3C components to coexist on the same bus, I2C components must avoid uncontrolled or parasitic actions. A specific start sequence is required for I3C components. Additionally, the presence of 50 ns spike filters on the pads of I2C components ensures that high-frequency I3C communications remain undetected. The I3C bus supports communication speeds of up to 12.5 MHz.

Note: All ST I²C EEPROMs include a 50 ns spike filter.

3.3 20 mA open drain driver (IOL) not used

According to the I2C specification, I2C components can have IOL capability to drive up to 20 mA. However, this feature is incompatible with the I3C bus specification. To function correctly on an I3C bus, I2C products must not include this feature.

Note: This feature is not present in ST I²C EEPROMs.

3.4 10 bits addressing not used

The I3C bus supports only a 7-bit addressing mechanism. I2C components connected to an I3C bus can only be addressed using the 7-bit addressing mode. ST I2C EEPROMs use only 7-bit addressing.

To comply with the I3C bus, an I2C component must meet all the requirements listed above.

ST I2C EEPROMs are fully compliant with these constraints.

4 I3C bus configuration

The I3C bus is a specific communication bus. One of its characteristics is its backward compatibility with the I2C bus. However, not all I2C components behave the same way or have the same electrical capabilities. This means that the I3C bus can have several configurations depending on the components present on the bus. This chapter describes the different bus configurations and the main characteristics of these buses.

4.1 Pure bus: only I3C components

In this configuration, the bus consists only of I3C components, including hosts and targets. There are no clock restrictions, and the bus can operate at a maximum frequency of 12.5 MHz. I3C communication can occur using SDR at 12.5 Mbps, with one bit per clock cycle, or using HDR-DDR at 25 Mbps, with one bit per clock edge. This configuration benefits from full I3C performance and is not addressed in this application note.

4.2 Mixed fast bus: I3C and I2C components on the same bus

In this configuration, the bus consists of I3C components (host/target) and I2C components (target). The I2C components must comply with the constraints listed in Section 3. I3C communication can operate at up to 12.5 MHz in SDR or HDR-DDR, but this may be limited due to I²C pad loads. Additionally, I2C components must operate in Fm or Fm+ mode (400 kHz / 1 MHz). This configuration is addressed in this application note.

4.3 Mixed slow bus: I3C and I2C components on the same bus

In this configuration, the bus consists of I3C components (host and target) and I2C components (target).

If I2C components are not fully compliant with the constraints listed in Section 3, and if they do not have a 50 ns spike filter, the I3C communication speed must be limited to the I2C component speed. If the communication speed is higher, the I2C component may interpret commands when it is not addressed and may exhibit activity when not required.

In addition to the frequency limitation, communication is restricted to the SDR format. In this configuration, there is no baud rate benefit from I3C. This configuration is not addressed by this application note, as all ST I2C products include a 50 ns spike filter.

4.4 I3C bus configuration conclusion

The "mixed fast bus" configuration allows users to benefit from the performance of the I3C protocol while maintaining compatibility with I2C components. ST I2C EEPROMs enable buses to operate in this configuration.

5 Bus connection and driver update

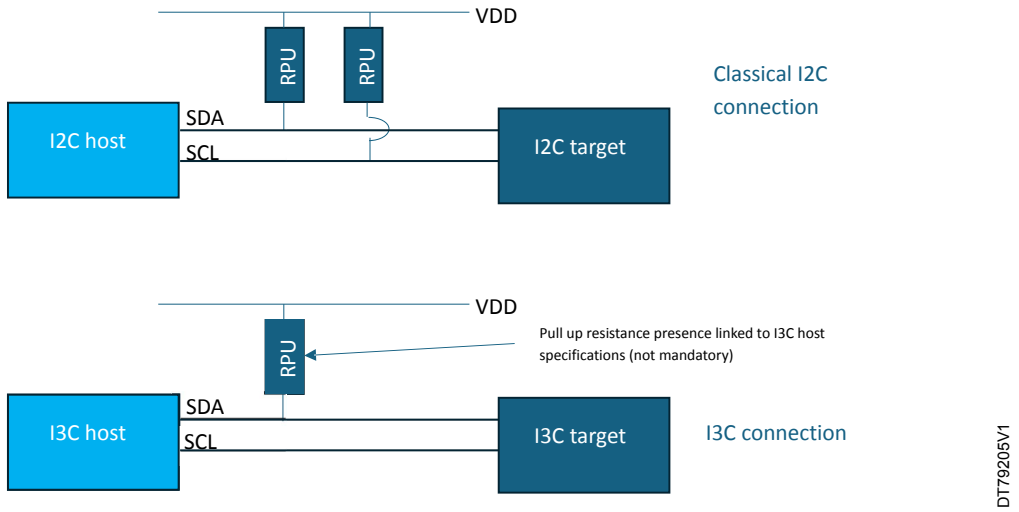
In the previous chapters, the general rules required for an I2C component to operate on an I3C bus have been reviewed. This chapter delves further into the implementation of such a bus, exploring both hardware and software aspects.

5.1 Hardware connection

I2C and I3C buses are connected using two wires: SDA and SCL pads. To function properly, an I2C bus requires external pull-up resistors on both wires.

On the I3C bus, the SCL line is driven by the host, and no pull-up resistor should be added to the line. For the SDA line, specific care is required. The I3C host must manage the line, and pull-up resistor management depends on the I3C host specification.

Figure 1. I2C and I3C connections



Finally, I3C and I2C components must communicate within the same voltage range. Therefore, I2C and I3C components must operate at the same voltage level.

ST I2C EEPROM products can operate at 3.3 V, 1.8 V, and 1.2 V (for 1.2 V I/O products) on the I3C bus.

5.2 Software

The I3C basic specification introduces the use of characteristic registers. In the document *I3C Characteristics Registers*, the following is stated:

Every legacy I2C device to be connected to an I3C bus must have one associated legacy virtual register. Since these are legacy devices, it is understood that this register exists virtually, for example, as part of the device's driver.

This LVR is 1 byte, as described in [3].

All I3C components have a BCR and a DCR. These registers allow the I3C host to identify which components are connected to the I3C bus. The host can perform a device inventory phase by requesting information about the components on the bus and their capabilities.

When an I2C component is present on the bus, the host must already have the necessary information, as a learning phase is not possible. The LVR is included in the component driver and provides the I2C component's capabilities. This LVR is described below:

Bits	Name	Values
LVR[7:5]	Legacy I2C-only	3'b000: Index 0: Spike filter, max SCL clock frequency tolerant
		3'b001: Index 1: No spike filter, max SCL clock frequency tolerant
		3'b010: Index 2: No spike filter, not max SCL clock frequency tolerant
		3'b011 – 3'b111: Index 3-7: Reserved
LVR[4]	I2C mode indicator	0: I2C Fm+
		1: I2C Fm
LVR[3:0]	MIPI Alliance I3C WG reserved	0: Reserved
		1-15: 15 available codes for describing the device's capabilities and function in the sensor system

For ST I2C EEPROM, this register can have two values:

- 0x00 for products able to operate at Fm+ / 1 MHz
- 0x10 for products limited to Fm / 400 kHz

6 Demonstration of ST I2C EEPROM compatibility on I3C bus

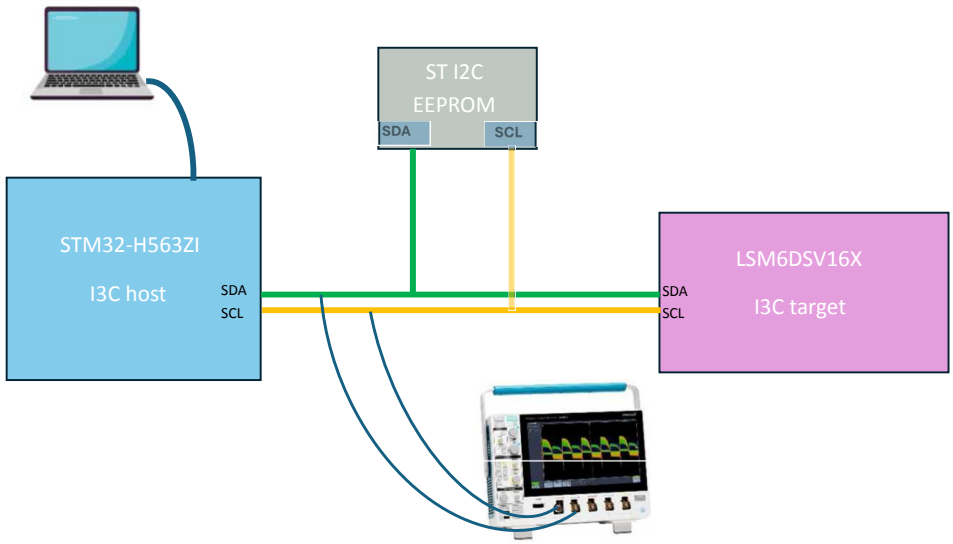
To delve deeper into the investigation of ST I2C EEPROM on the I3C bus, an experiment was set up.

The bench was initially built with I3C components, including an I3C host (STM32H563ZI) and an I3C target (LSM6DSV16X) communicating at a clock frequency of 12.5 MHz. The devices exchanged the BCR, DCR, and modified some capabilities, such as the data buffer size. The exchange occurred in both directions: host to target and target to host, at this speed. Initially, the bench was set up without the ST I2C EEPROM. The bus waveforms and data exchanges were verified. Subsequently, the ST I2C EEPROM was introduced, and the experiment was repeated. The data exchanges and waveform distortions were checked for I3C bus voltages of 3.3 V, 1.8 V, and 1.2 V I/O.

The purpose of the bench is to ensure that the ST I2C EEPROM does not introduce drawbacks when connected to the I3C bus.

The presence of the spike filter prevents the I2C component from misinterpreting an I3C command exchanged at a frequency that it cannot process. However, the presence of the I2C component can impact the rise and fall times of the SCL and SDA pads. This test bench evaluates the impact of the ST I2C EEPROM on these parameters.

Figure 2. Principle diagram of the bench



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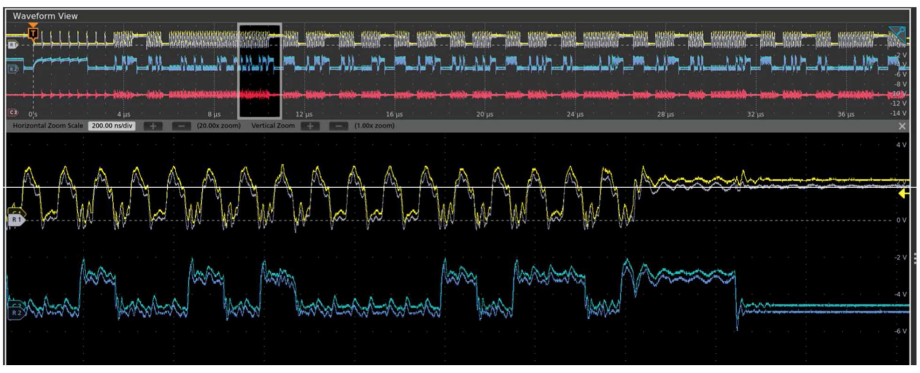
Example of I3C communication with and without ST I2C EEPROM running at 12.5 MHz

Figure 3. Example of I3C communication



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- The gray channel represents SCL probing without the ST I2C EEPROM on the bus.
- The yellow channel represents SCL probing with the ST I2C EEPROM on the bus.
- The dark blue channel represents SDA probing without the ST I2C EEPROM on the bus.
- The light blue channel represents SDA probing with the ST I2C EEPROM on the bus.

This experiment was conducted with several ST I2C EEPROMs, allowing multiple I3C bus voltages (3.3 V, 1.8 V, and 1.2 V I/O). All functional exchanges succeeded, and no signal distortion was observed during these experiments.

7 Conclusion

STMicroelectronics I2C EEPROMs are fully compatible with the I3C bus and do not negatively impact its operation. Tests show that these EEPROMs can be used in I³C bus configurations without introducing signal distortion, even at high communication frequencies such as 12.5 MHz. Due to their characteristics that meet I3C compatibility requirements (no clock stretching, 50 ns spike filters, no 20 mA open-drain driver, and 7-bit addressing), ST I2C EEPROMs can be integrated into I3C applications. This integration allows the advanced performance of the I³C protocol to be leveraged while maintaining compatibility with existing I2C components.

Revision history

Table 3. **Revision history**

Date	Version	Changes
27-Aug-2025	1	Initial release

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