Application note

Migrating from STM32WB0 to STM32WBA2 MCUs

Introduction

The designers of STM32 microcontroller applications must have the possibility to replace easily one microcontroller type with another one from the same product family or products from a different family. The reasons for migrating an application to a different microcontroller can be for example:

- To fulfill higher product requirements, extra demands on memory size, or additional peripherals.
- To meet cost reduction constraints that require switching to smaller components and shrink the PCB area.

This application note details the steps required to migrate from a design based on an STM32WB0 series device to an application based on one of the STM32WBA2 series MCUs.

This document provides guidelines for hardware and peripheral migration. To understand better the information inside this application note, the user must be familiar with the STM32 microcontroller family.

For additional information, refer to the product datasheets and reference manuals available on www.st.com.

1 General information

The STM32WBA2 devices use an embedded Arm® Cortex®-M33 with TrustZone® 32-bit core compared to the STM32WB0 using an Arm® Cortex®-M0+ 32-bit core. The core runs at 64 MHz for both the STM32WB0 and STM32WBA2 series. The STM32WBA2 core provides security features due to the presence of the ultralow power Arm® TrustZone® for Armv8-M.

Note: Arm® is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 STM32WBA2 series

The STM32WBA2 series devices are ultralow power and wireless MCUs, with enhanced efficiency, performance, and memory size such as:

- 512 Kbytes of single-bank flash memory with ECC accelerated by instruction/data caches and 96 Kbytes of embedded SRAM with optional parity.

The STM32WBA2 series includes an extended set of peripherals compared to the STM32WB0, such as the ones listed below:

- CPU
  - Replaced Cortec-M0+ with Cortex-M33
- Power consumption
  - Optimized power consumption in low-power mode using Stop modes.
- Interfaces
  - Improved AES hardware accelerator (AES)
  - Improved random number generator (RNG)
  - Replaced HSI64 by HSI16
  - Replaced LSI2 by LSI1
  - Replaced DMA and DMAMUX by low-power DMA (LPDMA)
  - Replaced I2C2 with I2C3
  - Added TrustZone security controller (GTZC)
  - Added HASH processor (HASH)
  - Added ICACHE
  - Added RAMCFG
  - Added timers (TIM2, TIM16, TIM17)
  - Added low-power timers (LPTIM1, LPTIM2)
  - Added serial audio interface (SAI)
  - Added full speed USB (1)
  - Added packet traffic arbitration (PTACONV)
  - Added tamper
  - Added RDP regression OEM key security
  - Added XSPI1 (1) interface with associated DLYBXS1, OTFDEC1, and MPCWM1
  - Added support for debug ETM
  - Added fractional PLL
  - Removed TIM1
  - Removed SPI1 and SPI2
  - Removed I2S functionality from SPI3

1. Available only for STM32WBA24/25 devices.

Both STM32WB0 and STM32WBA2 series embed high-speed memories and an extensive range of enhanced I/Os.

The STM32WB0 and STM32WBA2 series offer different memory sizes and use different packages.

Table 1. STM32WB0 and STM32WBA2 series overview

Package	Memory size		Device	
	Flash	SRAM	STM32WB0	STM32WBA2
VFQFPN32	192 Kbytes	24 Kbytes	STM32WB05KN	N/A
	256 Kbytes	32 Kbytes	STM32WB06KC	
		64 Kbytes	STM32WB07KC	

Package	Memory size		Device	
	Flash	SRAM	STM32WB0	STM32WBA2
VFQFPN32	512 Kbytes	64 Kbytes	STM32WB09KE	N/A
UFQFPN32	512 Kbytes	96 Kbytes	N/A	STM32WBA23KE
UFQFPN32 USB	512 Kbytes	96 Kbytes	N/A	STM32WBA24KE
WLCSP36	192 Kbytes	24 Kbytes	STM32WB05TN	N/A
	512 Kbytes	64 Kbytes	STM32WB09TE	
Thin WLCSP37 SMPS USB	512 Kbytes	96 Kbytes	N/A	STM32WBA25HE
VFQFPN48	256 Kbytes	32 Kbytes	STM32WB06CC	N/A
		64 Kbytes	STM32WB07CC	
UFQFPN48 SMPS	512 Kbytes	96 Kbytes	N/A	STM32WBA23CE
UFQFPN48 USB	512 Kbytes	96 Kbytes	N/A	STM32WBA24CE
UFQFPN48 SMPS USB	512 Kbytes	96 Kbytes	N/A	STM32WBA25CE
WLCSP49	256 Kbytes	32 Kbytes	STM32WB06CC	N/A
		64 Kbytes	STM32WB07CC	

2.1 Memory availability

The STM32WBA2 series embeds similar memory to the STM32WB0 series as shown in the table below.

Table 2. Memory size on STM32WB0 and STM32WBA2 series

Product	Flash memory		SRAM0	SRAM1	SRAM2	SRAM3
	Size	Bank				
STM32WBA2	512 Kbytes	Single	N/A	64 Kbytes (one page)	32 Kbytes (two pages 8 KB + 24 KB)	N/A
STM32WB0	Up to 512 Mbytes	Single	16 Kbytes (one page)	16 Kbytes (one page)	Up to 16 Kbytes (one page)	Up to 16 Kbytes (one page)

2.2 System architecture differences between STM32WB0 and STM32WBA2 series

Both STM32WB0 and STM32WBA2 series embed high-speed memories and an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, and a 32-bit multi-AHB bus matrix. Additionally, the STM32WBA2 series embeds an XSPI (quad-SPI) external memory interface.

The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation when several high-speed peripherals work simultaneously. STM32WBA2 has an ICACHE for internal and external code execution, which is not available in STM32WB0.

The STM32WBA2 series connects masters to the bus matrix which differ from the ones in the STM32WB0 series. The STM32WB0 series also embeds different peripherals on the internal buses.

The figures below detail the STM32WB0 and STM32WBA2 series system architectures.

Figure 1. **STM32WB0 system architecture**

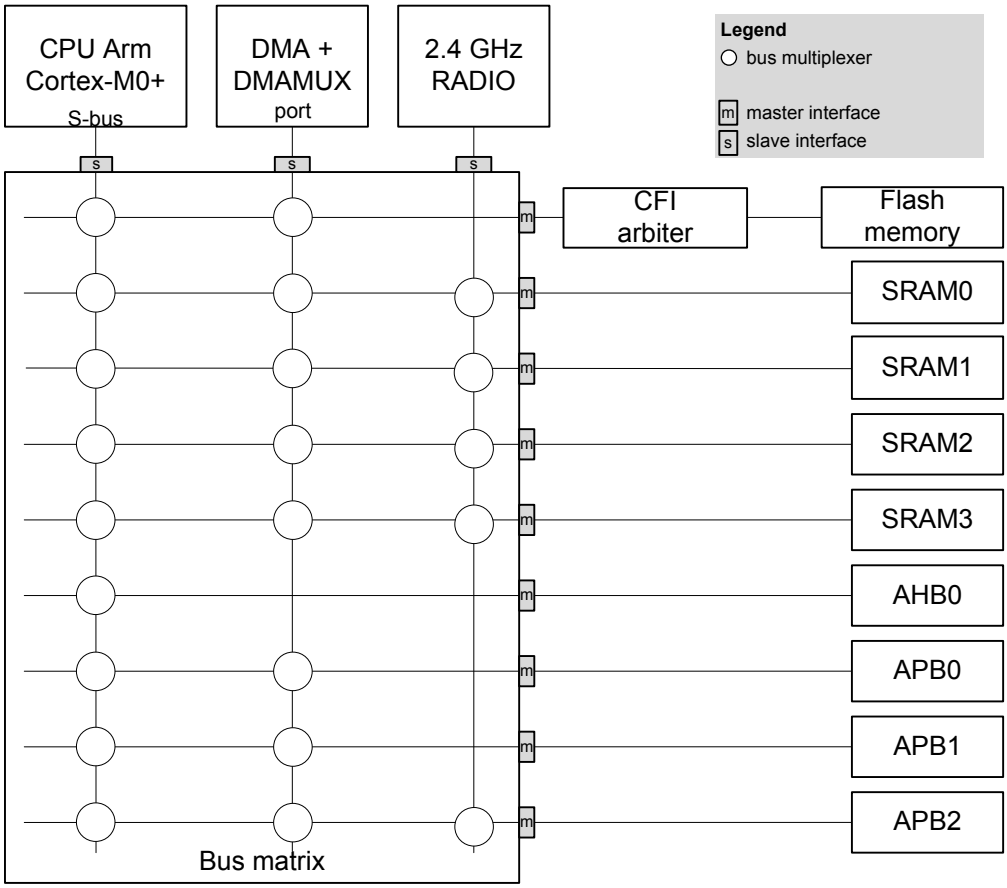
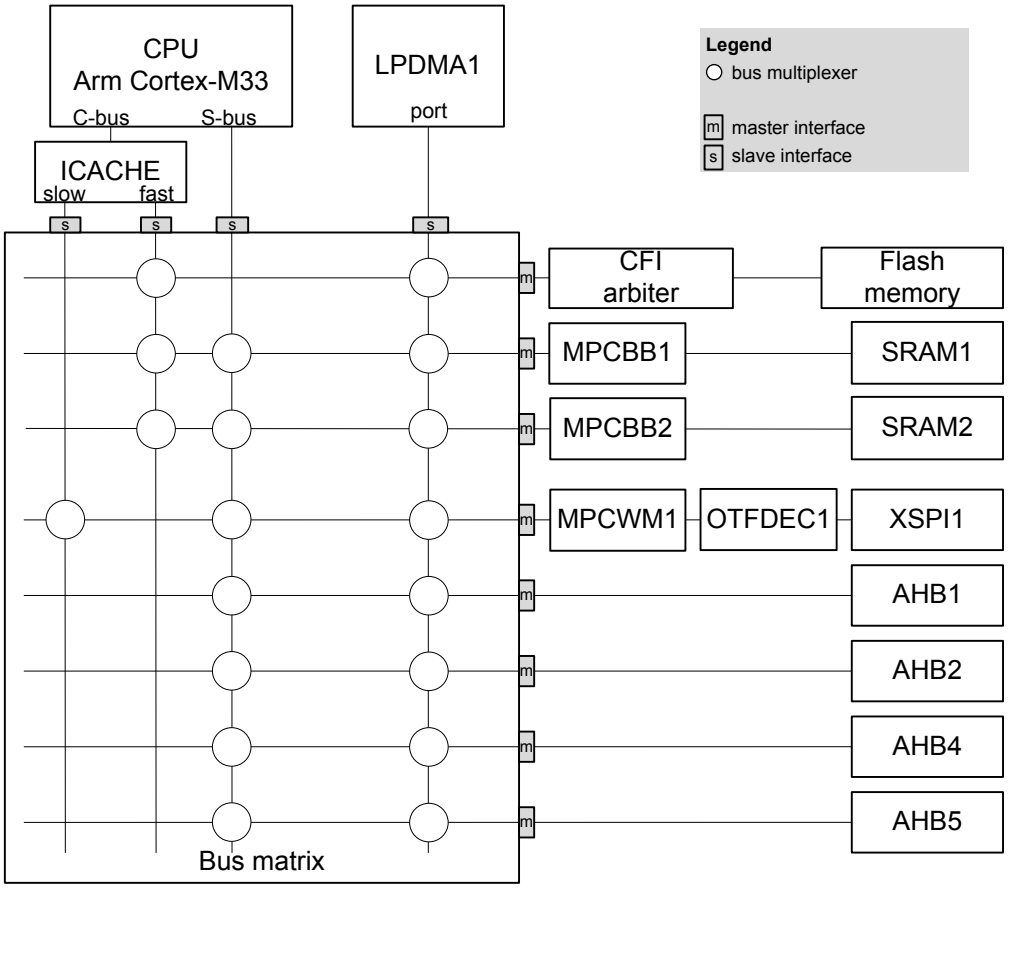


Figure 2. **STM32WBA2 system architecture**



The STM32WB0 and STM32WBA2 series architecture features a 32-bit multilayer AHB bus matrix that interconnects masters and slaves (see the tables below).

Table 3. **Masters connected to AHB bus matrix of STM32WB0 and STM32WBA2 series**

AHB bus matrix masters	Fast C-bus ICACHE	Slow C-bus ICACHE	S-bus	DMA	2.4 GHz RADIO
STM32WBA2	1	1	1	1	N/A
STM32WB0	N/A	N/A			1

Table 4. **Slaves connected to AHB bus matrix of STM32WB0 and STM32WBA2 series**

AHB bus matrix slaves	Internal flash memory	SRAMs	Peripherals								XSPI
			APB0	APB1	APB2	AHB0	AHB1	AHB2	AHB4	AHB5	
STM32WBA2	1	SRAM1, 2	N/A	N/A	N/A	N/A	1[1]	1	1[2]	1	1
STM32WB0		SRAM0, 1, 2, 3	1	1	1	1	N/A	N/A	N/A	N/A	N/A

1. *Including APB1 and APB2 peripherals.*
2. *Including APB7 peripherals.*

3 Hardware migration

The STM32WBA2 series offers several packages from 32 to 48 pins. The 48-pin packages have a reduced number of GPIOs. Four versions of pinout are available:

- Without internal SMPS and without USB FS: STM32WBA23 UFQFPN32 package
- Without internal SMPS and with USB FS: STM32WBA24
- With internal SMPS and without USB FS: STM32WBA23 UFQFPN48 package
- With internal SMPS and with USB FS: STM32WBA25

The STM32WBA2 series uses different packages compared to the STM32WB0. There is no package pin-2-pin compatibility.

Table 5. Packages between STM32WB0 and STM32WBA2 series

Package	STM32WB0	STM32WBA2
32-pin packages	20 GPIO	Up to 20 GPIO
48-pin packages	32 GPIO	Up to 27 GPIO
WLCSP36	29 GPIO	-
WLCSP37	-	15 GPIO
WLCSP49	29 GPIO	-

4 Boot mode compatibility

4.1 Boot modes selection

For the STM32WB0 series, the BOOT0 input pin comes from the PA10-BOOT0. For the STM32WBA2 series, the BOOT0 input pin may come from the PH3-BOOT0 pin or from an option bit, depending on the value of a user option bit to free the GPIO pad if needed.

Table 6. Boot pins on STM32WB0 and STM32WBA2

Pin	STM32WB0	STM32WBA2
PA8	IOBOOTVAL[0]	N/A
PA9	IOBOOTVAL[1]	
PA10	IOBOOTVAL[2] (Bootloader select)	
PA11	IOBOOTVAL[3]	
PH3	N/A	Bootloader select

The STM32WBA2 bootloader located in system memory is used to reprogram the flash memory by using USART, I2C, SPI, or USB FS (1) in device mode through the DFU (device firmware upgrade). The STM32WB0 bootloader only supports USART.

1. Only available on STM32WBA24/25 devices.

The STM32WB0 series boots from address 0x0000 0000 on flash or SRAM0 depending on REMAP. Where flash is located also at address 0x1004 0000.

The STM32WBA2 series has boot modes when TrustZone is disabled or enabled (see the tables below), using the Cortex-M33 VTOR. Where flash is located at address 0x0800 0000 and 0x0C00 0000. Refer to the series reference manual (RM0521) for more details.

Table 7. STM32WBA2 boot modes when TrustZone is disabled (TZEN = 0)

nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	Boot area	ST programmed default value
-	0	1	Boot address defined by user option bytes NSBOOTADD0[24:0]	User flash: 0x0800 0000
-	1	1	Boot address defined by user option bytes NSBOOTADD1[24:0]	Bootloader: 0x0BF8 8000
1	-	0	Boot address defined by user option bytes NSBOOTADD0[24:0]	User flash: 0x0800 0000
0	-	0	Boot address defined by user option bytes NSBOOTADD1[24:0]	Bootloader: 0x0BF8 8000

Table 8. STM32WBA2 boot modes when TrustZone is enabled (TZEN = 1)

BOOT_ LOCK	nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	RSS command	Boot area	STprogrammed default value
0	-	0	1	0	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	User flash: 0x0C000000
	-	1	1	0	RSS:	0x0FF80000

BOOT_LOCK	nBOOT0 FLASH_OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR[26]	RSS command	Boot area	STprogrammed default value
0	1	-	0	0	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	User flash: 0x0C000000
	0	-	0	0	RSS:	0x0FF80000
	-	-	-	0		
1	-	-	-	-	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	User flash: 0x0C000000

4.2 Embedded bootloader

The embedded bootloader is located in system memory and programmed by ST during production. This bootloader allows the user to reprogram the flash memory, using one of the serial interfaces listed in the table below.

Table 9. Bootloader interface on STM32WB0 and STM32WBA2 series

Peripheral	Pin name (number)	STM32WB0	STM32WBA2	
			STM32WBA23	STM32WBA24/25
DFU	USB_DP (PB8)	N/A		X
	USB_DM (PB9)			X
USART1	USART1_TX (PA1)	X	N/A	
	USART1_RX (PB0)	X		
	USART1_TX (PA6)	N/A	X	
	USART1_RX (PA12)		X	
I2C1	I2C1_SCL (PA15)	N/A	X	
	I2C1_SDA (PB3)		X	
I2C3	I2C3_SCL (PA6)	N/A	X	
	I2C3_SDA (PA7)		X	
SPI3	SPI3_NSS (PA5)	N/A	X	
	SPI3_SCK (PA8)		X	
	SPI3_MISO (PB4)		X	
	SPI3_MOSI (PA6)		X	

For more details on the bootloader, refer to the application note *STM32 microcontroller system memory boot mode* (AN2606).

5 Peripheral migration

5.1 STM32 products cross-compatibility

STM32 microcontrollers embed a set of peripherals that can be classified in the following groups:

- Group1: peripherals, by definition, common to all products

Those peripherals are identical, so they have the same structure, registers, and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.

- Group2: peripherals shared by all products but with only minor differences (in general to support new features)

Migration from one product to another is very easy and does not need any significant new development effort.

- Group3: peripherals that have considerable changes from one product to another (new architecture or new features for example)

For this group of peripherals, migration requires a new development at the application level.

The security architecture of STM32WBA2 series devices is based on Arm TrustZone with the Armv8-M mainline extension. The following elements can be configured as trusted or untrusted:

- Each GPIO or peripheral
- DMA channel
- Clock configuration register
- ICACHE
- Small part of flash memory or SRAM

The STM32WBA2 series microcontrollers innovative features include new Stop modes architecture, allowing wake-up from a reduced set of peripherals down to Stop 3 mode.

The table below summarizes the available peripherals in the STM32WB0 and STM32WBA2 series as well as their compatibility.

Table 10. STM32 peripheral compatibility between STM32WB0 and STM32WBA2 series

Peripheral		STM32WB0	STM32WBA2
Core		Cortex-M0+, MPU	Cortex-M33 TZ, MPU, FPU, DSP
Maximum CPU frequency		64 MHz	
Caches	ICACHE	N/A	1x ICACHE 4 KB
PWR/regulators	Power supply	1.71 to 3.6 V	
	LDO	Available on all products	
	LDO + internal SMPS	SMPS/LDO on-the-fly selection (1)	
	VOS range	Range 1	
		N/A	Range 1.5
			Range 2
Low-power mode		N/A	Stop 0
		N/A	Stop 1
		DeepStop	Stop 2
		N/A	Stop 3
		N/A	Standby retention
		Shutdown	Standby
Flash memory	Size	Up to 512 Kbytes	512 Kbytes
SRAMs	Bank	Single bank	Single bank with TrustZone

Peripheral		STM32WB0	STM32WBA2
Flash memory SRAMs	SRAM0	Up to 16 Kbytes (one page)	N/A
	SRAM1	Up to 16 Kbytes (one page)	64 Kbytes (one page)
	SRAM2	Up to 16 Kbytes (one page)	32 Kbytes with parity (two pages 8 KB and 24 KB)
	SRAM3	Up to 16 Kbytes with (one page)	N/A
DMA		DMA + DMAMUX (8 channels)	LPDMA (8 channels)
PLL		N/A	PLL (main)
GTZC (global TrustZone controller)		N/A	Three independent 32-bit AHB interfaces for TZSC, TZIC, and MPCBB, TZIC accessible only with secure transactions Secure and nonsecure access support privileged and unprivileged parts of TZSC Set of registers to define product security settings
Antitamper detection		N/A	Four tamper input/output pins 128-byte backup registers
CRC		1x CRC	
GPIO	Port A	PA[15:5,2:0]	
		PA[4:0]	N/A
	Port B	PB[15,12,9:8,6:2]	
		PB[14:13,11:10,7,1:0]	N/A
	Port C	N/A	PC[15:13]
	Port H		PH[3]
Timers	Advanced control	TIM1 (16-bit)	N/A
	General purpose	TIM2 (32-bit)	
	Basic	TIM16/17 (16-bit)	
	Low-power	N/A	LPTIM1/2 (16-bit) autonomous mode
	Watchdogs	1x IWDG	
		1x WWDG	N/A
	RTC	1x RTC + binary mode selection	
	SysTick	2	
Communication interfaces	SPI	SPI1	N/A
		SPI2 + I2S	
		SPI3 + I2S	SPI3 + autonomous mode
	I2C	I2C1	I2C1 + autonomous mode
		I2C2	N/A
		N/A	I2C3 + autonomous mode
	USART	USART1	USART1 + autonomous mode
	LPUART	LPUART1	LPUART1 + autonomous mode
	SAI	N/A (I2S in SPI)	SAI1
	XSPI	N/A	XSPI1, OTFDEC1, MPCWM1 (2)
	USB	N/A	USB full speed with embedded PHY(2)

Peripheral		STM32WB0	STM32WBA2
Analog peripherals	ADC	1x 12-bit ADC (1 Msps)	1x 12-bit ADC4 (2.5 Msps) + autonomous mode
Cryptographic peripherals	AES	1x AES in TRNG	1x AES
	PKA (private key accelerator)	1x PKA	
	HASH (SHA-256)	N/A	1x HASH
	RNG (true random number generator)	1x RNG	1x RNG (6 sources)
Debug		SWD	
		N/A	JTAG
		N/A	ETM

1. *Only available on STM32WBA23/25.*
2. *Only available on STM32WBA24/25.*

5.2 Secure and nonsecure boundaries of peripheral memory mapping

The peripheral address mapping is different between the STM32WB0 and the STM32WBA2 series. The STM32WBA2 TrustZone secure and nonsecure boundaries have been added to the memory map. For more details on the memory mapping, refer to the product reference manual.

6 Migration of security peripherals

6.1 TAMP

The STM32WBA2 series antitamper detection circuit is used to protect sensitive data from external attacks. Tamper is not available for STM32WB0. The table below lists the features of TAMP for the STM32WB0 and STM32WBA2 series.

Table 11. TAMP in STM32WB0 and STM32WBA2 series

Feature	STM32WB0	STM32WBA2
Tamper pin	N/A	TAMP_IN1/OUT2
		TAMP_IN2/OUT1
		TAMP_IN3/OUT4
		TAMPIN4/OUT3

6.2 OTFDEC (on-the-fly decryption engine)

The STM32WBA2 series embeds the OTFDEC1. The on-the-fly decryption engine is not available for the STM32WB0 series.

The OTFDEC1 decrypts in real time the encrypted content stored in the XSPI1, memory-mapped mode, external memory.

6.3 HASH (hash processor)

The STM32WBA2 series embeds the HASH processor. The HASH processor is not available for the STM32WB0 series.

The HASH provides hardware processing for secure hash algorithms SHA-1, SHA-224, SHA-256, and HMAC.

6.4 RNG (true random number generator)

The STM32WB0 and STM32WBA2 series embed both an RNG hardware accelerator with different features. The STM32WBA2 embeds an improved version with additional health test configuration registers and fewer noise sources.

Table 12. RNG features in STM32WB0 and STM32WBA2 series

Features	STM32WB0	STM32WBA2
AES	AES-CMAC 128-bit	(In AES)
Noise source	N/A	3
Health test configuration	N/A	HTCR0
		HTCR1
		HTCR2
		HTCR3

6.5 PKA (public key accelerator)

The STM32WB0 and STM32WBA2 series embed the same PKA hardware accelerator with similar features.

6.6 AES hardware accelerators

The STM32WBA2 series embeds an AES accelerator. In the STM32WB0 series, an AES function is available inside the TRNG.

Table 13. **AES features in STM32WB0 and STM32WBA2 series**

Features	STM32WB0	STM32WBA2
ECB, CCB chaining	N/A (AES-CMAC 128-bit in TRNG)	X
CTR, CCM, GCM chaining		X
AES 128-bit ECB encryption speed		51 cycles
256-bit key		X
AES tamer signal		X

6.7 GTZC (global TrustZone controller)

The STM32WBA2 series embeds the TrustZone security, which is not available for STM32WB0.

The security architecture of the STM32WBA2 series is based on Arm TrustZone with the Armv8-M mainline extension. The following elements can be configured as trusted or untrusted:

- Each GPIO or peripheral
- DMA channel
- Clock configuration register
- ICACHE
- Small part of flash memory or SRAM

The GTZC embedded in the STM32WBA2 series is used to configure secure-TrustZone and privileged attributes within the full system. It contains the following subblocks:

- TZSC: TrustZone security controller

This subblock defines the secure/privileged state of slave peripherals. It also controls the region sizes and properties for the memory protection controller watermark based (MPCWM). The TZSC informs some peripherals (such as RCC or GPIOs) about the secure status of each securable peripheral, by sharing with RCC and I/O logic.

- MPCBB: memory protection controller block-based

This subblock configures the internal RAM in a TrustZone-system product having segmented SRAM (pages of 512 bytes) with programmable security and privileged attributes.

- TZIC: TrustZone illegal access controller

This subblock gathers all illegal access events in the system and generates a secure interrupt towards NVIC.

6.7.1 GTZC implementation and resource assignments

The STM32WBA2 series implements GTZC peripherals and memory assignment.

Table 14. **MPCBB resources in STM32WBA2 series**

MPC	Resource	Block size (bytes)	Parameters	STM32WBA2
MPCBB1	SRAM1	512	Memory size (Kbytes)	64
			Number of blocks	128
			Number of superblocks	4
MPCBB2	SRAM2		Memory size (Kbytes)	32
			Number of blocks	64
			Number of superblocks	2

Table 15. **MPCWM resources in STM32WBA2 series**

MPC	Resource	Parameters	STM32WBA2
MPCWM1	XSPI1	Regions	2
		Water mark granularity (Kbytes)	128

6.7.2 TrustZone security architecture

When the TrustZone is enabled, the Armv8-M attributes define the access permissions based on secure and nonsecure state:

- SAU (security attribution unit): up to eight SAU configurable regions are available for security attribution
- IDAU (implementation defined attribution unit): provides a first memory partition as nonsecure or nonsecure callable attributes. This partition is then combined with the results from the SAU security attribution and the higher-security state is selected.

Based on IDAU security attribution, flash memory, system SRAMs, and peripheral memory space are aliased twice for secure and nonsecure states. However, the external memory space is not aliased.

6.7.3 TrustZone peripheral classification

When the TrustZone security is active, a peripheral can be either securable, or TrustZone-aware as follows:

- Securable: peripheral protected by an AHB/APB firewall gate that is controlled by TZSC to define security properties.
- TrustZone-aware: peripheral connected directly to AHB or APB bus. Implements a specific TrustZone behavior such as a subset of registers being secure.

7 Migration of 2.4 GHz RADIO

This section analyzes the differences and similarities for the 2.4 GHz RADIO implemented in the STM32WB0 and STM32WBA2 series.

7.1 2.4 GHz RADIO

The table below shows the differences between the 2.4 GHz RADIO in the STM32WB0 and in the STM32WBA2 series.

Table 16. 2.4 GHz RADIO features in STM32WB0 and STM32WBA2 series

Features		STM32WB0	STM32WBA23/24/25
Bluetooth® LE	2 Mbps	X	
	1 Mbps	X	
	500 kbps coded	X	
	125 kbps coded	X	
	Audio	X	
	AoA/AoD	X	
Zigbee	Beacon management	N/A	X
	Non-beaconed PAN	N/A	X
Thread		N/A	X
Matter		N/A	With an external host
Proprietary		Bluetooth-based	IEEE802.15.4 based
Concurrent modes	Bluetooth - Thread	N/A	X
	Bluetooth - Zigbee		X
	Zigbee - Thread		X
	Bluetooth - Thread - Zigbee		X
Packet traffic arbitration (PTA)		N/A	X
Maximum output power		+8 dBm	+10 dBm
External LNA (low noise amplifier)		X	N/A
External PA (power amplifier)		X	

8 Migration of system peripherals

This section analyzes the differences and similarities between system peripherals implemented in the STM32WB0 and STM32WBA2 series.

8.1 SYSCFG (system configuration controller)

The table below shows the differences between the SYSCFG in the STM32WB0 and in the STM32WBA2 series.

Table 17. SYSCFG features in STM32WB0 and STM32WBA2 series

Features	STM32WB0	STM32WBA2
Device ID	Yes	(In DBGMCU)
JTAG ID	Yes	(In DBGMCU)
Common features	N/A	Managing robustness feature
		Configuring TrustZone security register access
		Configuring FPU interrupts
	Driving capability on some I/Os and voltage booster for I/Os analog switches	
Managing I/O compensation cells	N/A	Compensation cells on V_{DD} the PVT conditions to control the current slew-rate and output impedance in I/O buffer
I^2C Fast-mode plus	I^2C I/Os fast mode plus drive is controlled from the I2C peripheral. This mode can still be enabled/disabled in SYSCFG for four I/Os when not used by I2C.	
GPIO port interrupt	Yes	(In EXTI)
WKUP	Yes	(In PWR)
Internal signal management	Yes	(In EXTI)
PVD interrupt	Yes	(In EXTI)
Flash operation abort	N/A	Flash operation abort on interrupt

8.2 Flash memory

The STM32WB0 and the STM32WBA2 series flash memory include similar memory space (see the table below).

Table 18. Flash memory features in STM32WB0 and STM32WBA2 devices

Feature	STM32WB0	STM32WBA2
Size	Up to 512 Kbytes single bank (256 x 2-Kbyte pages)	512 Kbytes single bank (64 x 4 Kbytes pages)
	OTP area: 1 Kbytes, base address 0x1000 1800	OTP area: 512 bytes, base address 0x0BF9 0000
	N/A	RSS + RSS lib, base address 0x0FF8 0000
	Bootloader, base address -	Bootloader, base address 0x0BF8 8000
	User area, base address 0x1004 0000	User area, base address 0x0800 0000
Access modes	Read (R) and write (W)	
	Single bank, 32-bit read/write access	Single bank, 64-bit read/write access
ECC	N/A	8 bits per 64-bit double word The ECC mechanism supports:

Feature	STM32WB0	STM32WBA2
		• One error detection and correction • Two errors detection
Read-access latency	Up to 1 wait-state (WS) depending on the frequency	Up to 1 wait-state (WS) depending on the supply voltage and the frequency
	N/A	The flash memory supports a low-power read mode (LPM). The number of WS depends on the supply voltage and the frequency
	N/A	Instruction prefetch through ICACHE can be enabled by setting the PRFTEN bit that increases code execution speed
Power-down mode per Bank	N/A	After reset, the bank is in normal mode. The bank can be put in power-down
Endurance capability	10 kcycles (written and erased) on all flash memory	N/A
Flash program and erase operations	Page/mass erase	N/A
	32-bit (word) programming	64-bit (double word) programming
	Burst 4 words, 4x 32-bit programming	Burst 16 double words, 16x 64-bit programming
Flash memory protection	Write protection (SEG)	Write protection (WRP)
	Readout protection (KEYWRITE)	Readout protection (RPD)
	N/A	One secure watermark- based area
		One secure watermark- based hide protection area
		HDP_PEND[6:0]
		HDPEN[7:0]
		HDP_ACCDIS[7:0]
		One secure watermark- based extended hide protection area
		HDP_PEXT[6:0]
		HDP_ACCDIS[7:0]
		On-the-fly programmable secure block-based areas with page granularity
		On-the-fly programmable privileged block-based areas with page granularity
Privileged register protection	N/A	For secure (SPRIV) and nonsecure (NSPRIV) accesses
Locking keys for RDP	N/A	OEM key protection for RDP regression between levels: • Possible RDP regression from L1 to L0 with OEM1 key • Possible RDP regression from L1 to L0.5 with OEM2 key • Possible RDP regression from L2 to L1 with OEM2 key
Operation abort	N/A	Operation abort on interrupt

The STM32WBA2 option bytes are configured by the end user depending on the application requirements. The STM32WBA2 new option bytes have been added to the register map. (See the table below and refer to the section 'Flash memory option bytes' of the product reference manual for more details).

Table 19. Main option bytes in STM32WB0 and STM32WBA2 devices

Option bit/byte	STM32WB0	STM32WBA2
Global TrustZone activation	N/A	TZEN: global TrustZone security enable
Readout protection	KEYWRITE level	RDP level
Reset	N/A	BOR_LEV [2:0]: BOR reset level
		NRST_STOP: reset generation in STOP mode
		NRST_STDBY: reset generation in Standby mode
		SRAM_RST: SRAM1 erased when a system reset occurs
		SRAM2_RST: SRAM2 erases when system reset occurs
Watchdog	N/A	WWDG_SW: window watchdog selection
		IWDG_SW: hardware or software independent watchdog selection
		IWDG_STOP: independent watchdog counter freeze in Stop mode
		IWDG_STDBY: independent watchdog counter freeze in Standby mode
Secure and nonsecure boot	N/A	NSWBOOT0: Software BOOT0
		NBOOT0 option bit
		NSBOOTADD0[24:0]: nonsecure boot base-address 0
		NSBOOTADD1[24:0]: nonsecure boot base-address 1
		SECBOOTADD0[24:0]: secure boot base-address 0
		BOOT_LOCK: boot lock
Flash memory secure watermark	N/A	SECWM_PSTRT[6:0]: first page of the secure area
		SECWM_PEND[6:0]: last page of the secure area
		HDP_PEND[6:0]: last page of HDP area
		HDPEN[7:0]: hide protection area enable
Flash memory write protection (WRP) areas	N/A	WRPA_PSTRT[6:0]: first page of the WPR area A
		WRPA_PEND[6:0]: the last page of the WPR area A
		UNLOCK WRP area A
		WRPB_PSTRT[6:0]: first page of the WPR area B
		WRPB_PEND[6:0]: the last page of the WPR area B
		UNLOCK WRP area B
Flash memory locking keys for RDP level regression	N/A	OEM1KEY[127:0]: OEM1 key
		OEM1KEYCRC[7:0]: read only
		OEM2KEY[127:0]: OEM2 key
		OEM2KEYCRC[7:0]: read only
RAM parity	N/A	SRAM2_PE: SRAM2 parity check enables option bit

8.3 SRAMs

In the STM32WBA2 series SRAM control is implemented in the RAMCFG controller (refer to section "RAMs configuration controller" in the product reference manual for more details).

The table below compares the embedded SRAM features in STM32WB0 and STM32WBA2 devices.

Table 20. SRAMs in STM32WB0 and STM32WBA2 devices

Features		STM32WB0	STM32WBA2
Size (Kbytes)		SRAM0: up to 16 Kbytes	N/A
		SRAM1: up to 16 Kbytes	SRAM1: 64 Kbytes
		SRAM2: up to 16 Kbytes	SRAM2 page 1: 8 Kbytes
			SRAM2 page 2: 24 Kbytes
		SRAM3: up to 16 Kbytes	N/A
Access by DMA and CPU		Bytes, half-words (16 bits) or full words (32 bits) possible access	
CPU access bus	System bus	Direct access	
	C-bus access	N/A	Direct access
			SRAM1, SRAM2 (through ICACHE remap)
Retention in Stop		N/A	SRAM1: 64 Kbytes
			SRAM2 page 1: 8 Kbytes
			SRAM2 page 2: 24 Kbytes
Retention in DeepStop/Standby retention		SRAM0: 16 Kbytes	N/A
		SRAM1: 16 Kbytes	SRAM1: 64 Kbytes
		SRAM2: 16 Kbytes	SRAM2 page 1: 8 Kbytes
			SRAM2 page 2: 24 Kbytes
		SRAM3: 16 Kbytes	N/A
Security		N/A	When the TrustZone security is enabled, all SRAMs are secure after reset
Security		N/A	The SRAMs can be programmed as nonsecure using the MPCBBx with a block granularity of 512 bytes
Hardware erase conditions		N/A	All SRAMs are erased by hardware in case of RDP level regression to L0.5 or L0.
			SRAM2 is protected by the tamper detection circuit and is erased by hardware in case of tamper detection
Software erase conditions		N/A	Each SRAM erase can be requested by executing a specific software sequence, detailed in section ‘RAMCFG’ of the product reference manuals.
System reset erase		N/A	SRAM2 is erased when a system reset occurs if the SRAM2_RST option is selected
			SRAM1 is erased when a system reset occurs if the SRAM1_RST option is selected
WRP		N/A	SRAM2 can be write protected with a page granularity of 1 Kbyte
Error detection		N/A	SRAM2 parity error can be detected if the SRAM2_PE option is selected
			Interrupts are generated when a SRAM2 parity error is detected: • NVIC parity interrupt • NMI parity interrupt Interrupts allow the device to exit Sleep, Stop 0 or Stop 1 mode

Features	STM32WB0	STM32WBA2
Error detection	N/A	SRAM2 parity error event can be linked to the BRK_IN break input of TIM16 or TIM17
Read access latency	0 wait-states	Up to 1 wait-state (WS) depending on voltage range 2 and AHB clock frequency (HCLK)

8.4 Caches

The STM32WBA2 series embed an ICACHE that allows for more efficient use of internal flash memory. ICACHE is not available from STM32WB0.

Table 21. ICACHE features in STM32WB0 and STM32WBA2 series

Features	STM32WB0	STM32WBA2
ICACHE size	N/A	4 KB
Fast port		32-bit (Flash, SRAM1, SRAM2)
Slow port (remap)		32-bit (XSPI bank)(1)

1. *Only available on STM32WBA24/25.*

8.5 DMA

The STM32WB0 series devices have a DMA plus DMAMUX whereas the STM32WBA2 series devices have an LPDMA.

The STM32WBA2 peripherals have been added to the DMA request and trigger map. (See the table below and refer to section 'DMA' of the product reference manual for more details).

Table 22. DMA features in STM32WB0 and STM32WBA2 series

Features	STM32WB0	STM32WBA2
Number of masters	Single bidirectional AHB master	Single bidirectional AHB master
Linked-list	N/A	Separately programmed source and destination transfers
		Programmable data handling between source and destination
		Block-level (programmable number of data bytes)
		Linear source and destination addressing: Programmable signed address offsets between successive burst transfers
Data transfers from source to destination	Peripheral-to-memory, memory-to-peripheral, memory-to-peripheral, and peripheral-to-peripheral	
Number of channels	8	
Number of requests/triggers	17 DMA requests	45 DMA requests
	N/A	28 triggers
Autonomous data transfer in Sleep and Stop modes	N/A	Autonomous data transfers and wake up during the low-power modes Stop 0
TrustZone privileged/unprivileged	N/A	Yes
Retention	N/A	Down to Stop 1 mode (Not retained in Stop 2 and Stop 3)

8.6 NVIC

The STM32WBA2 and STM32WB0 series devices have an extended NVIC mapping. The STM32WBA2 new peripherals have been added to the NVIC map.

Table 23. NVIC mapping in STM32WB0 and STM32WBA2 series

IRQ	Position	
	STM32WB0	STM32WBA2
NVM/FLASH	0	6 to 7
RCC	1	9 to 10
PVD	2	1
I2C1	3	41 to 42
I2C2	4	N/A
SPI1	5	N/A
SPI2	6	N/A
SPI3	7	57
USART1	8	43
LPUART1	9	44
TIM1	10	N/A
RTC	11	2 to 3
ADC4	12	59
PKA	13	56
GPIOA	15	(see EXTI)
GPIOB	16	(see EXTI)
DMA	17 (DMA)	28 to 35 (LPDMA CH0 to CH7)
RADIO	18 (BLE_TXRX)	60 (RADIO)
	21 (RADIO_CTRL)	N/A
	22 (MR_BLE)	
	23 (CPU_WKUP)	
	24 (BLE_WKUP)	60 (RADIO)
	25 (BLE_SEQ)	N/A
TAMP	N/A	4
RAMCFG	N/A	5
GTZC	N/A	8
EXTI0 to EXTI15	(see GPIOA and GPIOB)	11 to 26
IWDG	N/A	27
OTFDEC1	N/A	36
TIM2	N/A	40
LPTIM1	N/A	45
LPTIM2	N/A	46
TIM16	N/A	47
TIM17	N/A	48
I2C3	N/A	49 to 50
SAI	N/A	51

IRQ	Position	
	STM32WB0	STM32WBA2
AES	N/A	52
RNG	N/A	53
FPU	N/A	54
HASH	N/A	55
ICACHE	N/A	58
WKUP	N/A	61 to 62
RCC AUDIO	N/A	63
USB	N/A	64(1)
XSPI1	N/A	65(1)
RADIO_IO	N/A	66 to 67

1. *Only available on STM32WBA24/25.*

8.7 EXTI

The STM32WBA2 series devices have one EXTI. The STM32WB0 configurable signals are controlled in the SYSCFG.

Table 24. EXTI mapping in STM32WB0 and STM32WBA2 series

Event	Position	
	STM32WB0	STM32WBA2
GPIO	GPIOA and GPIOB (in SYSCFG)	0 to 15
PVD	PVD (in SYSCFG)	16
RADIO	N/A	19 to 20

8.8 RCC (reset and clock control)

The STM32WBA2 series RCC manages clocks and resets of system and peripherals, similar features as the STM32WB0.

Table 25. RCC features in STM32WB0 and STM32WBA2 series

Feature	STM32WB0	STM32WBA2
Safe and flexible reset management without external components	System reset, power reset	
	N/A	Backup domain reset
Internal clock sources	HSI64 with trimming (PLL mode with HSE)	N/A
	N/A	HSI16 with trimming
	LSI_LPMU 32 kHz 1%	LSI1 32 kHz 1%
	LSI2 32 kHz 500 ppm/°C	N/A
External clock sources	HSE32 32 MHz with trimming	
	LSE 32.768 kHz	
PLLs	N/A	PLL1 (main PLL 64 MHz)

The table below lists the RCC input/output signals and their mapping on the STM32WB0 and STM32WBA2 series.

Table 26. RCC pin names in STM32WB0 and STM32WBA2 series

Alternate function	Pin name STM32WB0	Pin name STM32WBA2
NRST	RSTN	NRST
OSC32_IN	PB13	N/A
	N/A	PC14
OSC32_OUT	PB12	N/A
	N/A	PC15
OSC_IN	OSCIN	OSC_IN
OSC_OUT	OSCOUT	OSC_OUT
MCO	PA5, PA11, PB15	N/A
	N/A	PA8
LSCO	PA4, PA5, PA6, PA9, PA10, PB12	N/A
	N/A	PA2
AUDIO_CLK	N/A	PA5

The table below details the RCC clock sources for STM32WB0 compared to the STM32WBA2 series.

Table 27. Clock sources in STM32WB0 and STM32WBA2 series

Clock source	STM32WB0	STM32WBA2
System clock	64 MHz maximum frequency	64 MHz maximum frequency
	16 MHz after reset, DeepStop, and Shutdown modes using HSI64 /4	16 MHz after reset, Stop, and Standby modes using HSI16
	HSI64, HSI64PLL, HSE	N/A
	N/A	HSI16, HSE32, PLL
HSE	32 MHz user trimmed	
HSI64	Generated from an internal 64 MHz RC oscillator 1% Is the system clock after reset	N/A
HSI64PLL	Generated from the HSE is an internal 64 MHz RC oscillator HSE accuracy	
HSI16	N/A	Generated from an internal 16 MHz RC oscillator 1% 16 MHz RC factory and user trimmed Can be used as a backup clock source (auxiliary clock) if the HSE crystal oscillator fails Is the system clock after wake up from Stop and Standby modes
LSE	32.768 kHz or 32.000 kHz configurable drive/consumption, available in the V_{DD} domain	
LSI	N/A	LSI1 32 kHz low consumption (refer to electrical characteristics section of the datasheet), available in the V_{DD} domain.
	LSI2 24 kHz – 49 kHz high accuracy (refer to electrical characteristics section of the datasheet), available in the V_{DD} domain	N/A
Clock-out capabilities MCO	HSE	HSE32

Clock source	STM32WB0	STM32WBA2
Clock-out capabilities MCO	HSI64, HSI64 /2048, SYSCLK, SMPS clock, ADC clock	N/A
	N/A	LSI, LSE, HSI16, SYSCLKPRE, pll1pclk, pll1qclk, pll1rclk, hclk5
Clock-out capabilities LSCO	LSI or LSE	
	LSI_LPMU	N/A
Clock measurement and calibration using timers	N/A	LSI calibration using TIM16/TIM17/ LPTIM1
		HSI16 calibration using TIM16/TIM17/ LPTIM2
Interrupt	N/A	HSECSS (linked to NMI IRQ)
	N/A	An equivalent interrupt vector to the one below is available for secure events, only when TrustZone is enabled
	N/A	LSECSS
	N/A	PLL1RDY
	LSIRDY, LSERDY, HSIRDY, and HSERDY	
	HSIPLLRDY, HSIPLLUNLOCKDET	N/A
	N/A	Audio synchronization CAF, COF, and CAEF
	RTCRST, IWDGRST	N/A
	CSCM EOF_SEQ	N/A

8.8.1 PLL

The STM32WBA2 series embeds a fractional PLL. Fractional PLL is not available for the STM32WB0 series.

Table 28. PLL max frequency in STM32WB0 and STM32WBA2 series

Product voltage range	STM32WB0	STM32WBA2
PLL clock out	N/A	Maximum 64 MHz

8.8.2 Bus frequencies versus voltage scaling

The STM32WB0 and STM32WBA2 series embed the following voltage scaling. There is additional voltage scaling added in STM32WBA2. The table below lists the maximum frequencies of internal bus in the STM32WB0 and STM32WBA2 series, depending on the product voltage range.

Table 29. Bus max frequency versus voltage scaling in STM32WB0 and STM32WBA2 series

Product voltage range	STM32WB0	STM32WBA2
Range 1	Maximum 64 MHz	AHB1, AHB2, AHB4: maximum 64 MHz
	N/A	AHB5: maximum 32 MHz
Range 1.5	N/A	AHB1, AHB2, AHB4: maximum 64 MHz
		AHB5: maximum 32 MHz
Range 2	Used in DEEPSTOP mode (no bus clock)	AHB1, AHB2, AHB4, AHB5: maximum 16 MHz

8.8.3 CSS (clock security system)

The STM32WBA2 series embeds CSS. CSS is not available for the STM32WB0 series.

Table 30. **CSS in STM32WB0 and STM32WBA2 series**

CSS clock source	STM32WB0	STM32WBA2
CSS on HSE	N/A	Same features
CSS on LSE modes	N/A	Run, Stop, Standby retention, same features

8.8.4 Specific ADC clock features

The STM32WB0 and STM32WBA2 series embed the following ADC clock features, in particular:

- If the STM32WBA2 ADC is precisely triggered by a TIMx timer without any uncertainty, the HCLK must be selected as the ADC kernel clock source. The other clock sources are asynchronous to TIMx timers. The LPTIMx timers are also asynchronous.

Table 31. **ADC in STM32WB0 and STM32WBA2 series**

Feature	STM32WB0	STM32WBA2
ADC bus clock	PCLK	HCLK
ADC kernel clock	HSI64 or HSI64PLL divided by 4 (16 MHz)	N/A
	N/A	HCLK
		HSE32
		HSI16ker
		pll1pclk

8.8.5 RTC and TAMP clock

The STM32WB0 and STM32WBA2 series embed similar RTC clocks. The STM32WB0 series has no TAMP clocks. The table below lists the features of RTC and TAMP clock sources for the STM32WB0 and STM32WBA2 series.

Table 32. **RTC and TAMP clock in STM32WB0 and STM32WBA2 series**

Features		STM32WB0	STM32WBA2
Clock source for RTC and TAMP		LSE, or LSI	
		SYSCLK /2048	N/A
		N/A	HSE32 /32
Only the backup registers used in TAMP with tampers in edge detection mode		No kernel clock required	
Backup domain active clocks		LSE and LSI	
Operational	Run	Operations	
	Stop 0, 1, 2	N/A	Operational
	DeepStop/Stop 2	Operational	
	Stop 3	N/A	Not operational (retained)
	Standby retention	N/A	Not operational (power down)
	Shutdown/Standby	Not operational (power down)	

8.8.6 Timer and watchdog clock sources

The STM32WBA2 timer clock frequencies are automatically defined by hardware, with the following cases:

- If the APB prescaler equals one, the timer clock frequencies are set to the APB domain frequency.
- Otherwise, they are set to twice (x 2) the APB domain frequency.

If the independent watchdog (IWDG) is started by either hardware option or software access, the LSI oscillator is forced on and cannot be disabled. After the LSI oscillator temporization, the LSI 32 kHz clock is provided to the IWDG.

The STM32WB0 timer clock is either 64 MHz or 32 MHz depending on the SYSCLK clock source used (HSI64 or HSE32).

The STM32WB0 and STM32WBA2 series embed similar RTC clocks. The STM32WB0 has no TAMP clocks. The table below lists the features of RTC and TAMP clock sources for the STM32WB0 and STM32WBA2 series.

Table 33. TIM and IWDG clock in STM32WB0 and STM32WBA2 series

Feature	STM32WB0	STM32WBA2
TIM	SYSCLK (HSI64 or HSE)	N/A
	N/A	PCLK or PCLK x2
IWDG	LSI	
	LSE	N/A
	SYSCLK /2048	

8.8.7 Peripheral clock gating and reset

The STM32WBA2 series peripheral clock gating and reset provide similar features as the STM32WB0 series. The STM32WBA2 has additional Sleep mode peripheral clock which enables bits allowing background autonomous mode operation. The table below shows the RCC registers used for peripheral access configuration for the STM32WB0 and STM32WBA2 series.

Table 34. RCC clock and reset registers for STM32WB0 and STM32WBA2 series

Register	STM32WB0	STM32WBA2
AHB: [enter/exit] AHB peripherals from Reset	RCC_AHBRSTR	RCC_AHB1RSTR RCC_AHB2RSTR RCC_AHB4RSTR RCC_AHB5RSTR
APB: [enter/exit] APB peripherals from Reset	RCC_APB0RSTR RCC_APB1RSTR RCC_APB2RSTR	RCC_APB1RSTR1 RCC_APB1RSTR2 RCC_APB2RSTR RCC_APB7RSTR
AHB: [enable/disable] the AHB peripheral clock	AHBENR	RCC_AHB1ENR RCC_AHB2ENR RCC_AHB4ENR RCC_AHB5ENR
APB: [enable/disable] the APB peripheral clock	RCC_APB0ENR RCC_APB1ENR RCC_APB2ENR	RCC_APB1ENR1 RCC_APB1ENR2 RCC_APB2ENR RCC_APB7ENR
AHB: [enable/disable] the AHB peripheral clock in Sleep mode	N/A	RCC_AHB1SMENR RCC_AHB2SMENR RCC_AHB4SMENR RCC_AHB5SMENR
APB: [enable/disable] the APB peripheral clock in Sleep mode	N/A	RCC_APB1SMENR1 RCC_APB1SMENR2 RCC_APB2SMENR RCC_APB7SMENR

8.8.8 Peripheral clock source migration

The STM32WBA2 series peripheral clock gating and reset provides similar features as the STM32WB0 series.

Table 35. Peripheral clock sources in STM32WB0 and STM32WBA2 series

Peripheral	STM32WB0	STM32WBA2
IWDG	LSI	
	LSE, SYSCLK /2048	N/A
RTC/TAMP	LSE, LSI	
	SYSCLK /2048	N/A
	N/A	HSE32 /32
LPTIMx (x = 1, 2)	N/A	HSI16, lsesys, LSI
TIM1	SYSCLK source (HSI64 or HSE)	N/A
TIM2	N/A	PCLK1
TIMx (x = 16, 17)	N/A	PCLK2
USART1	16 MHz	HSI16, lsesys, PCLK2, SYSCLK
LPUART1	16 MHz	HSI16, lsesys, PCLK7, SYSCLK
SPI1	16 MHz	N/A
SPI2	16 MHz	N/A
SPI3	16 MHz	HSI16, PCLK7, SYSCLK
I2C1	16 MHz	HSI16, PCLK1, SYSCLK
I2C2	16 MHz	N/A
I2C3	N/A	HSI16, PCLK7, SYSCLK
XSPI(1)	N/A	AHB
		Feedback clock delay DLYBXS1
SAI1	N/A	HSI16, SYSCLK, pll1pclk, pll1qclk, AUDIOCLK (external)
USB FS(1)	N/A	pll1pclk
RNG	16 MHz	HSI16, lsesys, LSI, pll1qclk/2
ADC4	16 MHz	HSI16, HCLK1, SYSCLK, HSE, pll1pclk
CPU system timer	HCLK	
	N/A	HSI16/4, lsesys, LSI, HCLK1/8
GPIOx	HCLK (x = A, B)	HCLK2 (x = A, B, C, H)
PKA	HCLK	HCLK2
AES	N/A	HCLK2
CRC	HCLK	HCLK1
RCC AUDIO synchronization	N/A	pll1pclk, pll1qclk

1. *Only available on STM32WBA24/25.*

8.8.9 System clock and low-power modes

This system clock used before and after wake up in the STM32WB0 and STM32WBA2 series are similar. The STM32WBA2 new low-power modes have been added.

Table 36. System clock before entering low-power mode in STM32WB0 and STM32WBA2 series

Power mode	STM32WB0	STM32WBA2
Sleep	Any	
Stop 0, Stop 1	N/A	Any
DeepStop/Stop 2	HSI64 or HSI64PLL	
Stop 3	N/A	
Stanby retention	N/A	Any
Shutdown/Standby	HSI64 or HSI64PLL	Any

Table 37. System source after wake up in STM32WB0 and STM32WBA2 series

Power mode	STM32WB0	STM32WBA2
Sleep	Same clock as before entering Sleep mode	
Stop 0, Stop 1	N/A	HSI16 at 16 MHz
DeepStop/Stop 2	Same clock as before entering DeepStop mode (HSI64 or HSI64PLL)	
Stop 3	N/A	
Standby retention	N/A	
Shutdown/Standby	HSI64 at 16 MHz	

8.8.10 Autonomous peripheral mode

The STM32WBA2 series embeds autonomous peripheral modes.

For STM32WBA2 series microcontrollers, some peripherals support an autonomous mode in Stop 0, Stop 1, and Stop 2 modes:

- Autonomous peripherals can generate a kernel clock request and a bus clock request when needed, even in Stop mode.
- The selected oscillator is woken up.
- In autonomous mode with DMA, the bus clocks as well as the oscillator (HSI16) are automatically switched off as soon as the transfer is finished. The device automatically goes back to the selected low-power mode.
- If the autonomous peripheral is configured with interrupt enabled, the interrupt wakes up the device into Run mode.

Furthermore, the following capabilities exist in Stop mode when needed:

- If USARTs, LPUARTs and I2C select HSI16 as the kernel clock source, it can be enabled by these peripherals in Stop 0, Stop 1 or Stop 2 mode.
- The LSE can remain always ON in Stop mode, with no on-the-fly activation capability, when it drives USARTs, LPUARTs, LPTIMs.

The STM32WB0 series microcontrollers do not support autonomous peripherals.

The table below lists the main features of the autonomous mode supported by the STM32WB0 and STM32WBA2 series.

Table 38. Autonomous peripherals in STM32WB0 and STM32WBA2 series

Features	STM32WB0	STM32WBA2
Stop 0 and Stop 1 retained peripherals	N/A	Autonomous peripherals in Stop 0 and Stop 1 modes only. Enabled if both xxEN and xxSMEN bits of the peripheral are set (xx = instance name). LPDMA1 is associated. SRAM1 and SRAM2 are associated.

Features	STM32WB0	STM32WBA2
DeepStop/Stop 2 retained peripherals	N/A	Autonomous peripherals in Stop 2 modes. Enabled if both xxEN and xxSMEN bits of the peripheral are set (xx = instance name) Autonomous peripherals mapped on AHB4 or APB7. No DMA association.
Autonomous peripherals in Stop 0 and Stop 1	N/A	USART1
		LPUART1
		SPI3
		I2Cx (x = 1, 3)
		LPTIMx (x = 1, 2)
		ADC4
		LPDMA
Autonomous peripherals in Stop 2	N/A	LPUART1
		SPI3
		I2C3
		LPTIM1
Autonomous peripherals in Stop 3	N/A	None
Autonomous peripheral requesting its kernel clock in Stop	N/A	If the peripheral kernel clock request selects HSI16, the internal oscillator (HSI16) is woken up if it was off. The kernel clock is propagated only to the peripherals requesting it. When all peripheral kernel clock requests selecting HSI16 are released, the HSI16 is switched off.
Autonomous peripheral requesting its bus clock in Stop 0 or Stop 1 mode	N/A	Stop 0 mode is entered. The internal oscillator (HSI16) is woken up if it was off. The system clock is propagated to all peripherals configured with both xxEN and xxSMEN bits set. When all peripherals release their bus clock request, the system clock is stopped, and if also all peripheral kernel clock requests selecting HSI16 are released, the HSI16 is switched off.
Forcing HSI16 ON in Stop mode	N/A	Can be done by configuring HSIKERON. The oscillator is propagated only to the kernel clock of the enabled autonomous peripherals with this oscillator selected as the kernel clock. This allows the peripheral baud rates or conversion rates increase, as there is no need to wait for the oscillator wake up time when the peripheral requests its kernel clock.
LSE or LSI as kernel clock	N/A	The LSE or LSI selected as the peripheral kernel clock remains always ON in Stop mode.

8.8.11 Operating modes

The table below lists the main operating modes and main clock sources of the STM32WB0 and STM32WBA2 series.

Table 39. Operating modes in the STM32WB0 and STM32WBA2 series

Features	STM32WB0	STM32WBA2
Run	CPU running Peripheral bus and kernel clocks can be disabled by software	
	System clock active on HSI64, HSI64PLL, or HSE	System clock active on PLL, HSI16, or HSE
Sleep mode	Stops the CPU hclk clock. The memory interface clocks can be stopped by software during Sleep mode. AHB to APB bridge clocks are disabled by hardware during Sleep mode, when all the clocks of the peripherals connected to them are disabled	
Stop 0 mode	N/A	Stops the system clock when there is no autonomous peripheral bus clock request Disables the PLL Disables HSI16, HSE oscillators when not requested by an autonomous peripheral
Stop 1 mode	N/A	Stops the system clock Disables the PLL and HSE oscillator. Disables HSI16 when not requested by an autonomous peripheral
DeepStop/Stop 2 mode	Stop the system clock. Disable the HSI64, HSE oscillators	Stops the system clock Disables the PLL and HSE oscillator Disables HSI16 when not requested by an autonomous peripheral
Stop 3 mode	N/A	Stops the system clock Disables the PLL and HSI16, HSE oscillators No autonomous peripheral. Stops LSE and LSI clock in VCORE domain
Standby retention	N/A	Stops the system clock. Disables the PLLs and HSI16, HSE oscillators
Shutdown/Standby modes	Stop all the clocks. Disable the HSI64, HSE, LSI, and LSE oscillators	Stop the system clock Disable the PLLs and HSI16, HSE oscillators
LSE or LSI oscillators	Remain active in Stop mode and DeepStop mode. Stopped in Shutdown mode	Remain active in Stop mode and Standby mode
Low-power modes and memory/bus operation	If a flash memory programming operation is ongoing, low-power mode entry is delayed until the flash memory interface access is finished. If one access to the APB domain is ongoing, low-power mode entry is delayed until the APB access is finished	

8.8.12 RCC security and privilege functional description

The STM32WBA2 series embeds TrustZone security, which is not available from STM32WB0.

When the TrustZone security is activated, the RCC can secure RCC configuration and status bits from being modified by nonsecure accesses. The RCC_SECCFGR register is used in the STM32WBA2 series to prevent nonsecure access to read or modify the items listed in the table below.

Table 40. **Secured RCC items in STM32WB0 and STM32WBA2 series**

Features	STM32WB0	STM32WBA2
Clock sources configuration and status bits	N/A	HSE, HSECSS, HSI16, LSI, LSE, LSECSS
PLL, AHB, and APB prescaler configuration and status bits		PLL1, AHB, and APB
System and independent clocks		SYSCLK, SysTick
Clock out capability		MCO and LSCO
Remove reset flags settings		RMVF

8.8.13 RCC privilege protection modes

The STM32WBA2 series embeds the TrustZone privilege, which is not available for the STM32WB0 series.

In the STM32WBA2 series, there are dedicated register bits for privileged and unprivileged access: RCC_PRIVCFGR (SPRIV and NSPRIV bits).

By default, after a reset, all RCC registers can be read or written with privileged and unprivileged access. The only exception being RCC_PRIVCFGR, which can be written with privileged access only.

8.9 Power (PWR)

The STM32WB0 and STM32WBA2 series have different PWR features:

- STM32WBA2 Stop 0, Stop 1, and Stop 3 mode, not available for STM32WB0
- STM32WBA2 Stop 2 mode comparable with STM32WB0 DeepStop mode
- STM32WBA2 Standby retention mode, not available for STM32WB0
- STM32WBA2 Standby mode comparable with STM32WB0 Shutdown mode
- STM32WBA2 USB supply, not available for STM32WB0
- STM32WBA2 SMPS is different from STM32WB0 SMPS

8.9.1 Power-supply pins

The STM32WB0 and STM32WBA2 series have different power supplies. The table below lists the differences between STM32WB0 and STM32WBA2 supply pins.

Table 41. **Power-supply pins in STM32WB0 and STM32WBA2 series**

Pin name	
STM32WB0	**STM32WBA2**
VDD	
N/A	VDDUSB(1)
VDDA decoupling	VDDA supply input
VDDSD	VDDSMPS(2)
VLXSD	VLXSMPS(2)
VSSSD	VSSSMPS(2)
VFBSD	N/A (merged with VDD11)
VCAP	VDD11(2), VCAP(3)
VDDRF	
N/A	VDDRFPA
N/A	VDDANA(2)
N/A	VDDHPA
VSSRF	

Pin name	
STM32WB0	STM32WBA2
VSSRFTRX	N/A
VSSSX	N/A
VSSIFADC	N/A
VSSA	
VSSIO	VSS

1. *Only available on STM32WBA24/25 devices.*
2. *Only available on STM32WBA23/25 devices.*
3. *Only available on STM32WBA23/24 devices.*

The table below details pins that are specific to low lower modes.

Table 42. Specific pins in STM32WB0 and STM32WBA2 series

Pin name	STM32WB0	STM32WBA2
WKUPx	N/A	WKUPx (x = 1 to 4 and 6 to 8) input interrupt and wake up pins Up to 11 multiplexed interrupt and wake up pins from Run, Sleep, Stop, and Standby modes
CSleep	N/A	CSLEEP output MCU in Sleep mode
CStop	N/A	CSTOP output CPU domain in Stop mode

8.9.2 SMPS power supply

The STM32WB0 and STM32WBA2 series support different similar low-power modes. STM32WBA2 supports additional low-power modes. The table below shows the related STM32WBA2 series SMPS and supply pins compared to those in STM32WB0.

The STM32WBA2 SMPS provides the VCORE voltage level, whereas the STM32WB0 SMPS provides an intermediate voltage of 1.4 V.

Table 43. Specific SMPS pins in STM32WB0 and STM32WBA2 series

Pin name	STM32WB0	STM32WBA2
VDDSMPS	VDDSD supply	VDDSMPS supply
VLXSMPS	VLXSD output	VLXSMPS output
VSSSMPS	VSS ground	VDDSMPS ground
VFBSD	VFBSD regulated feedback 1.4 V	N/A
VDD11/VCAP	VCAP VCORE decoupling	VDD11 SMPS regulated feedback input VCORE VCAP VCORE decoupling

8.9.3 Power modes

The STM32WB0 and STM32WBA2 series support both different and similar low-power modes. STM32WBA2 supports additional low-power modes. The table below shows the related STM32WBA2 series power modes compared to those in the STM32WB0 series.

Table 44. Power modes in STM32WB0 and STM32WBA2 series

Power mode	STM32WB0	STM32WBA2
Run mode	Run voltage scaling range 1	
	N/A	Run voltage scaling range 1.5

Power mode	STM32WB0	STM32WBA2
Run mode	N/A	Run voltage scaling range 2
Sleep	Sleep voltage scaling range 1 (entered from Run voltage range 1)	
	N/A	Sleep voltage scaling range 1.5 (entered from Run voltage range 1.5)
	N/A	Sleep voltage scaling range 2 (entered from Run voltage range 2)
DeepStop/Stop	SRAM pages can be powered down in DeepStop mode	SRAM pages can be powered down in Stop modes
	N/A	Stop 0 voltage scaling range 1 (entered from Run voltage range 1)
		Stop 0 voltage scaling range 1.5 (entered from Run voltage range 1.5)
		Stop 0 voltage scaling range 2 (entered from Run voltage range 2)
	N/A	Stop 1 BOR can be set in ultralow power mode
	DeepStop BOR is enabled	Stop 2 BOR can be set in ultralow power mode
	N/A	Stop 3 BOR can be set in ultralow power mode
Standby retention	N/A	SRAM pages, RTC/TAMP, 2.4 GHz RADIO RAMS, and sleep timer can be retained in Standby mode BOR can be set in ultralow power mode
Shutdown/Standby	Shutdown BOR can be disabled in Shutdown mode	Standby BOR can be set in ultralow power mode
	N/A	IWDG is retained in Standby mode

8.9.4 Peripheral power migration

The STM32WBA2 series peripheral power management provides similar features as the STM32WB0 series.

Table 45. Peripheral power in STM32WB0 and STM32WBA2 series

Peripheral	STM32WB0	STM32WBA2
Low-power flags	N/A	STOPF
	DEEPSTOPF	STOP2F
	N/A	SBF
USB FS supply(1)	N/A	USV
SRAM0 retention	N/A always retained	N/A
SRAM1 retention	RAMRET1	R1RSB1, SRAM1PDS1
SRAM2 retention	RAMRET2	R2RSB1, SRAM2PDS1 (page 1)
	N/A	R2RSB2, SRAM2PDS2 (page 2)
SRAM3 retention	RAMRET3	N/A
PKA RAM retention	N/A	PKARAMPDS
2.4 GHz RADIO retention	N/A	RADIORSB
Stop 2 mode PTA signals state retention	N/A	PTASREN, PTASR
Standby mode GPIO state retention	GPIO PA[15:5,2:0]: PUA, PDA, APC	GPIO PA[15:5,2:0]: IORETEN, IORET
	GPIO PA[4:3]: PUA, PDA, APC	N/A

Peripheral	STM32WB0	STM32WBA2
Standby mode GPIO state retention	GPIO PB[15,12,9:8,6:2]: PUB, PDB, APC	GPIO PB[15,12,9:8,6:2]: IORETEN, IORET
	GPIO PB[14:13,10,7,1:0]: PUB, PDB, APC	N/A
	N/A	GPIO PC[15:13]: IORETEN, IORET
	N/A	GPIO PH[3]: IORETEN, IORET

1. *Only available on STM32WBA24/25.*

8.9.5 PWR security and privilege

The STM32WBA2 series embeds TrustZone security, which is not available for the STM32WB0 series.

When the TrustZone security is activated, the PWR can secure PWR configuration and status bits from being modified by nonsecure accesses.

By default, after a reset, all PWR registers can be read or written with privileged and unprivileged accesses. The only exception being PWR_PRIVCFGR, which can be written with privileged access only.

Table 46. Secured PWR items in STM32WB0 and STM32WBA2 series

Features	STM32WB0	STM32WBA2
Low-power mode configuration and status bits	N/A	SRAM RSB and DS bits, RADIORSB, LPMS, FLASHFWU, CSSF
Voltage detection		PVDLS, PVDE, FSTEN, REGSEL
Backup domain		DBP
Wake up pin		WUP

8.9.6 PWR interrupts

The power interrupts sources of the STM32WB0 and STM32WBA2 series are listed in the table below.

Table 47. PWR interrupt sources of STM32WB0 and STM32WBA2 series

Interrupt vector	Description	Event flag	STM32WB0	STM32WBA2
PWR_WKUP	Wake up pin interrupt	WUFx (x = 1 to 4 and 6 to 8)	N/A (wake up in SYSCFG)	11 pins
PWR_WKUPS	Wake up pin secure interrupt			
PVD_PVM	Programmable voltage detector	-	PVD_ISC	N/A EXTI line 16

8.10 CRC

The CRC architecture is the same in both STM32WB0 and STM32WBA2 series, with the same features.

9 Migration of timer peripherals

The STM32WB0 and STM32WBA2 series embed similar timers with similar features. The STM32WBA2 new timers and features have been added.

9.1 Advanced-control timers (TIM1)

The STM32WB0 series embeds one advanced-control timer, TIM1. There is no advanced-control timer in the STM32WBA2 series.

9.2 GP timers with up, down, up-down autoreload counter (TIM2)

The general-purpose timers consist of a 16-bit or 32-bit autoreload counter driven by a programmable prescaler. The STM32WBA2 series embeds general-purpose timer TIM2. There is no general-purpose timer in the STM32WB0 series.

The STM32WB0 and STM32WBA2 series AF pins of general-purpose timer TIM2 is mapped as described in the table below.

Table 48. TIM2 AF pins on STM32WB0 and STM32WBA2 series

AF pin	STM32WB0	STM32WBA2
TIM2_ETR	N/A	PA5, PB6, PB12
TIM2_CH1		PA5, PB6, PB12
TIM2_CH2		PA8
TIM2_CH3		PA7
TIM2_CH4		PA6

9.3 GP timers with autoreload upcounter (TIM16/17)

The STM32WBA2 series embeds two 16-bit resolution general-purpose timers with a 16-bit autoreload upcounter (TIM16 and TIM17). There is no general-purpose timer in the STM32WB0 series.

The STM32WB0 and STM32WBA2 series AF pins of general-purpose timers TIM16/17 are mapped as described in the table below.

Table 49. TIM16/17 AF pins on STM32WB0 and STM32WBA2 series

AF pin	STM32WB0	STM32WBA2
TIM16_BKIN	N/A	PB15
TIM16_CH1		PA2, PB9
TIM16_CH1N		PB8
TIM17_BKIN		PA15
TIM17_CH1		PA1, PB4
TIM17_CH1N		PB3

9.4 Low-power timers (LPTIM1/2)

The STM32WBA2 series embeds two 16-bit resolution low-power timers with a 16-bit autoreload upcounter (LPTIM1 and LPTIM2). There is no general-purpose timer in the STM32WB0 series.

The STM32WB0 and STM32WBA2 series AF pins of low-power timers LPTIM1/2 are mapped as described in the table below.

Table 50. **LPTIM1/2 AF pins on STM32WB0 and STM32WBA2 series**

AF pin	STM32WB0	STM32WBA2
LPTIM1_ETR	N/A	PB8
LPTIM1_CH1		PA12
LPTIM1_CH2		PA8, PA15
LPTIM1_IN1		PA0
LPTIM1_IN2		PB3
LPTIM2_ETR		PA5
LPTIM2_CH1		PA11
LPTIM2_CH2		PA1
LPTIM2_IN1		PB9
LPTIM2_IN2		PB4

9.5 Watchdogs

The STM32WB0 and STM32WBA2 series embed the same IWDG watchdogs. An independent watchdog (IWDG) with similar features.

Table 51. **IWDG features on STM32WB0 and STM32WBA2 series**

Features	STM32WB0	STM32WBA2
Prescaler	/4 to /256	
	N/A	/512 to /1024
Status	PVU, RVU, WVU	
	N/A	EWU, ONF, EWIF
Early wake up	N/A	X

9.6 Real-time clock (RTC)

The STM32WB0 and STM32WBA2 series embed a similar RTC with similar features.

Table 52. **RTC operation in STM32WB0 and STM32WBA2 series**

AF pin	STM32WB0	STM32WBA2
Run	Operational	
Stop 0, Stop 1, Stop 2	N/A	Operational
Stop 3		Not operational (retained)
Standby retention/DeepStop	Operational	
Standby/Shutdown	Not operational (powered down)	

The STM32WB0 and STM32WBA2 series AF pins of RTC are mapped as described in the table below.

Table 53. **RTC AF pins in STM32WB0 and STM32WBA2 series**

AF pin	STM32WB0	STM32WBA2
RTC REFIN	N/A	PB9
RTC_TS	N/A	PC13
RTC_OUT1	PA8, PA9	PC13

AF pin	STM32WB0	STM32WBA2
RTC_OUT2	N/A	PB2

9.7 SysTick timer

The STM32WB0 series Cortex-M0+, embeds one SysTick timer. The STM32WBA2 series Cortex-M33 with TrustZone embeds two SysTick timers when TrustZone is activated, but only one SysTick when TrustZone is disabled.

The STM32WBA2 supports an additional SysTicktimer clock source.

Table 54. SysTick in STM32WB0 and STM32WBA2 series

Feature	STM32WB0	STM32WBA2
SysTick clock source	HCLK	HCLK
	N/A	HCLK1/8
		LSI
		lsesys
		HSI16/4

10 Migration of communication peripherals

10.1 Serial peripheral interface (SPI)

The STM32WB0 and STM32WBA2 series embed similar SPI with similar features. Additionally, the STM32WB0 series embeds SPI1, SPI2, I2S2, and I2S3.

The STM32WB0 and STM32WBA2 series AF pins of SPI1/2/3 and I2S2/3 are mapped as described in the table below.

Table 55. SPI AF pins in STM32WB0 and STM32WBA2 series

AF pin function	STM32WB0	STM32WBA2
SPI1_MOSI	PA8, PA10, PA15, PB14	N/A
SPI1_MISO	PA14, PB13	
SPI1_SCK	PA9, PA13, PB11, PB12	
SPI1_NSS	PA11, PA12, PB10	
SPI2_MOSI	PA6, PA12	
SPI2_MISO	PA1, PA7, PA13	
SPI2_SCK	PA5, PA7, PB10	
SPI2_NSS	PA4, PA6, PB11	
I2S2_SD	PA6, PA12, PB5	
I2S2_SCK	PA5, PA7, PB7, PB10	
I2S2_MCK	PA0, PB9	
I2S2_WS	PA4, PA6, PB6, PB11	
SPI3_MOSI	PA11	N/A
	N/A	PA6, PA9, PB8
SPI3_MISO	PA8	N/A
	N/A	PA7, PA10, PB4, PB9
SPI3_SCK	PA3	N/A
	N/A	PA0, PA8
SPI3_NSS	PA9	N/A
	N/A	PA5
SPI3_RDY	N/A	PA6, PA8
I2S3_SD	PA11	(see SAI)
I2S3_SCK	PA3	
I2S3_MCK	PA2, PA10	
I2S3_WS	PA9	

10.1.1 SPI autonomous mode

The SPI3 peripheral in the STM32WBA2 series supports autonomous operation down to Stop 2 mode.

10.2 I2C

The STM32WBA2 series embeds the I2C1 and I2C3.

The STM32WB0 series embeds the I2C1 and I2C2.

The STM32WB0 and STM32WBA2 series AF pins of I2CI1/2/3 are mapped as described in the table below.

Table 56. **I2C AF pins in STM32WB0 and STM32WBA2 series**

AF pin function	STM32WB0	STM32WBA2
I2C1_SCL	PA0, PB11	N/A
	N/A	PA15, PB2
I2C1_SDA	PA1, PB10	N/A
	N/A	PA11, PB3
I2C1_SMBA	PB15	
	PA12	N/A
I2C2_SCL	PA13, PB6, PB13	N/A
I2C2_SDA	PA14, PB7, PB14	
I2C2_SMBA	PA15	
I2C3_SCL	N/A	PA6, PB2
I2C3_SDA		PA7, PA8, PA11
I2C3_SMBA		PB15

10.2.1 I2C autonomous mode

The I2C1 peripheral in the STM32WBA2 series supports autonomous operation down to Stop 1 mode.
The I2C3 peripheral in the STM32WBA2 series supports autonomous operation down to Stop 2 mode.

10.3 U(S)ART and LPUART

The STM32WB0 and STM32WBA2 series embed the same USART1, and LPUART1 with similar features.
The STM32WB0 and STM32WBA2 series AF pins of USART1 and LPUART1 are mapped as described in the table below.

Table 57. **U(S)ART/LPUART AF pins in STM32WB0 and STM32WBA2 series**

AF pin function	STM32WB0	STM32WBA2
USART1_TX	PA1, PA9, PB9, PB15	N/A
	N/A	PA5, PA6, PB2. PB12
USART1_RX	PA8, PB0, PB14	N/A
	N/A	PA7, PA8, PA9, PA12
USART1_CK	PA2, PB8	N/A
	N/A	PA1, PA5
USART1_CTS	PA0, PB3, PB6	N/A
	N/A	PA7, PB4
USART1_RTS_DE	PA3, PB2, PB7	N/A
	N/A	PA2, PA6
LPUART1_TX	PA4, PB3, PB4, PB6	N/A
	N/A	PA2, PB5, PH3
LPUART1_RX	PA5, PB5, PB7, PB8	N/A
	N/A	PA1, PA10
LPUART1_CTS	PA6, PB9	N/A
	N/A	PA0, PB15, PB8
LPUART1_RTS	PA7, PB0	N/A

AF pin function	STM32WB0	STM32WBA2
LPUART1_RTS	N/A	PA9, PA10, PB9, PH3

10.4 Serial audio interface (SAI)

The STM32WBA2 series embeds the SAI. The STM32WB0 series embeds I2S feature in SPI2 and SPI3.
The STM32WBA2 series AF pins of SAI1 are mapped as described in the table below.

Table 58. SAI AF pins in STM32WB0 and STM32WBA2 series

AF pin function	STM32WB0	STM32WBA2
SAI1_SD_A	N/A (in I2S2 and I2S3, see SPI)	PA6, PB12
SAI1_FS_A		PA8
SAI1_SCK_A		PA5, PA7
SAI1_MCLK_A		PA6
SAI1_SD_B	N/A	PA12
SAI1_FS_B		N/A
SAI1_SCK_B		
SAI1_MCLK_B		
SAI1_D1		PA2, PA8, PA10
SAI1_D2		PA5, PB5
SAI1_CK1		PA1, PA9, PB4
SAI1_CK2		PA6

10.5 Universal serial bus interface (USB)

The STM32WBA2 series USB full speed has been added. There is no USB FS in the STM32WB0 series.
The STM32WBA2 series AF pins of USB FS are mapped as described in the table below.

Note: USB FS is only available on STM32WBA24/25.

Table 59. USB pins in STM32WB0 and STM32WBA2 devices

Pin name	STM32WB0	STM32WBA24/25
USB_SOF	N/A	PA8
USB_NOE		PA13
USB_DM		PB9
USB_DP		PB8

11 Migration of analog peripherals

11.1 Analog-to-digital converter (ADC)

The STM32WBA2 series embeds a 12-bit ADC4 single ended. The STM32WB0 series embeds a 12-bit ADC4 differential.

The STM32WBA2 embeds fewer external channels.

The STM32WB0 and STM32WBA2 series AF pins of ADC4 are mapped as described in the table below.

Table 60. ADC implementation in STM32WB0 and STM32WBA2 devices

Features	STM32WB0	STM32WBA2
ADC4_IN1	ADC_VINP0 PB3	N/A
	N/A	ADC4_IN1 PA8
ADC4_IN2	ADC_VINM0 PB2	N/A
	N/A	ADC4_IN2 PA7
ADC4_IN3	ADC_VINP1 PB1	N/A
	N/A	ADC4_IN3 PA6
ADC4_IN4	ADC_VINM1 PB0	N/A
	N/A	ADC4_IN4 PA5
ADC4_IN5	ADC_VINP2 PA15	N/A
ADC4_IN6	ADC_VINM2 PA14	N/A
ADC4_IN7	ADC_VINP3 PA13	N/A
	N/A	ADC4_IN5 PA2
ADC4_IN8	ADC_VINM3 PA12	N/A
	N/A	ADC4_IN6 PA1
ADC4_IN9	N/A	ADC4_IN7 PA0
VDDA	VDDA(1)	VDDA

1. *Only available on WLCSP package.*

12 Migration of external memory interface peripherals

The STM32WBA2 series microcontrollers embeds an external memory interface XSPI.

12.1 Extended-SPI interface (XSPI)

The STM32WBA2 series embeds an external memory interface XSPI1 with associated OTFDEC1 and DLYBXS1.
The STM32WB0 has no external memory interface.

Note: XSPI1 is only available on STM32WBA24/25.

Table 61. Extended-SPI implementation in STM32WB0 and STM32WBA2 devices

Features	STM32WB0	STM32WBA2
Quad-SPI	N/A	XSPI1
Feedback delay		DLYBXS1
OTFDEC		OTFDEC1
MPCWM		MPCWM1

13 Software migration

The STM32WBA2 series embeds a Cortex®-M33, whereas the STM32WB0 series embeds a Cortex®-M0+.:

13.1 Reference documents

Check the following documents for more details:

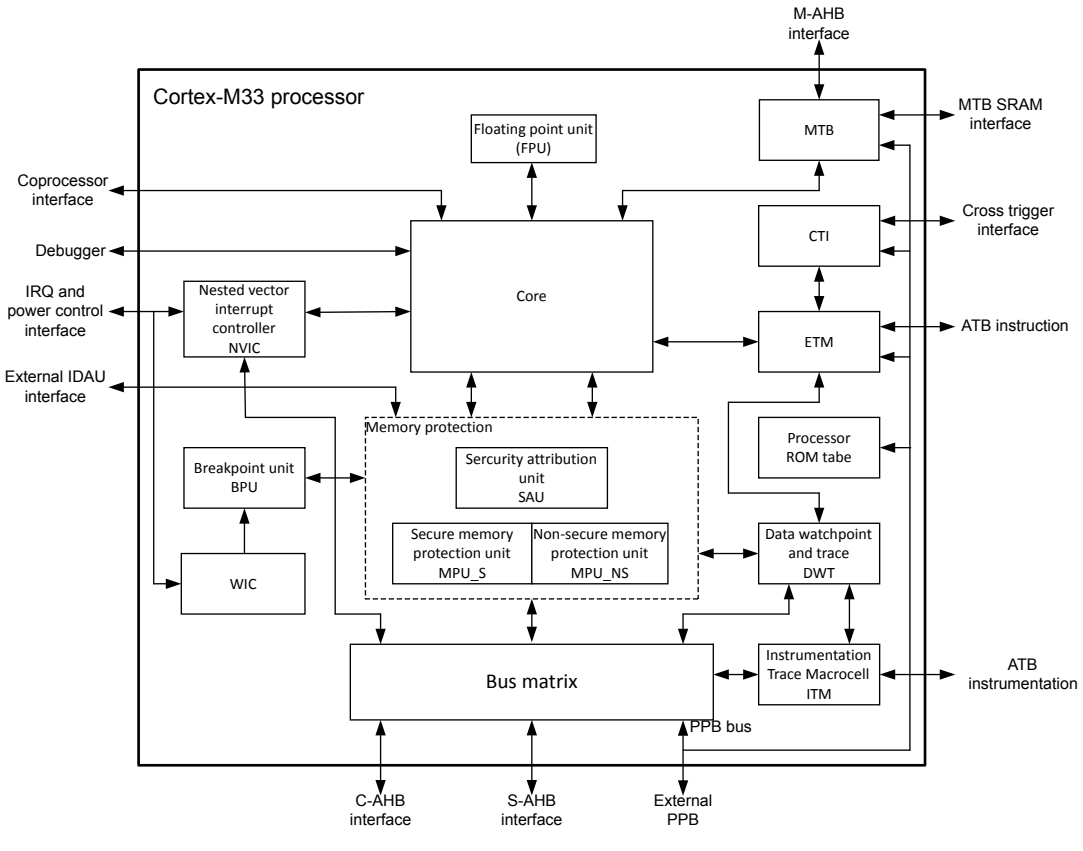
- STM32Cortex®-M33MCUs programming manual (PM0264)
- Cortex®-M33 processor technical reference manual, available on Arm® website
- STM32Cortex®-M0+MCUs programming manual (PM0223)
- Cortex®-M0+ processor technical reference manual, available on Arm® website

13.2 Cortex-M33 overview

The Cortex-M33 processor is excellent in ultralow power, performance, and security. This processor is based on the Armv8-M architecture for use in environments requiring more security implementation. The Cortex-M33 core implements a full set of DSP (digital signal processing) instructions, TrustZone aware support and a memory protection unit (MPU) that enhances application security.

The Cortex-M33 core also features a single-precision floating-point unit (FPU), that supports all the Arm single-precision data-processing instructions and all the data types. The STM32 Cortex-M33 implementation is illustrated in the figure below.

Figure 3. STM32 Cortex-M33 implementation



Cortex-M33key features are listed below:

- Arm-v8Marchitecture with 2/3 stage pipeline, Harvard, 1.5 DMIPS/MHz

- Single-cyclebranch, no branch prediction
- Hardware divide instruction
- Debug (CoreSight™ compliant)
- Memory exclusive instructions
- NVIC up to 68 interrupts (16 priority levels)
- Enhanced MPU, more flexible (32 bytes) up to eight regions (for each one of the secure and nonsecure states)
- NewAMBA®5AHB interface, support of security state extension to the system
- Support of external implementation defined attribution unit
- Fully compatible with TrustZone system

The differences between Cortex-M0+ and Cortex-M33 are presented in the table below.

Table 62. Cortex-M0+ versus Cortex-M33

Features	Cortex-M0+ (STM32WB0)	Cortex-M33 (STM32WBA2)
Instruction set architecture	Armv6-M	Armv8-M
	Thumb, Thumb-2	
TrustZone	No	Yes
Performance efficiency (CoreMark/MHz)	2.46	4.10
DMIPS/MHz	0.95	1.50
Pipeline	2-stage	3-stage
Memory protection (MPU)	8 areas	8 secure areas + 8 nonsecure areas
Floating-point units (FPU)	No	Yes
DSP instructions	No	Yes
CMSIS support	Yes	Yes

13.3 Cortex-M33 software point of view

The Cortex-M33 includes the following features:

- Implementing Armv8-M architecture
- Implementing the latest FPU specification (based on Arm FPv5 architecture)
- Using the AHB5 specification for the system and memory interface to extend security across the whole system
- Using the latest version of the MPU specification for the setup of regions
- Optional execution trace using MTB or ETM
- Enhanced debug components to simplify usage
- Hardware stack limit checking
- TrustZone security features adding efficient security features

14 Conclusion

This application note is a complement to the STM32WB0 and STM32WBA2 series datasheets and reference manuals. This document provides a simple guideline to migrate an existing product based on STM32WB0 to the STM32WBA2 devices.

Revision history

Table 63. **Document revision history**

Date	Version	Changes
26-Jun-2025	1	Initial release.

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