L99LDLH32 and LDLL16EN - FTP programming guide

Introduction

The L99LDLH32 and LDLL16EN can fully operate in Bus Driven mode, using a CAN FD light compatible interface, or in Standalone/Fail Safe mode, using the direct drive functionality and the configuration defined in the internal Few-Time Programmable (FTP) memory registers.

Both devices are equipped with 2 kbits EEPROM, used to store device configuration data.

Part of this memory is managed by the customer to define the device's way of operating in Fail Safe mode.

FTP can be programmed through any CAN FD light-compatible interface.

The programming can be enabled by setting the CS pin to “1” either via HW or via SW.

In HW mode, the CS level is related to the CS pin voltage; CS = 0 means CS pin at GND, CS = 1 means CS pin at 5 V. While in SW mode it is exactly the bit value.

For safety reasons, any FTP sector/row can be locked to avoid unintentional writing.

1 Memory organization

L99LDLH32 and LDLL16EN have RAM memory in which data for volatile registers are stored and a Non-Volatile Memory (also referred as Few-Time Programmable memory) in which some configuration data are saved. During the Initialization State, few configuration data stored in FTP are loaded inside some RAM registers; we refer to such registers as Shadow Registers.

We can divide the registers' organization, based on RAM and FTP, into three different types:

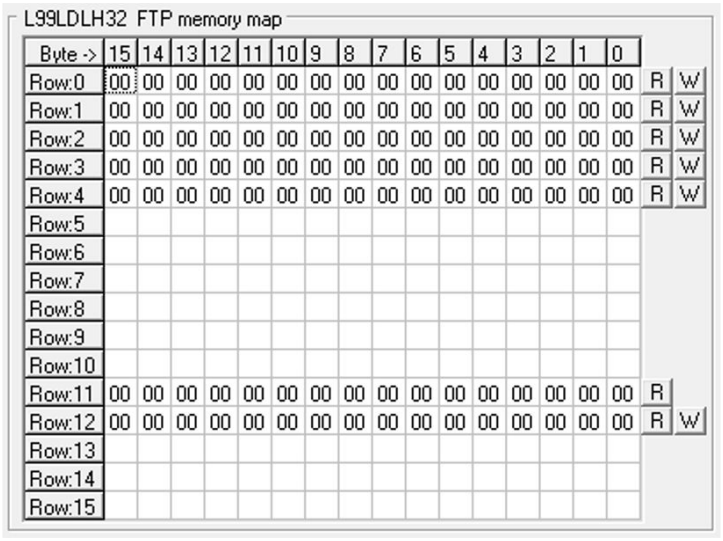
- Volatile registers are in RAM
- Shadow registers are in RAM but as a copy of FTP registers
- Non-volatile registers are in FTP

In this document, we focus only on the FTP section; for the complete memory mapping and the way the device uses it, refer to the datasheet.

The FTP memory is organized in 16 sections/rows of 16 bytes each.

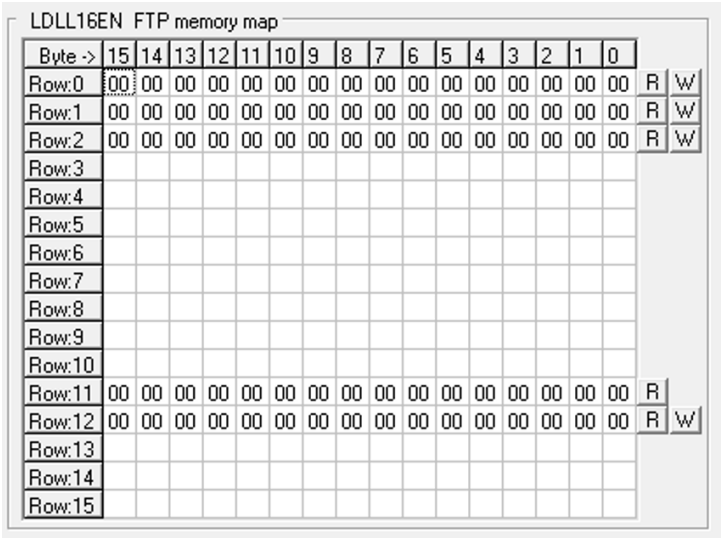
In the L99LDH32, the customer has access to 6 rows in Write/Read mode and to 1 row in Read only.

Figure 1. FTP mapping of L99LDH32



In the LDLL16EN, the customer has access to 4 rows in Write/Read mode and 1 row in Read only.

Figure 2. FTP mapping of LDLL16EN



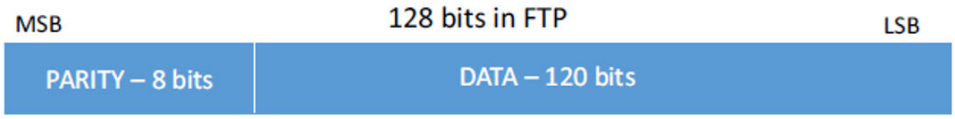
2 Memory mapping

Each row has 16 bytes and not all the 128bit of each section are used. The not used bits are free for customer usage.

Special care must be taken to Row 0 because it includes Lock_Row_x bit; once written to 1 the addressed Row is no longer accessible in Write mode. Double care to bit 16 which is the Lock_Row_0, meaning that it locks itself.

About the Responder ID, it must be considered that only the values multiple of 4 are valid, because the two less significant bits are internally masked to 0.

Figure 3. FTP Sector/Row generic structure



Here below the detailed mapping of each row for both devices, for the detailed explanation of each bit refer to the datasheet.

Table 1. Row 0 of LDLL16EN

Bit	Name	Default	Description
127-120	Parity	0	
119-29	Free	0	
28	Lock_Row_12	0	0: Row_12 unlocked (R/W access) - 1: Row_12 locked (R only access)
27-19	Free	0	
18	Lock_Row_2	0	0: Row_2 unlocked (R/W access) - 1: Row_2 locked (R only access)
17	Lock_Row_1	0	0: Row_1 unlocked (R/W access) - 1: Row_1 locked (R only access)
16	Lock_Row_0	0	0: Row_0 unlocked (R/W access) - 1: Row_0 locked (R only access)
15-10	Free	0	
9	Lock_Responder ID	0	0: Responder ID unlocked (R/W access) - 1: Responder ID locked (R only access)
8-0	Responder ID	0	Device identifier

Table 2. Row 1 of LDLL16EN

Bit	Name	Default	Description
127-120	Parity	0	
119-108	Free	0	
107-104	SHT-THR_GRP_1	0	Short-circuit detection threshold for Group 1 channels, adjustable in 556 mV steps
103-100	Free	0	
99-96	SHT-THR_GRP_0	0	Short-circuit detection threshold for Group 0 channels, adjustable in 556 mV steps
95	Free	0	
94	DIN_MAP_CH7	0	Mapping channel 7 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
93	Free	0	
92	DIN_MAP_CH6	0	Mapping channel 6 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
91	Free	0	
90	DIN_MAP_CH5	0	Mapping channel 5 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
89	Free	0	

Bit	Name	Default	Description
88	DIN_MAP_CH4	0	Mapping channel 4 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
87	Free	0	
86	DIN_MAP_CH3	0	Mapping channel 3 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
85	Free	0	
84	DIN_MAP_CH2	0	Mapping channel 2 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
83	Free	0	
82	DIN_MAP_CH1	0	Mapping channel 1 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
81	Free	0	
80	DIN_MAP_CH0	0	Mapping channel 0 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
79-72	FS_OUT[7..0]_EN	0	Output [7..0] permanent ON in Fail Safe state: 0 = Disabled; 1 = Enabled
71-64	Free	0	
63-0	CUR_SET_CH[7..0]	0	Linear individual analog dimming for channels [7..0] in 1/256 steps

Table 3. Row 2 of LDLL16EN

Bit	Name	Default	Description
127-120	Parity	0	
119-96	Free	0	
95	Free	0	
94	DIN_MAP_CH15	0	Mapping channel 15 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
93	Free	0	
92	DIN_MAP_CH14	0	Mapping channel 14 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
91	Free	0	
90	DIN_MAP_CH13	0	Mapping channel 13 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
89	Free	0	
88	DIN_MAP_CH12	0	Mapping channel 12 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
87	Free	0	
86	DIN_MAP_CH11	0	Mapping channel 11 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
85	Free	0	
84	DIN_MAP_CH10	0	Mapping channel 10 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
83	Free	0	
82	DIN_MAP_CH9	0	Mapping channel 9 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
81	Free	0	
80	DIN_MAP_CH8	0	Mapping channel 8 to direct input: 0 = NOT mapped, group 0; 1 = mapped, group 1
79-72	FS_OUT[15..8]_EN	0	Output [15..8] permanent ON in Fail Safe state: 0 = Disabled; 1 = Enabled
71-64	Free	0	
63-0	CUR_SET_CH[15..8]	0	Linear individual analog dimming for channels [15..8] in 1/256 steps

Table 4. Row 11 of LDLL16EN (Read only)

Bit	Name	Default	Description
127-120	Reserved	-	
119-0	TRACE_CODE	-	ENCRYPTED TRACEABILITY CODE - Read only

Table 5. Row 12 of LDLL16EN

Bit	Name	Default	Description
127-120	Parity	0	
119-117	DITHERING	0	Set the percentage of frequency modulation of 20 MHz oscillator
116-112	CAN SAMPLING	0	CAN bit sampling point
111-104	Free	0	
103-96	PG_TH_VPREG	0	Power Good threshold for VPREG, adjustable in 78.4 mV steps; clamped to 4 V
95-93	Free	0	
92	SYNC_IO_PC	0	0 = Provider mode – SYNC_IO pin is output; 1 = Consumer mode – SYNC_IO pin is input
91-90	POR_DELAY	0	Power-on reset delay time (t_{POR_DELAY}); delay time to activate outputs in FS after POR
89	Free	0	
88	SHT_DET_EN	0	Short-circuit detection: 0 = Disabled; 1 = Enabled
87-86	WD_CONF	0	Watchdog timeout period (t_{WD})
85-84	Free	0	
83	STB_CONF	0	STB pin configuration: 0 = Normal Low; 1 = Normal High
82-80	VNTC_TH	0	NTC voltage threshold related to the start of derating
79-72	Free	0	
71-69	PWM_FREQ	0	PWM frequency
68	OL_EN	0	Open-load fault propagation on FAULT pin for group 1: 0 = Disabled; 1 = Enabled
67-66	Free	0	
65	FAULT_REACT_GRP1	0	Group 1 reaction mode for one string fault: 0 = all strings OFF; 1 = no action
64	FAULT_REACT_GRP0	0	Group 0 reaction mode for one string fault: 0 = all strings OFF; 1 = no action
63-56	Free	0	
55	SHT_EN	0	Short-circuit fault propagation on FAULT pin for group 1: 0 = Disabled; 1 = Enabled
54	SHT_OFF_GRP1	0	Output deactivation in case of Shot detection for group 1: 0 = Disabled; 1 = Enabled
53	SHT_OFF_GRP0	0	Output deactivation in case of Shot detection for group 0: 0 = Disabled; 1 = Enabled
52-44	Free	0	
43-42	DIAG_BLANK_GRP1	0	Diagnostic blanking time after rising edge (incl. PWM) for group 1
41-40	DIAG_BLANK_GRP0	0	Diagnostic blanking time after rising edge (incl. PWM) for group 0
39-37	PHASE_DEV	0	PWM phase shift in Consumer mode with regards to SYNC_IO
36	OUT_DELAY	0	Gradual output delay: 0 = Disabled; 1 = Enabled
35-33	Free	0	
32	PWM_FS_ALL_EN	0	Internal PWM dimming in Fail Safe state for group 1: 0 = Disabled; 1 = Enabled
31-8	Free	0	
7-0	PWM_DUTY_ALL	0	Linear Global PWM dimming for outputs mapped to DIN, adjustable in 1/256 steps

Table 6. Row 0 of L99LDLH32

Bit	Name	Default	Description
127-120	Parity	0	
119-29	Free	0	
28	Lock_Row_12	0	0: Row_12 unlocked (R/W access) - 1: Row_12 locked (R only access)

Bit	Name	Default	Description
27-21	Free	0	
20	Lock_Row_4	0	0: Row_4 unlocked (R/W access) - 1: Row_4 locked (R only access)
19	Lock_Row_3	0	0: Row_3 unlocked (R/W access) - 1: Row_3 locked (R only access)
18	Lock_Row_2	0	0: Row_2 unlocked (R/W access) - 1: Row_2 locked (R only access)
17	Lock_Row_1	0	0: Row_1 unlocked (R/W access) - 1: Row_1 locked (R only access)
16	Lock_Row_0	0	0: Row_0 unlocked (R/W access) - 1: Row_0 locked (R only access)
15-10	Free	0	
9	Lock_Responder ID	0	0: Responder ID unlocked (R/W access) - 1: Responder ID locked (R only access)
8-0	Responder ID	0	Device identifier

Table 7. Row 1 of L99LDLH32

Bit	Name	Default	Description
127-120	Parity	0	
119-108	Free	0	
107-104	SHT-THR_GRP_1	0	Short-circuit detection threshold for Group 1 channels, adjustable in 314 mV steps
103-100	Free	0	
99-96	SHT-THR_GRP_0	0	Short-circuit detection threshold for Group 0 channels, adjustable in 314 mV steps
95-94	DIN_MAP_CH7	0	Mapping channel 7 to direct input: x0 = NOT mapped; x1 = mapped
93-92	DIN_MAP_CH6	0	Mapping channel 6 to direct input: x0 = NOT mapped; x1 = mapped
91-90	DIN_MAP_CH5	0	Mapping channel 5 to direct input: x0 = NOT mapped; x1 = mapped
89-88	DIN_MAP_CH4	0	Mapping channel 4 to direct input: x0 = NOT mapped; x1 = mapped
87-86	DIN_MAP_CH3	0	Mapping channel 3 to direct input: x0 = NOT mapped; x1 = mapped
85-84	DIN_MAP_CH2	0	Mapping channel 2 to direct input: x0 = NOT mapped; x1 = mapped
83-82	DIN_MAP_CH1	0	Mapping channel 1 to direct input: x0 = NOT mapped; x1 = mapped
81-80	DIN_MAP_CH0	0	Mapping channel 0 to direct input: x0 = NOT mapped; x1 = mapped
79-72	FS_OUT[7..0]_EN	0	Output [7..0] permanent ON in Fail Safe state: 0 = Disabled; 1 = Enabled
71-64	Free	0	
63-0	CUR_SET_CH[7..0]	0	Linear individual analog dimming for channels [7..0] in 1/256 steps

Table 8. Row 2 of L99LDLH32

Bit	Name	Default	Description
127-120	Parity	0	
119-96	Free	0	
95-94	DIN_MAP_CH15	0	Mapping channel 15 to direct input: x0 = NOT mapped; x1 = mapped
93-92	DIN_MAP_CH14	0	Mapping channel 14 to direct input: x0 = NOT mapped; x1 = mapped
91-90	DIN_MAP_CH13	0	Mapping channel 13 to direct input: x0 = NOT mapped; x1 = mapped
89-88	DIN_MAP_CH12	0	Mapping channel 12 to direct input: x0 = NOT mapped; x1 = mapped
87-86	DIN_MAP_CH11	0	Mapping channel 11 to direct input: x0 = NOT mapped; x1 = mapped
85-84	DIN_MAP_CH10	0	Mapping channel 10 to direct input: x0 = NOT mapped; x1 = mapped
83-82	DIN_MAP_CH9	0	Mapping channel 9 to direct input: x0 = NOT mapped; x1 = mapped
81-80	DIN_MAP_CH8	0	Mapping channel 8 to direct input: x0 = NOT mapped; x1 = mapped

Bit	Name	Default	Description
79-72	FS_OUT[15..8]_EN	0	Output [15..8] permanent ON in Fail Safe state: 0 = Disabled; 1 = Enabled
71-64	Free	0	
63-0	CUR_SET_CH[15..8]	0	Linear individual analog dimming for channels [15..8] in 1/256 steps

Table 9. Row 3 of L99LDLH32

Bit	Name	Default	Description
127-120	Parity	0	
119-96	Free	0	
95-94	DIN_MAP_CH23	0	Mapping channel 23 to direct input: x0 = NOT mapped; x1 = mapped
93-92	DIN_MAP_CH22	0	Mapping channel 22 to direct input: x0 = NOT mapped; x1 = mapped
91-90	DIN_MAP_CH21	0	Mapping channel 21 to direct input: x0 = NOT mapped; x1 = mapped
89-88	DIN_MAP_CH20	0	Mapping channel 20 to direct input: x0 = NOT mapped; x1 = mapped
87-86	DIN_MAP_CH19	0	Mapping channel 19 to direct input: x0 = NOT mapped; x1 = mapped
85-84	DIN_MAP_CH18	0	Mapping channel 18 to direct input: x0 = NOT mapped; x1 = mapped
83-82	DIN_MAP_CH17	0	Mapping channel 17 to direct input: x0 = NOT mapped; x1 = mapped
81-80	DIN_MAP_CH16	0	Mapping channel 16 to direct input: x0 = NOT mapped; x1 = mapped
79-72	FS_OUT[23..16]_EN	0	Output [23..16] permanent ON in Fail Safe state: 0 = Disabled; 1 = Enabled
71-64	Free	0	
63-0	CUR_SET_CH[23..16]	0	Linear individual analog dimming for channels [23..16] in 1/256 steps

Table 10. Row 4 of L99LDLH32

Bit	Name	Default	Description
127-120	Parity	0	
119-96	Free	0	
95-94	DIN_MAP_CH31	0	Mapping channel 31 to direct input: x0 = NOT mapped; x1 = mapped
93-92	DIN_MAP_CH30	0	Mapping channel 30 to direct input: x0 = NOT mapped; x1 = mapped
91-90	DIN_MAP_CH29	0	Mapping channel 29 to direct input: x0 = NOT mapped; x1 = mapped
89-88	DIN_MAP_CH28	0	Mapping channel 28 to direct input: x0 = NOT mapped; x1 = mapped
87-86	DIN_MAP_CH27	0	Mapping channel 27 to direct input: x0 = NOT mapped; x1 = mapped
85-84	DIN_MAP_CH26	0	Mapping channel 26 to direct input: x0 = NOT mapped; x1 = mapped
83-82	DIN_MAP_CH25	0	Mapping channel 25 to direct input: x0 = NOT mapped; x1 = mapped
81-80	DIN_MAP_CH24	0	Mapping channel 24 to direct input: x0 = NOT mapped; x1 = mapped
79-72	FS_OUT[31..24]_EN	0	Output [31..24] permanent ON in Fail Safe state: 0 = Disabled; 1 = Enabled
71-64	Free	0	
63-0	CUR_SET_CH[31..24]	0	Linear individual analog dimming for channels [31..24] in 1/256 steps

Table 11. Row 11 of L99LDLH32 (Read only)

Bit	Name	Default	Description
127-120	Reserved	-	
119-0	TRACE_CODE	-	ENCRYPTED TRACEABILITY CODE - Read only

Table 12. Row 12 of L99LDLH32

Bit	Name	Default	Description
127-120	Parity	0	
119-117	DITHERING	0	Set the percentage of frequency modulation of 20 MHz oscillator
116-112	CAN SAMPLING	0	CAN bit sampling point
111-104	Free	0	
103-96	PG_TH_VPRE_REG	0	Power Good threshold for VPRE_REG, adjustable in 157 mV steps
95-93	Free	0	
92	SYNC_I/O_P/C	0	0 = Provider mode – SYNC_IO pin is output; 1 = Consumer mode – SYNC_IO pin is input
91-90	POR_DELAY	0	Power-on reset delay time (t_{POR_DELAY}); delay time to activate outputs in FS after POR
89	Free	0	
88	SHT_DET_EN	0	Short-circuit detection for channels mapped to VPRE_REG: 0 = Disabled; 1 = Enabled
87-86	WD_CONF	0	Watchdog timeout period (t_{WD})
85	VREF_PRE_REG	0	VREF_PRE_REG disable: 0 = Enabled; 1 = Disabled
84-83	Free	0	
82-80	VNTC_TH	0	NTC voltage threshold related to the start of derating
79-72	Free	0	
71-69	PWM_FREQ	0	PWM frequency
68	OL_EN	0	Open-load fault propagation on FAULT pin for group 1: 0 = Disabled; 1 = Enabled
67-66	Free	0	
65	FAULT_REACT_GRP01	0	Group 01 reaction mode for one string fault: 0 = all strings OFF; 1 = no action
64	FAULT_REACT_GRP00	0	Group 00 reaction mode for one string fault: 0 = all strings OFF; 1 = no action
63-56	Free	0	
55	SHT_EN	0	Short-circuit fault propagation on FAULT pin for group 1: 0 = Disabled; 1 = Enabled
54	SHT_OFF_GRP01	0	Output deactivation in case of Shot detection for group 01: 0 = Disabled; 1 = Enabled
53	SHT_OFF_GRP00	0	Output deactivation in case of Shot detection for group 00: 0 = Disabled; 1 = Enabled
52-44	Free	0	
43-42	DIAG_BLANK_GRP01	0	Diagnostic blanking time after rising edge (incl. PWM) for group 01
41-40	DIAG_BLANK_GRP00	0	Diagnostic blanking time after rising edge (incl. PWM) for group 00
39-37	PHASE_DEV	0	Phase shift in Consumer mode with regards to STNC_IO
36	OUT_DELAY	0	Gradual output delay: 0 = Disabled; 1 = Enabled
35-33	Free	0	
32	PWM_FS_ALL_EN	0	Internal PWM dimming in Fail Safe mode for group 01: 0 = Disabled; 1 = Enabled
31-16	Free	0	
15-8	PWM_DUTY_ALL_ALT	0	Alternative Exponential global PWM dimming for outputs mapped to DIN
7-0	PWM_DUTY_ALL	0	Exponential global PWM dimming for outputs mapped to DIN in Fail Safe mode Default values of Linear Global PWM dimming for outputs mapped to DIN in Normal mode

For both devices the content of NVM is fully reset when leaving ST, so the Default value for each bit is 0.

3 Entering and leaving the FTP programming mode

The first step to program FTP is setting the CS to “1”.

This can be done in HW, acting on the physical CS pin or in SW setting the CS bit (b2 of Address 18h).

When there are few devices on the same CAN bus, the FTP access using the CS bit is possible if each device already has a unique Responder ID set. If not, it is necessary to act on the physical CS pin to select the device to be programmed. The latter is true for the first FTP programming of multi-fresh devices sharing the same CAN FD light bus.

The access to FTP programming through setting the CS bit can be used once all devices on the CAN bus are already programmed with unique Responder IDs. Or in case there is a single device on the CAN FD light bus.

This is because the commands to be used are Unicast write and when there are more responders with the same ID the command is received by all which try to answer, creating a possible bus conflict.

For programming the FTP (either using the physical CS pin or CS bit) the device must be in one of the Active modes, meaning Normal/Bus mode or Fail Safe/Standalone mode.

Once CS is set to “1”, in the HW or SW way, to get complete access to the Customer FTP area, the key word for Test Mode Customer “0000DCBA” must be written to Address 1Eh.

Access to Address 1Eh is enabled only if CS is set, and this is the way to select one device among many with the same Responder ID.

The simplest way to know if the device has entered Test Mode Customer, is to check if b0 of Address 1Eh is set. This can be done if the addressed device has already a unique ID, otherwise more than one device answers the Unicast command, creating a conflict. If more than one device on the bus has the same ID, it is suggested to try an FTP Row Read, the command is executed only if the device has accepted the key word, and it is entered in Test Mode Customer.

To leave Test Mode Customer for blocking the FTP access, it is enough to set CS to “0”.

After modifying the FTP and exiting the FTP programming mode, the device continues to operate according to the previous FTP content in the shadow registers. The new FTP content is loaded into the shadow registers after the device transitions to the initialization state – see Figure 6 Device state diagram.

Figure 4. FTP programming flow by setting SW bit CS

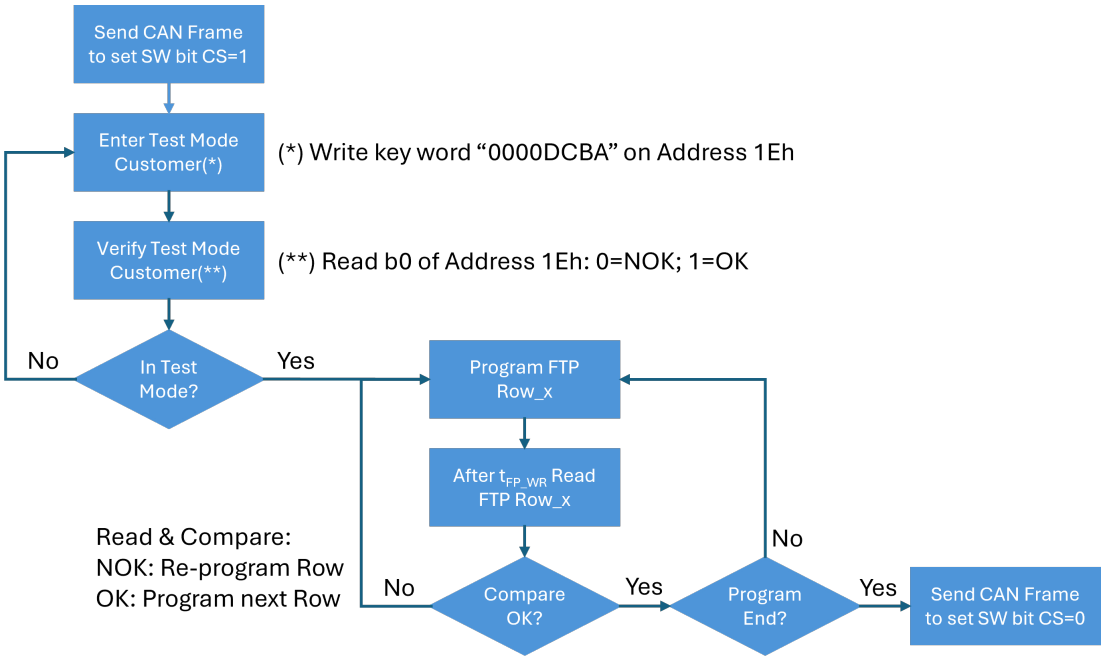
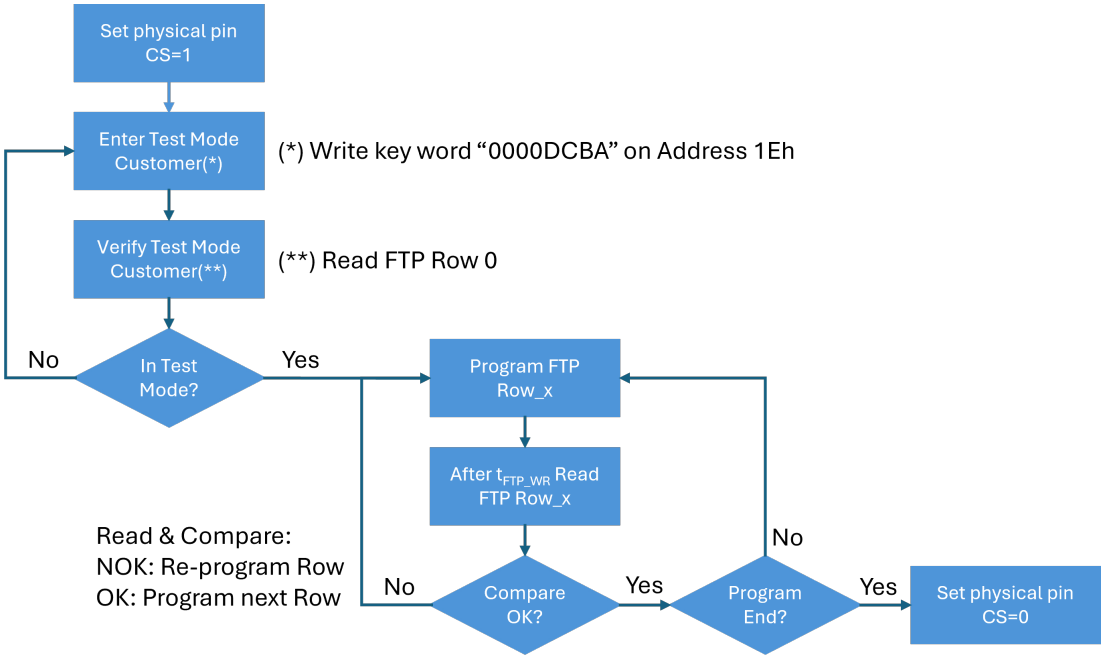


Figure 5. FTP programming flow by setting physical pin CS



It is always good practice to send a WakeUp Pattern, before starting the programming sequence, to be sure that all the devices exit from StandBy to enter in an Active state and to ensure the correct synchronization of all responders to commander.

4 CAN FD light FTP commands

4.1 Unicast commands

To get access to the FTP space it is necessary to use basic Unicast commands. They are described in the datasheet, but for convenience we report hereafter those useful to build a complete sequence CTR, composed of 6 bits that are fixed to the configuration “001000”, meaning that the FD frame (FDF bit) is always recessive, while all the others are dominant.

Table 13. WakeUp pattern (WUP) frame

ID	CTRL	DLC	B0	B1	B2	B3	B4	B5	B6	B7
43C	"001000"	8	FE	0F	0F	0F	0F	0F	0F	0F

Unicast single RAM write command is used to send the key word to the address 1Eh. In this case, only the device with CS set answers. Also, this type of command is used to toggle the Watch Dog bit.

Table 14. Commander request for single RAM write and responder answer frame

	ID field bit												Data field = 5 bytes						
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Add	Payload					
Commander request =	0	0	Responder ID									CTRL	00 + Address	Data 3	Data 2	Data 1	Data 0	CRC	ACK/EOF
Responder answer =	0	1	Responder ID									CTRL	GSB	CRC	ACK/EOF				

4.2 FTP write command

This is a Unicast command used to write data in a specific FTP Row address.

The commander request frame contains 16 data bytes. The first byte contains, in the High Nibble, the OP code (Bh = FTP write) and, in the Low Nibble, the FTP Row address; followed by 15 bytes of the FTP data.

The FTP write operation is performed within t_{FTP_WR} time, which is typically 12 ms. During this time, no commands must be sent on the CAN bus.

The FTP write command is effective only if the device is in FTP programming mode.

The device is not providing any answer to this command.

Table 15. FTP write frame structure

	ID field bit												Data field = 16 bytes					
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Add	Payload				
Commander request =	0	0	Responder ID									CTRL	1011 + Row	Data byte 14	...	Data byte 0	CRC	ACK/EOF

4.3 FTP read command

This Unicast command allows you to read the content of the specified FTP Row address.

The commander request frame contains 16 data bytes. The first byte contains, in the High Nibble, the OP code (Ah - FTP read) and, in the Low Nibble, the FTP Row address; the other 15 bytes are “Don’t care”.

The responder answers with 16 data byte frames containing the data of the addressed FTP Row.

This command is effective only if the device is in FTP programming mode, otherwise no answer is sent.

Table 16. FTP read frame and answer frame structure

	ID field bit												Data field = 16 bytes						
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Add	Payload					
Commander request =	0	0	Responder ID									CTRL	1010 + Row	Don't care 14	...	Don't care 0		CRC	ACK/EOF
Responder answer =	0	1	Responder ID									CTRL	Don't care	Data byte 14	...	Data byte 0		CRC	ACK/EOF

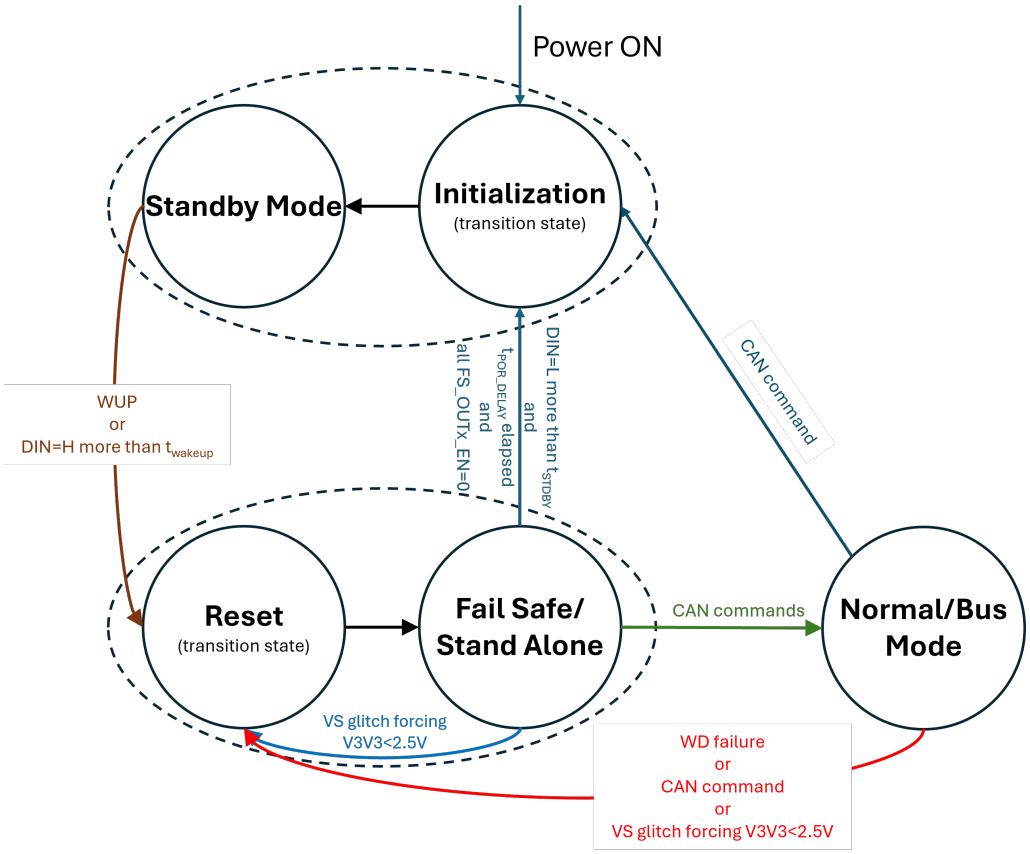
5 Operating modes

As seen in Section 3, the device must be in Active mode to enter FTP programming.

Active modes are: Fail Safe/Standalone mode state and Normal/Bus mode state.

Using the following state diagram (simplified in respect to the complete one in the datasheet), we see how to keep the device in Fail Safe state or in Normal state.

Figure 6. Device state diagram



After Power-ON the device enters in Initialization state, where the shadow registers and device configuration are loaded with FTP data. After $t_{STARTUP}$ (500 µs maximum), the device enters Standby; in this state, the RAM is cleared but the shadow registers are preserved.

The device exits from Standby if a WUP is received or after wakeup (about 30 µs) if the DIN pin is set High.

From Standby the device enters Fail Safe/Standalone state transiting from Reset in about 400 ns.

Neglecting the case of power supply problems, the device can exit from Fail Safe mode because of a CAN command to enter in Normal mode, or because DIN is Low for more than t_{STDBY} (about 15 ms) and t_{POR_DELAY} (configurable in FTP: 0 ms, 25 ms, 50 ms, 100 ms) is elapsed and all the FS_OUTx_EN bits are set to 0 (defined in FTP).

If we consider a device with the FTP at Default values, it exits from Fail Safe mode after 15 ms unless the DIN pin is set High.

For that described above, the easiest way to bring and keep a device in Fail Safe mode is to force the DIN pin to High level.

The device can reach Normal mode only from Fail Safe state by CAN commands. It can leave this state by a CAN command or because the Watch Dog refresh fails (always neglecting the power supply problems). This means that the only way to keep the device in Normal mode is to properly manage the WD refresh.

In the case of multi devices with the same Responder ID, it is not possible to keep them in Normal mode because of WD handling, so the simplest, and unique, way to program FTP is doing it in Fail Safe mode.

6 FTP programming for multi new devices in Fail Safe state

As mentioned, the default FTP condition of the new devices is a Clear state, meaning all the bits are set to 0.

This means that, the Responder ID is set to 0, the t_{POR_DELAY} is set to 0 ms, and all the FS_OUTx_EN bits are set, as well, to 0.

Looking at the state diagram, and considering the above-mentioned initial values, there are two ways to bring the device in Fail Safe state, one temporary and one stable.

6.1 Fail Safe state with DIN = Low

Once the power supply is applied, the device enters in Initialization and after about 500 µs moves to Standby.

Sending a Wake-Up Pattern the device goes to Fail Safe passing through Reset. Since the DIN pin is Low the device remains in Fail Safe for only 15 ms before moving back to Standby via Initialization.

While the device is in Fail Safe it is possible to program one Row of FTP, only one Row because of the timing.

As soon as the device enters in Fail Safe, it is possible to rise High the physical CS pin, send the key word to Address 1Eh, try an FTP Row read to verify if the device accepted the FTP enable request, send the FTP write command, wait for the FTP memory writing time (t_{FTP_WR} = 12 ms) and read back the just programmed Row to verify the result.

All these actions basically consume all the 15 ms given by $t_{STANDBY}$, so at the end of the Row write the device falls back to Standby. But it is important to consider that it passes through the Initialization state. In such a transition, all the new FTP values are loaded into shadow registers and applied to the device.

For this reason, it is suggested to leave at the end the programming of Row 0, which includes Responder ID and Lock_Row bits.

If programming Row 12, the t_{POR_DELAY} is changed to a value different than 0 ms, the device, during the following loop, stays in Fail Safe state for a longer period than 15 ms following the t_{POR_DELAY} setting.

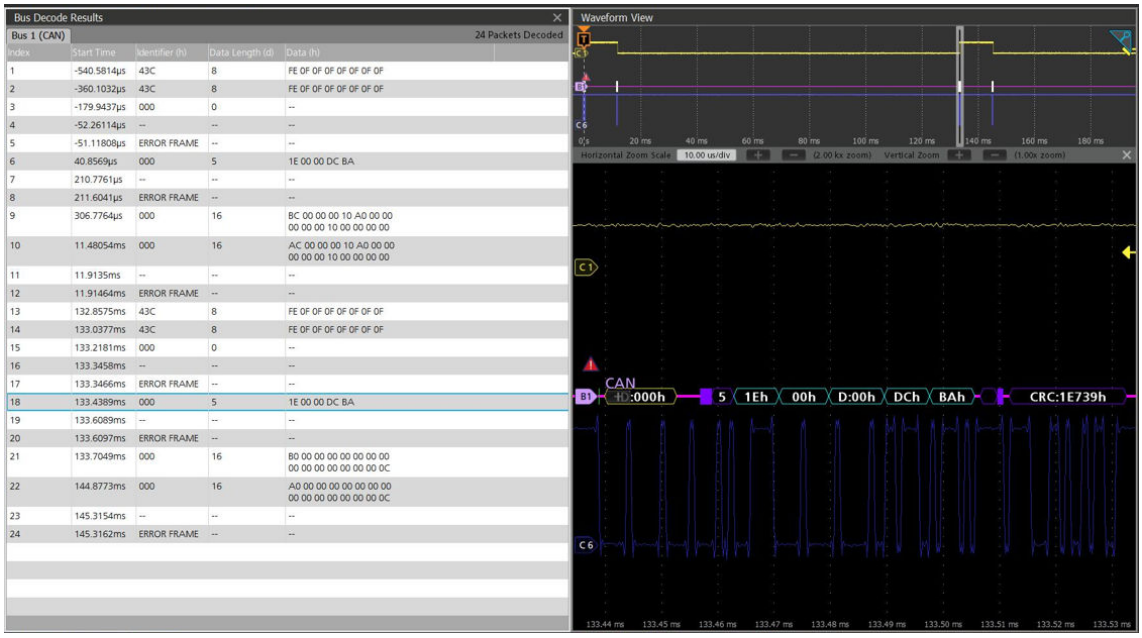
While, if during the programming some FS_OUTx_EN bits are set to 1, in the following loop the device enters in Fail Safe state in a stable way.

Meaning that all the modifications applied to the FTP bits are not uploaded to the shadow registers and applied to the device up to a Power-OFF/ON cycle or through a CAN command cycle.

The FTP programming strategy, for DIN = Low, must be decided considering the just described cases.

Here below an example, in which the strategy used is to execute a writing cycle every 100 ms (the longest period of t_{POR_DELAY}). Each cycle is executed always in the same way independently of whether the device was in Standby or in Fail Safe state, also because it is good practice to start any cycle using WUP as synchronization pattern.

Figure 7. Plot of FTP programming Row by Row with 100 ms cycle



The yellow plot is the physical CS pin controlled by the microcontroller; it is lifted just before the key word sending.

The same procedure, sniffed by a dongle, is reported in the next Table, because due to the long acquisition period the oscilloscope is failing in decoding some frames.

Table 17. CAN FD sniffing of FTP programming Row by Row with 100 ms cycle

Time stamp (ms)	ID	Data length	Data (h)	CAN command
0.0	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
0.1	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
0.3	0	0		Frame no data
0.3	200	1	05	GSB answer > b0 at 1 = Fail Safe
0.5	0	5	1E 00 00 DC BA	Key word to 1Eh
0.6	200	1	05	GSB answer > b0 at 1 = Fail Safe
0.9	0	16	BC 00 00 00 10 A0 00 00 00 00 00 10 00 00 00 00	FTP write Row 12 => "BC"
12.1	0	16	AC 00 00 00 10 A0 00 00 00 00 00 10 00 00 00 00	FTP read Row 12 => "AC"
12.3	200	16	00 00 00 00 10 A0 00 00 00 00 00 10 00 00 00 00	Row 12 content
133.4	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
133.5	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
133.7	0	0		Frame no data
133.7	200	1	05	GSB answer > b0 at 1 = Fail Safe
133.9	0	5	1E 00 00 DC BA	Key word to 1Eh
134.0	200	1	05	GSB answer > b0 at 1 = Fail Safe
134.3	0	16	B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 0C	FTP write Row 0 => "B0"
145.5	0	16	A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 0C	FTP read Row 0 => "A0"
145.7	200	16	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 0C	Row 0 content

Of course, this is a portion, the last two rows only, of the complete FTP programming of one device.

The complete order was from Row 1 to Row 12 and only at the end Row 0.

This portion shows the programming of Row 12 (time stamp 0.9 ms: Op Code “B” and Row “C”) followed by Row 0 (time stamp 133.9 ms: Op Code “B” and Row “0”) in which the ID value defined is 12 (00Ch) and no Lock_Row has been set.

Once the first device has been completed, the microcontroller moves to control the physical CS pin of the second device and apply the same CAN command sequence for programming the FTP with a different content, at least for the Responder ID.

The double WUP is used, for the L99LDLH32 mainly, to ensure proper synchronization to the commander’s clock after the startup. While the “no data frame” (or get GSB command) is used as a dummy command in case the first Unicast command after WUP is not well decoded.

6.2 Fail Safe state with DIN = High

Once the power supply is applied, the device enters in Initialization and after about 500 µs moves to Standby.

Because DIN = High, after t_{WAKEUP} (typically it is 30 µs) the device moves directly to Fail Safe, transiting in Reset, and stays there up to when a CAN command changes the state.

In this case, the FTP programming can be much faster than the previous one.

Because the device remains in Fail Safe, it is possible to execute each FTP write command in sequence without any waiting time.

The CAN command sequence used for FTP Row write is the same as the one for DIN = Low, simply they are not delayed by more than 100 ms.

In the following trace example, the order of the addressed Rows and the basic sequence is kept the same (Row 1, Row 2, Row 3, Row 4, Row 12, and Row 0, for L99LDLH32; Row 1, Row 2, Row 12, and Row 0 for LDLL16EN) as the previous one, just for easier code implementation. Anyway, when the device is kept in Fail Safe state the new FTP values are not immediately used and so it is also possible to write Row 0 as the first one without having any problem with Responder ID change for the following Row writing and Lock_Row.

The new FTP values are uploaded and used by the device the next time it passes from Initialization state.

Table 18. CAN FD sniffing of FTP programming Row by Row with fast cycle

Time stamp (ms)	ID	Data length	Data (h)	CAN command
0	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
0.2	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
0.3	0	0		Frame no data
0.4	200	1	05	GSB answer > b0 at 1 = Fail Safe
0.6	0	5	1E 00 00 DC BA	Key word to 1Eh
0.6	200	1	05	GSB answer > b0 at 1 = Fail Safe
0.9	0	16	B1 00 00 00 00 00 00 00 00 00 00 00 00 12 12	FTP write Row 1 => "B1"
11.5	0	16	A1 00 00 00 00 00 00 00 00 00 00 00 00 12 12	FTP read Row 1 => "A1"
11.7	200	16	00 00 00 00 00 00 00 00 00 00 00 00 00 12 12	Row 1 content
17.7	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
17.9	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
18.0	0	0		Frame no data
18.0	200	1	05	GSB answer > b0 at 1 = Fail Safe
18.2	0	5	1E 00 00 DC BA	Key word to 1Eh
18.3	200	1	05	GSB answer > b0 at 1 = Fail Safe
18.6	0	16	B2 00 00 00 00 00 00 00 00 00 00 12 00 00 00 00	FTP write Row 2 => "B2"
29.7	0	16	A2 00 00 00 00 00 00 00 00 00 00 12 00 00 00 00	FTP read Row 2 => "A2"
29.9	200	16	00 00 00 00 00 00 00 00 00 00 00 12 00 00 00 00	Row 2 content
36.5	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP

Time stamp (ms)	ID	Data length	Data (h)	CAN command
36.6	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
36.7	0	0		Frame no data
36.8	200	1	05	GSB answer > b0 at 1 = Fail Safe
37.0	0	5	1E 00 00 DC BA	Key word to 1Eh
37.1	200	1	05	GSB answer > b0 at 1 = Fail Safe
37.4	0	16	B3 00 00 00 00 00 00 00 00 00 00 00 00 12 00 00	FTP write Row 3 => "B3"
47.9	0	16	A3 00 00 00 00 00 00 00 00 00 00 00 00 12 00 00	FTP read Row 3 => "A3"
48.1	200	16	00 00 00 00 00 00 00 00 00 00 00 00 00 12 00 00	Row 3 content
54.3	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
54.5	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
54.6	0	0		Frame no data
54.7	200	1	05	GSB answer > b0 at 1 = Fail Safe
54.9	0	5	1E 00 00 DC BA	Key word to 1Eh
54.9	200	1	05	GSB answer > b0 at 1 = Fail Safe
55.2	0	16	B4 00 00 00 00 00 00 00 12 00 00 00 00 00 00 00	FTP write Row 4 => "B4"
66.1	0	16	A4 00 00 00 00 00 00 00 12 00 00 00 00 00 00 00	FTP read Row 4 => "A4"
66.3	200	16	00 00 00 00 00 00 00 00 12 00 00 00 00 00 00 00	Row 4 content
72.5	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
72.7	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
72.8	0	0		Frame no data
72.9	200	1	05	GSB answer > b0 at 1 = Fail Safe
73.1	0	5	1E 00 00 DC BA	Key word to 1Eh
73.2	200	1	05	GSB answer > b0 at 1 = Fail Safe
73.5	0	16	BC 00 00 00 10 A0 00 00 00 00 00 10 00 00 00 00	FTP write Row 12 => "BC"
84.3	0	16	AC 00 00 00 10 A0 00 00 00 00 00 10 00 00 00 00	FTP read Row 12 => "AC"
84.5	200	16	00 00 00 00 10 A0 00 00 00 00 00 10 00 00 00 00	Row 12 content
90.5	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
90.6	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
90.7	0	0		Frame no data
90.8	200	1	05	GSB answer > b0 at 1 = Fail Safe
91.0	0	5	1E 00 00 DC BA	Key word to 1Eh
91.1	200	1	05	GSB answer > b0 at 1 = Fail Safe
91.4	0	16	B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 0C	FTP write Row 0 => "B0"
102.5	0	16	A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 0C	FTP read Row 0 => "A0"
102.7	200	16	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 0C	Row 0 content

The above reported sequence is repeated for each device present on the same CAN bus, addressing it by selecting the appropriate CS pin and applying its unique Responder ID, on top of the appropriate FTP values.

Being sure that the device remains in Fail Safe state, because of DIN = High, it is possible to further speed up the FTP programming, following the Figure 5 flow chart and using the first Row read as feedback of Test Mode Customer entered.

Here below the example of CAN command sequence for LDLL16EN, time stamp is just an indication.

Table 19. Example of possible CAN command sequence for LDLL16EN to speed up FTP programming

Time stamp (ms)	ID	Data length	Data (h)	CAN command (LDLL16EN)
	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
	0	5	1E 00 00 DC BA	Key word to 1Eh
	200	1	05	GSB answer > b0 at 1 = Fail Safe
	0	16	B1 00 00 00 00 00 00 00 00 00 00 00 00 00 12 12	FTP write Row 1 => "B1"
+12	0	16	A1 00 00 00 00 00 00 00 00 00 00 00 00 00 12 12	FTP read Row 1 => "A1"
	200	16	00 00 00 00 00 00 00 00 00 00 00 00 00 00 12 12	Row 1 content
	0	16	B2 00 00 00 00 00 00 00 00 00 00 12 00 00 00 00	FTP write Row 2 => "B2"
+12	0	16	A2 00 00 00 00 00 00 00 00 00 00 12 00 00 00 00	FTP read Row 2 => "A2"
	200	16	00 00 00 00 00 00 00 00 00 00 00 12 00 00 00 00	Row 2 content
	0	16	BC 00 00 00 10 A0 00 00 00 00 00 10 00 00 00 00	FTP write Row 12 => "BC"
+12	0	16	AC 00 00 00 10 A0 00 00 00 00 00 10 00 00 00 00	FTP read Row 12 => "AC"
	200	16	00 00 00 00 10 A0 00 00 00 00 00 10 00 00 00 00	Row 12 content
	0	16	B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 0C	FTP write Row 0 => "B0"
+12	0	16	A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 0C	FTP read Row 0 => "A0"
	200	16	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 0C	Row 0 content

7 FTP programming for devices with already unique Responder ID

7.1 FTP programming in Fail Safe using CS bit

If each device has a unique Responder ID, it is possible to access each one of them without any conflict with the other devices on the same CAN bus.

So, it is possible to apply everything described above simply by writing the CS bit (b2 of Address 18h) instead of lifting the physical CS pin. This means an extra CAN command before sending the key word; for the rest everything described in chapters 6.1 and 6.2 is applicable.

Table 20. Example of CS bit setting for unique Responder ID 00Ch

#	ID	Data length	Data (h)	CAN command
1	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
2	C	5	18 00 00 00 04	CS bit set in Fail Safe state
3	20C	1	05	GSB answer > b0 at 1 = Fail Safe
4	C	5	1E 00 00 DC BA	Key word to 1Eh
5	20C	1	05	GSB answer > b0 at 1 = Fail Safe
6	C	16	B2 00 00 00 00 00 00 00 00 00 00 00 00 00 12 12	FTP write Row 2 => "B2"
7	C	16	A2 00 00 00 00 00 00 00 00 00 00 00 00 00 12 12	FTP read Row 2 => "A2"
8	20C	16	00 00 00 00 00 00 00 00 00 00 00 00 00 00 12 12	Row 1 content
…	…	…	…	…

7.2 FTP programming in Normal mode using CS bit

Looking at Figure 6. Device state diagram, the only way to bring the device in Normal mode is to send the appropriate setting (BUSMODE b0 = 1 and GOSTBY b1 = 0) to address 18h using a unicast single RAM write command.

To keep the device in Normal mode, the WD_TRIG bit (b0 of Address 19h) must be cyclically toggled within a period configured by WD_CONF bits (b86 and b87 of Row 12) to refresh the watchdog.

The watchdog timeout period is set by default (both bits set to 0) to 50 ms, leaving enough time to write at least one FTP Row.

It depends on the way that the controller code is written, but normally we can consider the watchdog refresh routine running in the background in respect to the main code. This means that it could be asynchronous versus the main commands and if the time elapses in the middle of an FTP Row writing it could create a programming issue. For this reason, the best practice is to toggle the WD_TRIG bit, resetting the timeout period, before initiating the FTP Row write. This ensures that no interruption happens during the 12 ms necessary to complete the FTP Row programming.

In the following example the “no data frame” is used to get confirmation of the mode change.

The answer to the command is about the device condition at the time that the command arrives and before the execution of command content.

In case the device is already in Normal mode, it is possible to start from command # 6.

Table 21. Example of Row 12 programming for Responder ID 00Ch in Normal mode

#	ID	Data length	Data (h)	CAN command
1	43C	8	FE 0F 0F 0F 0F 0F 0F 0F	WUP
2	C	5	18 00 00 00 01	Enter in Normal mode
3	20C	1	05	GSB answer > b0 at 1 = Fail Safe
4	C	0		Frame no data
5	20C	1	80	GSB answer > Normal mode
6	C	5	19 00 00 00 01	Toggling WD_TRIG bit
7	20C	1	80	GSB answer > Normal mode
8	C	5	18 00 00 00 05	CS bit set in Normal mode
9	20C	1	80	GSB answer > Normal mode
10	C	5	1E 00 00 DC BA	Key word to 1Eh
11	20C	1	80	GSB answer > Normal mode
12	C	16	BC 00 00 00 10 A0 00 00 00 00 00 10 00 00 00 00	FTP write Row 12 => "BC"
13	C	16	AC 00 00 00 10 A0 00 00 00 00 00 10 00 00 00 00	FTP read Row 12 => "AC"
14	20C	16	00 00 00 00 10 A0 00 00 00 00 00 10 00 00 00 00	Row 12 content
15	C	5	18 00 00 00 01	CS bit reset
16	20C	1	80	Normal mode
…	…	…	…	…

7.3 FTP programming in Normal mode using physical CS pin

It is possible to enter Test Mode Customer to access FTP programming using the physical CS pin also when the device is in Normal mode, but it could be a little more complex than using a CS bit.

In practice, instead of sending the CS bit setting command, step # 8 of Table 21, it is required to lift the physical CS pin.

The following command sequence, and the special attention to the watchdog refresh, remains unchanged.

Revision history

Table 22. **Document revision history**

Date	Version	Changes
25-Aug-2025	1	Initial release.

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