Migrating from STM32WBA5 to STM32WBA2 MCUs

Introduction

The designers of STM32 microcontroller applications must have the possibility to easily replace one microcontroller type with another one from the same product family or products from a different family. The reasons for migrating an application to a different microcontroller can be, for example:

- To fulfill higher product requirements, extra demands on memory size, or an increased number of I/Os
- To meet cost reduction constraints that require switching to smaller components and shrink the PCB area

This application note details the steps required to migrate from a design based on an STM32WBA5 device to an application based on one of the STM32WBA2 MCUs.

This document provides guidelines for hardware and peripheral migration. To better understand the information inside this application note, the user must be familiar with the STM32 microcontroller family.

For additional information, refer to the product datasheets and reference manuals available on www.st.com

Table 1. Applicable products

Type	Products
Microcontroller	STM32WBA20, STM32WBA23, STM32WBA25 product lines STM32WBA50, STM32WBA52, STM32WBA54/55 product lines

1 General information

This document applies to the STM32WBA2 and STM32WBA5 Arm® Cortex®-M33-based microcontrollers.

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Reference documents

Table 2. List of documents

Reference	Name/address	Title
[1]	PM0264	STM32 Cortex®-M33 MCUs programming manual
[2]	AN2606	Introduction to system memory boot mode on STM32 MCUs

1. *This URL is active at document publication. However, STMicroelectronics shall not be liable for any change, move, or inactivation of the URL or the referenced material.*

Table 3. External references

Reference	Name/address	Title
[3]	https://www.arm.com/	Cortex®-M33 Processor Technical Reference Manual

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2 STM32WBA2 series

The STM32WBA2 devices are ultra-low-power and wireless MCUs, with enhanced efficiency, performance, and memory size such as:

- 512 Kbytes of single-bank flash memory with ECC accelerated by instruction/data caches and up to 96 Kbytes of embedded SRAM with optional parity.

These devices reuse the same embedded Arm® Cortex®-M33 32-bit core as the STM32WBA5 series. This core runs at 100 MHz for the STM32WBA5 and 64 MHz for the STM32WBA2 series. This core provides improved security features due to the presence of the ultra-low-power Arm® TrustZone® for Armv8-M.

The STM32WBA2 series includes a reduced set of peripherals with some new peripherals compared to the STM32WBA5 series, such as the ones listed below:

- Power consumption
  - Optimized power consumption in low-power mode, using Stop 2, and Stop 3 mode
- Interfaces
  - Reduced GPIOs
  - Reduced ICACHE memory
  - Removed serial peripheral interface (SPI1)
  - Removed universal serial receive transmit (USART2)
  - Removed watchdog (WWDG)
  - Removed Hardware semaphore (HSEM)
  - Removed secure AES (SAES)
  - Removed Radio SRAM block-based security (MPCBB6)
  - Removed Touch sense (TSC)
  - Removed 16-bit advanced control timer (TIM1)
  - Removed 16-bit general purpose timer (TIM3)
  - Replaced GPDMA by LPDMA
  - Improved random number generator (RNG)
  - Improved RDP regression OEM key security
  - Added Flash HDP extension
  - Added USB FS(1)
  - Added XSPI(1) interface with associated DLYBXS1, OTFDEC1, and MPCWM1
  - Support for debug ETM

1. *Available only for STM32WBA25xx devices.*

Both STM32WBA5 and STM32WBA2 series embed high-speed memories and an extensive range of enhanced I/Os.

Table 4. STM32WBA5 and STM32WBA2 series overview

Package	Memory size		Device	
	Flash	SRAM	STM32WBA5	STM32WBA2
UFQFPN32	1 Mbytes	128 Kbytes	STM32WBA52KG	N/A
			STM32WBA54KG	
	512 Kbytes	96 Kbytes	STM32WBA52KE	STM32WBA23KE
			STM32WBA54KE	
Thin WLCSP37 SMPS USB	512 Kbytes	96 Kbytes	N/A	STM32WBA25HE
Thin WLCSP41 SMPS	1 Mbytes	128 Kbytes	STM32WBA55HG	N/A
	512 Kbytes	96 Kbytes	STM32WBA55HE	

Package	Memory size		Device	
	Flash	SRAM	STM32WBA5	STM32WBA2
UFQFPN48	1 Mbytes	128 Kbytes	STM32WBA52CG	N/A
			STM32WBA54CG	
	512 Kbytes	96 Kbytes	STM32WBA54CE	
			STM32WBA54CE	
UFQFPN48 SMPS	1 Mbytes	128 Kbytes	STM32WBA55CG	N/A
	512 Kbytes	96 Kbytes	STM32WBA55CE	STM32WBA23CE(1)
UFQFPN48 SMPS USB	512 Kbytes	96 Kbytes	N/A	STM32WBA25CE(1)
UFBGA59 SMPS	1 Mbytes	128 Kbytes	STM32WBA55UG	N/A
	512 Kbytes	96 Kbytes	STM32WBA55UE	

1. *Reduced GPIOs. See Section 2.1 Package compatibility with STM32WBA5.*

2.1 Memory availability

The STM32WBA2 series embeds similar memory as the STM32WBA5 series, shown in the table below.

Table 5. Memory size on STM32WBA5 and STM32WBA2 series

Product	Flash memory		SRAM1	SRAM2
	Size	Bank		
STM32WBA2	512 Kbytes	Single	64 Kbytes (one page)	32 Kbytes (two pages 8 KB + 24 kB
STM32WBA5	Up to 1 Mbytes	Single	Up to 64 Kbytes (one page)	64 Kbytes (one page)

2.2 System architecture differences between STM32WBA5 and STM32WBA2 series

Both STM32WBA5 and STM32WBA2 series embed high-speed memories and an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses and a 32-bit multi-AHB bus matrix. Additionally, the STM32WBA2 series embeds an XSPI (Quad-SPI) external memory interface.

The bus matrix provides access from a master to slave, enabling concurrent access and efficient operation when several high-speed peripherals work simultaneously. The STM32WBA5 series has a direct bus from ICACHE to the flash memory, which is not available in STM32WBA2 where the flash memory is accessed through the bus matrix.

The STM32WBA2 series connects different masters to the bus matrix than the STM32WBA5. The STM32WBA2 series also embeds less peripherals on internal buses.

The figures below detail the STM32WBA5 and STM32WBA2 series system architectures.

Figure 1. **STM32WBA5 system architecture**

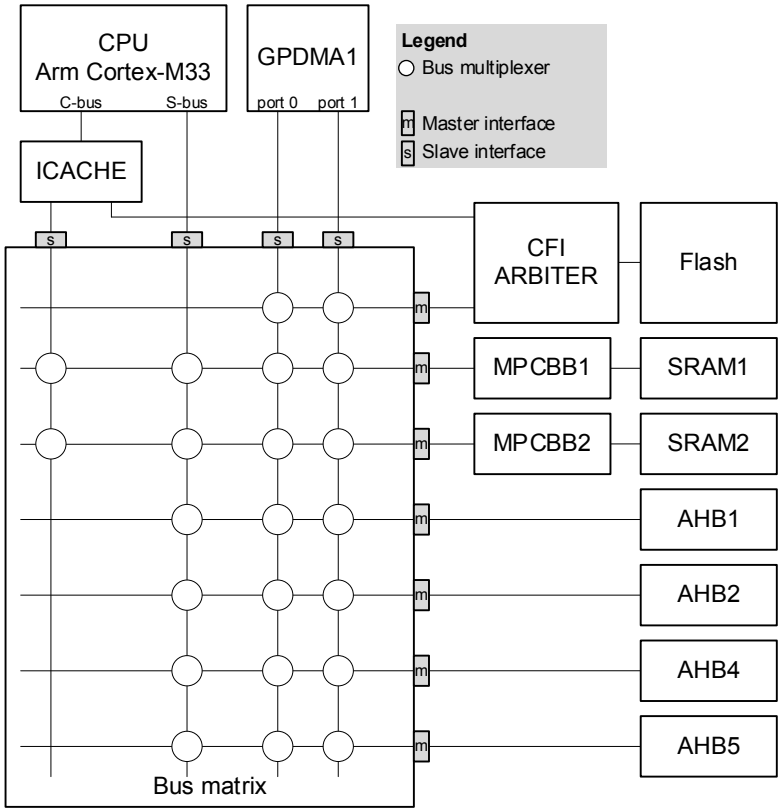
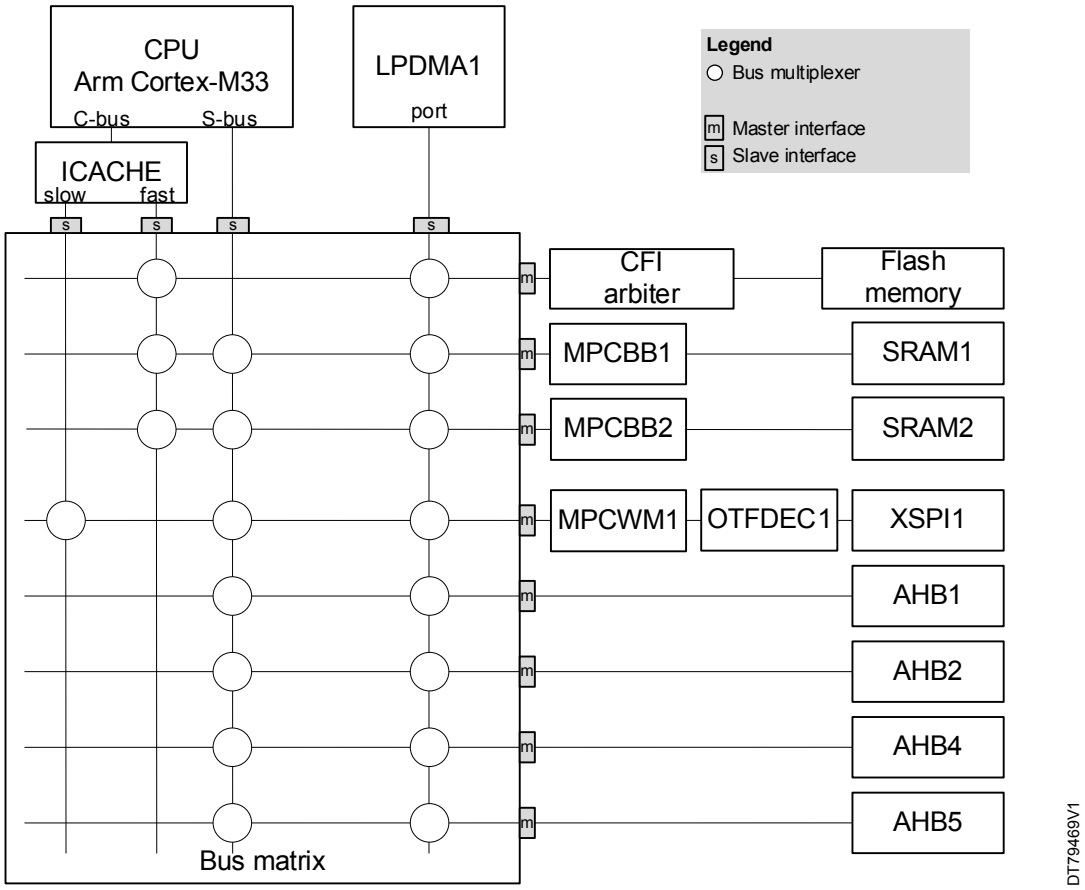


Figure 2. **STM32WBA2 system architecture**



The STM32WBA2 series architecture features a 32-bit multilayer AHB bus matrix that interconnects masters and slaves (see the tables below).

Table 6. **Masters connected to AHB bus matrix of STM32WBA5 and STM32WBA2 series**

AHB bus matrix masters	Fast C-bus ICACHE	Slow C-bus ICACHE	S-bus	DMA
STM32WBA2	1	1	1	1
STM32WBA5	Direct path to flash memory			2

Table 7. **Slaves connected to AHB bus matrix of STM32WBA5 and STM32WBA2 series**

AHB bus matrix slaves	Internal flash memory	SRAMs	AHB1 peripherals	AHB2 peripherals	AHB4 peripherals	AHB5 peripherals	XSPI
STM32WBA2	1(1)	SRAM1/2	1(2)	1	1(3)	1	1
STM32WBA5							N/A

1. *In addition to this master port, the STM32WBA5 embed a 128-bit cache refill bus that connects the flash memory to the ICACHE. This allows optimized core execution through the use of direct access to embedded flash memory.*
2. *Including APB1 and APB2 peripherals.*
3. *Including APB7 peripherals.*

3 Hardware migration

The STM32WBA2 series offers several packages from 32 to 48 pins. The 48-pin packages have a reduced number of GPIOs. Four versions of pinout are available:

- Without internal SMPS and without USB FS:
  - The 32-pin package is pin-2-pin compatible with STM32WBA5.
- With internal SMPS and without USB FS: pin-2-pin (with less GPIOs) compatible with STM32WBA5 48 pin package.
  - The 48-pin package compared to STM32WBA5 has four fewer GPIOs.
- With internal SMPS and with USB FS: (with less GPIOs) compared to STM32WBA5 48 pin package.
  - The 48-pin package has one pin of differences needed by the internal USB FS and compared to STM32WBA5 has four fewer GPIOs.

The USB FS is available only on the STM32WBA25xx devices.

The SMPS is available on all STM32WBA2xxx devices.

The table below lists the available packages without SMPS on the STM32WBA2 series compared with similar packages of STM32WBA5. It also lists the pinout compatibility and differences between these packages.

Table 8. Packages without SMPS on STM32WBA5 and STM32WBA2 series

STM32WBA2 Package	STM32WBA2 versus STM32WBA5	Pinout differences (pin name)		
		Pin number	STM32WBA5	STM32WBA2(1)
UFQFPN32	Pin-2-pin compatible	-	All compatible	All compatible

1. *N/C = not connected pin.*

Table 9. Packages with SMPS on STM32WBA5 and STM32WBA2 series

STM32WBA2 Package	STM32WBA2 versus STM32WBA5	Pinout differences (pin name)		
		Pin number	STM32WBA5	STM32WBA2(1)
UFQFPN48 SMPS	Compatible with four GPIOs less (the other pins are pin-2-pin compatible)	19	PB7	N/C
		31	PB1	
		32	PB0	
		48	PB14	
UFQFPN48 SMPS USB	Compatible with one difference on pin 13 and four GPIOs less (the other pins pin-2-pin compatible)	13	PA0	VDDUSB
		19	PB7	N/C
		31	PB1	
		32	PB0	
		48	PB14	

1. *N/C = not connected pin*

3.1 Package compatibility between STM32WBA5 and STM32WBA2

Figure 3. Package STM32WBA2 UFQFPN32 compatibility

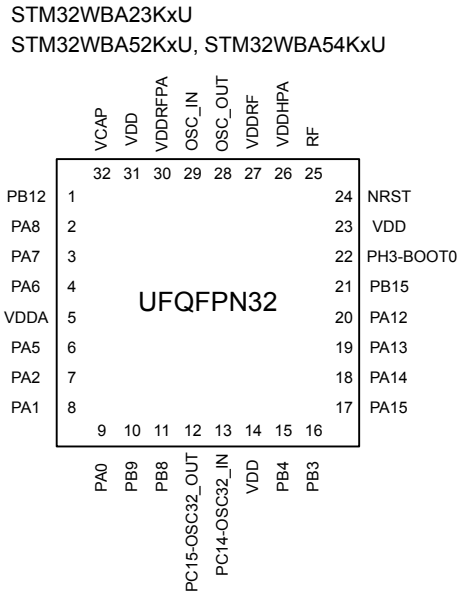


Figure 4. Package STM32WBA2 UFQFPN48_SMPS compatibility

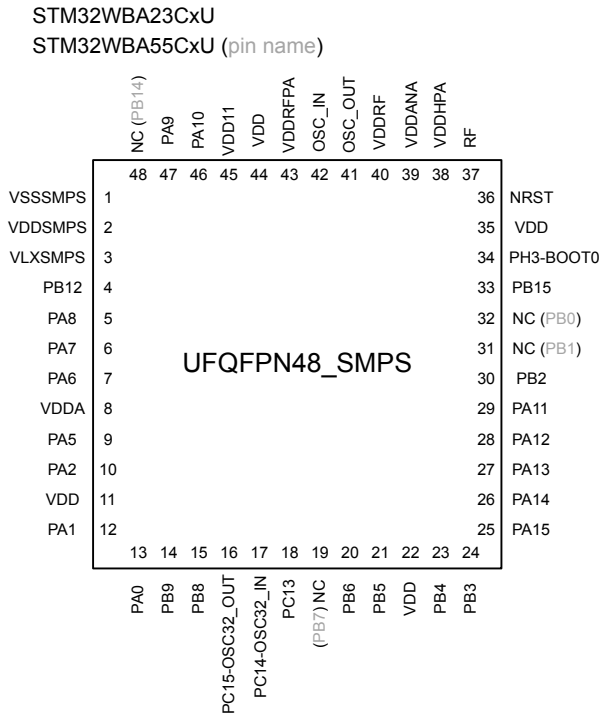
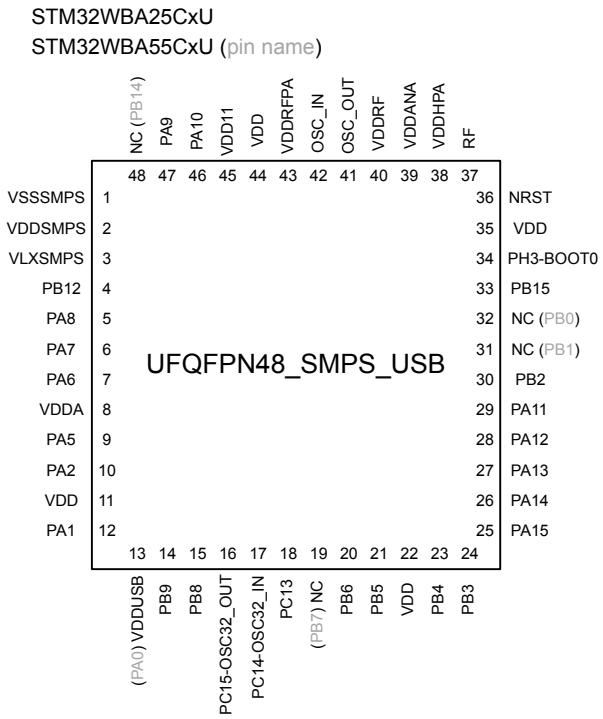


Figure 5. Package STM32WBA2 UFQFPN48_SMPS_USB compatibility



4 Boot mode compatibility

4.1 Boot modes selection

For the STM32WBA5 and STM32WBA2 series, the BOOT0 input pin may come from the PH3-BOOT0 pin or from an option bit, depending on the value of a user option bit to free the GPIO pad if needed.

The bootloader located in system memory is used to reprogram the flash memory by using USART, I2C, SPI, or USB FS in device mode through the DFU (device firmware upgrade).

The STM32WBA5 and STM32WBA2 series have compatible boot modes when TrustZone® is disabled or enabled (see the tables below). Refer to the series reference manual (RM0521) for more details.

Table 10. Bootmodes when TrustZone® is disabled (TZEN = 0) on STM32WBA5 and STM32WBA2 series

nBOOT0 FLASH_OPTR[27]	BOOT0 pin PH3	nSWBOOT0FLASH_OPTR[26]	Boot area	ST programmed default value
-	0	1	Boot address defined by user option bytes NSBOOTADD0[24:0]	User flash memory: 0x0800 0000
-	1	1	Boot address defined by user option bytes NSBOOTADD1[24:0]	Bootloader: 0x0BF8 8000
1	-	0	Boot address defined by user option bytes NSBOOTADD0[24:0]	User flash memory: 0x0800 0000
0	-	0	Boot address defined by user option bytes NSBOOTADD1[24:0]	Bootloader: 0x0BF8 8000

Table 11. Boot modes when TrustZone® is enabled (TZEN = 1)

BOOT_LOCK	nBOOT0 FLASH_OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR[26]	RSS command	Boot area	ST programmed default value
0	-	0	1	0	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	User flash memory: 0x0C00 0000
	-	1	1	0	RSS:	0x0FF8 0000
	1	-	0	0	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	User flash memory: 0x0C00 0000
	0	-	0	0	RSS:	0x0FF8 0000
	-	-	-	≠0		
1	-	-	-	-	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	User flash memory: 0x0C00 0000

4.2 Embedded bootloader

The embedded bootloader located in system memory and programmed by ST during production. This bootloader allows the user to reprogram the flash memory, using one of the serial interfaces listed in the table below.

Table 12. Bootloader interface on STM32WBA5 and STM32WBA2 series

Peripheral	Pinname (number)	STM32WBA5	STM32WBA2	
			STM32WBA23xx	STM32WBA25xx
DFU	USB_DP (PB8)	N/A		X
	USB_DM (PB9)			X

Peripheral	Pinname (number)	STM32WBA5	STM32WBA2	
			STM32WBA23xx	STM32WBA25xx
USART1	USART1_TX(PB12)	X	N/A	
	USART1_RX(PA8)	X		
	USART1_TX(PA6)	N/A	X	
	USART1_RX(PA12)		X	
USART2	USART2_TX(PA12)	X	N/A	
	USART2_RX(PA11)	X		
I2C1	I2C1_SCL(PB2)	X	N/A	
	I2C1_SDA (PB1)	X		
	I2C1_SCL(PA15)	N/A	X	
	I2C1_SDA (PB3)		X	
I2C3	I2C3_SCL(PA6)	X	N/A	
	I2C3_SDA (PA7)	X		
	I2C3_SCL(PB2)	N/A	X	
	I2C3_SDA (PA11)		X	
SPI3	SPI3_NSS (PA5)	X	X	
	SPI3_SCK (PA0)	X	N/A	
	SPI3_MISO (PB9)	X		
	SPI3_MOSI (PB8)	X		
	SPI3_SCK (PA8)	N/A	X	
	SPI3_MISO (PB4)		X	
	SPI3_MOSI (PA6)		X	

For more details on the bootloader, refer to document [2].

5 Peripheral migration

5.1 STM32 products cross-compatibility

STM32 microcontrollers embed a set of peripherals that can be classified in the following groups:

- Group1: peripherals, by definition, common to all products

Those peripherals are identical, so they have the same structure, registers, and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.

- Group2: peripherals shared by all products but with only minor differences (in general to support new features)

The migration from one product to another is very easy and does not need any significant new development effort.

- Group3: peripherals that have considerable changes from one product to another (new architecture or new features for example)

For this group of peripherals, the migration requires a new development at application level.

The security architecture of STM32WBA2 series devices and STM32WBA5 is based on Arm® TrustZone® with the Armv8-M mainline extension. Each GPIO or peripheral, DMA channel, clock configuration register, ICACHE, or small part of flash memory or SRAM, can be configured as trusted or untrusted.

The STM32WBA2 series microcontrollers innovative features include a new Stop2 and Stop 3 mode architecture, allowing wake-up from a reduced set of peripherals down to Stop 3 mode.

The table below summarizes the available peripherals in STM32WBA5 and STM32WBA2 series as well as their compatibility.

Table 13. STM32 peripheral compatibility between STM32WBA5 and STM32WBA2 series

<table>
<tr><th colspan="2">Peripheral</th><th>STM32WBA5</th><th>STM32WBA2</th></tr>
<tr><td colspan="2">Core</td><td colspan="2">Cortex-M33 TZ, MPU, FPU, DSP</td></tr>
<tr><td colspan="2">Maximum CPU frequency</td><td>100 MHz</td><td>64 MHz</td></tr>
<tr><td>Caches</td><td>ICACHE</td><td>1x ICACHE 8 KB</td><td>1x ICACHE 4 KB</td></tr>
<tr><td rowspan="7">PWR/regulators</td><td>Power supply</td><td colspan="2">1.71 to 3.6V</td></tr>
<tr><td>LDO</td><td colspan="2">Available on all products</td></tr>
<tr><td>LDO +</td><td colspan="2" rowspan="2">SMPS/LDO on-the-fly selection(1)</td></tr>
<tr><td>Internal SMPS</td></tr>
<tr><td rowspan="3">VOS range</td><td colspan="2">Range 1</td></tr>
<tr><td>N/A</td><td>Range 1.5</td></tr>
<tr><td colspan="2">Range 2</td></tr>
<tr><td colspan="2" rowspan="6">Low-power mode</td><td colspan="2">Stop 0</td></tr>
<tr><td colspan="2">Stop 1</td></tr>
<tr><td rowspan="2">N/A</td><td>Stop 2</td></tr>
<tr><td>Stop 3</td></tr>
<tr><td colspan="2">Standby retention</td></tr>
<tr><td colspan="2">Standby</td></tr>
<tr><td rowspan="2">Flash memory</td><td>Size</td><td>Up to 1 Mbytes</td><td>512 Kbytes</td></tr>
<tr><td>Bank</td><td colspan="2">Single bank with TrustZone®</td></tr>
<tr><td rowspan="2">SRAMs</td><td>SRAM1</td><td>Up to 64 Kbytes (one page)</td><td>Up to 64 Kbytes (one page)</td></tr>
<tr><td>SRAM2</td><td>64 Kbytes with parity (one page)</td><td>Up to 32 Kbytes with parity</td></tr>
</table>

Peripheral		STM32WBA5	STM32WBA2
SRAMs	SRAM2	64 Kbytes with parity (one page)	Up to 32Kbytes with parity (two pages 8 KB and 24 KB)
DMA		GPDMA (eight channels)	LPDMA (eight channels)
PLL		PLL (main)	
GTZC (global TrustZone® controller)		Three independent 32-bit AHB interface for TZSC, TZIC and MPCBB, TZIC accessible only with secure transactions. Secure and nonsecure access supported for privileged and unprivileged parts of TZSC. Set of registers to define product security settings	
Anti-tamper detection		Six tamper input/output pins	Four tamper input/output pins
		128-byte backup registers	128-byte backup registers
CRC		1x CRC	
GPIO	Port A	PA[15:5,2:0]	
		PA[4:3]	N/A
	Port B	PB[15,12,9:8,6:2]	
		PB[14:13,11:10,7,1:0]	N/A
	Port C	PC[15:13]	
	Port D	N/A	
	Port E	N/A	
	Port G	N/A	
	Port H	PH[3]	
Timers	Advanced control	TIM1 (16-bit)	N/A
	General purpose	TIM2 (32-bit)	
		TIM3 (16-bit)	N/A
	Basic	TIM16/17 (16-bit)	
	Low-power	LPTIM1/2 (16-bit) Autonomous mode	
	Watchdogs	1x IWDG	
		1x WWDG	N/A
	RTC	1x RTC + Binary mode selection	
	SysTick	2	
Communication interfaces	SPI	SPI1/3 + Autonomous mode	SPI3 + Autonomous mode SPI3 in Stop 2 mode
	I2C	I2C1/3 + Autonomous mode	I2C1/3 + Autonomous mode I2C3 in Stop 2 mode
	USART	USART1/2 + Autonomous mode	USART1 + Autonomous mode
	LPUART	LPUART1 + Autonomous mode	LPUART1 + Autonomous mode LPUART1 in Stop 2 mode
	SAI (audio interface)	SAI1 (port A and B)	SAI1 (port A + SD port B)
	XSPI	N/A	XSPI1, OFTDEC1, MPCWM1(2)
	USB	N/A	USB full speed with embedded PHY(2)
Analog peripherals	ADC	1x 12-bit ADC4 (2.5 Msps)+ Autonomous mode	
	COMP	2x comparators	N/A
	Voltage reference buffer(1)	N/A	
Cryptographic peripherals	AES	1x AES	1x AES with Key derivation

Peripheral		STM32WBA5	STM32WBA2
Cryptographic peripherals	SAES (secure AES)	1x SAES	N/A
	PKA (private key accelerator)	1x PKA	
	HASH (SHA-256)	1x HASH	
	RNG (true random number generator)	1x RNG (3 sources)	1x RNG (6 sources)
Signal-processing coprocessors accelerators	TSC (touch sensing control)	12 channels	N/A
Debug		JTAG, SWD	
		N/A	ETM

1. *Only available on STM32WBA23xx/25xx.*
2. *Only available on STM32WBA25xx.*

5.2 Secure and nonsecure boundaries of peripheral memory mapping

The peripheral address mapping has been kept the same in the STM32WBA2 series compared to the STM32WBA5.

The STM32WBA2 new peripherals have been added to the memory map. For more details on the memory mapping, refer to the product reference manual.

6 Migration of security peripherals

6.1 TAMP

The STM32WBA2 series anti-tamper detection circuit is used to protect sensitive data from external attacks. 32 backup registers, each of 32-bit size, are retained in all low-power modes.

6.1.1 Tamper pins and internal events

The table below shows the differences between the TAMP in STM32WBA5 and in STM32WBA2 series.

Table 14. TAMP features in STM32WBA5 and STM32WBA2 series

Peripheral	STM32WBA5	STM32WBA2
Internal tampers	9x	
TAMP	IN1/OUT2	
	IN2/OUT1	
	IN3/OUT6	IN3/OUT4
	IN4/OUT5	IN4/OUT3
	IN5/OUT4	N/A
	IN6/OUT3	

6.1.2 Boot hardware key

The first eight backup registers can be used to store a boot master key, programmed during boot for the SAES (secureAES). Once locked, the eight backup registers cannot be accessed anymore by software: they are read as 0 and write to these registers is ignored.

The locking bit BHKLOCK cannot be cleared by software. It is cleared either by hardware following a tamper event or when the readout protection (RDP) is disabled. In both cases, the backup registers are also erased. Refer to section 'Boot hardware key' of the reference manual for more details.

6.2 OTFDEC (on-the-fly decryption engine)

The STM32WBA2 series embeds the OTFDEC1. On-the-fly decryption engine is not available from STM32WBA5.

The OTFDEC1 decrypts in real-time the encrypted content stored in the XSPI1, memory mapped mode, external memory.

6.3 HASH (hash processor)

The table below shows the differences between the HASH in STM32WBA5 and in STM32WBA2 series.

Table 15. HASH features in STM32WBA5 and STM32WBA2 series

Features	STM32WBA5	STM32WBA2
SHA-1	X	
SHA2-256	X	
HMAC	X	
MD5	X	N/A

6.4 RNG (true random number generator)

The STM32WBA5 and STM32WBA2 series embed both an RNG hardware accelerator with the same features. The STM32WBA2 embed an improved version with additional health test configuration registers and less noise sources.

6.5 PKA (public key accelerator)

The STM32WBA5 and STM32WBA2 series embed the same PKA hardware accelerator with the same features.

6.6 AES and SAES hardware accelerators

The STM32WBA5 series embed two AES accelerators: one secure AES (SAES) and a faster AES both with the same features. The STM32WBA2 series embed only one AES accelerators: that is faster AES with enhanced features.

Table 16. AES and SAES features in STM32WBA5 and STM32WBA2 series

Features	STM32WBA5		STM32WBA2	
	AES	SAES	AES	SAES
ECB, CCB chaining	X			N/A
CTR, CCM, GCM chaining	X			
AES 128-bit ECB encryption speed	51 cycles	528 cycles	51 cycles	
256-bit key	X			
DHUK and BHK key selection	N/A	X	N/A	
Shared key bus	X		N/A	
AES tamer signal	X			
Key derivation	N/A	KEYSEL	N/A	

6.7 GTZC (global TrustZone® controller)

The security architecture of STM32WBA5 and STM32WBA2 series is based on Arm® TrustZone® with the Armv8-M mainline extension. Each GPIO or peripheral, DMA channel, clock configuration register, ICACHE or small part of flash memory or SRAM can be configured as trusted or untrusted.

The GTZC embedded in the STM32WBA5 and STM32WBA2 series is used to configure secure-TrustZone® and privileged attributes within the full system. It contains the following sub-blocks:

- TZSC: TrustZone® security controller

This sub-block defines the secure/privileged state of slave peripherals. It also controls the region are size and properties for the memory protection controller watermark based (MPCWM). The TZSC informs some peripherals (such as RCC or GPIOs) about the secure status of each securable peripheral, by sharing with RCC and I/O logic.

- MPCBB: memory protection controller block-based

This sub-block configures the internal RAM in a TrustZone®-system product having segmented SRAM (pages of 512 bytes) with programmable-security and privileged attributes.

- TZIC: TrustZone® illegal access controller

This sub-block gathers all illegal access events in the system and generates a secure interrupt towards NVIC.

The STM32WBA5 and STM32WBA2 series GTZC registers for the same peripheral are the same. The STM32WBA2 new peripherals have been added to the register map.

6.7.1 GTZC implementation and resource assignments

The STM32WBA2 series and STM32WBA5 implement the same GTZC peripherals, except for MPCBB and MPCWM (see tables below).

Table 17. MPCBB resources in STM32WBA5 and STM32WBA2 series

MPC	Resource	Blocksize (bytes)	Parameters	STM32WBA5	STM32WBA2
MPCBB1	SRAM1	512	Memory size (Kbytes)	Up to 64	64
			Number of blocks	Up to 128	128
			Number of super-blocks	Up to 4	4
MPCBB2	SRAM2		Memory size (Kbytes)	64	32
			Number of blocks	128	64
			Number of super-blocks	4	2
MPCBB6	RXTXSRAM		Memory size (Kbytes)	16	N/A
			Number of blocks	32	
			Number of super-blocks	1	

Table 18. MPCWM resources in STM32WBA5 and STM32WBA2 series

MPC	Resource	Parameters	STM32WBA5	STM32WBA2
MPCWM1	XSPI1	Regions	N/A	2
		Water mark granularity (Kbytes)		128

6.7.2 TrustZone® peripheral classification

When the TrustZone® security is active, a peripheral can be either securable or TrustZone®-aware as follows:

- Securable: peripheral protected by an AHB/APB firewall gate that is controlled from TZSC to define security properties
- TrustZone®-aware: peripheral connected directly to AHB or APB bus and implementing a specific TrustZone® behavior such as a subset of registers being secure

The default system security state is the same for STM32WBA5 and STM32WBA2 series.

6.7.3 TrustZone® security architecture

When the TrustZone® is enabled, the Armv8-M attributes define the access permissions based on secure and nonsecure state:

- SAU (security attribution unit): up to eight SAU configurable regions available for security attribution
- IDAU (implementation defined attribution unit): provides a first memory partition as nonsecure or nonsecure callable attributes. This partition is then combined with the results from the SAU security attribution and the higher-security state is selected.

Based on IDAU security attribution, the flash memory, system SRAMs and peripheral memory space are aliased twice for secure and nonsecure states. However, the external memory space is not aliased.

The STM32WBA5 and STM32WBA2 series datasheets give the same example of memory map security attribution versus SAU configuration regions.

7 Migration of 2.4 GHz RADIO

This section analyzes the differences and similarities for the 2.4 GHz RADIO implemented in STM32WBA5 and STM32WBA2 series.

7.1 2.4 GHz RADIO

The table below shows the differences between the 2.4 GHz RADIO in STM32WBA5 and in STM32WBA2 series.

Table 19. 2.4 GHz RADIO features in STM32WBA5 and STM32WBA2 series

Features		STM32WBA5	STM32WBA25xx	STM32WBA23xx
Bluetooth LE	2 Mbps	X		
	1 Mbps	X		
	500 kbps coded	X		
	125 kbps coded	X		
	Audio	X		
	AoA/AoD	X		
Zigbee	Beacon management	X		
	Non-beaconed PAN	X		
Thread		X		
Matter		With external Host		
IEEE802.15.4	Proprietary	X		
Concurrent modes	Bluetooth - Thread	X		
	Bluetooth - Zigbee	X		
	Zigbee - Thread	X		
	Bluetooth – Thread - Zigbee	X		
Packet traffic arbitration (PTA)		X		
Maximum output power		+10 dBm		
External PA		X		

8 Migration of system peripherals

This section analyzes the differences and similarities between system peripherals implemented in STM32WBA5 and STM32WBA2 series.

8.1 SYSCFG (system configuration controller)

The table below shows the differences between the SYSCFG in STM32WBA5 and in STM32WBA2 series.

Features	STM32WBA5	STM32WBA2
Common features	Managing robustness feature	
	Configuring TrustZone® security register access	
	Configuring FPU interrupts	
	Driving capability on some I/Os and voltage booster for I/Os analog switches	
Managing I/O compensation cells	Compensation cells on VDD thePVT conditions to control the current slew-rate and output impedance in I/O buffer	
I2C Fast-mode Plus	I2CI/Os fast mode plus drive is controlled from the I2C peripheral. This mode can still be enabled/disabled in SYSCFGfor four I/Os when not used by I2C.	
Flash operation abort	N/A	Flash operation abort on interrupt

8.2 Flash memory

Compared to the STM32WBA5, the STM32WBA2 series flash memory includes smaller memory space (see the table below).

Table 20. Flash memory features in STM32WBA5 and STM32WBA2 devices

Feature	STM32WBA5	STM32WBA2
Size	Up to 1 Mbytes single bank (128 x 8-Kbyte pages)	512 Kbytes single bank (128x 4 Kbytes pages)
	OTP area: 512 bytes, base address 0x0BF9 0000	
	RSS + RSS lib, base address 0x0FF8 0000	
	Bootloader, base address 0x0BF8 8000	
Access modes	Read (R) and Write (W)	
	Single bank, 128 bit read/write access	Single bank, 64 bit read/write access
ECC	9 bits per 128-bit quad word. The ECC mechanism supports: • One error detection and correction • Two errors detection	8 bits per 64-bit double word. The ECC mechanism supports: • One error detection and correction • Two errors detection
Read-access latency	Up to three wait-states (WS) depending on the supply voltage and the frequency	Up to one wait-states (WS) depending on the supply voltage and the frequency
	The flash memory supports a low-power read mode (LPM). The number of WS depends on the supply voltage and the frequency	
	Instruction prefetch through ICACHE can be enabled by setting the PRFTEN bit that increases code execution speed	
Power-downmode per Bank	After reset, the bank is in normal mode. The bank can be put in power-down	
Endurance capability	10 Kcycles (written and erased) on all flash memory.	10 Kcycles (written and erased) on all flash memory.

Feature	STM32WBA5	STM32WBA2
	100 Kcycles (written and erased) on 256 Kbytes (32 pages).	
Flash program and erase operations	Page/mass erase	
	128-bit (quad word) programming	64-bit (double word) programming
Flash memory protection	Write protection (WRP)	
	Readout protection (RPD)	
	One secure watermark-based area	
	One secure watermark-based hide protection area	
	HDP_PEND[6:0]	
	HDPEN	HDPEN[7:0]
	HDP_ACCDIS	HDP_ACCDIS[7:0]
	N/A	One secure watermark-based extended hide protection area
		HDP_PEXT[6:0]
		HDP_ACCDIS[7:0]
	On-the-fly programmable secure block-based areas with page granularity	
	On-the-fly programmable privileged block-based areas with page granularity	
Privileged register protection	For secure (SPRIV) and nonsecure (NSPRIV) accesses	
Locking keys for RDP	OEM key protection for RDP regression between levels: • Possible RDP regression from L1 to L0 with OEM1 key • Possible RDP regression from L1 to L0.5 with OEM2 key • Possible RDP regression from L2 to L1 with OEM2 key	
Operation abort	N/A	Operation abort on interrupt

The option bytes are configured by the end user depending on the application requirements. The option bytes register address mapping has been kept the same in the STM32WBA2 series compared to the STM32WBA5. The STM32WBA2 new option bytes have been added to the register map. See the table below and refer to section 'Flash memory option bytes' of the product reference manual for more details.

Table 21. Main option bytes in STM32WBA5 and STM32WBA2 devices

Option bit/byte	STM32WBA5	STM32WBA2
Global TrustZone® activation	TZEN: global TrustZone® security enable	
Readout Protection	RDP level:	
Reset	BOR_LEV[2:0]: BOR reset level.	
	NRST_STOP: Reset generation in STOP mode	
	NRST_STDBY: Reset generation in Standby mode	
	SRAM_RST: SRAM1 erased when a system reset occurs	
	SRAM2_RST: SRAM2 erase when system reset occurs	
Watchdog	WWDG_SW: Window watchdog selection	
	IWDG_SW: Hardware or Software independent watchdog selection	
	IWDG_STOP: Independent watchdog counter freeze in Stop mode	
	IWDG_STDBY: Independent watchdog counter freeze in Standby mode	
Secure and nonsecure boot	NSWBOOT0: Software BOOT0	
	NBOOT0 option bit	

Option bit/byte	STM32WBA5	STM32WBA2
Secure and nonsecure boot	NSBOOTADD0[24:0]: Nonsecure boot base-address 0	
	NSBOOTADD1[24:0]: Nonsecure boot base-address 1	
	SECBOOTADD0[24:0]: Secure boot base-address 0	
	BOOT_LOCK: Boot lock	
Flash memory secure watermark	SECWM_PSTRT[6:0]: First page of the secure area	
	SECWM_PEND[6:0]: Last page of the secure area	
	LHDP_PEND[6:0]: lst page of HDP area	
	HDPEN: Hide protection area enable	HDPEN[7:0]: Hide protection area enable
Flash memory write protection (WRP) areas	WRPA_PSTRT[6:0]: First page of the WPR area A	
	WRPA_PEND[6:0]: The last page of the WPR area A	
	UNLOCK WRP area A	
	WRPB_PSTRT[6:0]: First page of the WPR area B	
	WRPB_PEND[6:0]: The last page of the WPR area B	
	UNLOCK WRP area B	
Flash memory locking keys for RDP level regression	OEM1KEY[63:0]: OEM1 key	OEM1KEY[127:0]: OEM1 key
	N/A	OEM1KEYCRC[7:0]: read only
	OEM2KEY[63:0]: OEM2 key	OEM2KEY[127:0]: OEM2 key
	N/A	OEM2KEYCRC[7:0]: read only
RAM parity	SRAM2_PE: SRAM2 parity check enable option bit	

8.3 SRAMs

In the STM32WBA5 and STM32WBA2 series SRAM control is implemented in the RAMCFG controller (refer to section 'RAMs configuration controller' in the product reference manual for more details).

The table below compares the embedded SRAMs features in STM32WBA5 and STM32WBA2 devices.

Table 22. SRAMs in STM32WBA5 and STM32WBA2 devices

Feature		STM32WBA5	STM32WBA2
Size (Kbytes)		SRAM1: up to 64 Kbytes	SRAM1: 64 Kbytes
		SRAM2: 64 Kbytes	SRAM2 page 1: 8 Kbytes
			SRAM2 page 2: 24 Kbytes
Access by DMA and CPU		SRAM1, SRAM2: Bytes, half-words (16 bits) or full words (32 bits) possible access	
CPU access bus	System bus	SRAM1, SRAM2	
	C-bus access	N/A	Direct access
		SRAM1, SRAM2 (through ICACHE remap)	SRAM1, SRAM2 (through ICACHE remap)
Retention in Stop and Standby		SRAM1: 64 Kbytes	SRAM1: 64 Kbytes
		SRAM2: 64 Kbytes	SRAM2 page 1: 8Kbytes
		N/A	SRAM2 page 2: 24 Kbytes
Security		When the TrustZone® security is enabled, all SRAMs are secure after reset.	
Security		The SRAMs can be programmed as nonsecure using the MPCBBx with a block granularity of 512 bytes.	

Feature	STM32WBA5	STM32WBA2
Hardware erase conditions	All SRAMs are erased by hardware in case of RDP level regression to L0.5 or L0.	
	SRAM2 is protected by the tamper detection circuit and is erased by hardware in case of tamper detection.	
Software erase conditions	Each SRAM erase can be requested by executing a specific software sequence,detailed in section 'RAMCFG' of the product reference manuals.	
System reset erase	SRAM2 is erased when a system reset occurs if SRAM2_RST option is selected	
	SRAM1 is erased when a system reset occursif SRAM1_RST option is selected	
WRP	SRAM2 can be write protected with a page granularity of 1 Kbyte.	
Errors detection	SRAM2 parity error can be detected if SRAM2_PE option is selected	
	Interrupts are generated when a SRAM2 parity error is detected: • NVIC parity interrupt • NMI parity interrupt Interrupts allow the device to exit Sleep, Stop 0 or Stop 1 mode.	
	SRAM2 parity error event can be linked to the BRK_IN break input of TIM16 or TIM17	
Read access latency	Up to one wait-states (WS) depending on voltage range 2 and AHB clock frequency (HCLK)	

8.4 Caches

The STM32WBA5 and STM32WBA2 series embed the same ICACHE that allow for more efficient use of the internal flash memory.

Table 23. ICACHE features in STM32WBA5 and STM32WBA2 series

Features	STM32WBA5	STM32WBA2
ICACHE size	8 KB	4 KB
Fast port	128-bit (Flash)	32-bit (Flash, SRAM1, SRAM2)
Slow port (remap)	32-bit (SRAM1, SRAM2)	32-bit (XSPI bank)(1)

1. *Only 32 Kbytes available on STM32WBA25xx.*

8.5 DMA

The STM32WBA5 series devices have a GPDMA whereas the STM32WBA2series devices have a LPDMA.

STM32WBA series DMA module is named GPDMA (general-purpose DMA) or LPDMA (low-power DMA). The DMA request and trigger mapping has been compressed in the STM32WBA2 series compared to the STM32WBA5. The STM32WBA2 new peripherals have been added to the DMA request and trigger map. See the table below and refer to section 'GPDMA' of the product reference manual for more details.

Table 24. DMA features in STM32WBA5 and STM32WBA2 series

Features	STM32WBA5	STM32WBA2
Number of masters	Dual bidirectional AHB master	Single bidirectional AHB master
Linked-List	Separately programmed source and destination transfers	

Features	STM32WBA5	STM32WBA2
Linked-List	Programmable data handling between source and destination	
	Block-level (programmable number of data bytes)	
	Linear source and destination addressing: • Programmable signed address offsets between successive burst transfers	
Linked-List 2D addressing	2D source and destination addressing	N/A
	Scatter-gather (multi-buffer transfers), data interleaving and deinterleaving via 2D addressing	
Data transfers from source to destination	Peripheral-to-memory, memory-to-peripheral, memory-to-peripheral and peripheral-to-peripheral	
Number of channels	8	
Number of requests/triggers	52 DMA requests	45 DMA requests
	30 triggers	28 triggers
Autonomous data transfer in Sleep and Stop modes	Autonomous data transfers and wakeup during the low-power modes Stop 0	
TrustZone® privileged/unprivileged	Same features	
Retention	Down to Stop 1 mode	Down to Stop 1 mode (Not retained in Stop 2 and Stop 3)

8.6 NVIC

The STM32WBA2 series devices have a compressed NVIC mapping. The STM32WBA2 new peripherals have been added to the NVIC map.

Table 25. NVIC mapping in STM32WBA5 and STM32WBA2 series

IRQ	Position	
	STM32WBA5	STM32WBA2
WWDG	0	N/A
PVD	1	
RTC	2 to 3	
TAMP	4	
RAMCFG	5	
FLASH	6 to 7	
GTZC	8	
RCC	9 to 10	
EXTI0 to EXTI15	11 to 26	
IWDG	27	
SEAS	28	N/A
DMA1_CH0 to DMA1_CH7	29 to 36 (GPDMA)	28 to 35 (LPDMA)
OTFDEC1	N/A	36
TIM1	37 to 40	N/A
TIM2	41	40
TIM3	42	N/A
I2C1	43 to 44	41 to 42

IRQ	Position	
	STM32WBA5	STM32WBA2
SPI1	45	N/A
USART1	46	43
USART2	47	N/A
LPUART1	48	44
LPTIM1	49	45
LPTIM2	50	46
TIM16	51	47
TIM17	52	48
COMP	53	N/A
I2C3	54 to 55	49 to 50
SAI	56	51
TSC	57	N/A
AES	58	52
RNG	59	53
FPU	60	54
HASH	61	55
PKA	62	56
SPI3	63	57
ICACHE	64	58
ADC4	65	59
RADIO	66	60
WKUP	67 and 70	61 to 62
HSEM	68 to 69	N/A
RCC_AUDIO	71	63
USB	N/A	64
XSPI1	N/A	65
RADIO_IO	N/A	66 to 67

8.7 EXTI

The STM32WBA5 and STM32WBA2 series devices have the same EXTI mapping. The STM32WBA2 new events have been added to the EXTI map.

Table 26. EXTI mapping in STM32WBA5 and STM32WBA2 series

Event	Position	
	STM32WBA5	STM32WBA2
GPIO	0 to 15	
PVD	16	
COMP	17 to 18	N/A
RADIO	N/A	19 to 20

8.8 RCC (reset and clock control)

The STM32WBA2 series RCC manages clocks and resets of system and peripherals, the same features as the STM32WBA5 series. The RCC register mapping has been kept the same in the STM32WBA2 series compared to the STM32WBA5 series. The STM32WBA2 new peripherals have been added to the RCC register map.

Table 27. RCC features in STM32WBA5 and STM32WBA2 series

Feature	STM32WBA5	STM32WBA2
Safe and flexible reset management without external components	System reset, power reset and Backup domain reset	
Internal clock sources	HSI16 with trimming	
	LSI1 32 kHz 1%	
	LSI2 32 kHz 500 ppm/°C	N.A
External clock sources	HSE 32 32 MHz with trimming	
	LSE 32.768 kHz	
PLLs	PLL1 (main PLL 100 MHz)	PLL1 (main PLL 64 MHz)

The table below lists the RCC input/output signals and their mapping on STM32WBA5 and STM32WBA2 series.

Table 28. RCC pin names in STM32WBA5 and STM32WBA2 series

Alternate function	Pin name STM32WBA5	Pin name STM32WBA2
NRST	NRST	
OSC32_IN	PC14	
OSC32_OUT	PC15	
OSC_IN	OSC_IN	
OSC_OUT	OSC_OUT	
MCO	PA8	
LSCO	PA2	
AUDIO_CLK	PA4	N/A
	PA5	

The table below details the RCC clock sources for STM32WBA5 compared to STM32WBA2 series.

Table 29. Clock sources in STM32WBA5 and STM32WBA2 series

Clock source	STM32WBA5	STM32WBA2
System clock	100 MHz maximum frequency	64 MHz maximum frequency
	16MHz after reset, Stop, and Standby modes using HSI16	
	HSI16, HSE32, or PLL	
HSE	32 MHz user trimmed	
HSI16	Generated from an internal 16 MHz RC oscillator 16 MHz RC factory and user trimmed Can be used as a backup clock source (auxiliary clock) if HSE crystal oscillator fails Is the system clock after wake-up from Stop and Standby modes	
LSE	32.768 kHz or 32.000 kHz configurable drive/consumption, available in V_{DD} domain	

Clock source	STM32WBA5	STM32WBA2
LSI	LSI1 32 kHz low consumption (refer to electrical characteristics section of the datasheet), available in VDD domain.	
	LSI2 24 kHz – 49 kHz high accuracy (refer to electrical characteristics section of the datasheet), available in V_{DD} domain.	N/A
Clock-out capabilities MCO and LSCO	One of the following clock signals can be selected as MCO: LSI, LSE, HSI16,HSE32, SYSCLKpre, pll1pclk, pll1qclk, pll1rclk, hclk5	
	One of the following clock signals can be selected as LSCO: LSI or LSE. This output remains available in Stop and Standby modes.	
Clock measurement and calibration using Timers	LSI calibration using TIM16/TIM17/LPTIM1	
	HSI16 calibration using TIM16/TIM17/LPTIM2	
Interrupts	HSECSS (linked to NMI IRQ)	
	An equivalent interrupt vector to the one below is available for secure events, only when TrustZone® is enabled.	
	LSECSS	
	PLL1RDY	
	LSI1RDY, LSI2RDY,LSERDY, HSIRDY and HSERDY	
	Audio synchronization CAF, COF, and CAEF	

8.8.1 PLL

The STM32WBA5 and STM32WBA2 series embed the same fractional PLL.

Table 30. PLL max frequency in STM32WBA5 and STM32WBA2 series

Product voltage range	STM32WBA5	STM32WBA2
PLL clock out	Maximum 100 MHz	Maximum 64 MHz

8.8.2 Bus frequencies versus voltage scaling

The STM32WBA5 and STM32WBA2 series embed the same voltage scaling. There is additional voltage scaling added in STM32WBA2. The table below lists the maximum frequencies of internal bus in STM32WBA5 and STM32WBA2 series, depending on the product voltage range.

Table 31. Bus max frequency versus voltage scaling in STM32WBA5 and STM32WBA2 series

Product voltage range	STM32WBA5	STM32WBA2
Range1	AHB1, AHB2, AHB4: maximum 100 MHz	AHB1, AHB2, AHB4: maximum 64 MHz
	AHB5: maximum 32 MHz	
Range 1.5	N/A	AHB1, AHB2, AHB4: maximum 64 MHz
		AHB5: maximum 32 MHz
Range2	AHB1, AHB2, AHB4, AHB5: maximum 16 MHz	

8.8.3 CSS (clock security system)

The STM32WBA5 and STM32WBA2 series embed the same CSS.

Table 32. CSS in STM32WBA5 and STM32WBA2 series

CSS clock source	STM32WBA5	STM32WBA2
CSS on HSE	Same features	
CSS on LSE modes	Run, Stop, Standby retention, Same features	
	Standby mode	N/A

8.8.4 Specific ADC clocks features

The STM32WBA5 and STM32WBA2 series embed the same ADC clocks and features, in particular if ADC is precisely triggered by a TIMx timer without any uncertainty, the HCLK must be selected as ADC kernel clock source. The other clock sources are asynchronous to TIMx timers. The LPTIMx timers are also asynchronous.

Table 33. ADC in STM32WBA5 and STM32WBA2 series

Feature	STM32WBA5	STM32WBA2
ADC channel	IN1:4,7:9	
	IN5:6,10	N/A

8.8.5 RTC and TAMP clock

The STM32WBA5 and STM32WBA2 series embed the same RTC and TAMP clocks. The table below lists the features of RTC and TAMP clock sources for STM32WBA5 and STM32WBA2 series.

Table 34. RTC and TAMP clock in STM32WBA5 and STM32WBA2 series

Feature		STM32WBA5	STM32WBA2
Clock source for RTC and TAMP		HSE32 / 32, LSE, or LSI	
Only the backup registers used in TAMP with tampers in edge detection mode		No kernel clock required	
TAMPER pin		TAMP_IN1/OUT2	
		TAMP_IN2/OUT1	
		TAMP_IN3/OUT6	TAMP_IN3/OUT4
		TAMP_IN4/OUT5	TAMPIN4/OUT3
		TAMP_IN5/OUT4	N/A
		TAMP_IN6/OUT3	N/A
Backup domain active clocks		LSE and LSI	
Operational	Run, Stop 1	Operations	
	Stop 2	N/A	Operational
	Stop 3	N/A	Not operational (retained)
	Standby retention	Operational	
	Standby	Operational	Not operational (power down)

8.8.6 Timer and watchdog clock sources

The timer clock frequencies are automatically defined by hardware, with the following cases:

- If the APB prescaler equals one, the timer clock frequencies are set to the APB domain frequency.
- Otherwise, they are set to twice the APB domain frequency.

If the independent watchdog (IWDG) is started by either hardware option or software access, the LSI oscillator is forced on and cannot be disabled. After the LSI oscillator temporization, the LSI 32 kHz clock is provided to the IWDG.

8.8.7 Peripherals clock gating and reset

The STM32WBA2 series peripheral clock gating and reset provide the same features as the STM32WBA5 series. The RCC register mapping has been kept the same in the STM32WBA2 series compared to the STM32WBA5 series. The STM32WBA2 new peripherals have been added to the RCC register map.

The table below shows the RCC registers used for peripheral access configuration for STM32WBA5 and STM32WBA2 series.

Table 35. RCC clock and reset registers for STM32WBA5 and STM32WBA2 series

Register	STM32WBA5	STM32WBA2
AHB: [enter/exit] AHB peripherals from Reset	RCC_AHB1RSTR RCC_AHB2RSTR RCC_AHB4RSTR RCC_AHB5RSTR	
APB: [enter/exit] APB peripherals from Reset	RCC_APB1RSTR1 RCC_APB1RSTR2 RCC_APB2RSTR RCC_APB7RSTR	
AHB: [enable/disable] the AHB peripheral clock	RCC_AHB1ENR RCC_AHB2ENR RCC_AHB4ENR RCC_AHB5ENR	
APB: [enable/disable] the APB peripheral clock	RCC_APB1ENR1 RCC_APB1ENR2 RCC_APB2ENR RCC_APB7ENR	
AHB: [enable/disable] the AHB peripheral clock in Sleep mode	RCC_AHB1SMENR RCC_AHB2SMENR RCC_AHB4SMENR RCC_AHB5SMENR	
APB: [enable/disable] the APB peripheral clock in Sleep mode	RCC_APB1SMENR1 RCC_APB1SMENR2 RCC_APB2SMENR RCC_APB7SMENR	

8.8.8 Peripheral clock source migration

The STM32WBA2 series peripheral clock gating and reset provide the same features as the STM32WBA5 series. The RCC register mapping has been kept the same in the STM32WBA2 series compared to the STM32WBA5 series. The STM32WBA2 new peripherals have been added to the RCC register map.

Table 36. Peripheral clock sources in STM32WBA5 and STM32WBA2 series

Peripheral	STM32WBA5	STM32WBA2
IWDG	LSI	
WWDG	PCLK1	N/A
RTC / TAMP	LSE, LSI, or HSE/32	
LPTIMx (x = 1, 2)	HSI16, lsesys, LSI	
TIM2	PCLK1	

Peripheral	STM32WBA5	STM32WBA2
TIM3	PCLK1	N/A
TIM1	PCLK2	N/A
TIMx (x = 16, 17)	PCLK2	
USART2	HSI16, lsesys, PCLK1, SYSCLK	N/A
USART1	HSI16, lsesys, PCLK2, SYSCLK	
LPUART1	HSI16, lsesys, PCLK7, SYSCLK	N/A
SPI1	HSI16, PCLK2, SYSCLK	N/A
SPI3	HSI16, PCLK7, SYSCLK	
I2C1	HSI16, PCLK1, SYSCLK	
I2C3	HSI16, PCLK7, SYSCLK	
XSPI(1)	N/A	AHB
		Feedback clock delay DLYBXS1
SAI1	HSI16, SYSCLK, pll1pclk, pll1qclk, AUDIOCLK (external)	
USB FS(1)	N/A	pll1pclk
RNG	HSI16, lsesys, LSI, pll1qclk/2	
ADC4	HSI16, HCLK1, SYSCLK, HSE, pll1pclk	
CPU system timer	lsesys, LSI, HCLK1/8	HSI16/4, lsesys, LSI, HCLK1/8
GPIOx (x = A, B, C, H)	HCLK2	
COMP	PCLK7	N/A
PKA	HCLK2	
AES	HCLK2	
TSC	HCLK1	N/A
CRC	HCLK1	
RCC AUDIO synchronization	pll1pclk, pll1qclk	

8.8.9 System clock after wake-up

This system clock used after wake-up in STM32WBA5 and STM32WBA2 series is the same. The STM32WBA2 new low-power modes have been added.

Table 37. System source after wake-up in STM32WBA5 and STM32WBA2 series

Power mode	STM32WBA5	STM32WBA2
Sleep	Same clock as before entering Sleep mode	
Stop0, Stop 1	HSI16 at 16 MHz	
Stop2, Stop 3	N/A	HSI16 at 16 MHz
Standby retention, Standby	HSI16 at 16 MHz	

8.8.10 Autonomous peripheral mode

The STM32WBA5 and STM32WBA2 series embed the same autonomous peripheral modes.

For STM32WBA5, some peripherals support an autonomous mode in Stop 0 and Stop 1 modes:

- Autonomous peripheral scan generate a kernel clock request and a bus clockrequest when needed, even in Stop mode.
- The selected oscillator is woken up.
- In autonomous mode with DMA, the bus clocks as well as the oscillator (HSI16) are automatically switched off as soon as the transfer is finished. The device automatically goes back to the selected low-power mode.
- If the autonomous peripheral is configured with interrupt enabled, the interrupt wakes up the device into Run mode.

Furthermore, the following capabilities exist in Stop mode when needed:

- If USARTs, LPUARTs and I2C selected HSI16 as kernel clock source for, it can be enabled by these peripherals in Stop 0 or Stop 1 mode.
- The LSE can remain always ON in Stop mode, with no on-the-fly activation capability, when it drives USARTs, LPUARTs, LPTIMs.

In STM32WBA2 series microcontrollers, some peripherals support autonomous mode also in Stop 2. In Stop 3 there are no autonomous peripherals.

The table below lists the main features of the autonomous mode supported by the STM32WBA5 and STM32WBA2 series.

Table 38. Autonomous peripherals in STM32WBA5 and STM32WBA2 series

Feature	STM32WBA5	STM32WBA2
Stop 0 and Stop 1 retained peripherals	Autonomous peripherals in Stop 0 and Stop 1 modes only Enabled if both xxEN and xxSMEN bits of the peripheral are set (xx = instance name) (GP/LP) DMA1 is associated. SRAM1, SRAM2 are associated.	
Stop 2 retained peripherals	-	Autonomous peripherals in Stop 2 modes Enabled if both xxEN and xxSMEN bits of the peripheral are set (xx = instance name) Autonomous peripherals mapped on AHB4 or APB7 No DMA association.
Autonomous peripherals in Stop 0 and Stop 1	USART1	
	USART2	N/A
	LPUART1	
	SPI1	N/A
	SPI3	
	I2Cx (x = 1, 3)	
	LPTIMx (x = 1, 2)	
	ADC4	
	GPDMA1	LPDMA
	N/A	LPUART1
	N/A	SPI3
	N/A	I2C3
	N/A	LPTIM1
	N/A	None
Autonomous peripheral requesting its kernel clock in Stop	If the peripheral kernel clock request selects HSI16, the internal oscillator (HSI16) is woken up if it was off. The kernel clock is propagated only to the peripherals requesting it.	

Feature	STM32WBA5	STM32WBA2
	When all peripheral kernel clock requests selecting HSI16 are released, the HSI16 is switched off.	
Autonomous peripheral requesting its bus clock in Stop 0 or Stop 1 mode	Stop 0 mode is entered. The internal oscillator (HSI16) is woken up if it was off. The system clock is propagated to all peripherals configured with both xxEN and xxSMEN bits set. When all peripherals release their bus clock request, the system clock is stopped, and if also all peripheral kernel clock requests selecting HSI16 are released, the HSI16 is switched off.	
Forcing HSI16 ON in Stop mode	Can be done by configuring HSIKERON. The oscillator is propagated only to the kernel clock of the enabled autonomous peripherals with this oscillator selected as kernel clock. This allows the peripheral baud rates or conversion rates increase, as there is no need to wait for the oscillator wake-up time when the peripheral requests its kernel clock.	
LSE or LSI as kernel clock	The LSE or LSI selected as peripheral kernel clock remains always ON in Stop mode.	

8.8.11 Operating modes

The table below lists the main operating modes and main clock sources of STM32WBA5 and STM32WBA2 series.

Table 39. Operating modes in STM32WBA5 and STM32WBA2 series

Feature	STM32WBA5	STM32WBA2
Run	CPU running System clock active on PLL, HSI16 or HSE. Peripheral bus and kernel clocks can be disabled by software.	
Sleep mode	Stops the CPU hclk clock. The memory interface clocks can be stopped by software during Sleep mode. AHB to APB bridge clocks are disabled by hardware during Sleep mode, when all the clocks of the peripherals connected to them are disabled.	
Stop 0 mode	Stop the system clock when there is no autonomous peripheral bus clock request. Disable the PLL. Disable HSI16, HSE oscillators when not requested by an autonomous peripheral.	
Stop 1 mode	Stop the system clock. Disable the PLL and HSE oscillator. Disable HSI16 when not requested by an autonomous peripheral.	
Stop 2 mode	N/A	Stop the system clock. Disable the PLL and HSE oscillator. Disable HSI16 when not requested by an autonomous peripheral.
Stop 3 mode	N/A	Stop the system clock. Disable the PLL and HSI16, HSE oscillators. No autonomous peripheral. Stop LSE and LSI clock in V_{core} domain.
Standby modes	Stop the system clock. Disable the PLLs and HSI16, HSE oscillators.	

Feature	STM32WBA5	STM32WBA2
LSE or LSI oscillators	Remain active in Stop mode and Standby mode.	
Low-power modes and memory/bus operation	If a flash memory programming operation is ongoing, Stop or Standby mode entry is delayed until the flash memory interface access is finished. If an access to the APB domain is ongoing, Stop or Standby mode entry is delayed until the APB access is finished.	

8.8.12 RCC security and privilege functional description

When the TrustZone® security is activated, the RCC can secure RCC configuration and status bits from being modified by nonsecure accesses. The RCC_SECCFGR register is used in both STM32WBA5 and STM32WBA2 series to prevent nonsecure access to read or modify the items listed in the table below.

The security configuration bits in RCC_SECCFGR are the same in STM32WBA5 and STM32WBA2 series.

Table 40. Secured RCC items in STM32WBA5 and STM32WBA2 series

Feature	STM32WBA5	STM32WBA2
Clock sources configuration and status bits	HSE, HSECSS, HSI16, LSI, LSE, LSECSS	
PLL, AHB and APB prescaler configuration and status bits	PLL1,AHB, and APB	
System and independent clocks	SYSCLK, systick	
Clock out capability	MCO and LSCO	
Remove reset flag settings	RMVF	

8.8.13 RCC privilege protection modes

In STM32WBA5 and STM32WBA2 series, there are the same dedicated register bits for privileged and unprivileged access: RCC_PRIVCFGR (SPRIV and NSPRIV bits).

By default, after a reset, all RCC registers can be read or written with privileged and unprivileged access, except RCC_PRIVCFGR that can be written with privileged access only.

8.9 Power (PWR)

The STM32WBA5 and STM32WBA2 series have the same PWR features, except:

- the following STM32WBA2 features, not available in STM32WBA5:
  - Stop 2 and Stop 3 modes
  - USB (only available from STM32WBA25xx devices)

8.9.1 Power-supply pins

The STM32WBA5 and STM32WBA2 series have the same power supplies. The STM32WBA2 supports some additional supply pins. The table below list the differences between STM32WBA5 and STM32WBA2 supply pins.

Table 41. Power-supply pins in STM32WBA5 and STM32WBA2 series

Pin name	
STM32WBA5	STM32WBA2
VDD	
N/A	VDDUSB(1)
VDDA	
VDDSMPS(2)	
VLXSMPS(2)	

Pin name	
STM32WBA5	STM32WBA2
VSSSMPS(2)	
VDD11(2), VCAP(3)	
VDDRF	
VDDRFPA	
VDDANA(2)	
VDDHPA	
VSSRF	
VSSA	
VSS	

1. *Only available on STM32WBA25xx devices.*
2. *Only available on STM32WBA23x/25xx devices.*
3. *Only available on STM32WBA23xx devices.*

The table below details pins that are specific to low-power modes.

Table 42. Specific pins in STM32WBA5 and STM32WBA2 series

Pin name	STM32WBA5	STM32WBA2
WKUPx	WKUPx (x = 1 to 8) input interrupt and wake-up pins Up to 16 multiplexed interrupt and wake-up pins from Run, Sleep, Stop, and Standby modes	WKUPx (x = 1 to 4 and 6 to 8) input interrupt and wake-up pins Up to 11 multiplexed interrupt and wake-up pins from Run, Sleep, Stop, and Standby modes
CSLEEP	CSLEEP output MCU in Sleep mode	
CSTOP	CDSTOP output CPU domain in Stop mode	

8.9.2 Power modes

The STM32WBA5 and STM32WBA2 series support the same low-power modes. The STM32WBA2 in addition supports a Stop 2 and Stop 3 mode. The table below shows the related STM32WBA2 series power modes compared to those in STM32WBA5.

The STM32WBA5 and STM32WBA2 series support the same low-power modes. The STM32WBA2 in addition supports a Stop 2 and Stop 3 mode. The table below shows the related STM32WBA2 series power modes compared to those in STM32WBA5.

Table 43. Power modes in STM32WBA5 and STM32WBA2 series

Power mode	STM32WBA5	STM32WBA2
Run mode	Run voltage scaling range 1	
	N/A	Run voltage scaling range 1.5
	Run voltage scaling range 2	
Sleep	Sleep voltage scaling range 1 (entered from Run voltage range 1)	
	N/A	Sleep voltage scaling range 1.5 (entered from Run voltage range 1.5)
	Sleep voltage scaling range 2 (entered from Run voltage range 2)	
Stop	SRAM pages can be powered down in Stop modes	
	Stop 0 voltage scaling range 1 (entered from Run voltage range 1)	

Power mode	STM32WBA5	STM32WBA2
Stop	N/A	Stop 0 voltage scaling range 1.5 (entered from Run voltage range 1.5)
	Stop 0 voltage scaling range 2 (entered from Run voltage range 2)	
	Stop 1	
	N/A	Stop 2
		Stop 3
Standby retention	SRAM pages, 2.4 GHz RADIO RAMS, and sleep timer can be retained in Standby mode	
	RTC/TAMP is retained Standby mode	RTC/TAMP can be retained in Standby mode
Standby	RTC/TAMP is retained Standby mode	N/A
	IWDG is retained in Standby mode	

8.9.3 Peripheral power migration

The STM32WBA2 series peripheral power management provides the same features as the STM32WBA5. The PWR register mapping has been kept the same in the STM32WBA2 series compared to the STM32WBA5. The STM32WBA2 new peripherals power management has been added to the PWR register map.

Table 44. Peripheral power in STM32WBA5 and STM32WBA2 series

Peripheral	STM32WBA5	STM32WBA2
Low-power flags	STOPF	
	N/A	STOP2F
	SBF	
USB FS supply(1)	N/A	USV
SRAM1 retention	R1RSB1, SRAM1PDS1	
SRAM2 retention	R2RSB1, SRAM2PDS1	
	N/A	R2RSB2, SRAM2PDS2
ICACHE RAM retention	ICRAMPDS	N/A
PKA RAM retention	N/A	PKARAMPDS
2.4 GHz RADIO retention	RADIORSB	
Stop 2 mode PTA signals state retention	N/A	PTASREN, PTASR
Standby mode GPIO state retention	GPIO PA[15:5,2:0]: IORETEN, IORET	
	GPIO PA[4:3]: IORETEN, IORET	N/A
	GPIO PB[15,12,9:8,6:2]: IORETEN, IORET	
	GPIO PB[14:13,10,7,1:0]: IORETEN, IORET	N/A
	GPIO PC[15:13]: IORETEN, IORET	
	GPIO PH[3]: IORETEN, IORET	

1. *Only available on STM32WBA25xx.*

8.9.4 PWR security and privilege

When the TrustZone® security is activated, the PWR can secure PWR configuration and status bits from being modified by nonsecure accesses. The PWR_SECCFGR register is used in both STM32WBA5 and STM32WBA2 series to prevent nonsecure access to read or modify the items listed in the table below.

The security configuration bits in PWR_SECCFGR are the same in STM32WBA5 and STM32WBA2 series.

Table 45. Secured RCC items in STM32WBA5 and STM32WBA2 series

Feature	STM32WBA5	STM32WBA2
Low-power mode configuration and status bits	SRAM RSB and DS bits, RADIORSB, LPMS, FLASHFWU, CSSF	
Voltage detection	PVDLS, PVDE, FSTEN, REGSEL	
Backup domain	DBP	
Wake-up pin	WUP	

In STM32WBA5 and STM32WBA2 series, there are the same dedicated register bits for privileged and unprivileged access: PWR_PRIVCFGR (SPRIV and NSPRIV bits).

By default, after a reset, all PWR registers can be read or written with privileged and unprivileged access, except PWR_PRIVCFGR that can be written with privileged access only.

8.9.5 PWR interrupts

The power interrupts sources of the STM32WBA5 and STM32WBA2 series are listed in the table below.

Table 46. PWR interrupt sources of STM32WBA5 and STM32WBA2 series

Interrupt vector	Description	Event flag	STM32WBA5	STM32WBA2
PWR_WKUP	Wake-up pin interrupt	WUFx (x = 1 to 4 and 6 to 8)	16 pins	11 pins
PWR_WKUPS	Wake-up pin secure interrupt			
PWR_WKUP	Wake-up pin interrupt	WUF5		N/A
PWR_WKUPS	Wake-up pin secure interrupt			
PVD_PVM	Programmable voltage detector	PVDO	EXTI line 16	

8.10 CRC

The CRC architecture is the same in STM32WBA5 and STM32WBA2 series, with the same features.

9 Migration of timer peripherals

The STM32WBA5 and STM32WBA2 series embed the same timers with the same features. The STM32WBA2 new timers and features have been added.

9.1 Advanced-control timers (TIM1)

The STM32WBA5 series embed one advanced-control timers, TIM1. There is no advanced-control timer in STM32WBA2 series.

9.2 GP timers with up, down, up-down auto-reload counter (TIM2/3)

The general-purpose timers consist of a 16-bit or 32-bit auto-reload counter driven by a programmable prescaler. The STM32WBA5 and STM32WBA2 series embed the same general-purpose timer TIM2 with identical features. Additional STM32WBA5 embeds TIM3.

The STM32WBA5 and STM32WBA2 series AF pins of general-purpose timers TIM2/3 are mapped as described in the table below.

Table 47. TIM2/3 AF pins on STM32WBA5 and STM32WBA2 series

AF pin	STM32WBA5	STM32WBA2
TIM2_ETR	PA5, PB6, PB12	
TIM2_CH1	PA5, PB6, PB12	
TIM2_CH2	PA8	
TIM2_CH3	PA7	
TIM2_CH4	PA6	
TIM3_ETR	PA0, PB8, PB12	N/A
TIM3_CH1	PA2, PA10, PB5	
TIM3_CH2	PA1, PA9	
TIM3_CH3	PA0, PB14	
TIM3_CH4	PB9, PB13	

9.3 GP timers with auto-reload up-counter (TIM16/17)

The STM32WBA5 and STM32WBA2 series embed the same two 16-bit resolution general-purpose timers with a 16-bit auto-reload up-counter (TIM16 and TIM17) with identical features.

The STM32WBA5 and STM32WBA2 series AF pins of general-purpose timers TIM16/17 are mapped as described in the table below.

Table 48. TIM16/17AF pins on STM32WBA5 and STM32WBA2 series

AF pin	STM32WBA5	STM32WBA2
TIM16_BKIN	PB15	
	PB10	N/A
TIM16_CH1	PA2, PB9	
	PA4	N/A
TIM16_CH1N	PB8	
	PA3	N/A
TIM17_BKIN	PA15	
TIM17_CH1	PA1, PB4	
TIM17_CH1N	PB3	

9.4 Low-power timers (LPTIM1/2)

The STM32WBA5 and STM32WBA2 series embed the same two 16-bit resolution low-power timers with a 16-bit auto-reload up-counter (LPTIM1 and LPTIM2) with identical features.

The STM32WBA5 and STM32WBA2 series AF pins of low-power timers LPTIM1/2 are mapped as described in the table below.

Table 49. LPTIM1/2AF pins on STM32WBA5 and STM32WBA2 series

AF pin	STM32WBA5	STM32WBA2
LPTIM1_ETR	PB8	
	PB11	N/A
LPTIM1_CH1	PB11	N/A
	N/A	PA12
LPTIM1_CH2	PA8, PA15	
LPTIM1_IN1	PA0	
LPTIM1_IN2	PB3	
LPTIM2_ETR	PA5	
LPTIM2_CH1	PA11	
	N/A	PA2
LPTIM2_CH2	PA1	
LPTIM2_IN1	PB9	
LPTIM2_IN2	PB4	
	PB0	N/A

9.5 Watchdogs

The STM32WBA5 and STM32WBA2 series embed the same IWDG watchdogs. Additional STM32WBA5 embeds WWDG:

- a system window watchdog (WWDG) (only in STM32WBA5)
- an independent watchdog (IWDG) with same features

9.6 Real-time clock (RTC)

The STM32WBA5 and STM32WBA2 series embed the same the same RTC with the same features. In STM32WBA5 the RTC is operational in all power modes. In STM32WBA2 the RTC is only operational in Run, Stop 0, Stop 1, Stop 2, and Standby retention modes.

Table 50. RTC operation in STM32WBA5 and STM32WBA2 series

AF pin	STM32WBA5	STM32WBA2
Run	Operational	
Stop 0, Stop 1	Operational	
Stop 2	N/A	Operational
Stop 3		Not operational (retained)
Standby retention	Operational	
Standby	Operational	Not operational (powered down)

The STM32WBA5 series and STM32WBA2 AF pins of RTC are mapped as described in the table below.

Table 51. RTC AF pins in STM32WBA5 and STM32WBA2 series

AF pin	STM32WBA5	STM32WBA2
RTC_REFIN	PB14	PB9
RTC_TS	PC13	
RTC_OUT1	PC13	
RTC_OUT2	PB2	

9.7 SysTick timer

The STM32WBA5 and STM32WBA2 series Cortex®-M33 with TrustZone® embed two SysTick timers when TrustZone® is activated, but only one SysTick when TrustZone® is disabled.
The STM32WBA2 supports additional SysTick timer clock source.

Table 52. SysTick in STM32WBA5 and STM32WBA2 series

Feature	STM32WBA5	STM32WBA2
SysTick clock source	HCLK1 / 8	
	LSI	
	lsesys	
	N/A	HSI16 / 4

10 Migration of communication peripherals

10.1 Serial peripheral interface (SPI)

The STM32WBA5 and STM32WBA2 series embed the same SPI3 with identical features. Additional STM32WBA5 embeds SPI1.

The STM32WBA5 and STM32WBA2 series AF pins of SPI1/3 are mapped as described in the table below.

Table 53. SPI AF pins in STM32WBA5 and STM32WBA2 series

AF pin function	STM32WBA5	STM32WBA2
SPI1_MOSI	PA15	N/A
SPI1_MISO	PB3	
SPI1_SCK	PB4	
SPI1_NSS	PA12	
SPI1_RDY	PA1, PB12	
SPI3_MOSI	PB8	
	N/A	PA6, PA9
SPI3_MISO	PB9	
	N/A	PA7, PA10, PB4
SPI3_SCK	PA0	
	N/A	PA8
SPI3_NSS	PA5	
SPI3_RDY	PA6, PA8	

10.1.1 SPI autonomous mode

The SPI1 and SPI3 peripherals in STM32WBA5 series support autonomous operation down to Stop 1 mode.

The SPI3 peripheral in STM32WBA2 series supports autonomous operation down to Stop 2 mode.

10.2 I2C

The STM32WBA5 and STM32WBA2 series embed the same I2C1 and I2C3 with identical features.

The STM32WBA5 and STM32WBA2 series AF pins of I2CI1/3 are mapped as described in the table below.

Table 54. I2C AF pins in STM32WBA5 and STM32WBA2 series

AF pin function	STM32WBA5	STM32WBA2
I2C1_SCL	PA15, PB2	
I2C1_SDA	PB3	
	PB1	N/A
	N/A	PA11
I2C1_SMBA	PB15	
I2C3_SCL	PA6, PB2	
I2C3_SDA	PA7	
	PB1	N/A
	N/A	PA8, PA11
I2C3_SMBA	PB15	

10.3 U(S)ART and LPUART

The STM32WBA5 and STM32WBA2 series embed the same USART1, and LPUART1 with identical features. Additional STM32WBA5 embeds USART2.

The STM32WBA5 and STM32WBA2 series AF pins of USART1/2 and LPUART1 are mapped as described in the table below.

Table 55. U(S)ART/LPUART AF pins in STM32WBA5 and STM32WBA2 series

AF pin function	STM32WBA5	STM32WBA2
USART1_TX	PB12	
	PB14	N/A
	N/A	PA5, PA6, PB2
USART1_RX	PA8	
	N/A	PA7, PA9, PA12
USART1_CK	PA1, PA5	
	PB10	N/A
USART1_CTS	PA7	
	PA4	N/A
	N/A	PB4
USART1_RTS_DE	PA2, PA6	
	PA3	N/A
USART2_TX	PA12, PA14, PB0	N/A
USART2_RX	PA11, PB4, PB8	
USART2_CK	PB3	
USART2_CTS	PB12, PB15	
USART2_RTS_DE	PA15, PB1	
LPUART1_TX	PA2, PB5	
	PB11	N/A
	N/A	PH3
LPUART1_RX	PA1, PA10	
LPUART1_CTS	PA0, PB15	
	N/A	PB8
LPUART1_RTS	PA9, PB9	
	N/A	PH3, PA10

10.4 Serial-audio interface (SAI)

The STM32WBA5 and STM32WBA2 series embed the same SAI1 with identical features for block A. For block B STM32WBA2 only supports SD.

The STM32WBA5 and STM32WBA2 series AF pins of SAI1 are mapped as described in the table below.

Table 56. SAI AF pins in STM32WBA5 and STM32WBA2 series

AF pin function	STM32WBA5	STM32WBA2
SAI1_SD_A	PB12	
	PB14	N/A
	N/A	PA6

AF pin function	STM32WBA5	STM32WBA2
SAI1_FS_A	PA8	
SAI1_SCK_A	PA7	
	N/A	PA5
SAI1_MCLK_A	PA6	
SAI1_SD_B	PB7	N/A
	N/A	PA12
SAI1_FS_B	PB5	N/A
SAI1_SCK_B	PB6	N/A
SAI1_MCLK_B	PB4	N/A
SAI1_D1	PA2, PA10	
	N/A	PA8
SAI1_D2	PA5, PB5	
SAI1_CK1	PA1, PA9	
	N/A	PB4
SAI1_CK2	PA6	

10.5 Universal serial bus interface (USB)

The STM32WBA2 series USB full speed has been added.

The STM32WBA2 series AF pins of USB FS are mapped as described in the table below.

Note: USB FS is only available on STM32WBA25xx.

Table 57. USB pins in STM32WBA5 and STM32WBA2 devices

Pin name	STM32WBA5	STM32WBA25
USB_SOF	N/A	PA8
USB_NOE		PA13
USB_DM		PB9
USB_DP		PB8

11 Migration of analog peripherals

11.1 Analog-to-digital converter (ADC)

The STM32WBA5 and STM32WBA2 series embed the same 12-bit ADC4 with identical features. The STM32WBA2 series embeds fewer external channels.

The STM32WBA5 and STM32WBA2 series AF pins of ADC4 are mapped as described in the table below.

Table 58. ADC implementation in STM32WBA5 and STM32WBA2 devices

Features	STM32WBA5	STM32WBA2
ADC4_IN1	PA8	
ADC4_IN2	PA7	
ADC4_IN3	PA6	
ADC4_IN4	PA5	
ADC4_IN5	PA4	N/A
ADC4_IN6	PA3	N/A
ADC4_IN7	PA2	
ADC4_IN8	PA1	
ADC4_IN9	PA0	
ADC4_IN10	PB9	N/A

11.2 Comparator (COMP)

The STM32WBA5 series embed comparators COMP1 and COMP2.

The STM32WBA2 has no comparators.

12 Migration of signal processing accelerators

12.1 Touch sensing controller (TSC)

The STM32WBA5 series embed touch sensing controller TSC.

The STM32WBA2 series has no touch sensing controller.

13 Migration of external-memory interface peripherals

The STM32WBA2 series microcontrollers embeds an external memory interface XSPI.

13.1 Extended-SPI interface (XSPI)

The STM32WBA2 series embed an external memory interface XSPI1 with associated OTFDEC1 and DLYBXS1.
The STM32WBA5 series has no external memory interface.

Note: XSPI1 is only available on STM32WBA25xx.

Table 59. Extended-SPI implementation in STM32WBA5 and STM32WBA2 devices

Features	STM32WBA5	STM32WBA2
Quad-SPI	N/A	XSPI1
Feedback delay		DLYBXS1
OTFDEC		OTFDEC1
MPCWM		MPCWM1

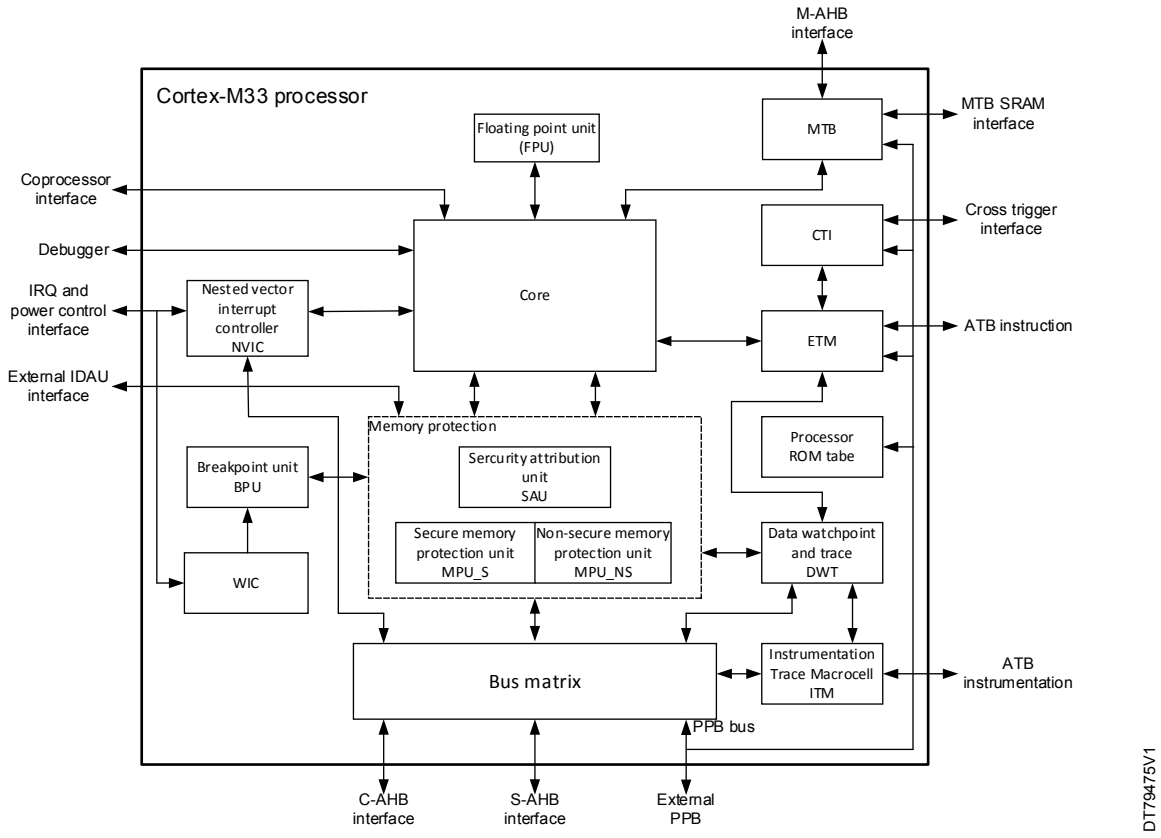
14 Software migration

14.1 Cortex®-M33 overview

The Cortex®-M33 processor is excellent in ultra-low-power, performance and security. This processor is based on the Armv8-M architecture for use in environments requiring more security implementation. The Cortex®-M33 core implements a full set of DSP (digital signal processing) instructions, TrustZone® aware support and a memory protection unit (MPU) that enhances application security.

The Cortex®-M33 core also features a single-precision floating-point unit (FPU), that supports all the Arm® single-precision data-processing instructions and all the data types. The STM32 Cortex®-M33 implementation is illustrated in the figure below.

Figure 6. STM32 Cortex-M33 implementation



Cortex®-M33 key features are listed below:

- Arm-v8 M architecture with 2/3 stage pipeline, Harvard, 1.5 DMIPS/MHz
- Single-cycle branch, no branch prediction
- Hardware divide instruction
- Debug (CoreSight compliant)
- Memory exclusive instructions
- NVIC without interrupts up to 68 (16 priority levels)
- Enhanced MPU, more flexible (32 bytes) up to 8 regions (for each one of the secure and nonsecure states)
- New AMBA® 5 AHB interface, support of security state extension to the system
- Support of external implementation defined attribution unit
- Fully compatible with TrustZone® system

14.2 Cortex®-M33 software point of view

The Cortex®-M33 includes the following features:

- Implementing Armv8-M architecture
- Implementing the latest FPU specification (based on Arm FPv5 architecture)
- Using the AHB5 specification for the system and memory interface to extend security across the whole system
- Using the latest version of the MPU specification for the setup of regions
- Optional execution trace using MTB or ETM
- Enhanced debug components to make simplify usage
- Hardware stack limit checking
- TrustZone® security features adding efficient security features

14.3 Cortex®-M33 mapping overview

The mapping on Cortex®-M33 is illustrated on the table below.

Table 60. Cortex®-M33 overview mapping for STM32WBA5 and STM32WBA2 series

Architecture		STM32WBA5	STM32WBA2
Core	NVIC (nested vectored interrupt controller), not including the 16 interrupt lines of the Cortex-M33 with FPU)	72	68
	EXTI (extended interrupts and events controller)	19	21
Mapping (base address)	ITM	0xE000 0000	
	DWT	0xE000 1000	
	BPU	0xE000 2000	
	SCS	0xE000 E000	
	System timer	0xE000 E010	
	NVIC	0xE000 E100	
	MPU	0xE000 ED90	
	FPU	0xE000 EF30	
	TPIU	0xE004 0000	
	ETM	N/A	0xE004 1000
	CTI	0xE004 2000	
	DBGMCU	0xE004 4000	
	Processor ROM table	0xE00F F000	

15 Conclusion

This application note is a complement to the STM32WBA5 and STM32WBA2 series datasheets and reference manuals. This document provides a simple guideline to migrate an existing product based on STM32WBA5 to the STM32WBA2 devices.

Revision history

Table 61. **Document revision history**

Date	Version	Changes
11-Feb-2026	1	Initial release.

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