How to design a transition mode PFC boost pre-regulator based on L6462A

Introduction

This application note describes the main steps to design a transition mode (TM) power factor corrector (PFC) boost pre-regulator based on the L6462A [1] controller.

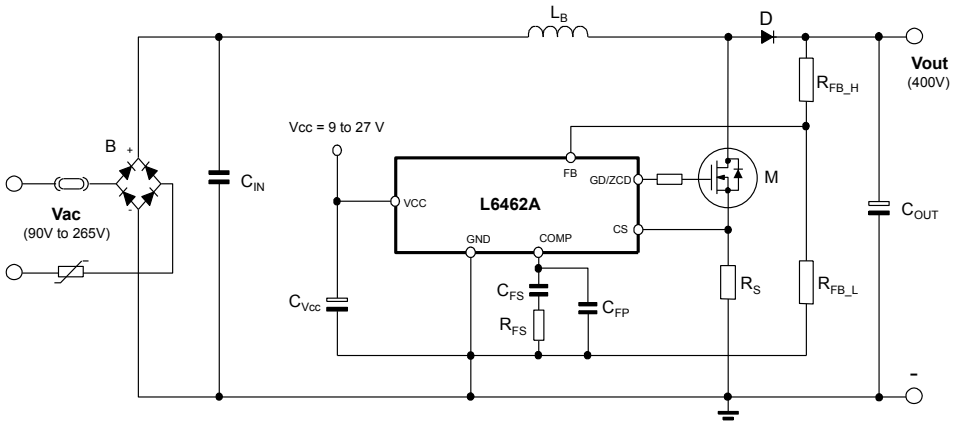
The L6462A is a control IC specifically designed for a PFC boost topology operating in TM with frequency reduction at medium-light load (valleys skipping), suitable for building cost-sensitive and energy efficient solutions.

It embeds a special implementation of current mode control that enables wide-range-mains operation with low THD over a broad load range with no need for input voltage sensing. A pair of internal special circuits (CRG and CRS circuit) shape the reference for the peak current of the inductor to maintain a sinusoidal input current regardless of converter's operation, whether TM or DCM (Discontinuous Conduction Mode). In this way it is possible to improve efficiency at intermediate and light loads with minimum impact on input current distortion.

The device at full load and low AC line synchronizes the turn-on of the power switch to the valley of the ringing following boost inductor's demagnetization (valley switching – quasi resonant operation). At high AC line and as the load is reduced, the IC skips ringing valleys to reduce the operating frequency progressively so that, though keeping valley switching, the converter operates in DCM to optimize the efficiency.

Boost inductor demagnetization sensing is done via the gate driver output (GD/ZCD multifunction pin); no auxiliary winding or other interface components are needed.

Figure 1. Typical application based on L6462A



1 Control technique

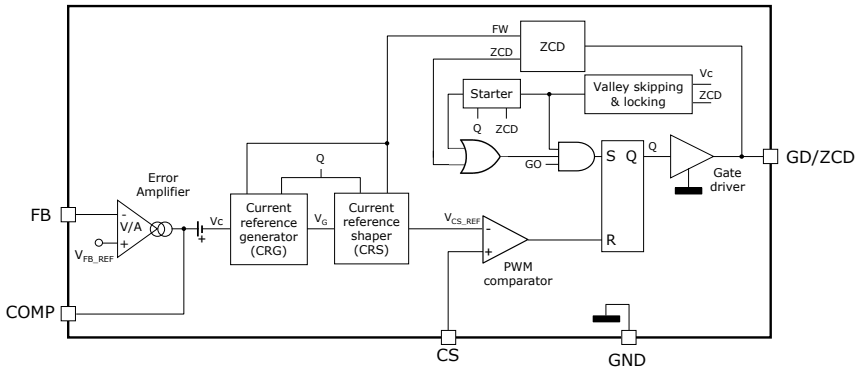
L6462A implements a peak-current mode control operating in TM/DCM (skipping the valleys) with valley turn-on as illustrated by the basic schematic in Figure 2.

Figure 3 and Figure 4 show the key waveforms both on the switching cycle time scale and on the line frequency time scale when the boost PFC works in TM. Figure 5 and Figure 6 the same when the Boost PFC converter works in DCM.

Considering the Figure 2, the basic turn-on and off mechanisms of the MOSFET are not different from those of the traditional current mode control method. Switching cycles (i.e., MOSFET's turn-on) can be initiated by either the ZCD (Zero current detector) block that senses boost inductor's demagnetization or by the Starter block when no signal is coming from the ZCD block. In steady-state operation, all cycles are initiated by the ZCD block by synchronizing them to the drain voltage reaching the valley of the ringing that occurs after demagnetization (valley switching).

The end of the ON-time of the power MOSFET is determined by comparing in the PWM comparator the signal on pin CS (that is a ramp proportional to the instantaneous inductor current $I_L(t,\theta)$) to the current reference $V_{CS\_REF}(\theta)$. When the two signals are equal a reset signal is given to the PWM latch and the power MOSFET is switched off.

Figure 2. Control loop connections



The trans-conductance Error Amplifier V/A compares a portion of the output voltage V_{OUT}, brought at its inverting input externally available on pin FB via the resistor divider R_{FB_H}-R_{FB_L}, with an accurate internal reference V_{FB_REF} (2.5 V typ.) connected to the non-inverting input, and generates an error signal V_C proportional to their difference. If the bandwidth of the error amplifier, essentially determined by the frequency compensation network connected between pin COMP and ground, is narrow enough – typically below 20 Hz – and a steady-state operation is assumed, the V_C error signal available at pin COMP can be regarded as a DC level, at least as a first approximation. Referring to the L6462A datasheet, the V_C voltage is then used by the CRG circuitry that, based also on the FW and Q signals, generates a voltage expressed by:

Equation 1

$$V_G(\theta) = K_1 \cdot V_C \cdot \frac{V_{IN}(\theta)}{V_{OUT}} \quad (1)$$

where K_1 is the circuitry gain (constant term) $V_{IN}(\theta) = |V_{AC}(\theta)| = V_{IN,pk} \cdot \sin\theta$ (with $0 \le \theta \le \pi$, as a result of the rectification operated by the input bridge) is the instantaneous line input voltage.

Equation (1) shows as the $V_G(\theta)$ voltage is proportional to the $V_{IN}(\theta)$ input voltage and to the V_C control voltage like in a standard current-mode PFC, but without using the standard multiplier block and without the AC line sensing.

The $V_G(\theta)$ voltage is then managed by the CRS circuitry that opportunely shapes the $V_G(\theta)$ voltage in order to achieve ideally sinusoidal input current. As reported in the L6462A datasheet [1], the resulting internal current reference voltage can be expressed by:

Equation 2

$$V_{CS\_REF}(\theta) = G_{CR} \cdot V_C \cdot \frac{T(\theta)}{T_{ON}(\theta) + T_{FW}(\theta)} \cdot \frac{V_{IN,pk}}{V_{OUT}} \cdot \sin\theta \quad (2)$$

where G_{CR} is the equivalent multiplier gain (see Electrical characteristics table in the L6462A datasheet for details), $T_{ON}(\theta)$ is the power switch on-time interval (Q=High), $T_{FW}(\theta)$ is the time interval while the boost inductor is demagnetizing (FW=High) and $T(\theta) = T_{ON}(\theta) + T_{FW}(\theta) + T_V$ is switching period (where T_V is the time interval while the boost inductor is fully demagnetized). It is wort noticing that when the converter operates in TM operation ($T_V \simeq 0$), the resulting current sense reference voltage is sinusoidal as in a standard TM PFC boost controller.

Figure 3. Key waveforms of the circuit in figure 1 in TM (valley switching) operation – Switching cycle time scale

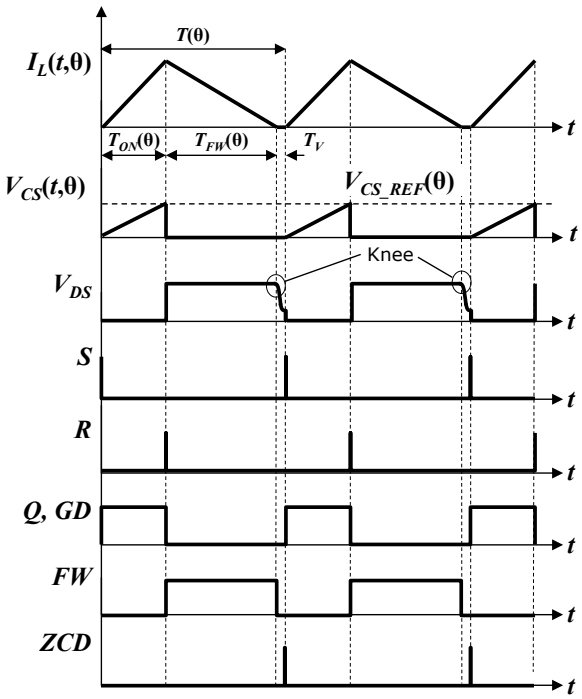
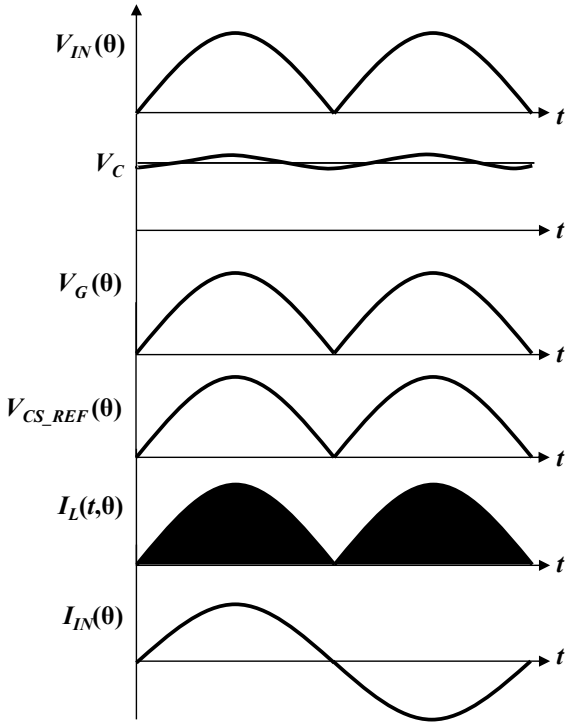


Figure 4. Key waveforms of the circuit in figure 1 in TM (valley switching) operation – Line cycle time scale



The internal current reference voltage $V_{CS\_REF}(\theta)$ is then compared with the current sense $V_{CS}(\theta)$ pin voltage, which is proportional to the inductor current through the current senser R_S resistor. Neglecting the mainly negative contribution of the ringing current to the average inductor current during T_V in DCM operation, the relationship between the peak value $I_{Lpk}(\theta)$ and the average value $I_L(\theta)$ of the inductor current in a switching cycle becomes:

Equation 3

$$I_L(\theta) = \frac{1}{2} \cdot \frac{T_{ON}(\theta) + T_{FW}(\theta)}{T(\theta)} \cdot I_{Lpk}(\theta). \quad (3)$$

Reminding that $I_{Lpk}(\theta) = V_{CS\_REF}(\theta) / Rs$, the resulting average inductor current and then input current $I_{IN}(\theta)$, is found from Equation (3) and Equation (2):

Equation 4

$$I_{IN}(\theta) = I_L(\theta) = \frac{1}{2} \cdot \frac{G_{CR}}{Rs} \cdot V_C \cdot \frac{V_{IN,pk}}{V_{OUT}} \cdot \sin\theta \quad (4)$$

which is sinusoidal and in phase with the $V_{IN}(\theta)$ input voltage (ideally zero-THD and unity-PF) regardless of whether the boost PFC converter works in TM or in DCM (valley skipping).

Figure 5. Key waveforms of the circuit in figure 1 in DCM operation with valley switching – Switching cycle time scale

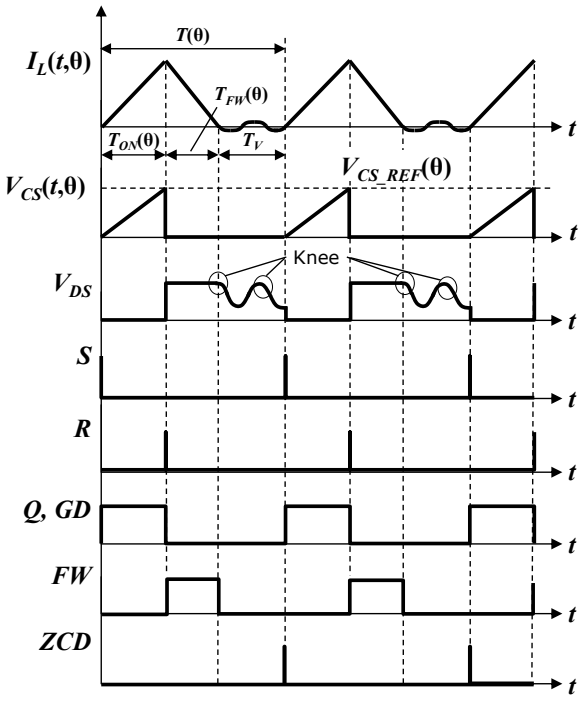
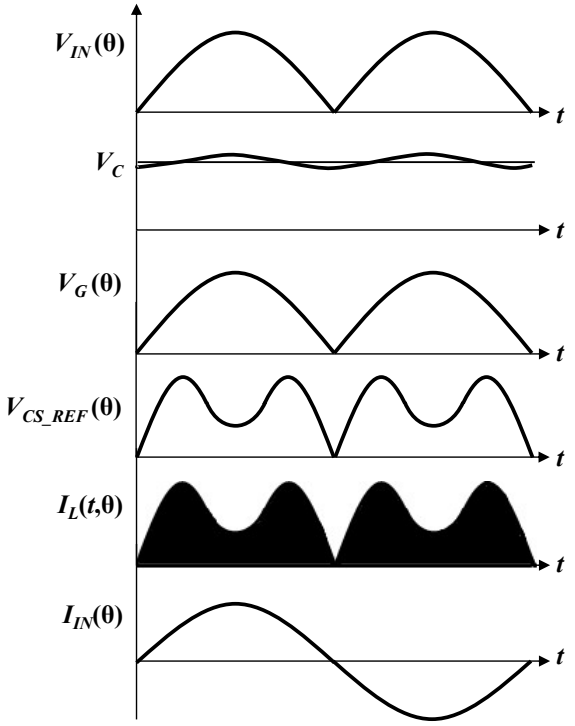


Figure 6. Key waveforms of the circuit in figure 1 in DCM operation with valley switching – Line cycle time scale



Finally, it is worth noticing that is possible to relate the control variable V_C to the operating conditions of the boost PFC converter (input voltage $V_{IN}(\theta)$ and output load) by multiplying Equation (4) by the input voltage $V_{IN}(\theta)$ thus determining the instantaneous input power Pin(θ):

Equation 5

$$P_{IN}(\theta) = V_{IN}(\theta) \cdot I_{IN}(\theta) = \frac{1}{2} \cdot \frac{G_{CR}}{Rs} \cdot V_C \cdot \frac{{V_{IN,pk}}^2}{V_{OUT}} \cdot \sin\theta^2 \quad (5)$$

which pulsates sinusoidally at $2 \cdot f_{line}$ from 0 to twice dc input power P_{IN}, which is found by averaging Equation (5) over a line half-cycle:

Finally, reminding that $P_{IN} = P_{OUT} / \eta$, solving Equation (6) for V_C results:

Equation 6

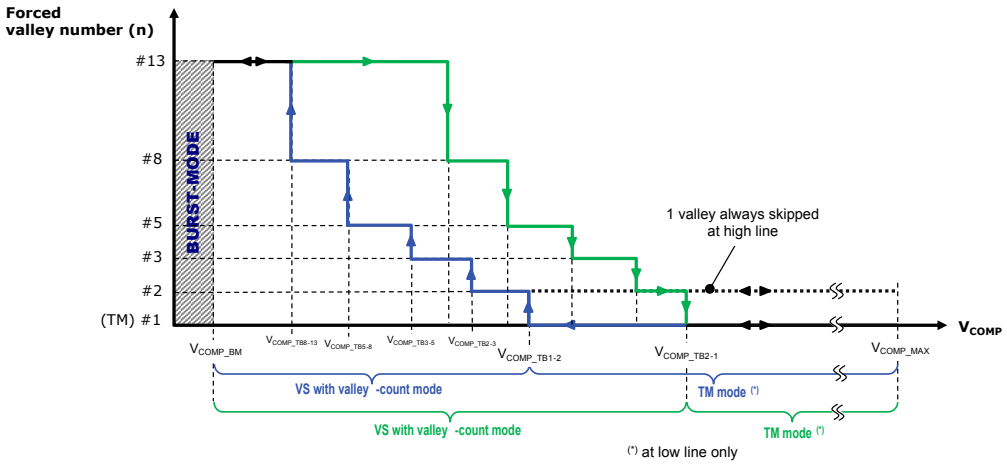
$$P_{IN} = \int_0^{\pi} V_{IN}(\theta) \cdot I_{IN}(\theta)\, d\theta = \frac{1}{4} \cdot \frac{G_{CR}}{Rs} \cdot V_C \cdot \frac{{V_{IN,pk}}^2}{V_{OUT}} \quad (6)$$

Equation 7

$$V_C = \frac{4 \cdot R_S}{G_{CR}} \cdot \frac{P_{OUT}}{\eta} \cdot \frac{V_{OUT}}{{V_{IN,pk}}^2} = \frac{2 \cdot R_S}{G_{CR}} \cdot \frac{P_{OUT}}{\eta} \cdot \frac{V_{OUT}}{{V_{IN,rms}}^2} \quad (7)$$

With TM operation, as the load decreases f_{SW} increases and a mechanism of frequency limitation and foldback is introduced in the L6462A to prevent f_{SW} from reaching too high values and efficiency from quickly dropping at medium/light load. Specifically, at low AC line, when V_{COMP} voltage is lower than the V_{COMP_TB1-2} threshold the turn-on of the MOSFET is no longer commanded on the first valley of the drain voltage ringing after the demagnetization but on n-th valley of the ringing. A “valley counter” based on the ZCD pulse detection is implemented and the number of skipped valleys (n-1) is increased in discrete steps progressively longer and longer as V_{COMP} gets lower and lower due to a load decrease, as shown in the diagram of Figure 7 (turn-on at valley number n=1, n=2, n=3, n=5, n=8, n=13). In this way, converter’s switching frequency is forced to increasingly lower values (Frequency foldback), thus also reducing all frequency-related losses. At high AC line, VS operation is always enabled regardless of V_{COMP} voltage. This reduces the THD of the input current by improving its shape close to the zero crossings of the line voltage (crossover distortion) and may slightly improve efficiency as well.

Figure 7. Turn-on valley number (n) vs. V_{COMP} map



***Note**: to avoid unwanted valleys jump, the ripple on COMP pin has to be lower than the valley skipping hysteresis thresholds (200mV typ., see L6462A datasheet). This can be easily guaranteed selecting the appropriate compensation networks (C_{FP} capacitor value). See Section 2.3 paragraph for more details.*

2 L6462A biasing circuitry

In the following section is described the selection of the components around the L6462A.

2.1 Output voltage divider resistors

In steady-state condition the FB pin is equal to the internal voltage reference V_{REF}, so the programmed output voltage V_{OUT} results:

Equation 8

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{FB\_H}}{R_{FB\_L}}\right) \quad (8)$$

where the upper resistor R_{FB_H} can be selected based on the maximum power dissipation P_d of the resistor divider network:

Equation 9

$$R_{FB\_H} \cong \frac{{V_{OUT}}^2}{P_d} \quad (9)$$

Typical value of R_{FB_H} resistor (which is typically composed by a series of resistors to sustain the high voltage drop V_{OUT}) in the range of 5-15 mW to limit the power dissipation P_d at few tens mW.

The R_{FB_L} resistor is then selected based on the desiderated output voltage V_{OUT}:

Equation 10

$$R_{FB\_L} = R_{FB\_H} \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}} \quad (10)$$

2.2 Current sense resistor

The current sense circuitry, which is typically composed by the parallel of two or more resistor (film or SMD type) to sustain own power dissipation, is placed in series to power MOSFET source and its equivalent resistor value R_S has to be opportunely selected to handle the maximum output power (P_{OUT_MAX}) also in the worst-case condition (e.g. at minimum input rms voltage $V_{AC,min}$). In particular, the R_S resistor value impacts on the voltage dynamics of pin CS and pin COMP.

Referring to the datasheet, the controller embeds an over current comparator OCP1 that limits the peak inductor current implementing a cycle-by-cycle over current protection. To maximize the dynamic of the CS voltage pin, the OCP1 is typically selected equal to the maximum output load considering the worst-case condition (minimum input voltage, minimum overcurrent internal threshold):

Equation 11

$$R_{S\_OCP1} = V_{CS\_OCP1,min} \cdot \frac{\eta \cdot V_{AC,min} \cdot PF}{2\sqrt{2} \cdot P_{OUT,max}} \quad (11)$$

where V_{CS_OCP1} is the internal over current threshold, h the estimated converter's efficiency and PF the expected power factor.

Considering Equation (7) and considering that the COMP pin voltage is V_C + 0.3 V (typ), the resulting current resistor that guarantee the respect of the dynamic of the pin COMP (e.g. voltage lower than the minimum upper saturation voltage $V_{COMP,min}$) is:

Equation 12

$$R_{S\_COMP} = \left(V_{COMP,min} - 0.3\right) \cdot \frac{G_{CR,min}}{2} \cdot \frac{\eta}{P_{OUT\_max}} \cdot \frac{{V_{AC,min}}^2}{V_{OUT}} \quad (12)$$

To guarantee both the previous two conditions, the current sense resistor R_S has to be selected equal or lower than the minimum:

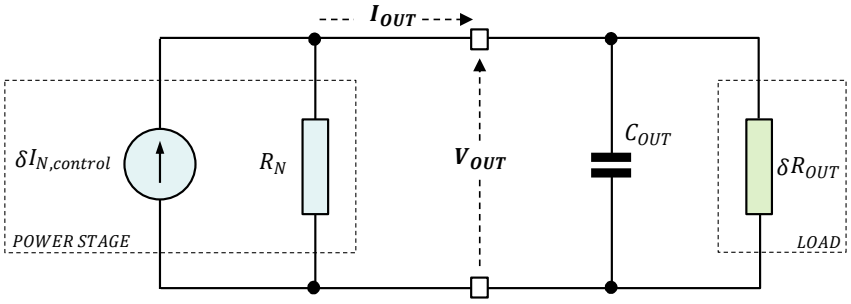
Equation 13

$$R_S = min\left(R_{S\_OCP1}, R_{S\_COMP}\right) \quad (13)$$

2.3 Compensation network

Figure 8 shows the small signal model of the PFC converter, where the power stage has been represented with the equivalent Norton circuit and the ESR (Equivalent Series Resistance) of the output capacitor has been neglected (cross over frequency fc of the PFC converter is much lower than ESR frequency zero $f_{z\_ESR} = 1 / 2\,\pi \cdot ESR \cdot C_{OUT}$).

Figure 8. Small signal model of the PFC converter



Considering Equation (7) and considering that $P_{OUT} = V_{OUT} * I_{OUT}$, the large signal control-to-output transfer function of the PFC converter based on the L6462A is:

Equation 14

$$I_{OUT} = V_C \cdot \frac{G_{CR}}{4\,R_s} \cdot \cdot \frac{{V_{IN,pk}}^2}{{V_{OUT}}^2} \quad (14)$$

and then the equivalent Norton current generator results:

Equation 15

$$\delta I_N = \delta V_C \frac{\partial I_{OUT}}{\partial V_C} = \delta V_C \frac{G_{CR}}{4\,R_s} \cdot \eta \cdot \frac{{V_{IN,pk}}^2}{{V_{OUT}}^2} \quad (15)$$

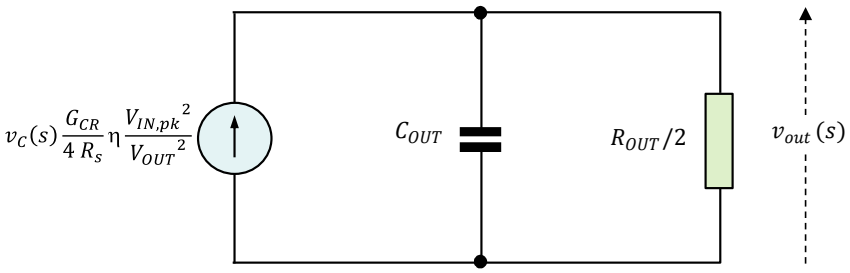
Still starting from Equation 14, the equivalent Norton resistor results:

Equation 16

$$R_N = -\frac{\partial V_{OUT}}{\partial I_{OUT}} = \frac{R_{OUT}}{2} \quad (16)$$

It is interesting to note that the equivalent Norton resistance is lower than in a standard multiplier-based PFC converter where R_N=R_{OUT}. Figure 9 shows the equivalent small-signal model of the converters in the Laplace domain, assuming as output load a DC-DC converter: in this case the equivalent load resistance δR_{OUT} is negative and equal to the R_{OUT} that is the equivalent large signal load resistance $\delta R_{OUT} = -R_{OUT} = -V_{OUT}/I_{OUT}$. As a result the equivalent output resistance is $R_{OUT}/2$ (R_N //-R_{OUT}).

Figure 9. Small signal model – control-to-output transfer function.



The control-to-output transfer function results:

Equation 17

$$G_{co}(s) = \frac{v_{out}(s)}{v_c(s)} = \frac{G_{CR}}{4\,R_s} \cdot \eta \cdot \frac{V_{IN,pk}{}^2}{V_{OUT}{}^2} \cdot \frac{R_{OUT}}{1 + s \cdot R_{OUT} \cdot C_{OUT}} \quad (17)$$

where it is interesting to note that the frequency pole $f_{p\_co} = 1 / 2\,\pi\,R_{OUT}\,C_{OUT}$ depends on the load condition and the low-frequency gain depends on input/output voltage set-points. The previous equation can be rewritten in the form:

Equation 18

$$G_{co}(s) = \frac{G_o}{1 + s \cdot t_{p\_co}} \quad (18)$$

where $G_o = \frac{G_{CR}}{4\,R_s} \cdot \eta \cdot \frac{V_{IN,pk}{}^2}{V_{OUT}{}^2} \cdot R_{OUT}$, $t_{p\_co} = R_{OUT} . C_{OUT}$

The control loop compensation network (composed by the R_{FS}, C_{FS}, C_{FP} components) is placed between the COMP pin and GND as shown in Figure 10, and the transfer function is:

Equation 19

$$H(s) = \frac{v_c(s)}{v_{out}(s)} = g_{m\_EA} \cdot \frac{R_{FB\_L}}{R_{FB\_L} + R_{FB\_H}} \cdot \frac{1}{s \cdot (C_{FS} + C_{FP})} \cdot \frac{1 + s \cdot R_{FS} \cdot C_{FS}}{1 + s \cdot R_{FS} \cdot \left(\frac{C_{FS} \cdot C_{FP}}{C_{FS} + C_{FP}}\right)} \quad (19)$$

that can be rewritten in the form:

Equation 20

$$H(s) = \frac{H_o}{s} \cdot \frac{1 + s \cdot t_z}{1 + s \cdot t_p} \quad (20)$$

where $H_o = \frac{g_{m\_EA} \cdot R_{FB\_L}}{\left(R_{FB_L} + R_{FB_H}\right)\left(C_{FS} + C_{FP}\right)}$, $t_z = R_{FS} \cdot C_{FS}$, $t_p = R_{FS} \cdot \frac{C_{FS}\,C_{FP}}{C_{FS} + C_{FP}}$

Equation (20) shows as the transfer function introduces two poles (one in the origin to achieve the DC output regulation) and one zero. It shows also that the compensation network transfer function has a non-zero gain at the second harmonic of the line frequency ($2 * f_{LINE}$) and this introduce a third-harmonic distortion of the current reference. In other words, the output voltage ripple ΔV_{OUT} ($2 * f_{LINE}$) is not eliminated by the compensation network and so its present at the COMP pin voltage ($\Delta V_{COMP} = \Delta V_{OUT} \cdot |H(j\,2\pi \cdot (2 \cdot f_{LINE})| = \Delta V_{OUT} \cdot H_{2f}$) introducing a distortion of the current reference V_{CS_REF}. Considering that the output voltage ripple (peak-to-peak) is:

Equation 21

$$\Delta V_{OUT} = \frac{I_{OUT}}{2\pi \cdot f_{LINE} \cdot C_{OUT}} \quad (21)$$

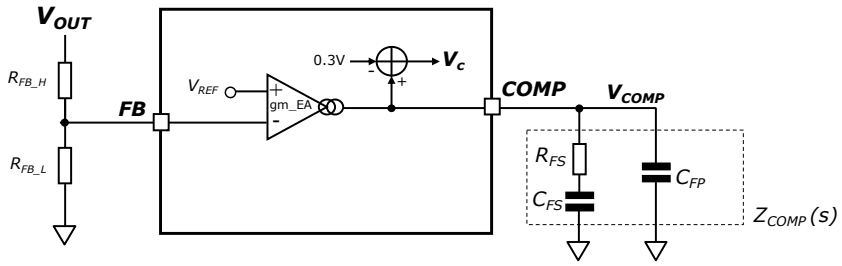
it is possible to demonstrate that the third-harmonic distortion of the current reference is given with a good approximation by:

Equation 22

$$D_3 = \frac{1}{2} \cdot \frac{\frac{\Delta V_{COMP}}{2}}{V_{COMP} - V_{C0}} = \frac{1}{2} \cdot \frac{\frac{\Delta V_{OUT}}{2} \cdot H_{2f}}{V_{COMP} - V_{C0}} \quad (22)$$

where V_{C0} is the “zero-power” level of the control voltage (V_{C0} = 0.3 V)

Figure 10. Small signal model – control-to-output transfer function



The open loop transfer function then results:

Equation 23

$$F(s) = G_{co}(s) \cdot H(s) = \frac{G_o}{1 + s \cdot t_{p\_co}} \frac{H_o}{s} \cdot \frac{1 + s \cdot t_z}{1 + s \cdot t_p} \quad (23)$$

and considering that s=jω, it can be rewritten in the form:

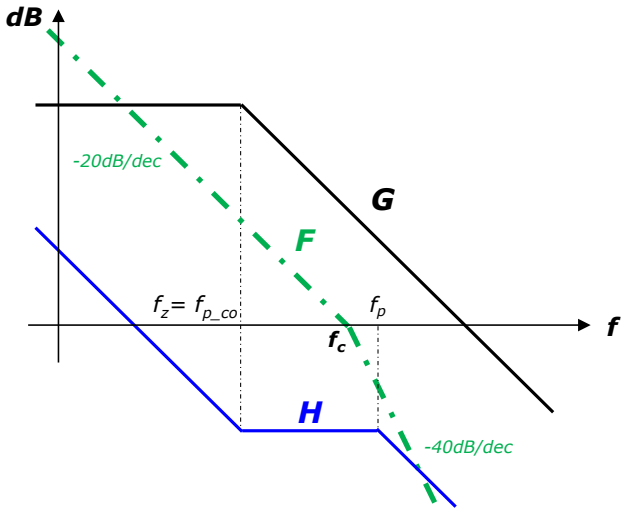
Equation 24

$$F(j\omega) = \frac{G_o \cdot H_o}{j\omega} \cdot \frac{1}{1 + \frac{j\omega}{2\pi \cdot f_{p\_co}}} \cdot \frac{1 + \frac{j\omega}{2\pi \cdot f_z}}{1 + \frac{j\omega}{2\pi \cdot f_p}} \quad (24)$$

To achieve a good closed-loop stability and THD performance, the compensation network is then designed using the following rules:

- f_z=f_{p_co}, to compensate the pole of the control-to-output transfer function and achieve the system stability.
- $H_{2f} = \frac{2 \cdot D_3 \cdot (V_{COMP} - V_{C0})}{\Delta V_{OUT}/2}$, to set the maximum third-harmonic distortion D_3% (at the maximum input voltage condition).
- f_p position to achieve the desiderated phase-margin (F_m).

Figure 11. **Asymptotic Bode Diagram - module**



Based on the previous considerations, and assuming C_{FP}<<C_{FS}, the suggested compensation network results:

Equation 25

$$H_{2f} = \frac{2 \cdot D_3 \cdot (V_{COMP} - V_{Co})}{\Delta V_{OUT}/2} = \frac{2 \cdot D_3 \cdot V_C}{\Delta V_{OUT}/2} \quad (25)$$

Equation 26

$$f_z = f_{p\_co} = \frac{1}{2\,\pi \cdot R_{OUT} \cdot C_{OUT}} \quad (26)$$

Equation 27

$$f_p = \sqrt{\frac{f_z \cdot 2\,f_{LINE} \cdot H_{2f} \cdot G_o \cdot tan\left(\frac{\pi}{180} \cdot \phi_m\right)}{\sqrt{1 + \frac{1}{\left(tan\left(\frac{\pi}{180} \cdot \phi_m\right)\right)^2}}}} \quad (27)$$

Equation 28

$$C_{FP} = \frac{g_{m\_EA} \cdot R_{FB\_L}}{R_{FB\_L} + R_{FB\_H}} \cdot \frac{1}{2\pi \cdot 2f_{LINE} \cdot H_{2f}} \quad (28)$$

Equation 29

$$C_{FS} = C_{FP} \cdot \frac{f_p - f_z}{f_z} \quad (29)$$

Equation 30

$$R_{FS} = \frac{1}{2\,\pi \cdot f_z \cdot C_{FS}} \quad (30)$$

***Note**: the output voltage ripple ΔV_{OUT} (at 2 *f_{LINE}) is not eliminated by the compensation network and so its present at the COMP pin voltage. To avoid unwanted valley jump the ripple voltage at the COMP pin has to be lower than the valley skipping hysteresis thresholds (200 mV typ., see L6462A datasheet on www.st.com). As previously reported, the peak-to peak ripple results:*

Equation 31

$$\Delta V_{COMP} = \Delta V_{OUT} \cdot \left|H(j\,2\pi \cdot (2 \cdot f_{LINE})\right| = \Delta V_{OUT} \cdot \frac{R_{FB\_L}}{\left(R_{FB_L} + R_{FB_H}\right)} \cdot \frac{g_{m\_EA}}{2\,\pi \cdot (2 \cdot f_{LINE}) \cdot C_{FB}} \quad (31)$$

and solving Equation (31) for the C_{FB} capacitor results:

Equation 32

$$C_{FB,min} = \Delta V_{OUT,max} \cdot \frac{R_{FB\_L}}{\left(R_{FB_L} + R_{FB_H}\right)} \cdot \frac{g_{m\_EA}}{2\,\pi \cdot \left(2 \cdot f_{LINE,min}\right) \cdot \Delta V_{COMP,max}} \quad (32)$$

where $\Delta V_{COMP,max}$ the maximum acceptable ripple on COMP pin voltage (e.g., $\Delta V_{COMP,max}$ = 175 mV to achieve some margin).

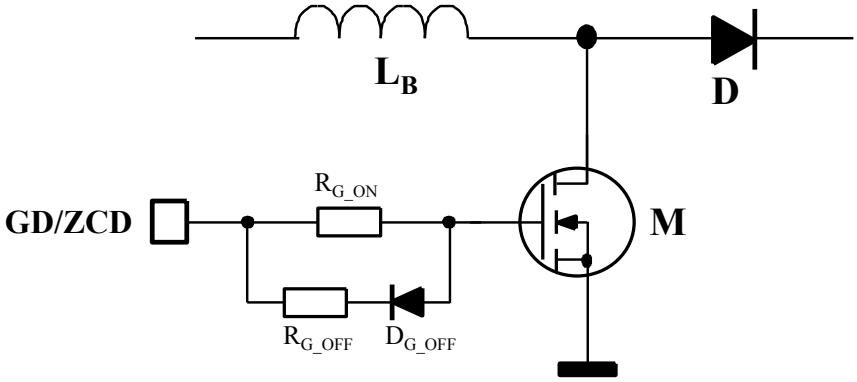
2.4 Gate driver

The GD/ZCD pin is the output of the driver block and is able to drive an external power MOSFET with at least 0.3 A source and 0.6 A sink capability.

The high-level voltage of this pin (V_{GDH}) is internally clamped at 10 V typ. to avoid excessive gate voltages in case the controller is supplied with a high VCC value.

To avoid undesired switch-on of the external MOSFET due to some leakage current when the supply of the L6462A is below the UVLO threshold, an internal pull-down circuit holds the pin low (the circuit guarantees 1.1 V maximum at I_{SINK}=1 mA); in case of using an external pull-down gate resistor, select a value >100 kΩ to avoid reducing the sensitivity of the ZCD detection circuitry.

Figure 12. Typical gate driver network



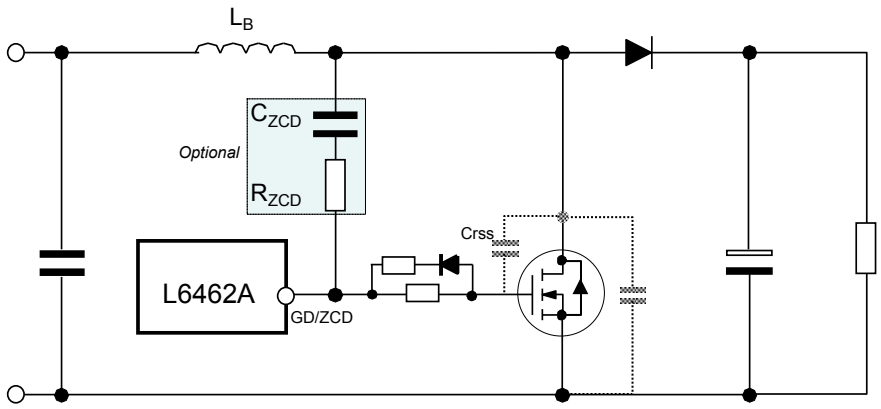
A gate resistor R_{G_ON} in series to GD/ZCD pin is typically added to limit the high dv/dt at power MOSFET turn on. To avoid excessive slowdown at power MOSFET turn-off, a second resistor R_{G_OFF} plus a signal diode can be used as shown in Figure 12.

Typical values of these resistors are in the range of 15 Ω÷30 Ω for R_{G_ON} and 4.7 Ω÷10 Ω for R_{G_OFF} in a standard PCB layout. In case of a PCB layout with long GD/ZCD and power GND return tracks, a higher gate resistor values should be used to avoid excessive high frequency spike due to parasitic inductance (e.g.,30 Ω÷47 Ω for R_{G_ON} and 8.2 Ω÷20 Ω for R_{G_OFF}).

2.5 Zero-Current Detection (ZCD) circuitry - optional

As showed in the L6462A datasheet, the controller detects the zero-current condition (ZCD) through the integrated current sensor on the pin GD/ZCD. In case one wants to increase the sensitivity of the internal current sensor, it is possible to add a few pF external capacitor (C_{ZCD}) between the drain and the gate of the power MOSFET, with a series resistor (R_{ZCD}) in the kΩ (e.g., 1¸10 kΩ) to limit noise injection into the gate driver pin as shown in Figure 13.

Figure 13. Optional supplementary external RC to increase ZCD circuit sensitivity



As reported in the L6462A datasheet, the I_{GD} sensed current during the drain oscillation has a sinusoidal shape and its maximum is:

Equation 33

$$I_{GDmax}(\theta) = 2\pi \cdot f_R \cdot C_{rss} \cdot (V_{OUT} - V_{IN}(\theta)) = \frac{C_{rss}}{\sqrt{L_B C_d}} \cdot (V_{OUT} - V_{IN}(\theta)) \quad (33)$$

where C_{rss} is the parasitic capacitance that exists between the gate and the drain terminals of the power MOSFET. The right ZCD detection is guaranteed till the $I_{GD,max}$ is higher than the internal arming threshold (I_{GD_A}=60 µA typ., see L6462A datasheet).

Solving Equation (33) for the C_{rss} capacitor, considering the maximum input voltage ($V_{AC,max}$) and 200 µA as target value to achieve same margin, results:

Equation 34

$$C_{rss,min} = 200\mu A \cdot \frac{\sqrt{L_B C_d}}{(V_{OUT} - \sqrt{2} V_{AC,max})} \quad (34)$$

In case the selected power MOSFET has a $C_{rss} < C_{rss,min}$, the external C_{ZCD} capacitor has to be added to achieve the 200 µA target (C_{rss} and C_{ZCD} capacitor are in parallel):

Equation 35

$$C_{ZCD} = 200\mu A \cdot \frac{\sqrt{L_B C_d}}{(V_{OUT} - \sqrt{2} V_{AC,max})} - C_{rss} \quad (35)$$

3 Power stage design

This section describes the step to design the components of the PFC boost power stage, based on the target specifications/requirements:

- AC line voltage range (rms): $V_{AC,min}$ ÷ $V_{AC,max}$
- Minimum line frequency: $f_{LINE,min}$
- Nominal output voltage: V_{OUT}
- Rated output power: $P_{OUT,max}$
- Expected efficiency: η
- Holdup time and minimum output voltage: T_{hold}, $V_{OUT,min}$
- Minimum switching frequency: $F_{SW,min}$
- Maximum ambient temperature: $T_{amb,max}$

3.1 Operating conditions

Starting from the target specifications it is possible to define the main parameters of the power stage:

- Rated DC output current ($I_{OUT,max}$)

Equation 36

$$I_{OUT,max} = \frac{P_{OUT,max}}{V_{OUT}} \quad (36)$$

- Maximum input power ($P_{IN,max}$)

Equation 37

$$P_{IN,max} = \frac{P_{OUT,max}}{\eta} \quad (37)$$

- Maximum RMS input current ($I_{IN\_RMS,max}$)

Equation 38

$$I_{IN\_RMS,max} = \frac{P_{OUT,max}}{\eta \cdot V_{AC} \cdot PF} \quad (38)$$

- Maximum peak inductor current ($I_{LPK,max}$)

Equation 39

$$I_{LPK,max} = 2\sqrt{2} \cdot I_{IN\_RMS,max} \quad (39)$$

- Maximum RMS inductor current ($I_{L\_RMS,max}$)

Equation 40

$$I_{L\_RMS,max} = \frac{2}{\sqrt{3}} \cdot I_{IN\_RMS,max} \quad (40)$$

- Maximum AC inductor current ($I_{L\_RMS,max}$)

Equation 41

$$I_{L\_AC,max} = \sqrt{I_{L\_RMS,max}{}^2 - I_{IN\_RMS,max}{}^2} \quad (41)$$

- Maximum RMS switch current ($I_{SW\_RMS,max}$)

Equation 42

$$I_{SW\_RMS,max} = I_{LPK,max} \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2}}{9\pi} \cdot \frac{V_{AC,min}}{V_{OUT}}} \quad (42)$$

- Maximum RMS diode current ($I_{D\_RMS,max}$)

Equation 43

$$I_{D\_RMS,max} = I_{LPK,max} \cdot \sqrt{\frac{4\sqrt{2}}{9\pi} \cdot \frac{V_{AC,min}}{V_{OUT}}} \quad (43)$$

3.2 Bridge diode rectifier (BD)

The input rectifier bridge can use standard slow recovery, low-cost devices. Typically, a 600 V device is selected, to have good margin against mains surges, and with an average current capability higher than:

Equation 44

$$I_{pk,avg\_bridge} = \sqrt{2} \cdot I_{in,rms_{bridge}} \quad (44)$$

where the input RMS current I_{in,rms_bridge} is:

Equation 45

$$I_{in,rms\_bridge} = \frac{\sqrt{2}}{2} \cdot \frac{P_{OUT}}{\eta \cdot V_{AC} \cdot PF} \quad (45)$$

The rectifier bridge power dissipation can be estimated with the following formula:

Equation 46

$$P_{bridge} = 4 \cdot R_{diode} \cdot I_{in,rms\_bridge}{}^2 + 4 \cdot V_{th,diode} \cdot \left(\frac{2}{\pi} \cdot I_{in,rms\_bridge}\right) \quad (46)$$

where $V_{th,diode}$ and R_{diode} are respectively the threshold voltage and dynamic resistance of a single diode of the bridge, which can be found in the component datasheet.

Based on the total power losses value (P_{bridge}) and based on the maximum acceptable bridge-diode's junction temperature target (e.g. $T_{j\_bridge,max}$=125 °C), it is possible to calculate the maximum thermal resistance of the heat-sink required to keep the bridge-diode's junction temperature below $T_{j\_bridge,max}$:

Equation 47

$$R_{th} \cong \frac{T_{j\_bridge,max} - T_{amb,max}}{P_{bridge}} \quad (47)$$

***Note**: an NTC resistor limiting the current at turn-on is required to avoid overstress to the diode bridge.*

3.3 Boost Inductor (L_B)

The boost inductor value (L_B) is selected based on the desiderated minimum switching frequency $F_{SW,min}$ at full load. Assuming a TM operation ($T_V \simeq 0$), the peak of the boost inductor current $I_{LPK}(\Theta)$ is sinusoidal and twice the input current:

Equation 48

$$I_{LPK}(\theta) = 2 \cdot I_{IN}(\theta) = I_{LPK} \cdot sin \quad (48)$$

where I_{LPK} can be calculated from Equation (38), Equation (39) and results:

Equation 49

$$I_{LPK} = 2\sqrt{2} \cdot \frac{P_{OUT}}{\eta \cdot V_{AC} \cdot PF} \quad (49)$$

During the power switch ON time the boost inductor is magnetized and it possible to write:

Equation 50

$$T_{ON}(V_{AC,},\theta\,) = \frac{L_B \cdot I_{LPK}(\theta\,)}{|V_{AC}(\,\theta)|} = \frac{L_B \cdot I_{LPK} \cdot sin\theta}{\sqrt{2}\,V_{AC} \cdot sin\theta} = \frac{L_B \cdot I_{LPK}}{\sqrt{2}\,V_{AC}} = cost \quad (50)$$

where it is interesting to note that does not depend on the angle of the mains phase but is constant over the entire mains cycle. Then, the resulting demagnetization time of the boost inductor is:

Equation 51

$$T_{FW}(V_{AC,},\theta\,) = \frac{L_B \cdot I_{LPK}(\theta\,)}{V_{OUT} - |V_{AC}(\theta\,)|} = \frac{L_B \cdot I_{LPK} \cdot sin\theta}{V_{OUT} - \sqrt{2}\,V_{AC} \cdot sin\theta} \quad (51)$$

Considering that in TM operation ($T_V \simeq 0$), the switching frequency is:

Equation 52

$$f_{sw}(V_{AC,},\theta\,) \cong \frac{1}{T_{ON}(V_{INpk,},\theta\,) + T_{FW}(V_{INpk,},\theta\,)} = \frac{\sqrt{2}\,V_{AC} \cdot (V_{OUT} - \sqrt{2}\,V_{AC} \cdot sin\theta)}{L_B \cdot I_{LPK} \cdot V_{OUT}} \quad (52)$$

Then replacing Equation (49) in the Equation (52) after some calculations results:

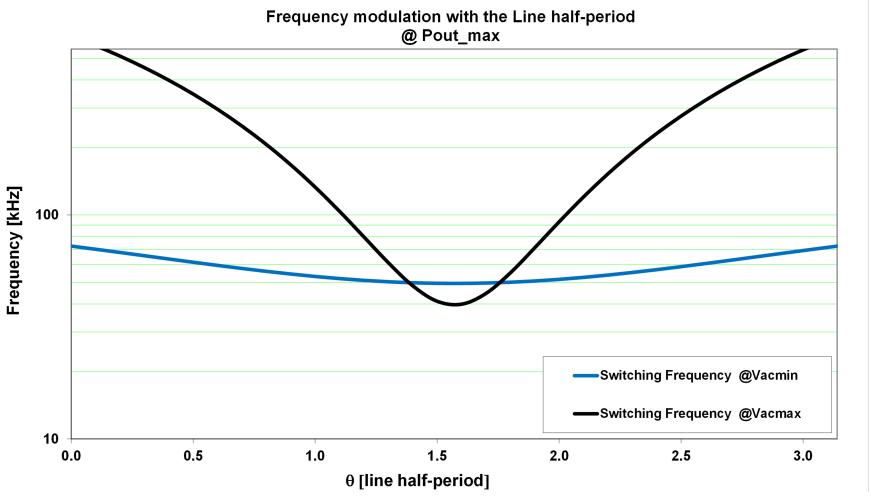
Equation 53

$$f_{sw}(V_{AC,},P_{OUT},\theta\,) \cong \frac{\eta \cdot PF}{2 \cdot L_B \cdot P_{OUT}} \cdot \frac{{V_{AC}}^2 \cdot (V_{OUT} - \sqrt{2}\,V_{AC} \cdot sin\theta)}{V_{OUT}} \quad (53)$$

It is worth noticing that:

- the switching frequency is minimal at the top of the sinusoid (Θ=π/2) and maximal at the zero crossings of the line voltage (Θ=0 or π => sinΘ=0),
- the absolute minimum switching frequency $F_{SW,min}$ can occur at either the maximum $V_{AC,max}$ or the minimum mains voltage $V_{AC,min}$ at maximum output power.

Figure 14. Switching frequency versus line voltage



Then, the selected inductor value is therefore equal to the minimum:

Equation 54

$$L_B = min\left[L_B(V_{AC,min}), L_B(V_{AC,max})\right] \quad (54)$$

where:

Equation 55

(55)

$$L_B(V_{AC,min}) = \frac{\eta \cdot PF}{2 \cdot F_{SW,min} \cdot P_{OUT\_MAX}} \cdot \frac{V_{AC,min}{}^2 \cdot (V_{OUT} - \sqrt{2}\, V_{AC,min})}{V_{OUT}}$$

$$L_B(V_{AC,max}) = \frac{\eta \cdot PF}{2 \cdot F_{SW,min} \cdot P_{OUT\_MAX}} \cdot \frac{V_{AC,max}{}^2 \cdot (V_{OUT} - \sqrt{2}\, V_{AC,max})}{V_{OUT}}$$

3.4 Input capacitor (C_{in})

The input filter capacitor (C_{in}), placed across the diode bridge output, smooths the high-frequency ripple and it sustains the maximum instantaneous input voltage. Then the minimum value can be calculated based on the maximum acceptable voltage ripple:

Equation 56

$$C_{in\_min} = \frac{I_{IN\_rms,max}}{2\pi \cdot F_{SW,min} \cdot r \cdot V_{AC\_min}} \quad (56)$$

where r is the coefficient ripple voltage and typically it is selected in the range of 0.05÷0.1 (voltage ripple across C_{in} between 5% and 10% of the minimum rated input voltage).

The maximum value of this capacitor has to be not much higher than the previous values to avoid the distortion of the input mains current, due to the residual voltage retained by the capacitor that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

3.5 Output capacitor (C_{out})

The output bulk capacitor value (C_{out}) is selected based on the expected output voltage ripple and hold-up time (if requested). Neglecting the contribution of the ESR, as the capacitive reactance is dominant, the minimum value of the output capacitor to respect the ripple specification is:

Equation 57

$$C_{out\_ripple} = \frac{I_{OUT,max}}{2\,\pi \cdot f_{LINE,min} \cdot \Delta V_{OUT}} = \frac{P_{OUT,max}}{2\,\pi \cdot f_{LINE,min} \cdot \Delta V_{OUT} \cdot V_{OUT}} \quad (57)$$

where ΔV_{OUT} is output voltage ripple (peak-to-peak).

If the PFC stage has to guarantee a specified hold-up time (T_{hold}), the calculation of the output capacitor is different. The value of the capacitor when the line voltage drops out, needed to deliver the output power for a certain time T_{hold} until the output voltage reaches the required minimum voltage value (V_{OUT_MIN}) depends on the load and the value of the ripple. When V_{OUT_MIN} is reached, a 'power fail' is detected, stopping the downstream system supplied by the PFC. The worst-case for the hold-up time is at minimum input voltage and full load, with the line drop starting at the valley of the sine-varying ripple of the output voltage.

The minimum capacitor to respect the hold-up time then results:

Equation 58

$$C_{out\_holdup} = \frac{2 \cdot P_{OUT,max} \cdot T_{hold}}{\left(V_{OUT} - \frac{\Delta V_{OUT}}{2}\right)^2 - (V_{OUT\_MIN})^2} \quad (58)$$

To respect both conditions, then $C_{out} > max\ (C_{out_{ripple}}, C_{out_{holdup}})$

3.6 Power MOSFET (M)

Selection of the power MOSFET (typically one or two in parallel) concerns mainly the equivalent on-resistance ($R_{DS(on)}$), that should be low in order to minimize conduction losses, without increasing the switching losses due to the MOSFET's equivalent output capacitance Coss. To achieve high-efficiency both $R_{DS(on)}$ and the Coss have to be taken into account, also considering the trade-off between cost versus performance.

The MOSFET breakdown voltage is selected considering the PFC nominal output voltage adding some margin (e.g., 20%) to guarantee reliable operation.

The total power losses of the MOSFETs are mainly given by the sum of conduction, switching and capacitive losses:

Equation 59

$$P_{loss}(V_{AC}, P_{OUT}) = P_{cond}(V_{AC}, P_{OUT}) + P_{sw}(V_{AC}, P_{OUT}) + P_{cap} \quad (59)$$

where conduction (P_{cond}) and switching (P_{sw}) losses depends on the input voltage and output power condition. The worst-case occurs typically at minimum input voltage ($V_{AC,min}$) and maximum output power ($P_{OUT,max}$).

The conduction losses can be estimated with:

Equation 60

$$P_{cond}(V_{AC}, P_{OUT}) = R_{dson} \cdot I_{sw,rms}(V_{AC}, P_{OUT})^2 \quad (60)$$

where the rms current into the switch is:

Equation 61

$$I_{sw,rms}(V_{AC}, P_{OUT}) = \ 2\sqrt{2} \cdot \frac{P_{OUT}}{\eta \cdot V_{AC} \cdot PF} \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2}}{9\pi} \cdot \frac{V_{AC}}{V_{OUT}}} \quad (61)$$

It is worth noticing that normally in the datasheets the $R_{DS(on)}$ is given at ambient temperature (25°C), then to properly calculate the conduction losses at the MOSFET junction operating temperature (e.g. T_j=100 °C), a multiplier factor should be taken into account. Multiplier factor that can be found on the datasheet looking at the normalized on-resistance versus temperature graph (e.g. typically a multiplier factor of 1.7 considering T_j=100 °C).

The switching losses are difficult to predict as they depend on the particular switching waveform, determined by many factors (driving current, gate resistors, MOSFET gate internal resistance, V_{th}, gate charge, total capacitance on the drain node including parasitic capacitances etc.). A good approximation to determine the generic switching losses due to the MOSFET commutation, that in this case occurring only at turn-off thanks to Quasi-Resonant operation, can be basically expressed by:

Equation 62

$$P_{sw} = \frac{1}{2} \cdot V_{DS} \cdot I_{DS} \cdot t_{fall} \cdot F_{sw} \quad (62)$$

where V_{DS} is the drain-to-source of MOSFET, I_{DS} the drain current and t_{fall} refer to the falling edge time of V_{DS}. The Equation (62) represents the crossing between the MOSFET current that decreases linearly during the fall time and the voltage on the MOSFET drain that increases. In fact, during the fall time, the current of the boost inductor flows into the parasitic capacitance of the MOSFET charging it and so for this reason the switching losses also depend on the total drain capacitance.

Starting from Equation (62), it is possible to demonstrate that the switching losses results:

Equation 63

$$P'_{sw}(V_{AC}, P_{OUT}, \theta) = \frac{{t_{fall}}^2}{C_d} \cdot \frac{1}{6} \cdot I_{LPK}(V_{AC}, P_{OUT}, \theta) \cdot f_{sw}(V_{AC}, P_{OUT}, \theta) \quad (63)$$

where C_d is the equivalent total drain capacitance (C_d=C_{oss}+C_{par} where C_{oss} is the MOSFET parasitic drain capacitance and C_{par} is the parasitic capacitances of the other components afferent to the drain node like the boost inductor).

Equation (63) depends on the phase angle on the sinusoidal waveform, then its average value it is found by averaging it over a line half-cycle:

Equation 64

$$P_{sw}\left(V_{AC}, P_{OUT}\right) = \frac{1}{\pi} \cdot \int_0^{\pi} P'_{sw}(V_{AC}, P_{OUT}, \theta)\, d\theta = \frac{{t_{fall}}^2}{C_d} \cdot \frac{1}{6\pi} \cdot \int_0^{\pi} I_{LPK}(V_{AC}, P_{OUT}, \theta) \cdot f_{sw}(V_{AC}, P_{OUT}, \theta)\, d\theta \quad (64)$$

Applying the Equation (48) and Equation (49), the average switching losses results:

Equation 65

$$P_{sw}\left(V_{AC}, P_{OUT}\right) = \frac{{t_{fall}}^2}{C_d} \cdot \frac{1}{6\pi} \cdot \left(\frac{2\sqrt{2} \cdot P_{OUT}}{\eta \cdot V_{AC} \cdot PF}\right) \cdot \int_0^{\pi} (sin\theta)^2 \cdot f_{sw}(V_{AC}, P_{OUT}, \theta)\, d\theta \quad (65)$$

where the switching frequency $f_{sw}(V_{AC}, P_{OUT}, \theta)$ is expressed by the Equation (53). The capacitive losses, due to the discharge of the total drain capacitance through the MOSFET at turn-on, can be estimated with this simple expression:

Equation 66

$$P_{cap} \cong \frac{1}{2} \cdot C_d \cdot {V_{DS}}^2 \cdot f_{sw} \tag{66}$$

where V_{DS} is the drain voltage at the MOSFET's turn-on instant and it depends on the phase angle θ, as shown in Figure 15 and Figure 16.

Figure 15. Drain voltage turn on – capacitive losses.

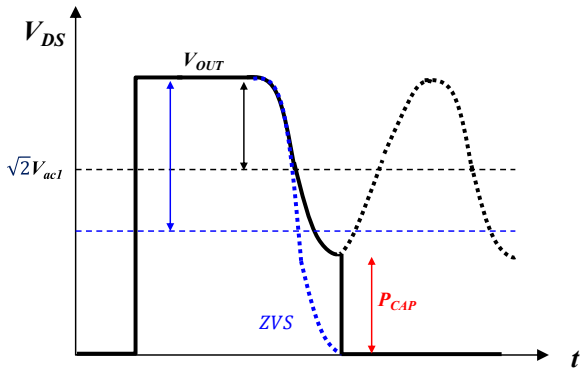
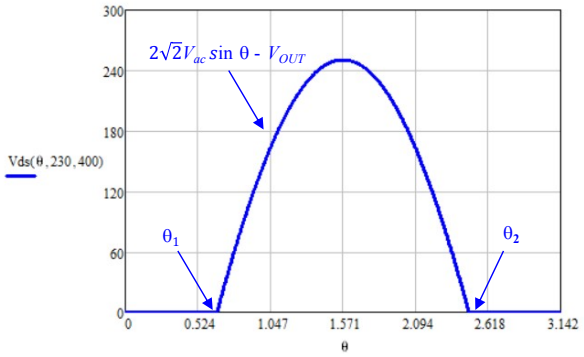


Figure 16. Drain voltage turn on – θ_1 and θ_2 angle



Basically, if the input voltage is lower than half of the output voltage, the resonance should ideally reach zero, achieving a zero-voltage operation and therefore avoiding any losses on this edge. Whereas if the input voltage is higher than half of the output voltage, the amplitude of the drain resonance is $\left(V_{OUT} - \sqrt{2} \cdot V_{AC}\right)$ and the MOSFET is turned-on once drain voltage is $2\sqrt{2} \cdot V_{AC} \cdot \sin\theta - V_{OUT}$

Taking into account that also the switching frequency (Equation (53)) depends on the phase angle q, then its average value it is found by averaging it over a line half-cycle:

Equation 67

$$P_{cap}\left(V_{AC}, P_{OUT}\right) \cong \frac{1}{\pi} \cdot \int_{\theta_1}^{\theta_2} \frac{1}{2} \cdot \left(2\sqrt{2} \cdot V_{AC} \cdot sin\theta - V_{OUT}\right)^2 \cdot f_{sw}(V_{AC}, P_{OUT}, \theta)\, d\theta \tag{67}$$

where θ_1 and θ_2 depend on the input voltage and are defined below:

Equation 68

$$\theta_1 = arcsin\left(\frac{V_{OUT}}{2\sqrt{2} \cdot V_{AC}}\right) \tag{68}$$

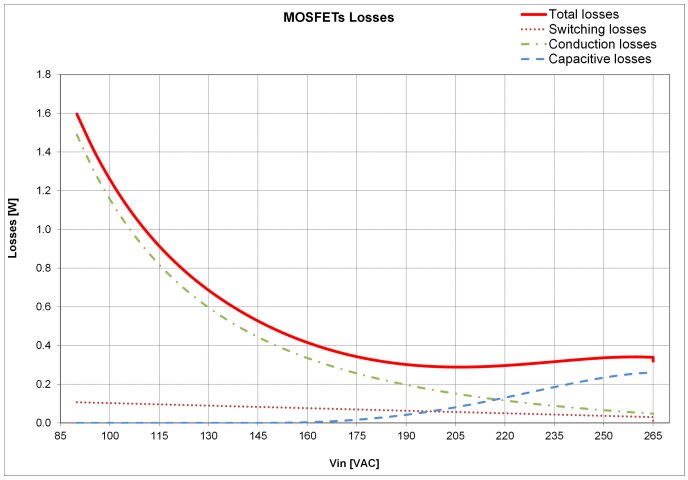
Equation 69

$$\theta_2 = \pi - \theta_1 \tag{69}$$

In practice, it is possible to estimate the capacitive losses by solving the integral of the switching frequency between θ_1 and θ_2 phase angle.

It is worth noticing that, as shown in Figure 17, typically the maximum total losses occur at the minimum input voltage ($V_{AC,min}$) where the conduction losses are dominant. Whereas the capacitive losses are dominant at high mains voltages.

Figure 17. Typical MOSFET power losses graph versus input voltage



Based on the total MOSFET power losses value (P_{loss}) and based on the maximum acceptable MOSFET junction temperature target (e.g. $T_{j\_MOSFET,max}$=125 °C), it is possible to calculate the maximum thermal resistance of the heat-sink required to keep the MOSFET's junction temperature below $T_{j\_MOSFET,max}$:

Equation 70

$$R_{th} \cong \frac{T_{j\_MOSFET,max} - T_{amb,max}}{P_{loss}} \tag{70}$$

3.7 Boost diode (D)

Following criteria similar to that used for MOSFET losses calculation, the output rectifier can be properly selected. A minimum breakdown voltage of 1.2·(V_{OUT}) and a current rating higher than 3·I_{OUT_MAX} can be considered for a rough selection of the rectifier.

The correct selection is then confirmed by the thermal calculation, as the diode junction temperature typically needs to work within 125 °C.

Since this circuit operates in the transition mode, the reverse recovery is not experienced by the diode, then power losses are mainly due to conduction and can be estimated by:

Equation 71

$$P_{diode} = V_{th\_diode} \cdot I_{OUT} + R_{d\_diode} \cdot {I_{D\_RMS}}^2 \tag{71}$$

where V_{th_diode} and R_{d_diode} are the rectifier threshold voltage/dynamic resistance respectively (see diode datasheet), and the maximum diode RMS current can be estimated substituting Equation (38) and Equation (39) in the Equation (43), resulting:

Equation 72

$$I_{D\_RMS,max} = 2\sqrt{2} \cdot \frac{P_{OUT,max}}{\eta \cdot V_{AC,min} \cdot PF} \cdot \sqrt{\frac{4\sqrt{2}}{9\pi} \cdot \frac{V_{AC,min}}{V_{OUT}}} \tag{72}$$

Based on the total power losses value (P_{diode}) and based on the maximum acceptable bridge-diode's junction temperature target (e.g. $T_{j\_diode,max}$=125 °C), it is possible to calculate the maximum thermal resistance of the heat-sink required to keep the bridge-diode's junction temperature below $T_{j\_diode,max}$:

Equation 73

$$R_{th} \cong \frac{T_{j\_diode,max} - T_{amb,max}}{P_{diode}} \tag{73}$$

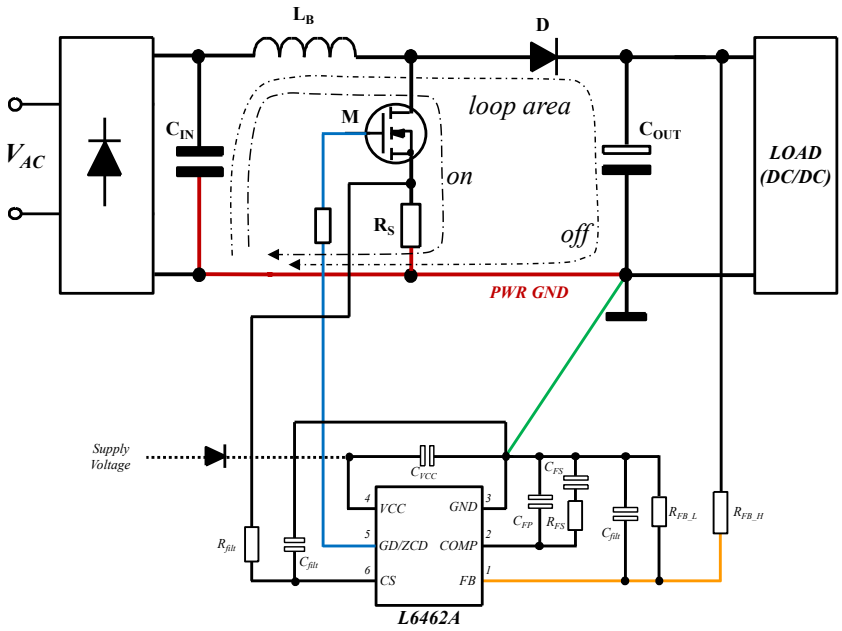
4 PCB design guidelines

The L6462A does not need any special attention to the layout, only requiring that the general layout rules for any switching power converter be carefully applied.

Referring to the Figure 18, the basic rules are:

- Keep the power and signal GND separated. Connect the return pins of the components carrying the high current switched at high frequency such as the PFC sense resistor (R_S), the input and output capacitors (C_{IN}, C_{OUT}) as close as possible. This point is the GND star point. A downstream converter must be connected to this return point.
- Connect the GND pin (#3) to the GND star point making the connections as short as possible and using a track width suitable to minimize its impedance. Keep this connection separated from any other GND connection, especially if carrying high currents.
- Minimize the length of the traces relevant to the boost inductor (L_B), MOSFET's drain (M), boost rectifier (D) and the output capacitor (C_{OUT}).
- Minimize the track length of the GD/ZCD pin (blue net) and keeps far from other high dV/dt signal tracks (to avoid noise injection during valleys detection time).
- Minimize the track length of the FB pin and keeps it far from high dV/dt signal tracks, such as the MOSFET's drain (FB is a high impedance pin).
- Minimize the loop area of the high frequency paths (dotted lines).
- Minimize the length of the power GND return paths (red nets).

Figure 18. Power section and signal component connections



- Place the VCC ceramic filter capacitor (e.g., 100 nF÷1 µF) close to the L6462A controller, connecting it to the VCC pin (#4) and to the GND pin (#3).
- Keep signal components as close as possible to each relevant pin of L6462A. Specifically:
  - Place compensation network (C_{FP}, R_{FS}, C_{FS}) close to COMP pin (#2) and connected to signal GND.
  - Place current sense filter (C_{filt}, R_{filt}) close to CS pin (#6) and connected to signal GND.
  - Place the output voltage resistors divider (R_{FB_L}, R_{FB_H}) close to FB pin (#1) and connected to signal GND.
  - Place high frequency filter of the feedback net (C_{filt}) close to FB pin (#1) and connected to signal GND.

5 Design example

A 250 W wide-input range PFC circuit is considered, with the following target specifications:

- AC line voltage range (rms): $V_{AC,min}$ = 90 V, $V_{AC,max}$ = 265 V
- Minimum line frequency: $f_{LINE,min}$ = 47 Hz (nominal 50 Hz, 60 Hz)
- Nominal output voltage: V_{OUT} = 400 V
- Rated output power: $P_{OUT,max}$ = 250 W
- Rated output current: $I_{OUT,max}$ = 0.625 A
- Expected efficiency at $V_{AC,min}$: η = 0.94
- Expected power factor at $V_{AC,min}$: PF = 0.99
- Minimum switching frequency: $F_{SW,min}$ = 40 kHz
- Ripple input voltage coefficient: r = 5%
- Maximum output low-frequency ripple (peak-to-peak): ΔV_{OUT} = 12 V
- Hold-up time and minimum output voltage: T_{hold} = 20 ms, V_{OUT_MIN} = 300 V
- System stability: Φ_m = 45° (phase margin), D_3 = 2.5% (maximum third-harmonic distortion)
- Maximum ambient temperature: 50 °C

5.1 Power section

Bridge rectifier

Considering that the RMS current into the bridge diode is (from Equation (45)):

Equation 74

$$I_{in,rms\_bridge} = \frac{\sqrt{2}}{2} \cdot \frac{P_{OUT}}{\eta \cdot V_{AC} \cdot PF} = \frac{\sqrt{2}}{2} \cdot \frac{250W}{0.94 \cdot 90V \cdot 0.99} = 2.11\ A \quad (74)$$

the sinusoidal peak value of the AC current results (from Equation (44)):

Equation 75

$$I_{pk,avg\_bridge} = \sqrt{2} \cdot I_{in,rms_{bridge}} = \sqrt{2} \cdot 2.11A = 2.98A \quad (75)$$

then a bridge diode D15XB60H is selected (600 V, 15 A/3.5 A). Assuming V_{th_diode}=0.7 V and R_{diode}=25 mΩ (extrapolated from the device datasheet), the estimated total power dissipation of the bridge diode results (from Equation (46)):

Equation 76

$$P_{bridge} = 4 \cdot R_{diode} \cdot {I_{in,rms_{bridge}}}^2 + 4 \cdot V_{th,diode} \cdot \left(\frac{2}{\pi} \cdot I_{in,rms_{bridge}}\right) \quad (76)$$
$$= 4 \cdot 25m\Omega \cdot 2.11A^2 + 4 \cdot 0.7V \cdot \left(\frac{2}{\pi} \cdot 2.11A\right) = 4.21\ W$$

To keep the junction temperature of the bridge diode below 125 °C ($T_{j\_bridge,max}$), it should be needed a heat-sink with a thermal resistance below (from Equation 47):

Equation 77

$$R_{th} \cong \frac{T_{j\_bridge,max} - T_{amb,max}}{P_{bridge}} = \frac{125℃ - 50℃}{4.21W} = 17.8\ ℃/W \quad (77)$$

Boost inductor

Considering a minimum switching frequency $F_{SW,min}$=40 kHz, the required maximum boost inductor L_B results (from Equation (55)):

Equation 78

$$L_B(V_{AC,min}) = \frac{\eta \cdot PF}{2 \cdot F_{SW,min} \cdot P_{OUT\_MAX}} \cdot \frac{{V_{AC,min}}^2 \cdot (V_{OUT} - \sqrt{2}\, V_{AC,min})}{V_{OUT}} \quad (78)$$
$$= \frac{0.94 \cdot 0.99}{2 \cdot 40kHz \cdot 250W} \cdot \frac{{90V}^2 \cdot (400V - \sqrt{2} \cdot 90V)}{400V} = 259\ \mu H$$

Equation 79

$$L_B(V_{AC,max}) = \frac{\eta \cdot PF}{2 \cdot F_{SW,min} \cdot P_{OUT_{MAX}}} \cdot \frac{{V_{AC,max}}^2 \cdot (V_{OUT} - \sqrt{2}\, V_{AC,max})}{V_{OUT}} \quad (79)$$
$$= \frac{0.94 \cdot 0.99}{2 \cdot 40kHz \cdot 250W} \cdot \frac{{265V}^2 \cdot (400V - \sqrt{2} \cdot 265V)}{400V} = 208\ \mu H$$

A nominal inductor L_B=210 µH is selected.

Input capacitor

The minimum required input filter capacitor C_{in} is calculated from Equation 56 considering that the maximum input rms current is $I_{IN\_RMS,max} = \frac{P_{OUT,max}}{\eta \cdot V_{AC} \cdot PF} = \frac{250W}{0.94 \cdot 90V \cdot 0.99} = 2.98A$(from Equation (38)):

Equation 80

$$C_{in\_min} = \frac{I_{IN\_rms,max}}{2\pi \cdot F_{SW,min} \cdot r \cdot V_{AC\_min}} = \frac{2.98A}{2\pi \cdot 40kHz \cdot 90V} = 1.31\ \mu F \quad (80)$$

A value of 1.47 µF (1 µF and 0.47 µF in parallel) is selected.

Output capacitor

The minimum output capacitor C_{out} to achieve the desiderated voltage ripple is (from Equation (57)):

Equation 81

(81)

$$C_{out_{ripple}} = \frac{I_{OUT,max}}{2\,\pi \cdot f_{LINE,min} \cdot \Delta V_{OUT}} = \frac{0.625A}{2\,\pi \cdot 47Hz \cdot 12V} = 175\ \mu F$$

and to achieve the desiderated holdup time is (from Equation (58)):

Equation 82

$$C_{out_{holdup}} = \frac{2 \cdot P_{OUT,max} \cdot T_{hold}}{\left(V_{OUT} - \frac{\Delta V_{OUT}}{2}\right)^2 - \left(V_{OUT_{MIN}}\right)^2} = \frac{2 \cdot 250W \cdot 20ms}{\left(400V - \frac{12V}{2}\right)^2 - (300V)^2} \quad (82)$$
$$= 153\ \mu F$$

A value of C_{out}=180 µF /450V is selected.

Power MOSFET

A 600 V/99 mΩ_{max} in TO-220FP power MOSFET is selected (STF36N60M6), as a good balance between the minimum break-down voltage (600 V) and static/dynamic performances ($R_{DS(on)}$/C_{oss}). Typically the maximum power losses are at minimum input voltage ($V_{AC,min}$) where the conduction losses are dominant, then the RMS current flowing into the power switch is (from Equation (61)):

Equation 83

$$I_{sw,rms} = 2\sqrt{2} \cdot \frac{P_{OUT}}{\eta \cdot V_{AC} \cdot PF} \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2}}{9\pi} \cdot \frac{V_{AC}}{V_{OUT}}} = 2\sqrt{2} \cdot \frac{250W}{0.94 \cdot 90V \cdot 0.99} \quad (83)$$
$$\cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2}}{9\pi} \cdot \frac{90V}{400V}} = 2.94\ A$$

then considering 100°C as maximum junction temperature of the power MOSFET (1.7 as multiplier factor for the $R_{DS(on)}$), the estimated conduction losses results (from Equation (60)):

Equation 84

$$P_{cond} = R_{dson} \cdot {I_{sw,rms}}^2 = (99m\Omega \cdot 1.7) \cdot (2.94A)^2 = 1.45\ W \quad (84)$$

Assuming a stray capacitance of 100 pF and considering the typical C_{OSS} of the power MOSFET at 100 V (93 pF, see STF36N60M6 datasheet), the total capacitance afferent to the drain node is about
$C_d = C_{OSS} \cdot N_{mos} + C_{stray} = 190pF$

Considering the Equation 53 (switching frequency versus input voltage, output power), the resulting estimated switching power losses at the minimum input voltage is (from Equation (45)):

Equation 85

$$P_{sw} = \frac{{t_{fall}}^2}{C_d} \cdot \frac{1}{6\pi} \cdot \left(\frac{2\sqrt{2} \cdot P_{OUT}}{\eta \cdot V_{AC} \cdot PF}\right) \cdot \int_0^{\pi} (sin\theta)^2 \cdot f_{sw}(V_{AC}, P_{OUT}, \theta)\, d\theta = \frac{10ns^2}{190pF} \cdot \frac{1}{6\pi} \quad (85)$$
$$\cdot \left(\frac{2\sqrt{2} \cdot 250W}{0.94 \cdot 90V \cdot 0.99}\right) \cdot \int_0^{\pi} (sin\theta)^2 \cdot f_{sw}(V_{AC}, P_{OUT}, \theta)\, d\theta = 0.105\ W$$

where has been considered t_{fall}=7ns (see STF36N60M6 datasheet).

Considering the Equation (68) and Equation (69), the capacitive losses can be estimated solving the integral in the Equation (66).

At the minimum input voltage results:

Equation 86

$$P_{cap}\left(V_{AC,\min},\ P_{OUT\_MAX}\right) \cong \frac{1}{\pi} \cdot \int_{\theta_1}^{\theta_2} \frac{1}{2} \cdot \left(2\sqrt{2} \cdot V_{AC,min} \cdot sin\theta - V_{OUT}\right)^2 \quad (86)$$
$$\cdot\ f_{sw}\left(V_{AC,\max},\ P_{OUT\_MAX}, \theta\right) d\theta = \frac{1}{\pi} \cdot \int_{\theta_1}^{\theta_2} \frac{1}{2} \cdot \left(2\sqrt{2 \cdot} 90V \cdot sin\theta - 400V\right)^2$$
$$\cdot\ f_{sw}(90V, 250W, \theta)\, d\theta \cong 0$$

Whereases at the maximum input voltage result:

Equation 87

$$P_{cap}\left(V_{AC,\max},\ P_{OUT\_MAX}\right) \cong \frac{1}{\pi} \cdot \int_{\theta_1}^{\theta_2} \frac{1}{2} \cdot \left(2\sqrt{2} \cdot V_{AC,max} \cdot sin\theta - V_{OUT}\right)^2 \quad (87)$$
$$\cdot\ f_{sw}\left(V_{AC,\max},\ P_{OUT\_MAX}, \theta\right) d\theta = \frac{1}{\pi} \cdot \int_{\theta_1}^{\theta_2} \frac{1}{2} \cdot \left(2\sqrt{2 \cdot} 265V \cdot sin\theta - 400V\right)^2$$
$$\cdot\ f_{sw}(90V, 250W, \theta)\, d\theta \cong 0.26\ W$$

The total estimated losses for the power switch, at the minimum input voltage and maximum output power, is then (from Equation (59)):

Equation 88

$$P_{loss} = P_{cond}\left(V_{AC,min}, P_{OUT_{MAX}}\right) + P_{sw}\left(V_{AC,min}, P_{OUT_{MAX}}\right) \quad (88)$$
$$+ P_{cap}\left(V_{AC,min}, P_{OUT_{MAX}}\right) = 1.45W + 0.105W + 0W \cong 1.55\ W$$

To keep the junction temperature of the MOSFET below 125 °C ($T_{j\_MOSFET,max}$), it should be needed a heat-sink with a thermal resistance below (from Equation (70)):

Equation 89

$$R_{th} \cong \frac{T_{j\_MOSFET,max} - T_{amb,max}}{P_{loss}} = \frac{125℃ - 50℃}{1.55W} = 48\frac{℃}{W} \quad (89)$$

Output diode

Considering the criteria for the output boost diode (minimum 1.2*V_{OUT}=480 V and 3*I_{OUT_MAX}=1.875 A), the ultrafast high STTH5L06FP (in TO-220 AC insulated package) is selected (600 V/5 A). Considering that the rms current flowing in the output diode is (from Equation (72)):

Equation 90

$$I_{D\_RMS,max} = 2\sqrt{2}\cdot\frac{P_{OUT,max}}{\eta\cdot V_{AC,min}\cdot PF}\cdot\sqrt{\frac{4\sqrt{2}}{9\pi}\cdot\frac{V_{AC,min}}{V_{OUT}}} = 2\sqrt{2}\cdot\frac{250W}{0.94\cdot 90V\cdot 0.99}\cdot\sqrt{\frac{4\sqrt{2}}{9\pi}\cdot\frac{90V}{400V}} = 1.78\,A \quad (90)$$

and that the threshold voltage/dynamic resistance are around 0.89 V/33 mΩ (from datasheet), the estimated conduction losses results (from Equation (71)):

Equation 91

$$P_{diode} = V_{th_{diode}}\cdot I_{OUT} + R_{d_{diode}}\cdot {I_{D,RMS}}^2 = 0.89V\cdot 0.625A + 33m\Omega\cdot 1.78A^2 = 0.66\ \mathrm{W} \quad (91)$$

To keep the junction temperature of the diode below 125 °C ($T_{j\_diode,max}$), it should be needed a heat-sink with a thermal resistance below (from Equation (73)):

Equation 92

$$R_{th} \cong \frac{T_{j\_diode,max} - T_{amb,max}}{P_{diode}} = \frac{125°\mathrm{C} - 50°\mathrm{C}}{0.66W} = 113\frac{°\mathrm{C}}{W} \quad (92)$$

5.2 Biasing circuitry

Assuming a power dissipation P_d of 12 mW for the output resistors divider, the upper resistor R_{FB_H} is (from Equation (9)):

Equation 93

$$\mathrm{R_{FB\_H}} \cong \frac{{\mathrm{V_{OUT}}}^2}{\mathrm{P_d}} = \frac{400\mathrm{V}^2}{12\mathrm{mW}} = 13.3\ \mathrm{M\Omega} \quad (93)$$

An equivalent resistor of 12.9 MΩ is selected (three resistor of 4.3 MΩ in series to sustain the high voltage drop), then considering that the L6462A reference voltage V_{REF} is 2.5 V typ., the lower resistor R_{FB_L} results (from Equation (10)):

Equation 94

$$R_{FB\_L} = R_{FB\_H}\cdot\frac{V_{REF}}{V_{OUT} - V_{REF}} = 12.9M\Omega\cdot\frac{2.5V}{400V - 2.5V} = 81.13\ k\Omega \quad (94)$$

A value of 81.13 kΩ is selected (two resistors in parallel, 100 kΩ // 430 kΩ).

Current sense resistor

The minimum value of the OCP1 threshold, at the 90 V minimum input voltage, is $V_{CS\_OCP1,min}$=0.48 V (from the L6462A datasheet), then to respect the dynamic of the CS pin the maximum current sense resistor should be (from Equation (11)):

Equation 95

$$R_{S_{OCP1}} = V_{CS\_OCP1,min}\cdot\frac{\eta\cdot V_{AC,min}\cdot PF}{2\sqrt{2}\cdot P_{OUT,max}} = 0.48V\cdot\frac{0.94\cdot 90V\cdot 0.99}{2\sqrt{2}\cdot 250W} = 56\,m\Omega \quad (95)$$

The minimum value of the upper COMP pin voltage $V_{COMP,min}$ is 3.1 V (from the L6462A datasheet), then to respect the dynamic of the COMP pin the maximum current sense resistor should be (from Equation (12)):

Equation 96

$$R_{S\_COMP} = \left(V_{COMP,min} - 0.3\right)\cdot\frac{G_{CR,min}}{2}\cdot\frac{\eta}{P_{OUT\_max}}\cdot{\frac{V_{AC,min}}{V_{OUT}}}^2 = (3.1V - 0.3V)\cdot\frac{0.534}{2}\cdot\frac{0.94}{250W}\cdot\frac{90V^2}{400V} = 58m\Omega \quad (96)$$

where for minimum value of the equivalent multiplier gain G_{CR} for $V_{AC,min}$=90 V is 0.534 (see L6462A datasheet).

To guarantee both the previous two conditions, the current sense resistor R_S has to be selected equal or lower than the minimum, then an equivalent resistor of 55 mΩ is selected, composed by two resistors of 0.100 Ω and 0.120 Ω (metal film resistor, 1 W, 5%) in parallel to sustain the power dissipation.

Compensation network

The maximum output voltage ripple V_{OUT} is (from Equation (21)):

Equation 97

$$\Delta V_{OUT} = \frac{I_{OUT.max}}{2\pi \cdot f_{LINE} \cdot C_{OUT}} = \frac{0.625A}{2\pi \cdot 47Hz \cdot 180\mu F} = 11.76\,V \quad (97)$$

and the V_C control voltage set-point, calculated at the maximum input voltage and rated output power is (from Equation (7)):

Equation 98

$$V_C = \frac{2 \cdot R_S}{G_{CR}} \cdot \frac{P_{OUT}}{\eta} \cdot \frac{V_{OUT}}{V_{IN,rms}{}^2} = \frac{2 \cdot 55m\Omega}{0.125} \cdot \frac{250W}{0.94} \cdot \frac{400V}{265V^2} = 1.33V \quad (98)$$

where the internal equivalent multiplier gain G_{CR} for V_{AC}=265 V is 0.125 (see L6462A datasheet). Then to the third-harmonic distortion D_3 at 2.5%, the compensation network gain at 2*f_{LINE} has to be (from Equation (25)):

Equation 99

$$H_{2f} = \frac{2 \cdot D_3 \cdot V_C}{\Delta V_{OUT}/2} = \frac{2 \cdot 0.025 \cdot (1.33V)}{11.76V/2} = 0.011 \quad (99)$$

and the suggested C_{FP} capacitor results (from Equation (28) and considering g_{m_EA}=100 µS typ. from the L6462A datasheet):

Equation 100

$$C_{FP} = \frac{g_{m\_EA} \cdot R_{FB\_L}}{R_{FB\_L} + R_{FB\_H}} \cdot \frac{1}{2\pi \cdot 2f_{LINE} \cdot H_{2f}} = \frac{100\mu S \cdot 81.13k\Omega}{(81.13k\Omega + 12.9M\Omega)} \cdot \frac{1}{2\pi \cdot 2 \cdot 47Hz \cdot 0.011} = 93\,nF \quad (100)$$

Considering the Equation (32), the minimum required C_{FP} capacitor value to respect that ripple voltage at the COMP pin is lower than the valley skipping hysteresis is (considering 175 mV as maximum acceptable ripple voltage to achieve some margin versus 200 mV typ. hysteresis value):

Equation 101

$$C_{FP,min} = \Delta V_{OUT,max} \cdot \frac{R_{FB_L}}{\left(R_{FB_L} + R_{FB_H}\right)} \cdot \frac{g_{m_{EA}}}{2\pi \cdot \left(2 \cdot f_{LINE,min}\right) \cdot \Delta V_{COMP,max}} = 11.76V \cdot \frac{81.13k}{(81.13k + 12.9M)} \cdot \frac{100\mu S}{2\pi \cdot (2 \cdot 47Hz) \cdot 175mV} = 71\,nF \quad (101)$$

The selected value is C_{FP}=100 nF.

External ZCD network (optional)

Applying the Equation (34), the minimum required C_{rss} capacitor is:

Equation 102

$$C_{rss,min} = 200\mu A \cdot \frac{\sqrt{L_B C_d}}{(V_{OUT} - \sqrt{2}V_{AC,max})} = 200\mu A \cdot \frac{\sqrt{210\mu H \cdot 160pF}}{(400V - \sqrt{2} \cdot 265V)} = 1.45\,pF \quad (102)$$

Selected power MOSFET STF36N60M6 has a C_{rss}=6 pF typ. (see datasheet), then it is no needed to add an external C_{ZCD} - R_{ZCD} network.

6 References

[1] L6462A: “DS14885” datasheet on www.st.com

Revision history

Table 1. **Document revision history**

Date	Version	Changes
11-Mar-2026	1	Initial release.

Contents

List of tables

List of figures