The STPMIC1L PCB layout guidelines

Introduction

This application note aims to provide some information about the placement of the STPMIC1L on a 4-layer PCB 2s2p (JEDEC standard), paying attention to the routing tracks and the switching part with a high-current path.

Therefore, the correct PCB routing and component placement are key factors in a highly integrated power management, and the following topics must be considered:

- High-frequency switching currents due to the intrinsic behavior of inductor-based DC-DC conversion
- Signal integrity of the digital interface
- Thermal management of dissipated power

This document shares some tips regarding the layout rules to follow to design the STPMIC1L evaluation board. The order code of the kit is "STEVAL-PMIC1LKV1", which includes the STPMIC1L evaluation board "STEVAL-PMIC1LM1A" and the I²C USB interface "STEVAL-USBDNGV1".

1 Power section layout considerations

A PCB layout that follows the tips in this document is key for the design of switching power supply, due to high switching currents and sensitive control signals in the surrounding area. Increased power losses, output ripple, EMI emissions, and the possibility of inaccurate regulation are direct consequences of an improper layout of the power section of any DC-DC converter. Less common effects are induced noise on digital lines, loop instability, and audible acoustic noise from passive components. In rare cases, stray inductance of long traces may cause abnormal voltage spikes which, in turn, may stress the STPMIC1L above its maximum voltage ratings (AMR). In the following sections, the root causes of the critical current paths and some recommendations about how to limit their effects on STPMIC1L performance are provided.

1.1 General recommendations

- Always consider and determine where and how the return currents flow.
- As in all switching DC-DC converter configurations, the minimum length of critical traces is a key factor, as well as the use of ground and power planes.
- Reduce the use of vias along the critical current paths.
- Route analog signals in the analog section of the board only.
- Do not route analog signals (voltage feedback signal) over ground plane gaps.
- In case a ground or power plane must be split (for mechanical and or electrical reasons), do not place any trace across the gap on an adjacent layer.
- Never underestimate the importance of decoupling capacitors. Decoupling is the process of placing a capacitor as close as possible to the STPMIC1L to provide the transient switching current. In a DC-DC converter, it is the process of placing an L-C network near the STPMIC1L to minimize the trace inductances causing overvoltage spikes. If the spikes exceed the AMR value, the device may be damaged.
- A high-capacity value of the decoupling capacitors is important for low-frequency decoupling effectiveness, but it is less important at high frequencies, where the most important rule is to reduce the stray inductance in series with the decoupling capacitors.
- All passive components should be placed as close as possible to the STPMIC1L pins, but when this device packs many regulators in a small area, this can be difficult. A criterion for passive component placement is to determine their distance from the STPMIC1L by following the priority list below, starting with the shortest distance:
  1. Input capacitors of each buck converter
  2. Input capacitors for each LDO and device power supply (V_{IN}, INTLDO…)
  3. Inductors for each DC-DC converter
  4. Output capacitors of each buck converter
  5. Output capacitors for each LDO regulator
- Grouping and orientation of capacitors should be carried out so that the ground side of the input capacitor and output capacitor of each DC-DC are very close to each other.
- The positive side of the output capacitor must be placed as close as possible to the inductor, and to its connection point. The voltage feedback trace should start towards the VOUT pin.

1.2 Buck converter critical current paths

Figure 1 and Figure 2 show the simplified schematic of a buck converter. The green/orange lines show the critical paths of switching currents during the inductor charging/discharging phases.

Figure 1. Buck converter schematic (charging phase)

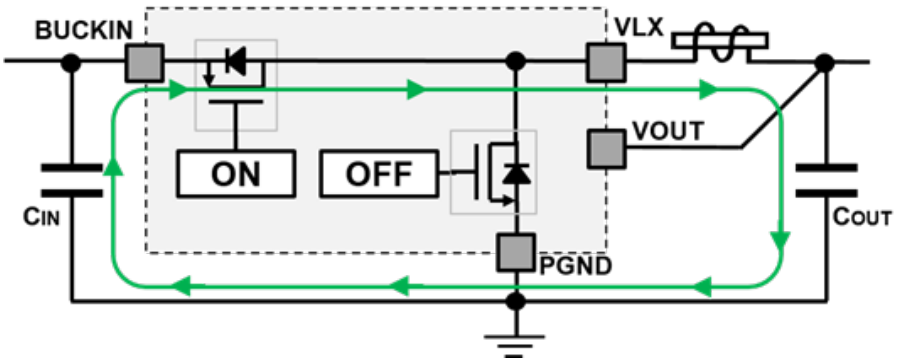
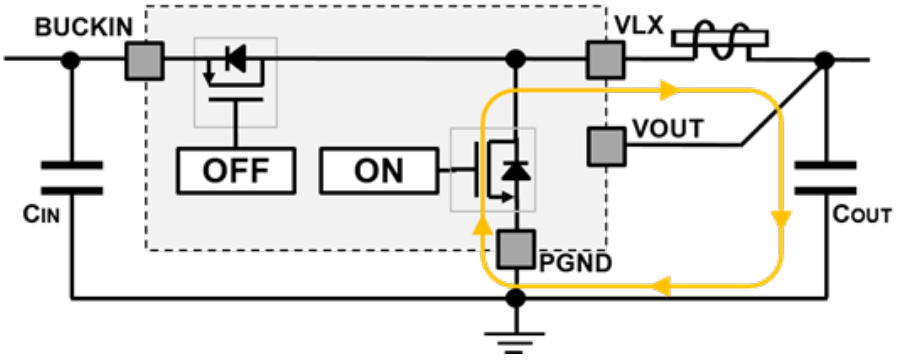


Figure 2. Buck converter schematic (discharging phase)



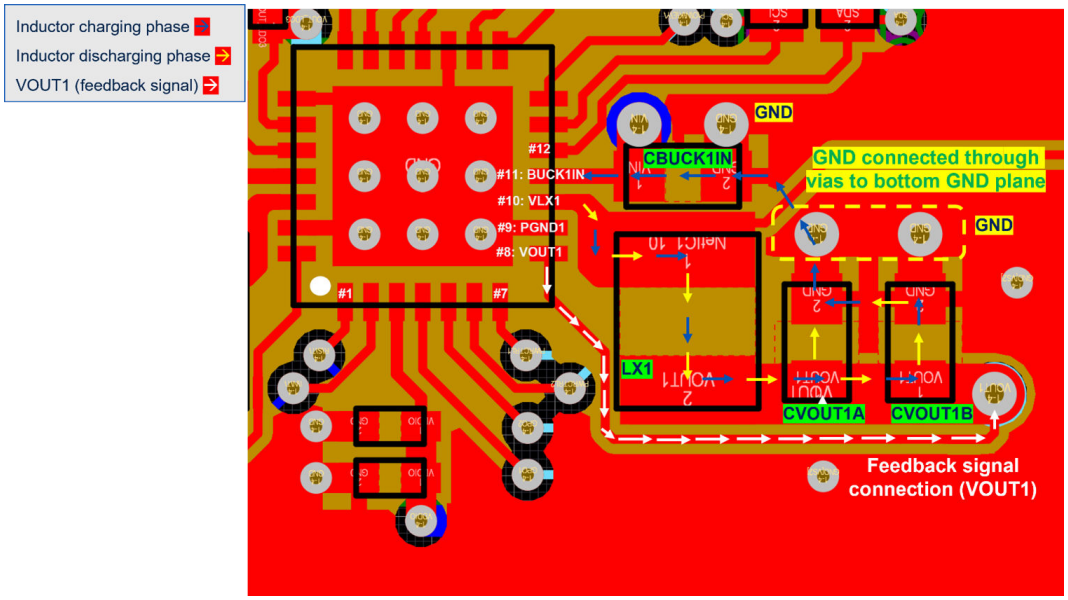
The capacitors and inductors should be placed as close as possible to the STPMIC1L device and routed with both wide and short traces. The input capacitor is the most critical component to be placed in the PCB layout. It must be placed as close as possible to the BUCKIN pin and the related PGND pin, to minimize GND loop. If properly routed, the input capacitor cuts the high voltage spikes produced by the switching activity of the device.

The output capacitor should be placed close to the inductor. It is recommended to connect at a single common point or directly to the ground plane using the appropriate number of vias:

- The ground side of the output capacitor
- The ground side of the input capacitor
- The PGND pin of the device

The output voltage feedback signal should be taken directly at the output capacitor and routed to the VOUT pin (feedback signal), avoiding noisy nets. To minimize noise pick-up, its trace should be tiny, placed away from switching traces. It is preferable to route it on a separate layer, shielded from switching lines by the ground plane, as shown in Figure 3.

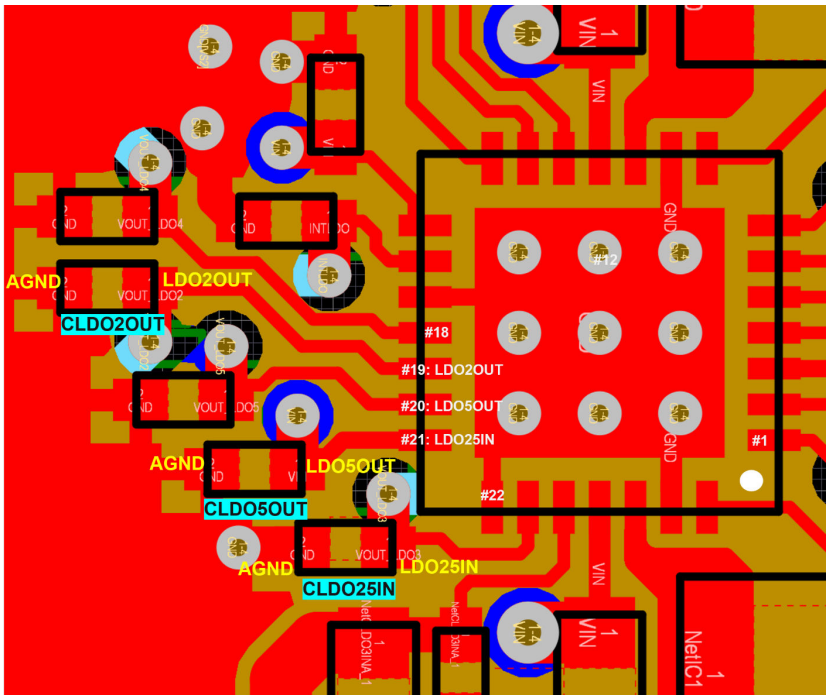
Figure 3. **Buck1 reference routing with critical paths**



1.3 LDOs

LDOs are not solely affected by the switching noise activity, but since they are physically very close to the active buck converters, the injected noise can be an issue. For this reason, each LDO supply should be filtered by a decoupling capacitor placed as close as possible to the input pin of the related LDO. Besides, to ensure the best performance, the output capacitor should be placed close to the LDO output, possibly with its ground side far away from any switching ground return, to avoid any noise injection.

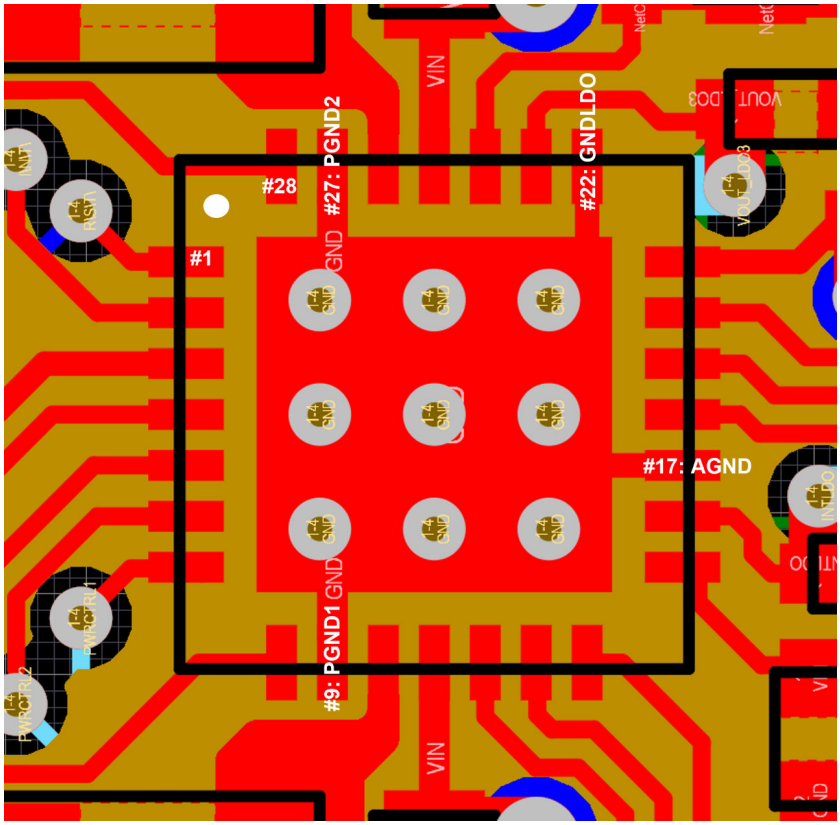
Figure 4. **LDO2 and LDO5 reference routing**



1.4 Connection between exposed pad and GND pins

The power GND pins (PGND1 pin#9 and PGND2 pin#27), the GNDLDO pin#22 and the AGND pin#17 have been connected to the exposed pad through direct tracks in the top layer, as shown in Figure 5.

Figure 5. Connection between exposed pad and power/analog GND pins



1.5 Thermal considerations

The package of the STPMIC1L is a VFQFPN 28L 4.0 x 4.0 x 1.0 mm with an exposed pad (ePad), which helps the thermal power dissipation of the device. In the PCB, a group of about a dozen thermal vias carry the heat away from the IC. It is strongly recommended that a minimum of 9 via holes (ground-fill) be put underneath the ePad of the device, since the PCB acts as a heat-sink by mainly using the ground plane for improved thermal power dissipation.

The exposed pad solder area can be segmented into a symmetric pad array, by applying the solder paste to approximately 50% to 75% of the area of the exposed pad.

Figure 6 and Figure 7 show the STPMIC1L package bottom, side, and top views and the recommended footprint outline.

Figure 6. **STPMIC1L package**

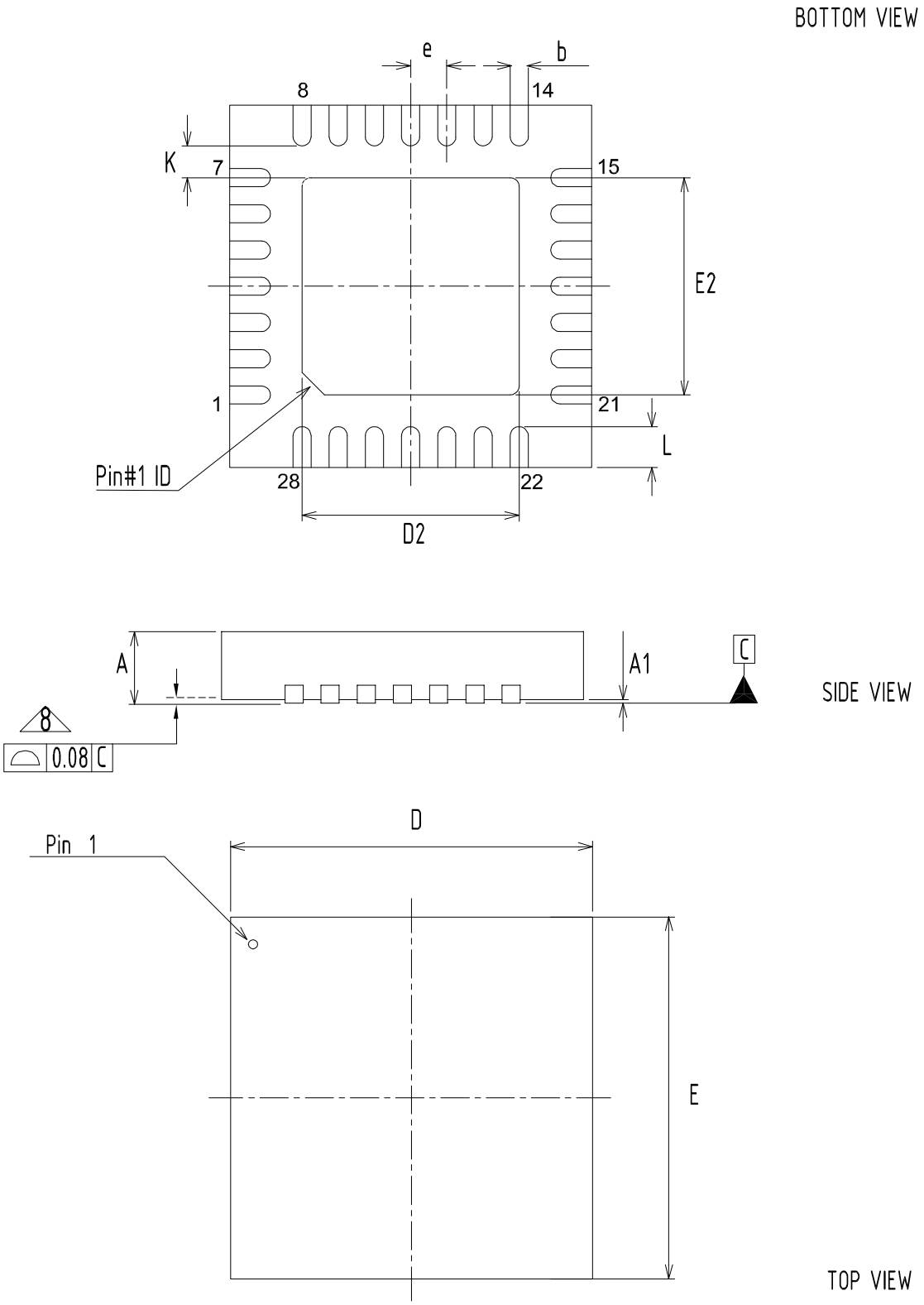


Figure 7. **STPMIC1L recommended footprint outline**

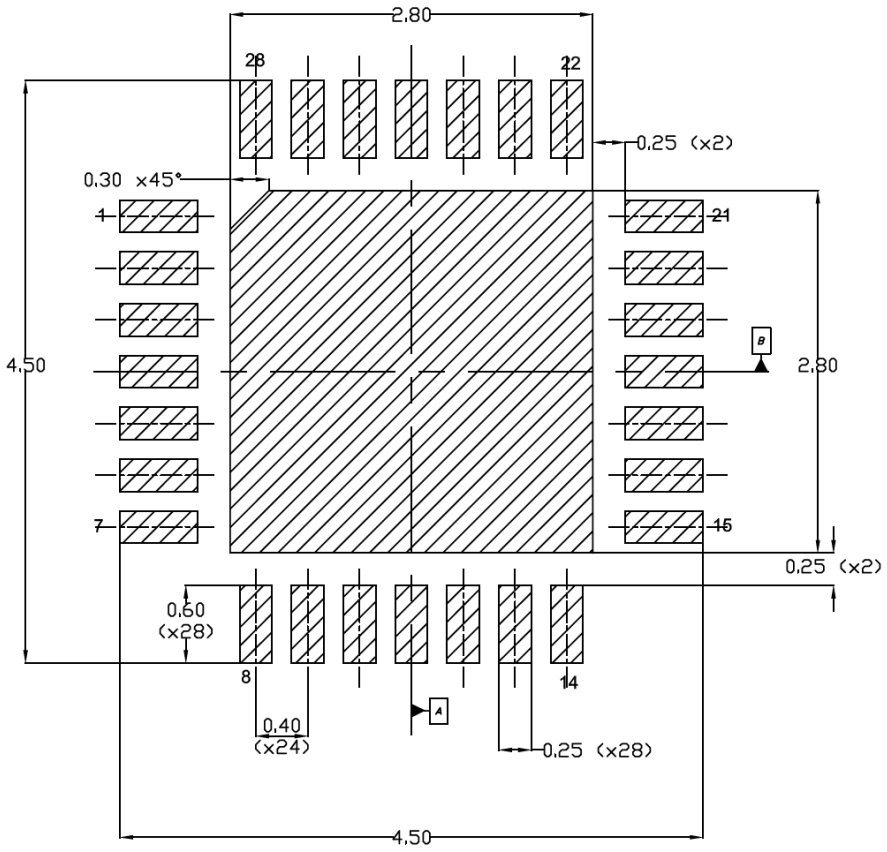
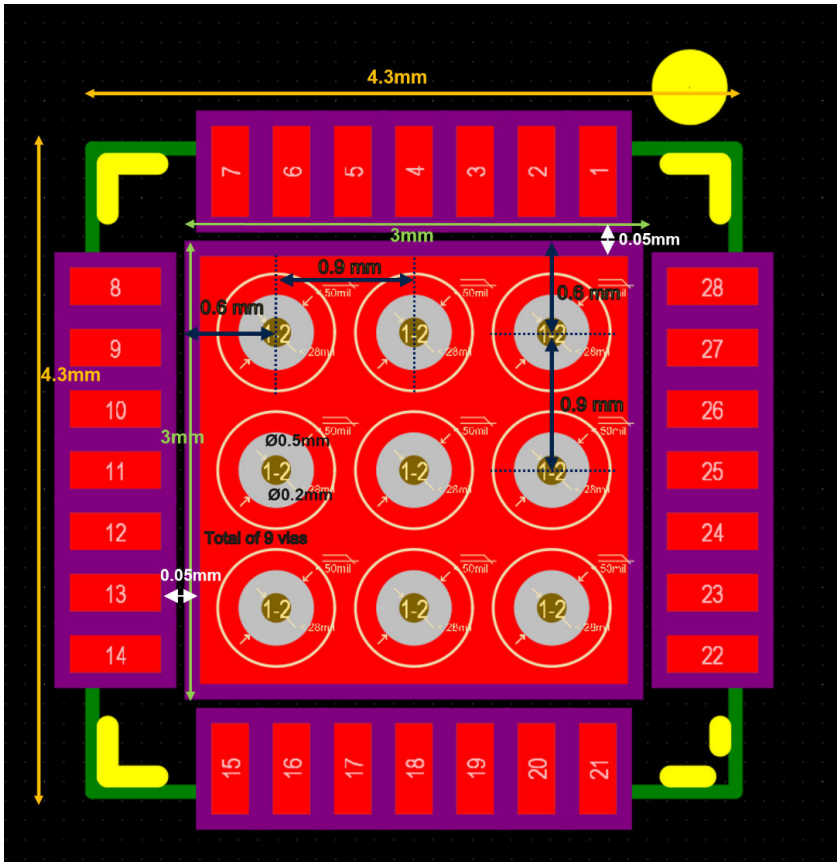


Figure 8 shows the footprint that was used in the STPMIC1L evaluation board for the VFQFPN package 4.0 x 4.0 x 1.0 mm and the arrangement of the thermal pads over the exposed pad.

Figure 8. Exposed pad and via placement on the TOP layer of the STPMIC1L evaluation board layout



As shown in Figure 8, STMicroelectronics suggests surrounding each pad with a 0.06 mm wide solder mask to prevent solder bridging.

For the thermal pads, a symmetric matrix of 3x3 vias was designed. It is strongly recommended that a minimum of 9 via holes (ground-fill) be put underneath the ePad of the device, since the PCB acts as a heat-sink by mainly using the ground plane for improved thermal power dissipation.

STMicroelectronics recommends placing thermal vias in the solder mask defined thermal pad to effectively transfer the heat from the top copper layer of the PCB to the inner or bottom copper layers. The recommended via external diameter is 0.5 mm or less, the internal hole diameter is 0.2 mm, and the recommended via spacing is 0.9 mm along the x and y axes.

2 Digital interface layout considerations

To avoid noise injection on the digital signals caused by the switching activity of the DC-DC converters, it is good practice to shield the digital traces using ground planes placed on adjacent layers. Additional recommendations are:

- Partition mixed-signal PCBs into separate analog and digital sections.
- Route digital signals only in the digital section of the board (I^2C BUS).
- If ground or power planes must be split for specific mechanical and/or electrical reasons, do not place any traces across the gap on an adjacent layer.
- The digital decoupling capacitor for the VIO pin should be connected directly to the digital ground if the VIO is supplied far away from the STPMIC1L.

3 PCB example: the STPMIC1L evaluation board layout

The STEVAL-PMIC1LKV1 evaluation board is based on a 4-layer PCB (2s2p) compliant with the JEDEC standard.

Figure 9 shows the PCB stack-up layer used for the STPMIC1L evaluation board.

Figure 9. STPMIC1L evaluation board: PCB stack-up layers

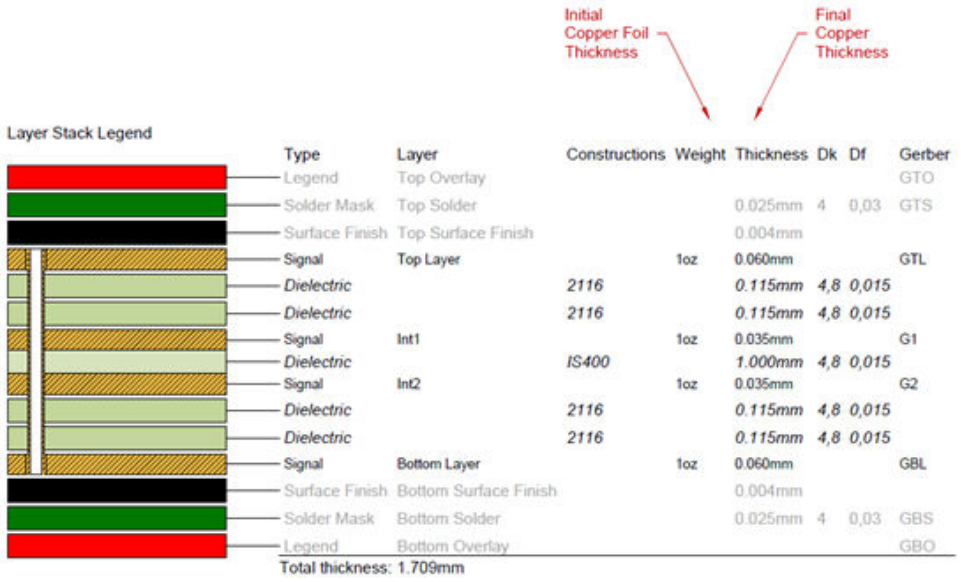


Table 1. STEVAL-PMIC1LKV1 evaluation board: stack-up layer details

Layer	Stack-up
Top	Component/power/signal
Internal 1	GND
Internal 2	Power/GND
Bottom	Power/GND

The following pictures show the board layout of the STPMIC1L evaluation board. All the guidelines described in the previous sections were applied to the design of the board to ensure the STPMIC1L achieves its best performance.

Figure 10. STEVAL-PMIC1LKV1 evaluation board: 3D layout

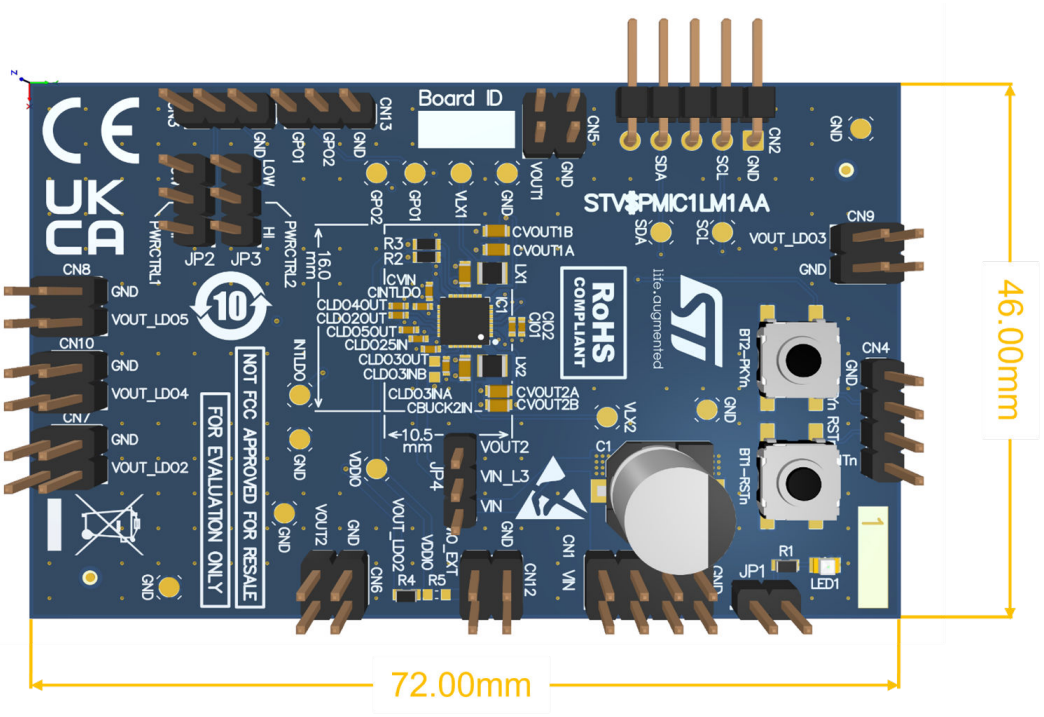


Figure 11. STEVAL-PMIC1LKV1 evaluation board: top layer (components/power/signal)

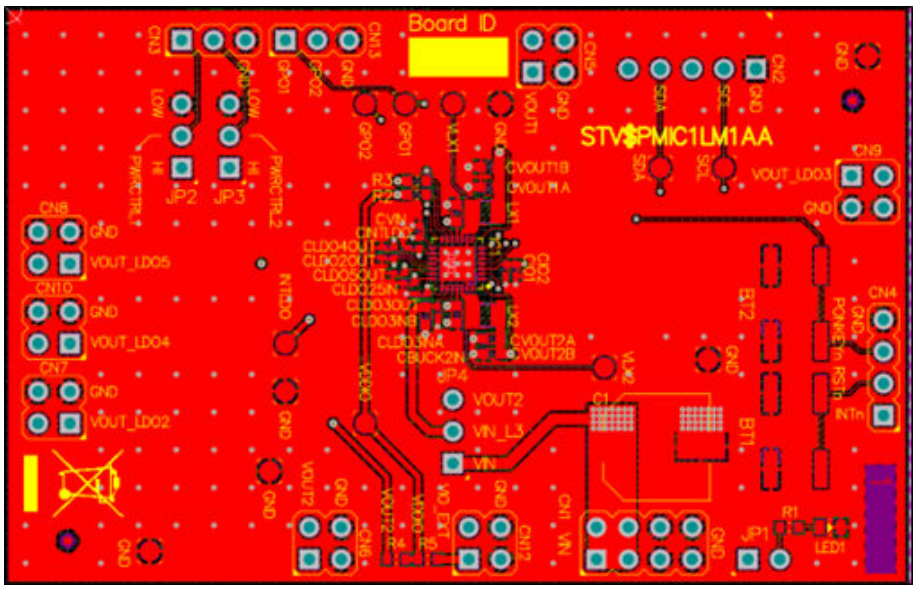


Figure 12. **STEVAL-PMIC1LKV1 evaluation board: internal layer 1 (GND)**

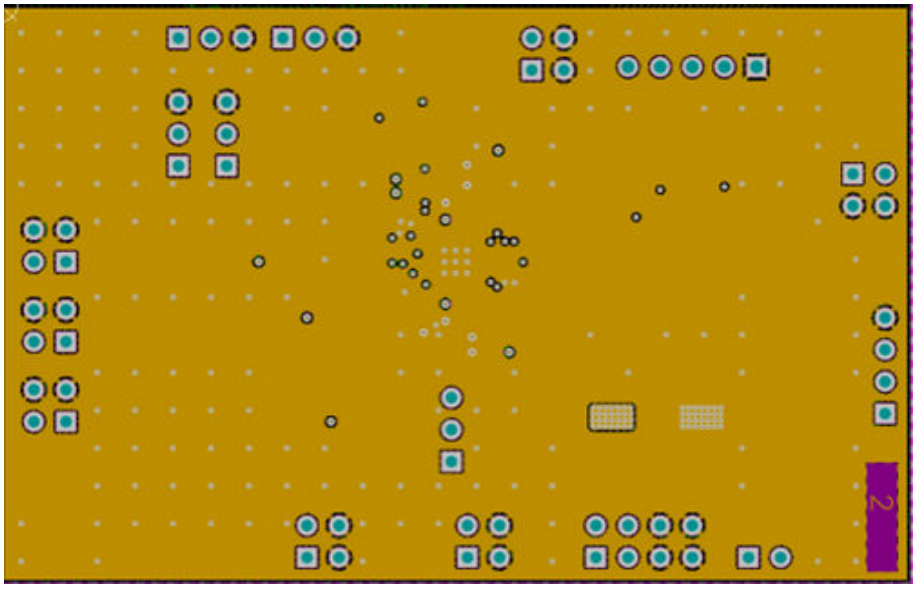


Figure 13. **STEVAL-PMIC1LKV1 evaluation board: internal layer 2 (Power/GND)**

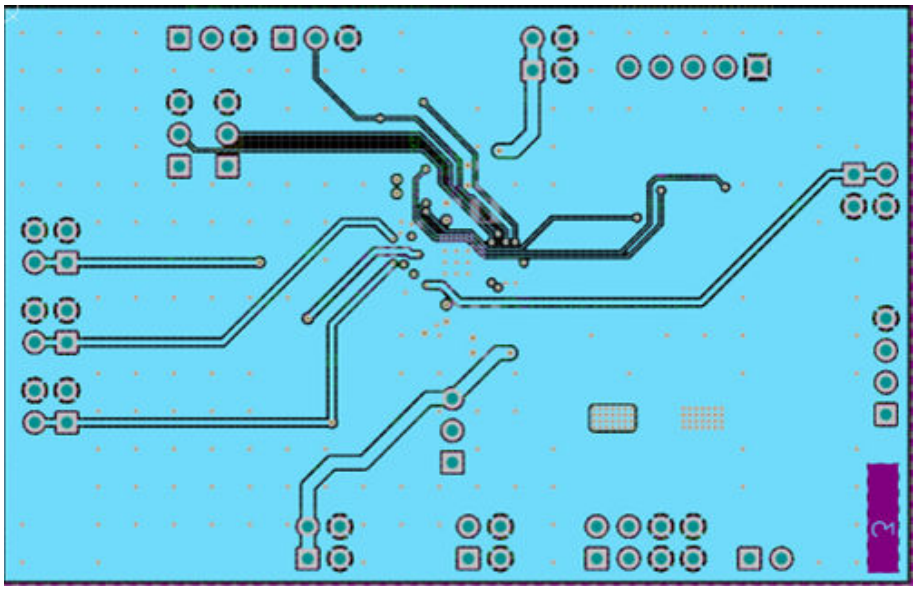
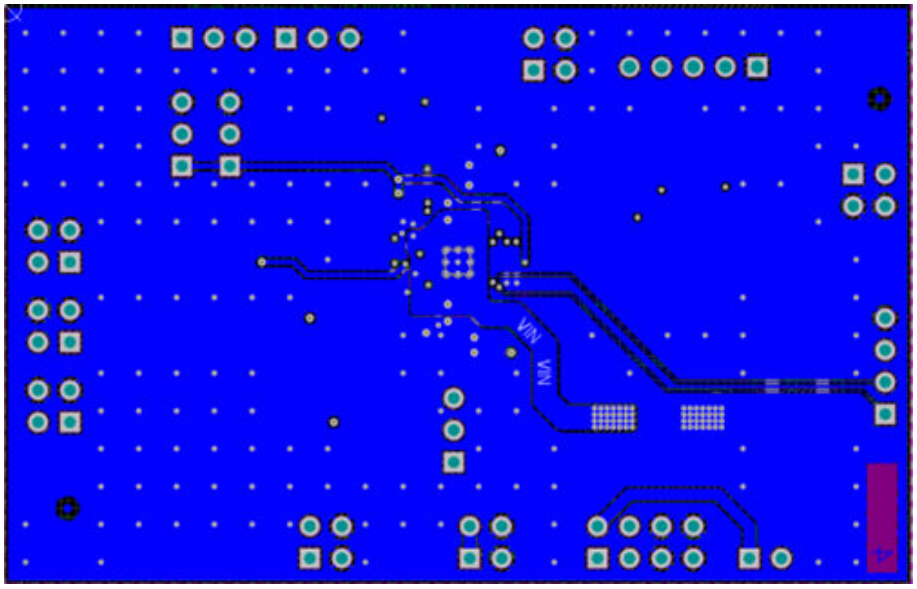


Figure 14. **STEVAL-PMIC1LKV1 evaluation board: bottom layer (Power/GND)**

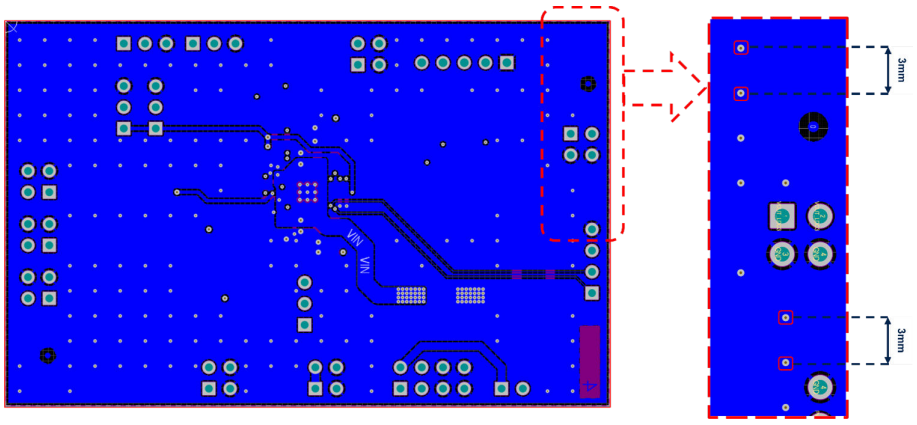


3.1 Power and ground planes

Since both POWER and GROUND are planes, inductive effects are minimized, providing a very low-impedance path to the STPMIC1L. The use of a continuous ground layer with multiple via holes is an effective way to achieve low-impedance ground returns. However, to maintain low impedance across all areas of the PCB, the continuous ground layer should never be narrowed or partitioned.

Figure 15 shows the internal layer 1 of the STPMIC1L evaluation board layout, with details of the GND vias placed all around the PCB edge with 3 mm spacing.

Figure 15. **Internal layer 1 (GND plane)**



The usage of flat and large plane shapes, if possible, is recommended for all high-current power supplies such as V_{IN} and V_{OUT}. This helps to reduce power losses. When examining the ground and power planes, make sure that plane continuity is not affected by an excessive number of vias.

Examples of power planes, via placement and plane shapes are shown in Figure 13 (internal layer 2), in which they are used to route V_{IN} and all V_{OUT} of the regulators to the connector headers.

3.2 Via holes

Although the ground plane provides a good ground reference, the presence of vias along ground returns introduces some stray inductance at high frequencies. Placing multiple via holes in a plane reduces this effect, since the stray inductances act in parallel. These via holes must be spaced in such a way that the power plane is not excessively cut up.

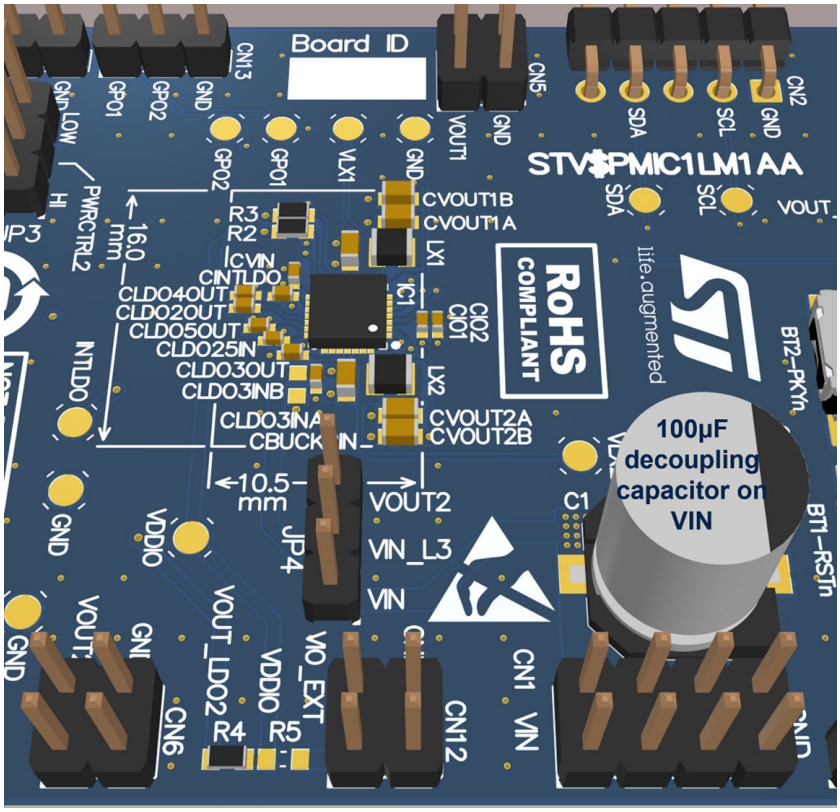
Table 2.

Via type	Hole size	Pad size
Via holes	0.2 mm	0.5 mm

3.3 Passive component placement around the STPMIC1L in the evaluation board

Figure 16 shows the STPMIC1L passive component arrangement (input and output capacitors, output coils, and resistors) around the STPMIC1L in the evaluation board. The aim was to shrink the total BOM into the smallest area around the STPMIC1L device (10.5 x 16 mm).

Figure 16. **STEVAL-PMIC1LKV1 evaluation board: passive component placement in the top layer**



All the suggestions described in this application note were followed in the STPMIC1L evaluation board.

Moreover, it is good practice to put all passive components on the top of the layout and to use the bottom side only if it is really necessary due to the application/board size.

A decoupling capacitor of 100 µF was placed on the input supply rail for two reasons:

- In case there is an input voltage drop, it provides adequate power to the STPMIC1L to maintain the voltage level.
- In case there is a voltage surge, it prevents the excess current from flowing through the STPMIC1L to keep the voltage stable.

Revision history

Table 3. **Document revision history**

Date	Version	Changes
22-Oct-2025	1	Initial release.

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