# L9965A/L99BM218 hardware design guide

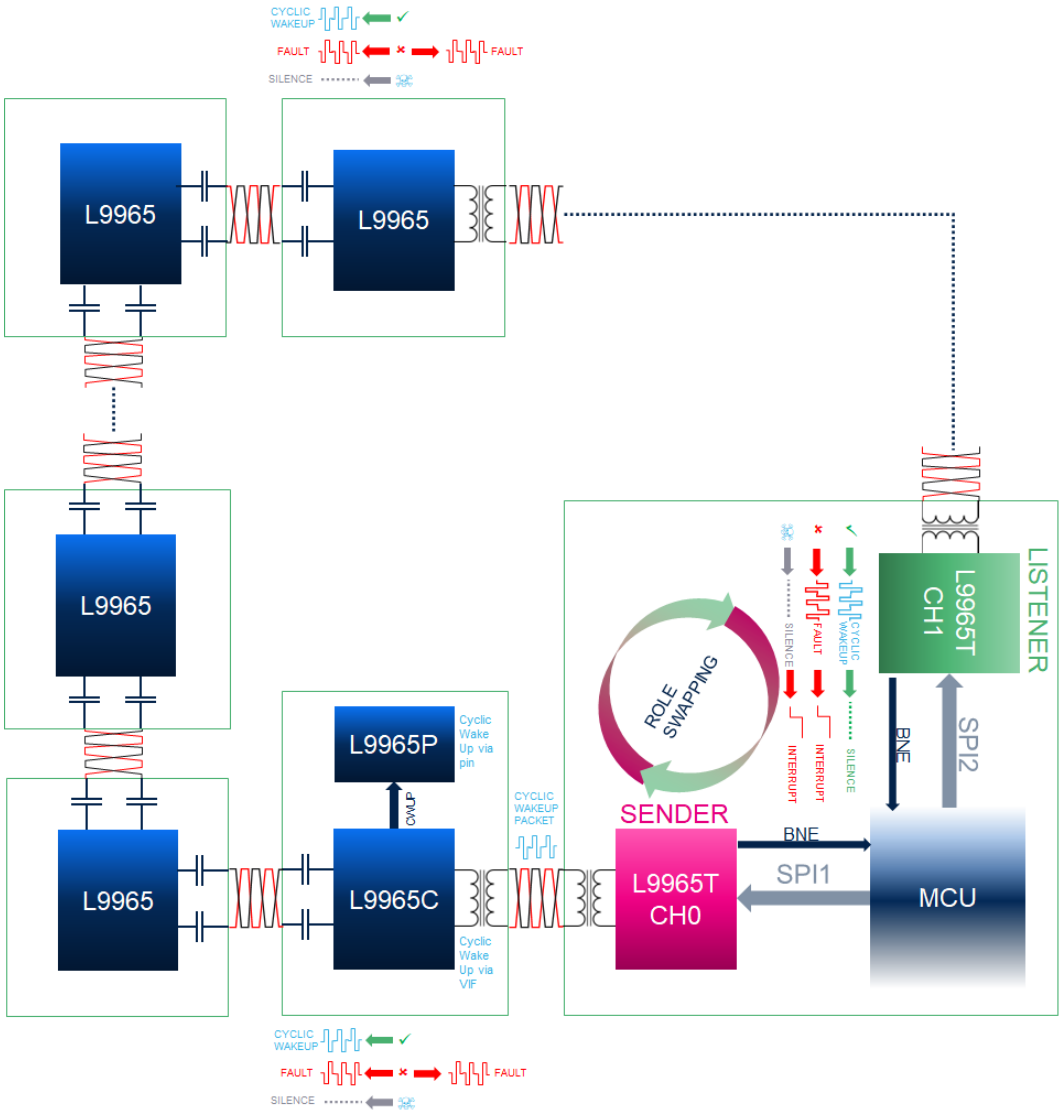
## Introduction

This document describes how to use the L9965A/L99BM218 with related components on a PCB to implement a contact-monitoring cells application.

The L9965A/L99BM218 (analog front end) provides:

- 18 independent ADC for cell voltage monitoring
- 10 GPIOs for temperature sensing using NTCs or absolute measurements for other sensors
- 18 integrated power-MOSFETs for passive balancing
- 1 dedicated ADC for bus bar monitoring
- Isolated serial communication interface (VIF)
- Integrated switching buck pre-regulator (VPRE)
- Integrated 5 V LDO (V5V) to supply external sensors (e.g. NTC)

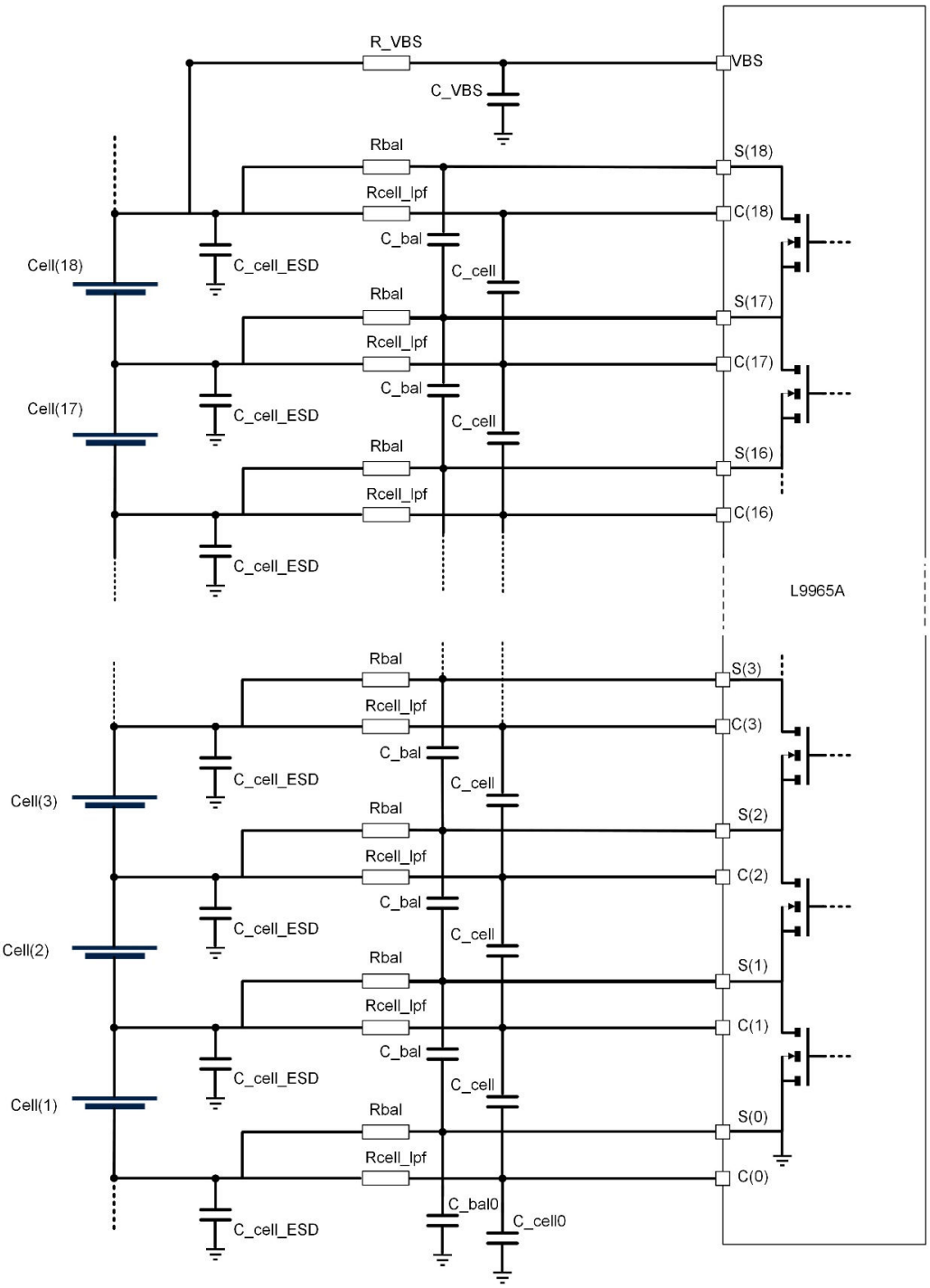
**Figure 1. Typical system configuration (dual ring)**



# 1 L9965A/L99BM218 hardware design guide

## 1.1 Cell voltage measurement and cell passive balancing

Figure 2. **Cell monitor and balancing circuit**



### 1.1.1 Cell voltage measurement

The device has a dedicated ADC for each C(x) pin to measure the differential voltages across the cells.

The $R_{CELL}$ and $C_{CELL}$ can be chosen according to the indications in Table 1. The cutoff frequency shall be sized according to application requirements. The IC has been characterized for noise and BCI immunity using the BOM in Table 1. A higher cutoff frequency means more external noise coupled to the IC pins, hence noisier measurements.

The $R_{CELL}$ can be incremented ensuring that no open load on Cell1 occurs during the open load diagnostic. Please refer to the document AN – open load diagnostic.

### 1.1.2 Cell balance

For the passive balancing, there is an integrated FET positioned between each S(x) and S(x-1) pins. $R_{BAL}$ shall be sized according to the target balancing current considering the max cell voltage and FET's AMR$I_{BAL}$ *(MAX)*.

Assuming the desired balance current $I_{BAL}$ *(MAX)* is known, the $R_{BAL}$ must be sized as follows:

$$I_{BAL} = \frac{V_{CELL}}{(2R_{BAL} + R_{DSON})} \quad (1)$$

$$R_{BAL} = \frac{\frac{V_{CELL}}{I_{BAL}} - R_{DSON}}{2} \quad (2)$$

Considering a cutoff frequency of 100 kHz, the capacitor of each differential channel S(x) is $C_{BAL}$=68 nF.

$$f_{cutoff} = \frac{1}{(2\pi * 2R_{BAL} * C_{BAL})} \quad (3)$$

The device is able to sustain +/- 8 kV ESD according to ISO 10605, system level network 150 pF/330 ohm, using $C_{CELL\_ESD} \geq 22$ nF.

### 1.1.3 Battery sensing

The ADC positioned on VBS is used for a single-ended measurement; consequently, the filtering capacity is referred to the ground and sized to sustain the $V_{BAT}$, 3 kHz is the suggested cutoff frequency, estimated with the formula:

$$f_{cutoff} = \frac{1}{(2\pi * R_{VBS} * C_{VBS})} \quad (4)$$

## 1.2 GPIO

The GPIO can be used as:

- NTC temperature measurement (Ratiometric)
- GPIO generic analog input (Absolute)

### 1.2.1 NTC temperature measurement

Using NTC sensors, the GPIO has to be configured as “Analog input ratiometric” by setting the field GPIOx_CONF=0b01 in the register GPIO_CONF_x.

The NTC's voltage divider must be supplied by the V5V regulator by means of the pull-up resistor $R_{PUNTC}$ chosen according to the NTC variable resistance. The GPIOs measure the voltage drops on the NTCs according to Figure 4.

Using a first order filter stage can be useful to improve measurement results and filter possible noise.

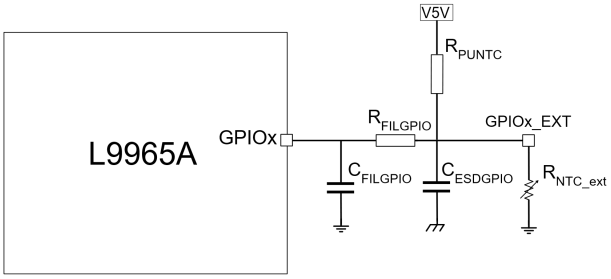
As an example, for an $R_{NTC\_EXT}$ with a max resistance of 10 kΩ, possible values for the components can be:

$R_{PUNTC}$= 10 kΩ;

$R_{(FIL\_GPIO)}$= 3.3 kΩ;

$C_{(FIL\_GPIO)}$= 100 nF;

**Figure 3. GPIO used as NTC**




GPIOs connected to external NTCs shall withstand short circuit to VB maximum operating voltage by means of external series resistors, keeping the injected current below 20 mA (a reasonable value to keep the device input safe).

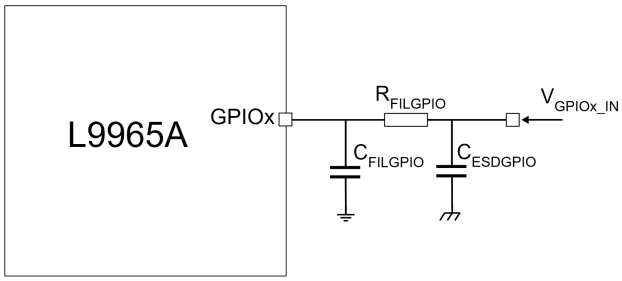
The unused GPIOs must be connected directly to GND as explained in the unused pin section of the product specification.

Optional ESD capacitor $C_{ESDGPIO}$ can be used to improve ESD immunity performance. A typical suggested value is $C_{ESDGPIO}$ = 6.8 nF to be placed as near the GPIO connectors as possible. The device is able to sustain +/- 8 kV ESD according to ISO 10605, system level network 150 pF/330 ohm, using $C_{ESDNTC}$.

### 1.2.2 GPIO generic analog input

The GPIOs can also be used to convert any $V_{GPIOx\_IN}$. In this case, GPIOx must be configured as an analog absolute input by setting the field GPIOx_CONF=0b00 in the register GPIO_CONF_x.

**Figure 4. GPIO used as analog absolute input**



## 1.3 Battery supply

The L9965A/L99BM218 is supplied from the VB pin, which must be connected to the topmost cell of the stack.

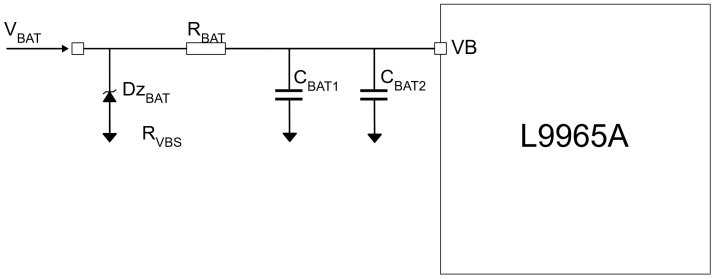
As reported in the datasheet, it is recommended to place a series resistance on the VB pin to protect it from hot plug inrush currents. A suitable value can be $R_{BAT}$= 10 Ω, to keep the total resistor voltage drop below 1 V.

As an additional protection for the VB pin, to avoid violation of the AMR voltage, it is recommended to add a diode $D_{ZBAT}$ as shown in . The diode's breakdown voltage value is chosen according to $V_{VB}$ AMR. a good candidate can be SM30T100AY. This component should be placed as near as possible to the $V_{BAT}$ connector.

To filter out possible supply noise, capacitors $C_{BAT1}$= 4.7 uF and $C_{BAT2}$= 100 nF are placed on the $V_{BAT}$ path. Both capacitors should be placed as close as possible to the VB pin.

When choosing a capacitor component, please take care of the DC bias effect.

**Figure 5. Battery supply**




## 1.4 VIF

The BMS controller can communicate with other devices in the daisy chain by means of the VIF (Vertical Isolated Interface).

Interconnections between modules can be realized either with UTP (Unshielded Twisted Pair) or STP (Shielded Twisted Pair). The recommended AWG is between 22 and 26, and the recommended cable length is up to 10 meters.

Two different isolation methods are supported:

- Capacitive isolation
- Inductive isolation

In case of capacitive isolation uses series capacitor on the ISO pins, it is recommended to use a 6.8 nF capacitor as $C_{ISO}$ . Keep tolerance low to avoid generating unwanted differential signals due to capacitor mismatches.

The capacitor voltage rating shall be sized according to the maximum isolation voltage to be guaranteed in the application:

- 100 V for adjacent devices
- 1 kV is recommended for other cases (this value can be chosen according to the max voltage of the battery pack).

In case of inductive isolation, a transformer between the ISOx_P and ISOx_M can be used. ST recommends using the transformer ESMIT- 4180/C, which shows a dielectric breakdown isolation of at least 3750 V.

A low pass filter can be added to ISOx_P and ISOx_M pins to reject noise and improve protection against the hot plug events and fast transients ($R_{ISO}$= 39 Ω, $C_{FIL}$= 100 pF). Consider sizing the filtering capacitor $C_{FIL}$ with a breakdown voltage of 25 V as suggested by the datasheet.

The use of TVS on external VIF lines is recommended as additional protection; the sizing depends on the system and can be defined on a case-by-case basis.

An optional CMC can be added to improve possible EMC issue (a suitable value is 100 uH).

Figure 6. **Isolated Vertical Interface (VIF) with capacitive isolation**

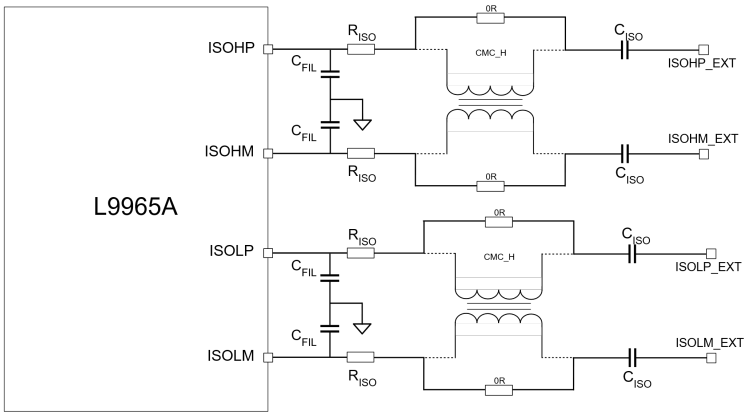
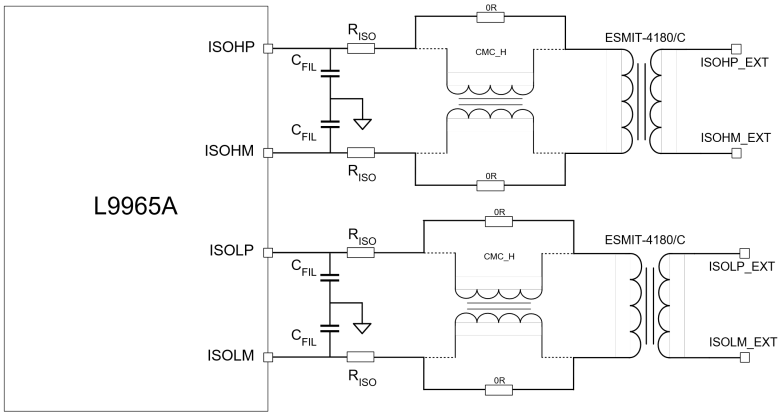



Figure 7. **Isolated Vertical Interface (VIF) with inductive isolation**

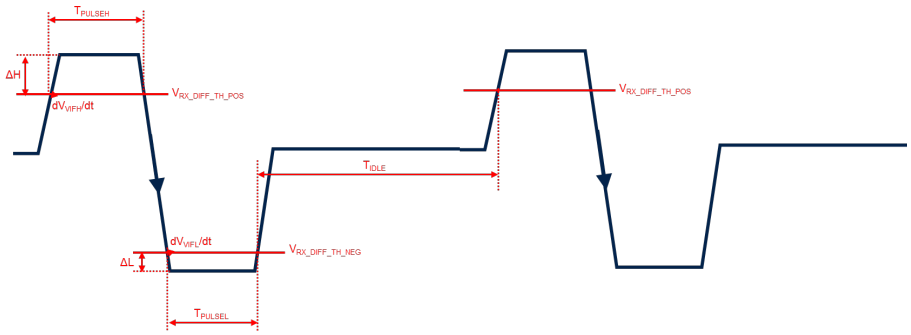


### 1.4.1 VIF signal integrity assessment

The VIF protocol is Manchester-encoded, meaning that bit ‘1’ or ‘0’ are represented using low==>high transitions or vice versa. The VIF decoding is based on analog differential comparators using fixed thresholds.

Figure 8 reports a reference differential waveform (ISOxP - ISOxM) encoding two consecutive bit.

**Figure 8. VIF differential waveform evaluation criteria**




Having defined $V_{VIF}$ as $V_{ISOxP}$-$V_{ISOxM}$, to be correctly interpreted by the receiver, a waveform shall satisfy the following criteria:

- Amplitude: pulse absolute peak value shall be 20% above receiver thresholds

$$\begin{cases} |\Delta H| \geq 1.2 \quad |V_{RX_{DIFFTH_{POS}}}| \\ |\Delta L| \geq 1.2 \quad |V_{RX_{DIFFTH_{NEG}}}| \end{cases} \tag{5}$$

- Duration: pulse duration shall be enough to allow comparator toggling within the expected time

$$\begin{cases} T_{PULSEH} \geq 45ns \\ T_{PULSEL} \geq 45ns \end{cases} \tag{6}$$

- Slope: pulse shall cross thresholds with a slope higher than the minimum specified to allow comparator toggling within the expected time

$$\begin{cases} \frac{dV_{VIFH}}{dt} \geq 0.2\frac{V}{ns} \\ \frac{dV_{VIFL}}{dt} \leq -0.2\frac{V}{ns} \end{cases} \tag{7}$$

- Idle: pulse differential amplitude shall be below both thresholds for a certain time interval to enable a correct symbol end condition

$$\begin{cases} V_{VIF} < V_{RXDIFFTHPOS} \\ V_{VIF} > V_{RXDIFFTHNEG} \end{cases} \quad for \quad T_{IDLE} > 110ns \tag{8}$$

A waveform not respecting such constraints may not be decoded correctly, leading to communication error detection.

VIF components listed in the Table 1 have been extensively validated in application and during EMC trials, and are recommended for a correct communication. Usage of different components is possible. However, the signal integrity shall be re-assessed during system trials.

### 1.4.2 Imbalance due to a VIF port disabled

In single-access daisy chains, the ISOH VIF port of the topmost device is unused and shall be terminated as prescribed in the Section 1.6 paragraph. User software can decide whether to keep this port closed or leave it enabled, based on consumption imbalance considerations.

The SoC imbalance due to one device in the stack having a VIF port disabled is totally negligible most of the times. It only becomes significant if small packs with low capacity are used.

For instance, consider the following system example:

- Suppose to have a single-access daisy chain with N stacked devices. User SW may disable the topmost device ISOH port, as no L9965T/L99BM2T is listening on the other side.
- Suppose to have a 100 ms thread collecting all cell voltage/temperature from the AFEs.
- Suppose to have a 400 V system with N = 7 stacked L9965A/L99BM218. The worst case happens when the pack capacity is small. A reasonably small 400 V system would store 10 kWh energy, thus having a 25 Ah capacity. Then, 1% of SoC corresponds to 0.25 Ah.

If using burst read, the communication loop time to recover all information will be <10 ms, so bus duty-cycle will be < 10%

However, the actual duty-cycle where ISOH/ISOL ports are transmitting is < 1%, due to interframe delays and VIF physical layer.

This 1% VIF TX duty-cycle is the parameter to account for calculating imbalancing.

Suppose all the AFEs are programmed with BIDI_ANSW = 1, except the last one, for which ISOH was disabled. In principle, this is not needed for a single-access chain. However, to compensate for VIF communication imbalance as much as possible, keeping BIDI_ANSW enabled is the right thing to do.

The main differences between the topmost L9965A/L99BM218 and the other ones are:

- When receiving an SoC command, it won't be propagated upwards. This corresponds to 5.125 us inactivity time of the ISOH port
- When receiving a burst read command, it won't be propagated upwards. This corresponds to 7 x 5.125 us inactivity time of the ISOH port
- When each AFE sends burst read data back to the XCVR, the LAST AFE will not propagate it upwards. This corresponds to ~14x100 us inactivity time of the ISOH port

The total inactivity time of the ISOH port of the last AFE can be estimated as 1.441 ms in a 100 ms loop time.

The amount of charge difference can then be estimated considering the typical ISO port transmitter consumption: 8.5 mA * 1.441 ms = $3.402*10^{-9}$ Ah. Such imbalance cumulates at each communication cycle.

With the calculated imbalance per cycle due to VIF, $7.3486*10^{7}$ communication cycles are needed to cumulate a 1% SoC imbalance (0.25 Ah). If communication cycle loop time is 100 ms, this corresponds to $7.3486*10^{6}$ seconds, which is $2.0413*10^{3}$ hours, thus ~85 days.

The days to have a 1% SoC imbalance would proportionally increase with pack capacitance. Therefore, the imbalance due to a VIF port disabled can be considered totally negligible in respect to cell self-discharge performances, which are something like ~10% in a month. In fact, since cells are not perfectly matched, it is reasonable to assume that imbalance cumulated due to self-discharge mismatch is significantly higher in a 30-day timespan.

To conclude, leaving ISOH port disabled will not imbalance packs in a significant way. However, leaving ISOH port enabled and terminated as prescribed, can be helpful when dealing with small capacity packs.

## 1.5 VPRE

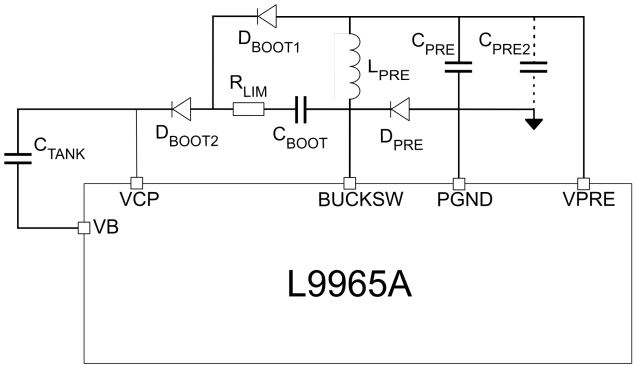
The VPRE pin is the output pin of the integrated buck regulator.

Its tank capacitor is sized with $C_{PRE}$= 4.7 uF, considering a minimum dielectric breakdown voltage of 100 V according to VPRE AMR value.

The buck converter inductor should have an inductance value $L_{PRE}$= 47 uH with saturation current up to 220 mA.

An additional $C_{PRE2}$= 10 nF capacitor on the VPRE pin can be added if needed.

Figure 9. **BUCK regulator**




## 1.6 Unused pins

The external connector must be designed to comply with the rules:

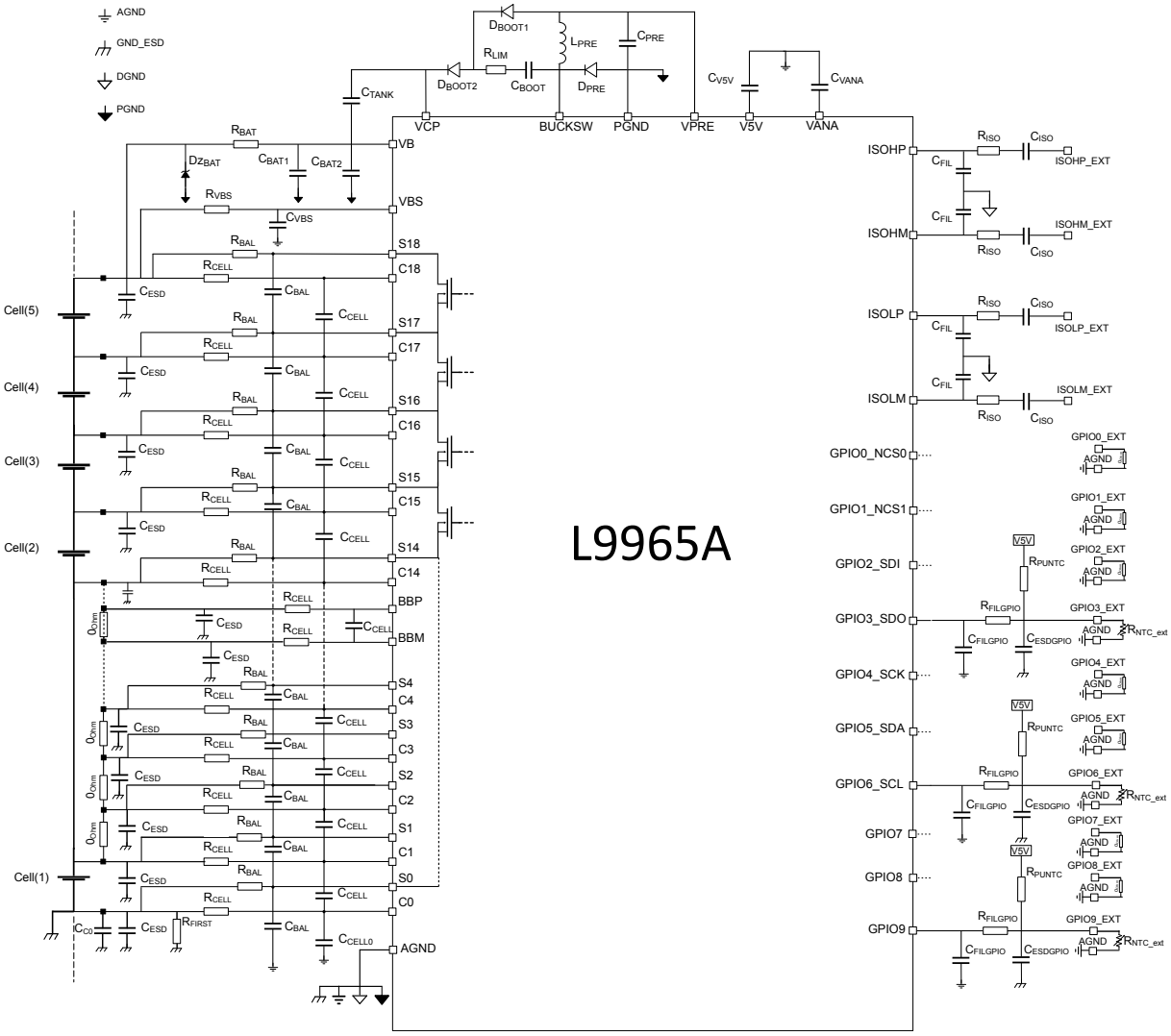
- A cell shall always be present between pins C0 and C1
- The remaining cells shall be mounted starting from the topmost (cell 18) and moving downwards
  - In case the C0-C1 pair is used as a busbar sensing channel, then the first cell shall be connected between C1 and C2 pins. However, open load diagnostics are not fully guaranteed in this case.

There can be two approaches for adapting a design to a different number of cells:

- *Hard-wired* approach: it is the most efficient in terms of the BOM, but requires redesigning the PCB for adapting to different modules. Given a number of unused cells, the design shall be adapted as follows:
  - Cell pairs C(x) – C(x-1), which are completely unused, should be short-circuited and connected to the negative terminal of the first mounted cell upwards
  - Unused balancing pairs S(x) – S(x-1), should be short-circuited and connected to the negative terminal of the first balancing stage upwards.
  - Cell pairs C(x) – C(x-1), which are used for busbar sensing, should be treated as regular cells and kept enabled. However, their balancing stage should be unused.
  - If the busbar pair BBP – BBM is unused, those pins shall be short-circuited and connected to AGND.
  - Unused GPIOs shall be connected to AGND. The GPIO must be configured as a digital input via GPIOx_CONF register
  - Unused VIF ports ISOxP – ISOxM shall be terminated by connecting a differential 160 Ω resistor and a common-mode 100 pF capacitor vs. AGND on each pin. Refer to Imbalance due to a VIF port disabled for further information
- *Flexible* approach: it is less efficient in terms of the BOM, since unused cells are still populated with analog front-end components. On the other hand, it enables quick readaptation of an existing PCB design to a different number of cells. Given a number of unused cells, the following substrategies are possible
  - The Short at PCB connector technique exploits shorts between unused connector pins. It still requires a small external rework, but it is limited to the cell connector and does not involve the PCB layout.
  - The Assembly option technique exploits design variants, replacing existing components with 0 Ω resistors to manage unused cells.
  - The Floating technique is as straightforward as it seems: just leave the corresponding PCB connectors floating whenever a cell is unused

### 1.6.1 Short at PCB connector

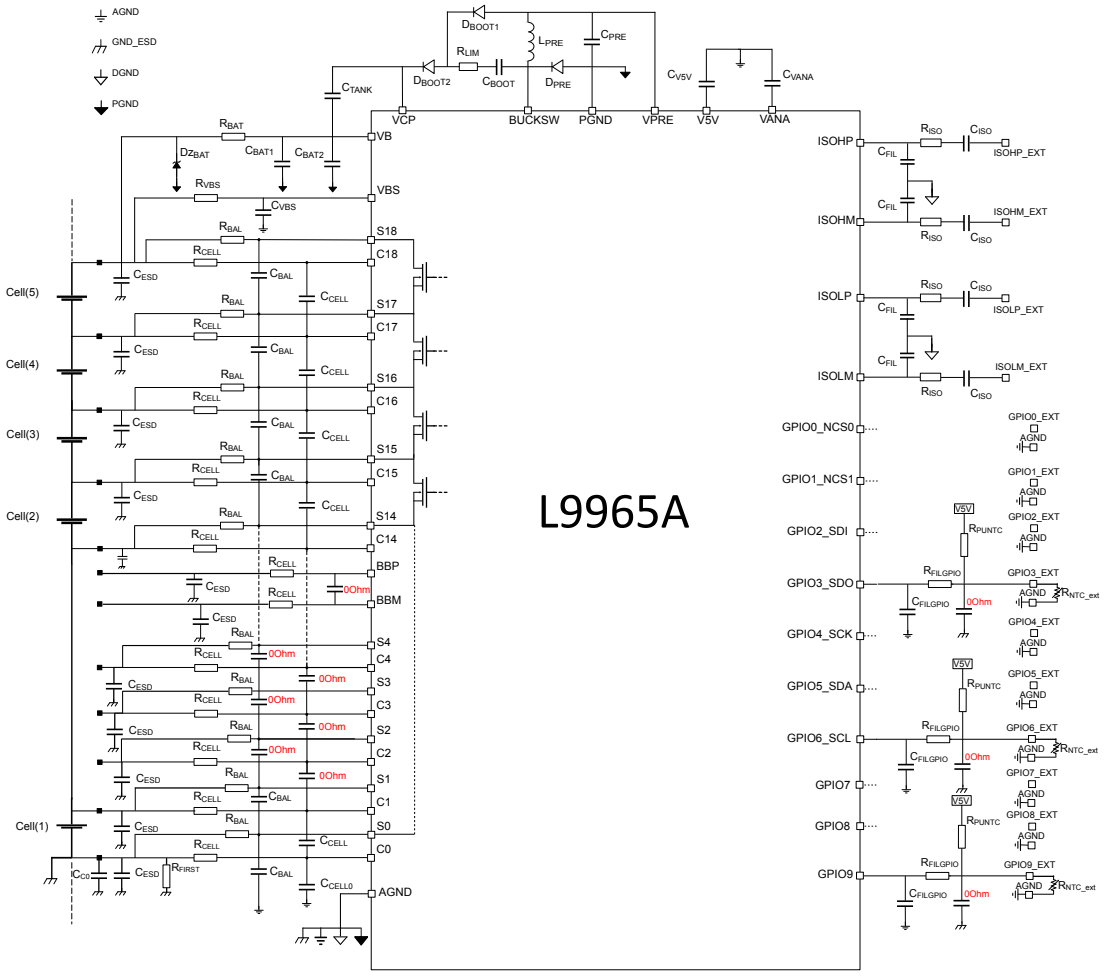
Figure 10. **Short at PCB connector**




As shown in the figure above, a 0 Ohm resistor (or eventually a physical short circuit) is placed on the external connector of the unused pins to connect the cell 1 positive terminal to the negative terminal of the following mounted cell. If the BB channel is brought to the connector, it can be short-circuited and connected to any potential mounted cell as well. Unused GPIO channels are shorted to AGND at the PCB connector.

### 1.6.2 Assembly option

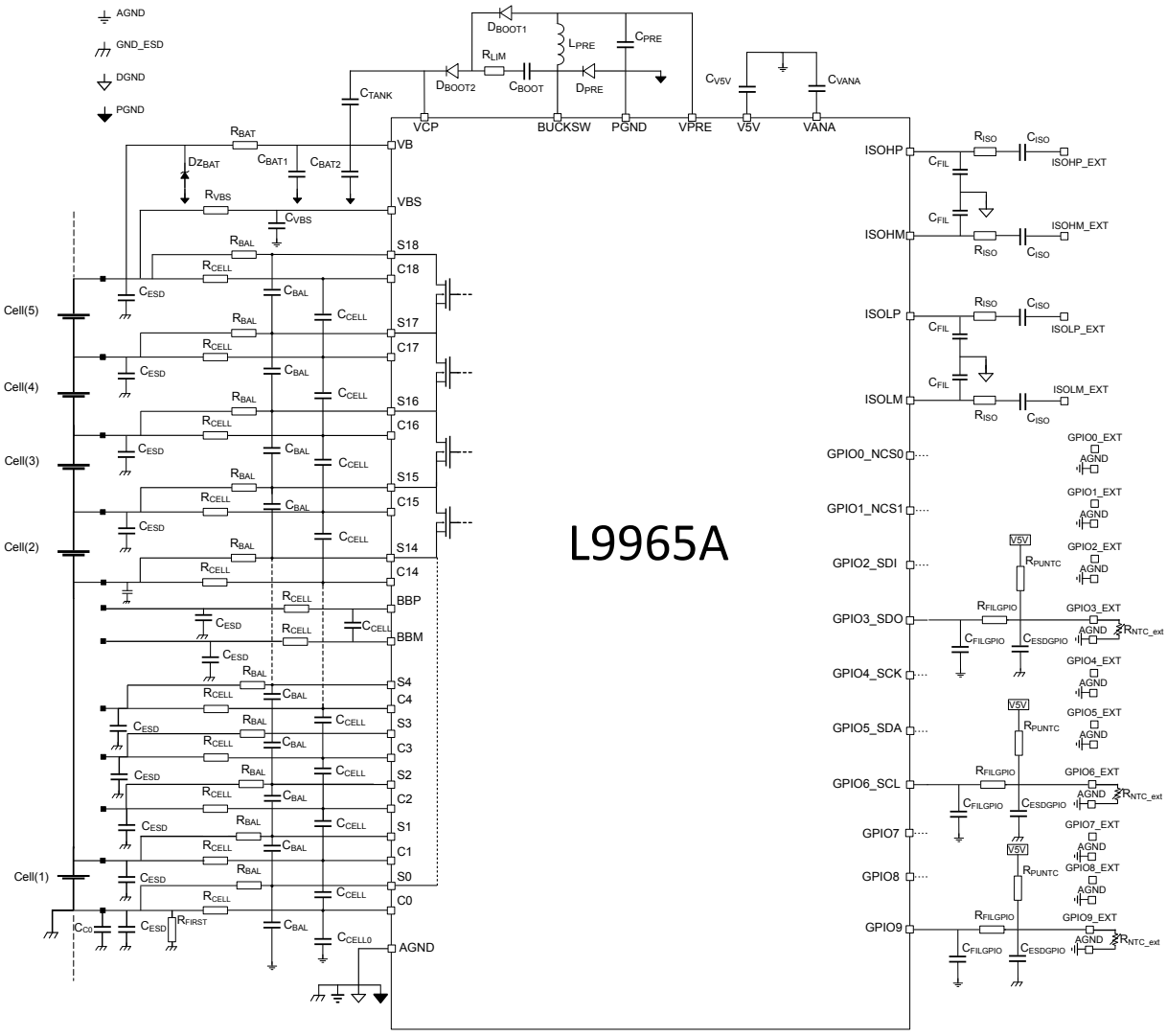
Figure 11. **Assembly option**



In the example above, unused cells and GPIOs are managed by replacing a few of their analog front-end capacitors with 0 Ohm resistors.

### 1.6.3 Floating

Figure 12. **Floating**



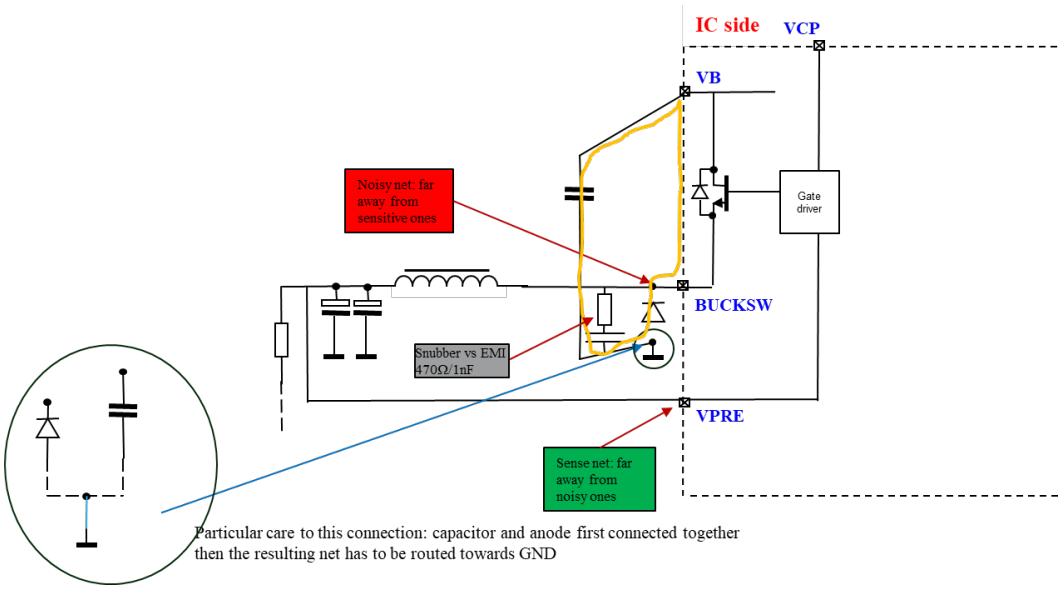

In the example above, unused cells and GPIOs are managed by simply leaving their PCB connectors floating. Their analog front-end BOM is totally populated with recommended components.

## 1.7 EMC considerations

To improve EMC robustness, the following actions are recommended:

Place all buck converter components near the IC as much as possible. To minimize parasitic effects, the PCB area under the buck coil should be free of metal layers and metal traces. Minimize the orange loop area in Figure 13.

**Figure 13. Buck converter layout rules**




Place protection and/or HV decoupling components, TVS, ESD Cap, ISO-SPI HV Cap, near the relevant external input connector as much as possible.

The L9965A/L99BM218 features 4 ground pins used as internal reference: AGND, DGND, PGND and EP (to be connected to AGND); additional GND can be present on PCB such as GND_PACK and ESD_GND.

To avoid relevant ground shifts and noise propagation on AGND, the different GNDs must be joined with a star as close as possible to the IC, and then brought to the PCB connector with a GND plane, connected to pack ground.

The ADC and NTC lines should run into inner layers of PCB.

The L9965A/L99BM218 promotional board of the PCB project is available as reference.

# 2 Application information

This section lists the components to be used in typical application scenarios.

## 2.1 Application circuit

**Figure 14. Typical application circuit**

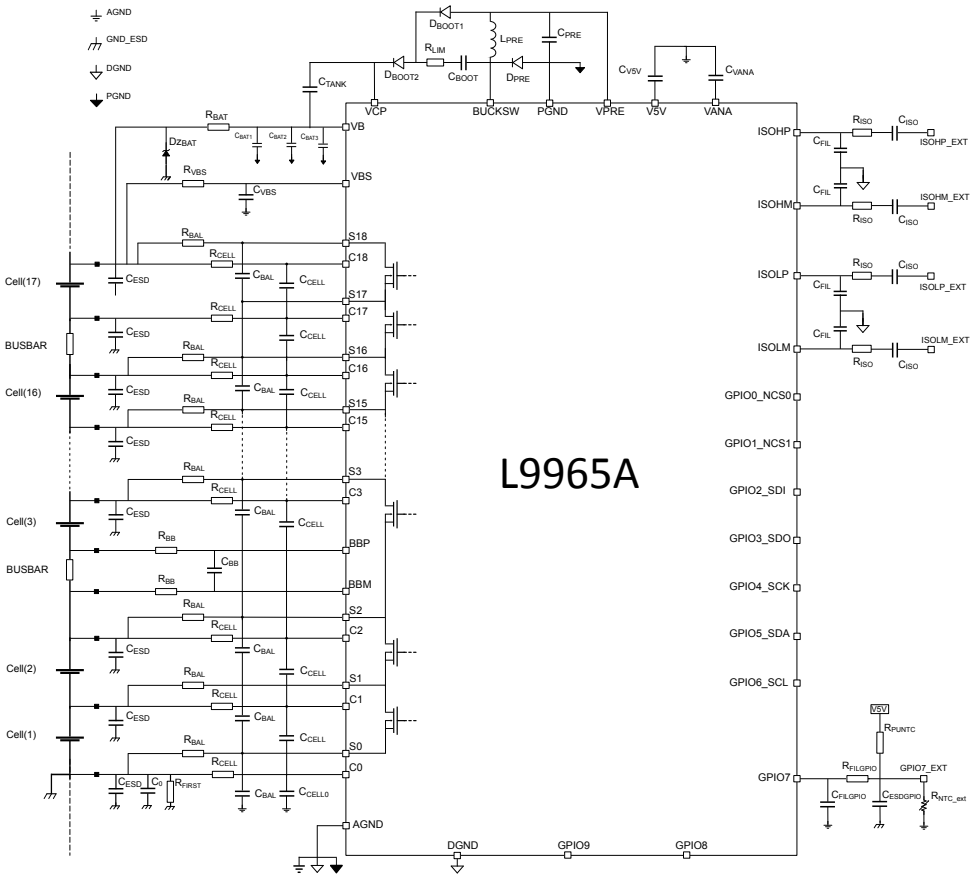


Figure 15. **Application circuit with BB on the first cell and unused cells**

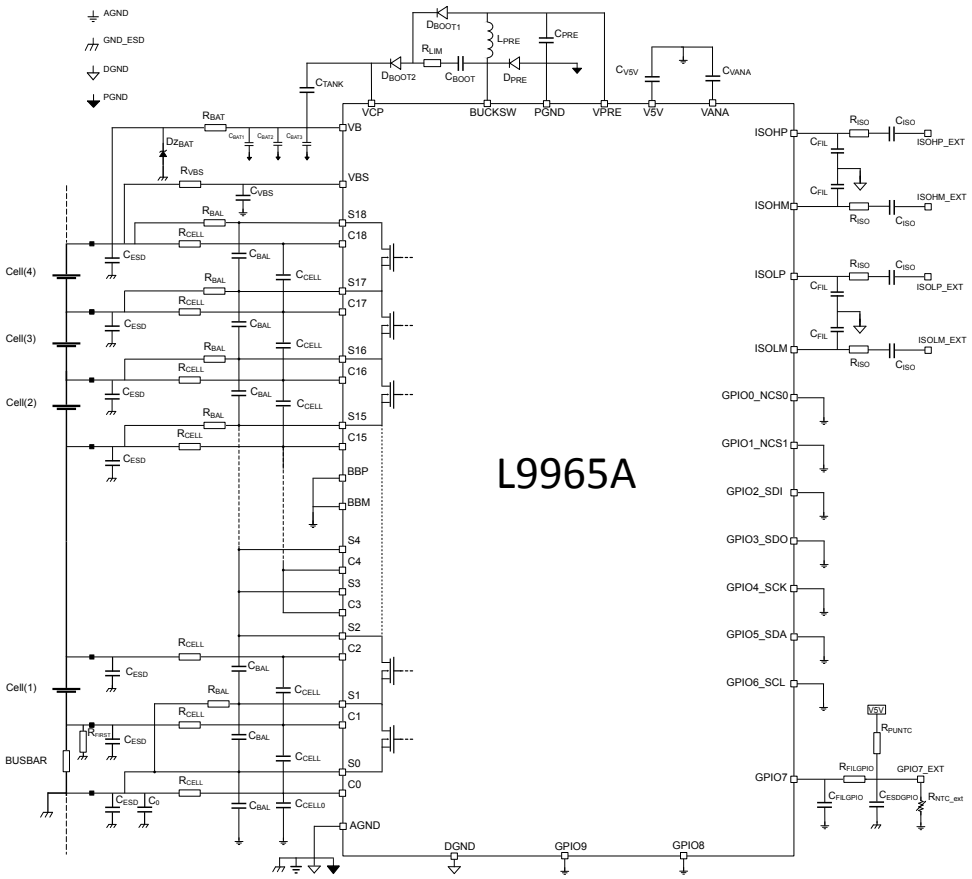
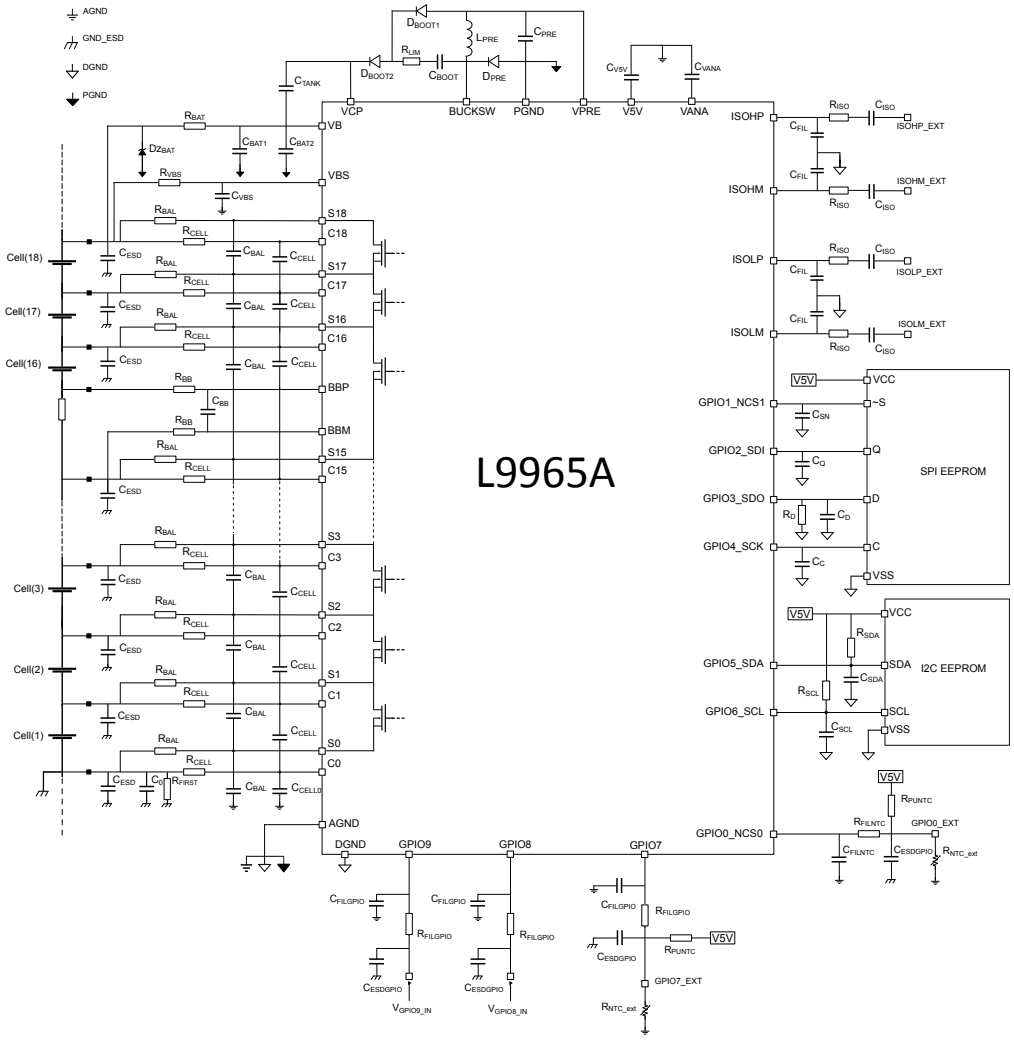


Figure 16. **Application scenario with SPI master and EEPROM**



## 2.2 Bill of material (BOM)

**Table 1. Bill of material**

| Symbol | Parameter | Value | Rating | Tolerance | Note |
|---|---|---|---|---|---|
| **Battery supply** | | | | | |
| $R_{BAT}$ | Series resistor for battery supply line | 10 Ω | 125 mW | 10% | Optional, it can be useful to limit possible hot plug spikes, according to specific customer application conditions. It shall be sized so that its voltage drop is kept < 1 V. |
| $D_{ZBAT}$ | TVS for battery supply line | SM30T100AY | NA | NA | Optional. Can be mounted to comply with surge and EFT tests. |
| $C_{BAT1}$ | Tank capacitor for battery supply line | 2.2 uF to 4.7 uF | 100 V | 20% | Lower rating is possible according to the module maximum voltage. |
| $C_{BAT2}$ | Filtering capacitor for battery supply line | 100 nF | 100 V | 20% | Optional, for improving EMC performances. Consider increasing voltage rating to compensate the DC bias effect. |
| $C_{BAT3}$ | Filtering capacitor for battery supply line | 10 nF | 100 V | 20% | Optional, for improving EMC performances. Consider increasing voltage rating to compensate the DC bias effect. |
| **Battery sensing** | | | | | |
| $R_{VBS}$ | Filtering resistor for battery sensing line | 240 Ω | 62.5 mW | 5% | VBS gain conversion error due to RVBS can be computed as $R_{VBS}/R_{VBS\_IN}$. Equalize $R_{VBS}C_{VBS}$ filter cutoff frequency to cells. |
| $C_{VBS}$ | Filtering capacitor for battery sensing line | 220 nF | 100 V | 10% | Consider increasing voltage rating to compensate the DC bias effect. Lower rating is possible according to the module maximum voltage. |
| **Cell and busbar sensing** | | | | | |
| $R_{CELL}$ | Filtering resistor for cell sensing line | 240 Ω | 62.5 mW | 5% | $R_{CELL}$ and $C_{CELL}$ values can be chosen to form an RC filter with ~3.3 kHz as cutoff frequency. Cell gain conversion error due to $R_{CELL}$ can be computed as $2R_{CELL}/R_{CELL\_DIFF\_IN}$. Do not go below 100 Ω for hotplug robustness. Do not go above 300 Ω to avoid false cell 1 open flagging. |
| $C_{CELL}$ | Differential filtering capacitor for cell sensing line | 100 nF | 16 V | 10% | |
| $C_{C0}$ | Grounded capacitor for improved BCI immunity on C0 connector | 1 nF | 16 V | 10% | |
| $C_{Cell0}$ | Consist of 3 grounded capacitors for improved BCI immunity on C0 | 100 nF1nF, 100 pF | 16 V | 10% | |
| $R_{BB}$ | Filtering resistor for busbar sensing line | 240 Ω | 62.5 mW | 5% | Equalize $R_{BB}C_{BB}$ filter cutoff frequency to cells. |
| $C_{BB}$ | Filtering capacitor for busbar sensing line | 100 nF | 16 V | 10% | |
| $R_{FIRST}$ | Pull down resistor on C0 pin | 10 k | 62.5k W | 5% | |
| **Cell balancing** | | | | | |

| Symbol | Parameter | Value | Rating | Tolerance | Note |
|---|---|---|---|---|---|
| $R_{BAL}$ | Balancing resistor for cell sensing line | 12 Ω | 500 mW | 5% | Sized to have a 180 mA max. balancing current when cell voltage is 4.3 V. |
| $C_{BAL}$ | Filtering capacitor for cell balancing line | 22 nF to 68 nF | 16 V | 20% | The maximum $R_{BAL}C_{BAL}$ cutoff frequency of 100 kHz is recommended for BCI robustness |
| **ESD** | | | | | |
| $C_{ESD}$ | ESD capacitor for pack connectors | 22 nF to 47 nF | 100 V | 20% | Optional, according to specific customer application requirements. Smaller values are possible if ESD-Safe MLCCs are used. Going below 6.8 nF is not recommended as it may jeopardize BCI performances |
| **LDOs** | | | | | |
| $C_{V5V}$ | 5 V LDO tank capacitor | 1 uF | 10 V | 10% | Consider increasing voltage rating to compensate the DC bias effect. |
| $C_{VANA}$ | 3.3 V LDO tank capacitor | 470 nF | 10 V | 10% | Consider increasing voltage rating to compensate the DC bias effect. |
| **VIF** | | | | | |
| CMC | Common mode choke for VIF H/L ports | ACT1210R-101-2P | | | Optional. Can be mounted to improve EMC performances |
| EMIF | Compact analog front-end for for VIF ports H/L | EMIF04-0410M8 | | | Optional. Can be used in place of $R_{ISO}$ and $C_{FIL}$ components |
| $R_{ISO}$ | Series resistor for ISO pins | 35 Ω to 41 Ω<br>39 Ω typical | 100 mW | 1% | Optional. Can be used in place of the EMIF component. Filters common mode and differential noise. Keep tolerance low to maximize differential line balancing. |
| $C_{ISO}$ | Isolation capacitor for VIF ports H/L | 2.2 nF to 6.8 nF | 100 V/1 kV | 2% | Optional. Can be used in place of XFMR component. Voltage rating shall be sized according to the maximum isolation voltage to be guaranteed in the application. Keep tolerance low to maximize differential line balancing. |
| XFMR | Isolation transformer for VIF ports H/L | ESMIT-4180/C | | | Optional. Can be used in place of $C_{ISO}$ component. Key parameters are:<br>• Inductance ≥ 120 µH @-40°C<br>• Winding resistance ≤ 0.5 Ω<br>*Note: EMC trials performed with recommended P/N.* |
| $C_{FIL}$ | Filtering capacitor for ISO termination | 100 pF | 25 V | 2% | Optional. Can be used in place of the EMIF component. Filters common mode and differential noise. Keep tolerance low to maximize differential line balancing. |
| $R_{TERM}$ | Termination resistor for unused port | 200 Ω | 0.5 W | 10% | Optional. To be used only on unused VIF port. |
| **GPIOs** | | | | | |
| $R_{PUNTC}$ | Pullup biasing for NTC measurement | 10 kΩ | 125 mW | 10% | Pullup resistor for NTC lines. Rating is to be increased to 0.5 W to protect and withstand short to battery. |
| $R_{FILGPIO}$ | Series resistor for GPIO pins | 3.3 kΩ | 125 mW | 10% | Filters noise on the GPIO pin. Rating is to be increased to 0.5 W to protect and withstand short to battery. |
| $C_{FILGPIO}$ | Filtering capacitor for GPIO pins | 100 nF | 16 V | 20% | Filters noise on the GPIO pin. Rating is to be increased to 100 V to withstand short to battery. |

| Symbol | Parameter | Value | Rating | Tolerance | Note |
|---|---|---|---|---|---|
| $C_{ESDGPIO}$ | ESD capacitor for GPIO pins connected to external lines | 6.8 nF | 16 V | 20% | Optional, according to specific customer application requirements. Rating is to be increased to 100 V to withstand short to battery. |
| **Charge pump** | | | | | |
| $D_{BOOT1}$, $D_{BOOT2}$ | Charge pump bootstrap diodes | MMBD1503A-D87Z | 100 V | NA | Bootstrap diodes rated to withstand maximum operating battery voltage. |
| $C_{TANK}$ | Charge pump tank capacitor | 47 nF | 100 V | 10% | Rated to withstand maximum operating battery voltage. |
| $C_{BOOT}$ | Charge pump flying bootstrap | 10 nF | 100 V | 10% | Rated to withstand maximum operating battery voltage. |
| $R_{LIM}$ | Bootstrap peak current limiter | 1 Ω | 100 mW | 10% | Needed to limit the current peak at the startup, when the $C_{TANK}$ is discharged. |
| **Buck preregulator** | | | | | |
| $C_{PRE}$ | Buck tank capacitor | 4.7 uF | 16 V | 10% | Rating is to be increased to 100 V to withstand short to battery. |
| $L_{PRE}$ | Buck inductor | 47 µH | ISAT >> 220 mA | 20% | Inductance value shall be constant up to 220 mA. |
| $D_{PRE}$ | Freewheeling diode | BAS19LT1G | 120 V | | Key parameters are:<br>• $V_R \geq 110$ V<br>• $I_F \geq 100\ mA_{DC}$<br>• $T_J \geq 150°C$<br>• $P_D \geq 100$ mW<br>• $V_F \leq 0.75$ V @10 mA @25°C<br>• $C_J \leq 10$ pF@0 V |

## Revision history

Table 2. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 04-Nov-2025 | 1 | Initial release. |
| 19-Feb-2026 | 2 | Updated Figure 10, Figure 11, Figure 12; Figure 14; Figure 15; Figure 16; added line in Cell balancing in Table 1; changed value in Charge pump in Table 1 and cancelled note of $R_{FIRST}$ in Table 1. |

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