# Capacitive Charging Mode (CCM) of VNF1248F

## Introduction

The purpose of this document is to demonstrate the functionality of the capacitive charging mode (CCM) feature in an application environment using the EV-VNF1248F easy board (Rev. 3.0). For major details, please refer to the updated easy board data brief (DB5511) and user manual (UM3487).

All tests were conducted on a typical sample representative of the standard population.

# 1 System Overview

## 1.1 VNF1248F Description

The VNF1248F is an advanced controller for a power MOSFET in a high-side configuration. It is designed to implement an intelligent high-side switch for 12 V, 24 V, and 48 V automotive applications. The control IC interfaces with a host microcontroller through a 3.3 V and 5 V CMOS-compatible SPI interface. It provides protection features and diagnostics signals for the system.

## 1.2 Block diagram and pin description

Figure 1. Block diagram

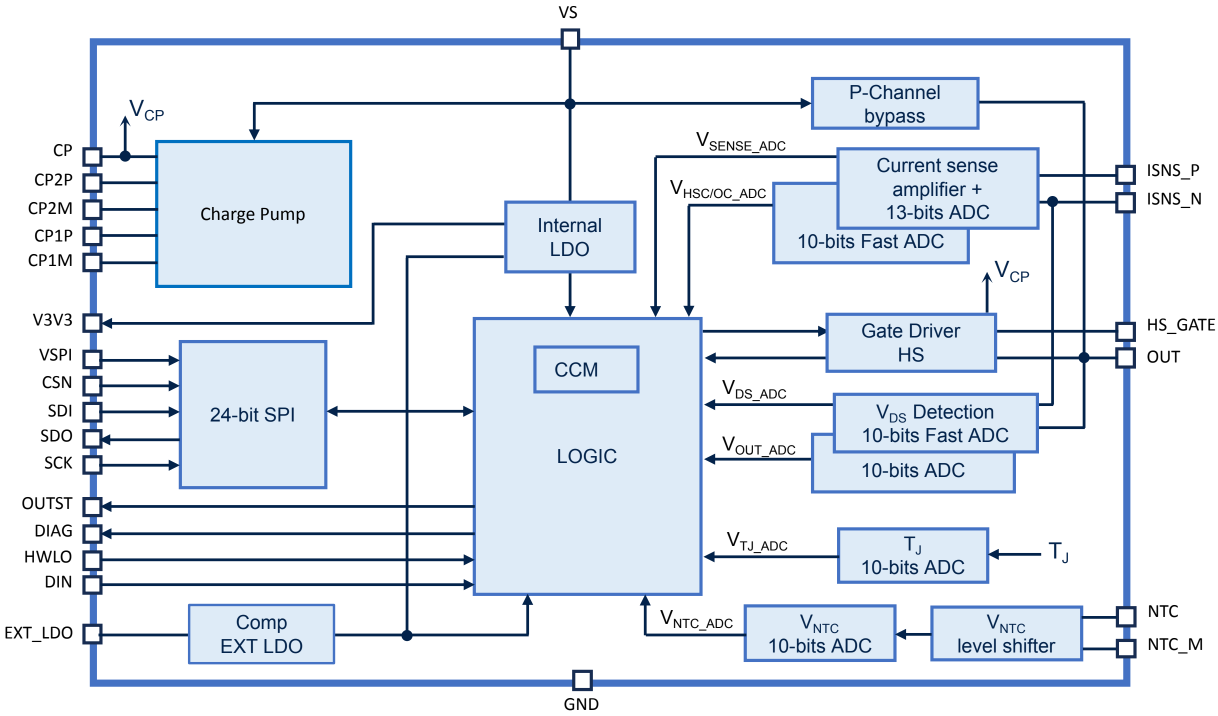
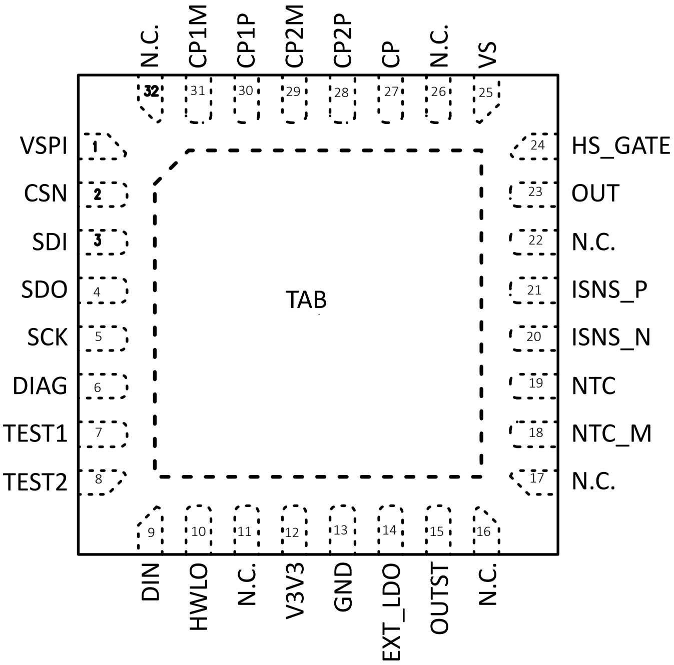


Figure 2. **Configuration diagram (top through view)**



*Note: TAB connection must be connected to the ground. TAB is not intended as the device reference ground (a dedicated pin shall be used).*

Table 1. **Pin functions**

| Pin # | Name | Function |
|---|---|---|
| TAB | | GND |
| 1 | VSPI | DC supply input for the SPI interface. 3.3 V and 5 V are compatible. |
| 2 | CSN | Chip select (active low) for SPI communication. It is the selection pin of the device. CMOS compatible input. |
| 3 | SDI | Serial data input for SPI communication. Data is transferred serially into the device and sampled on the SCK rising edge. |
| 4 | SDO | Serial data output for SPI communication. Data is transferred serially out of the device on the SCK falling edge. |
| 5 | SCK | Serial clock for SPI communication. It is a CMOS compatible input. |
| 6 | DIAG | Open drain logic output. Diagnostic feedback. DIAG = '0' if ((SR1.FAILSAFE_ST='1' or (CR1.AUTO_ON_DIS='1') and BYPASS_SAT='1') or (GSB.DIAGS = '1') or (GSB.DE = '1') or "internal oscillator fault event" else '1' |
| 7 | TEST1 | Test mode pin 1 - It must be connected to the ground through 1 kΩ resistor. |
| 8 | TEST2 | Test mode pin 2 - It must be connected to the ground through 1 kΩ resistor. |
| 9 | DIN | Direct input to wake up device from standby and to directly control gate turn-on/turn-off. If not used, it must be connected to the ground through 1 kΩ resistor. |
| 10 | HWLO | Active high input pin compatible with 3.3 V and 5 V CMOS. If not used, it must be connected to the ground through 1 kΩ resistor. |
| 11, 16,<br>17, 22,<br>26, 32 | N.C | Not connected. |
| 12 | V3V3 | Output of the 3.3 V internal LDO voltage regulator (logic and I/O supply).<br>Connect a low ESR capacitor (1 µF) close to this pin. |

| Pin # | Name | Function |
|---|---|---|
| 13 | GND | Ground connection. |
| 14 | EXT_LDO | External V3V3 supply. If not used, it must be connected to the ground through 1 kΩ resistor. |
| 15 | OUTST | Gate status monitor. |
| 18 | NTC_M | Negative input pin for external NTC resistor. |
| 19 | NTC | Positive input pin for external NTC resistor. |
| 20 | ISNS_N | Current sense amplifier negative input. |
| 21 | ISNS_P | Current sense amplifier positive input. |
| 23 | OUT | External FET source connection. |
| 24 | HS_GATE | Output of the gate driver for the external FET. |
| 25 | VS | Input supply pin. Connect to the 12 V, 24 V, 48 V battery voltage. |
| 27 | CP | Charge pump output. |
| 28 | CP2P | Charge pump–positive terminal of the flying capacitor $C_{P2}$. |
| 29 | CP2M | Charge pump–negative terminal of the flying capacitor $C_{P2}$. |
| 30 | CP1P | Charge pump–positive terminal of the flying capacitor $C_{P1}$. |
| 31 | CP1M | Charge pump–negative terminal of the flying capacitor $C_{P1}$. |

*Note: For more detailed information, please refer to the device datasheet.*

Typical application diagrams for 3.3 V and 5.0 V applications, as well as the suggested component of the bill of material, are reported in Section 1.3.

## 1.3 Typical application schematic

Figure 3. **EV-VNF1248F simplified schematic**

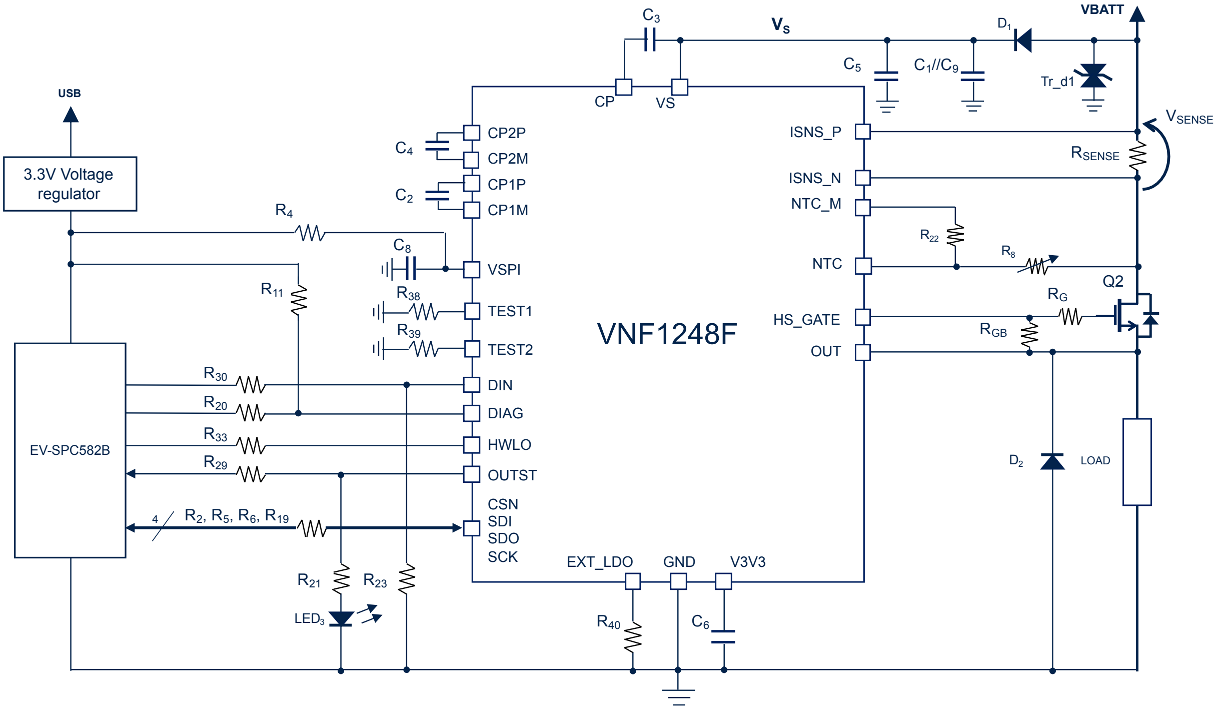


Table 2. **Adopted BOM on VNF1248F application easy board**

| General reference | EV-VNF1248F reference | Value |
|---|---|---|
| $C_S$ | $C_1$ // $C_9$ | 2*10 µF |
| $C_{S2}$ | $C_5$ | 100 nF |
| $C_{P1}$, $C_{P2}$ | $C_2$, $C_4$ | 470 nF |
| $C_P$ | $C_3$ | 470 nF |
| $C_{VSPI}$ | $C_8$ | 330 nF |
| $C_{V3V3}$ | $C_6$ | 1 µF |
| $R_{PU}$ | $R_{11}$ | 4.7 kΩ |
| $R_{PD}$ | $R_{23}$<br>$R_{21}$ | 47 kΩ<br>4.7 kΩ |
| $R_{PROT(SPI)}$ | $R_4$ | 330 Ω |
| $R_{PROT(OUTST)}$ | $R_{29}$ | 330 Ω |
| $R_{PROT}$ | $R_2$, $R_5$, $R_6$, $R_{19}$, $R_{20}$, $R_{30}$, $R_{33}$, $R_{38}$, $R_{39}$, $R_{40}$ | 1 kΩ |
| $R_{GATE}$ | $R_G$ | 1 Ω |
| $R_{GB}$ | $R_{GB}$ | 47 kΩ |
| $R_{REF}$ | $R_{22}$ | 10 kΩ ± 1% |
| $R_{SHUNT}$ | $R_{SENSE}$ | 5 mΩ |
| $R_{NTC}$ | $R_8$ | B57232V5103F360 |
| External MOSFET | $Q_2$ | STL135N8F7AG |
| Reverse polarity protection | $D_1$ | STPS2H100AY |
| Free wheeling diode | $D_2$ | STPS5H100-Y |
| -- | LED3 | Red LED |
| Voltage suppressor | Tr_d1 | SM15T68CAY |

## Figure 4. Schematic of adopted VNF1248F application easy board

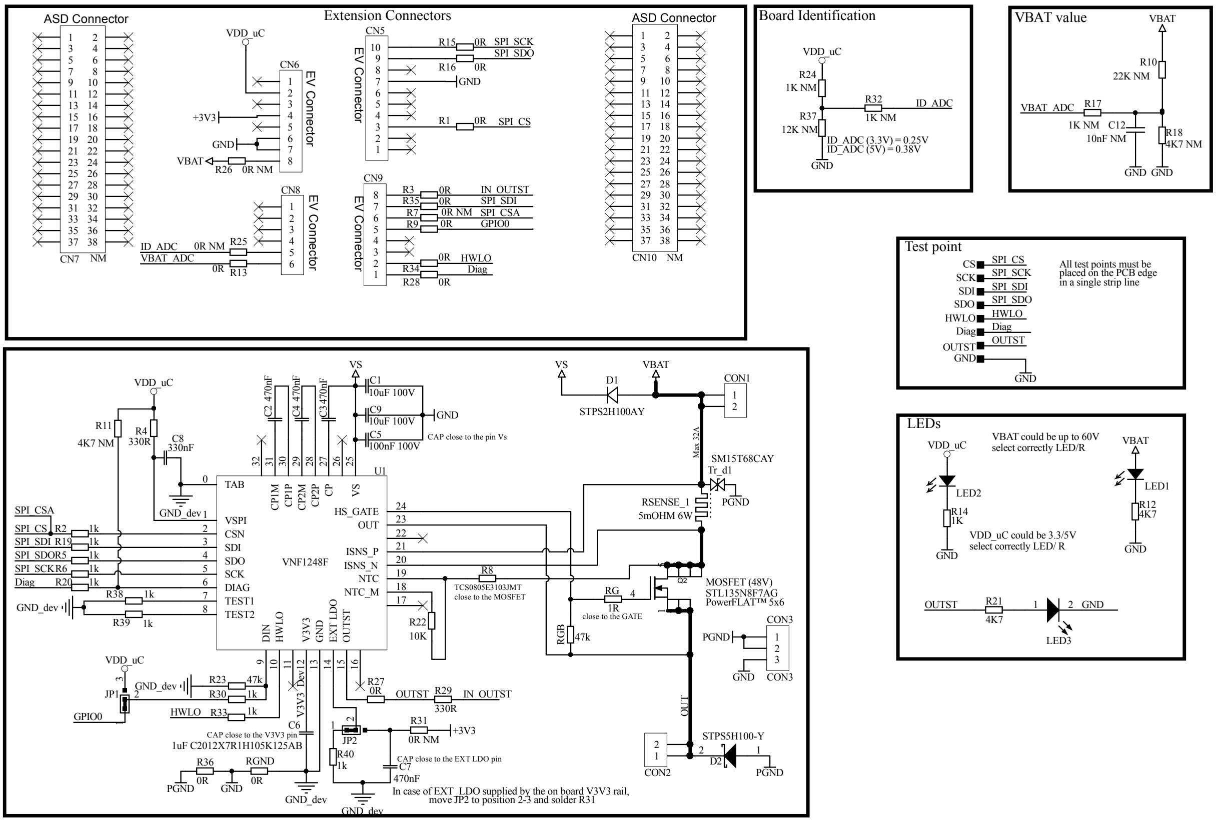
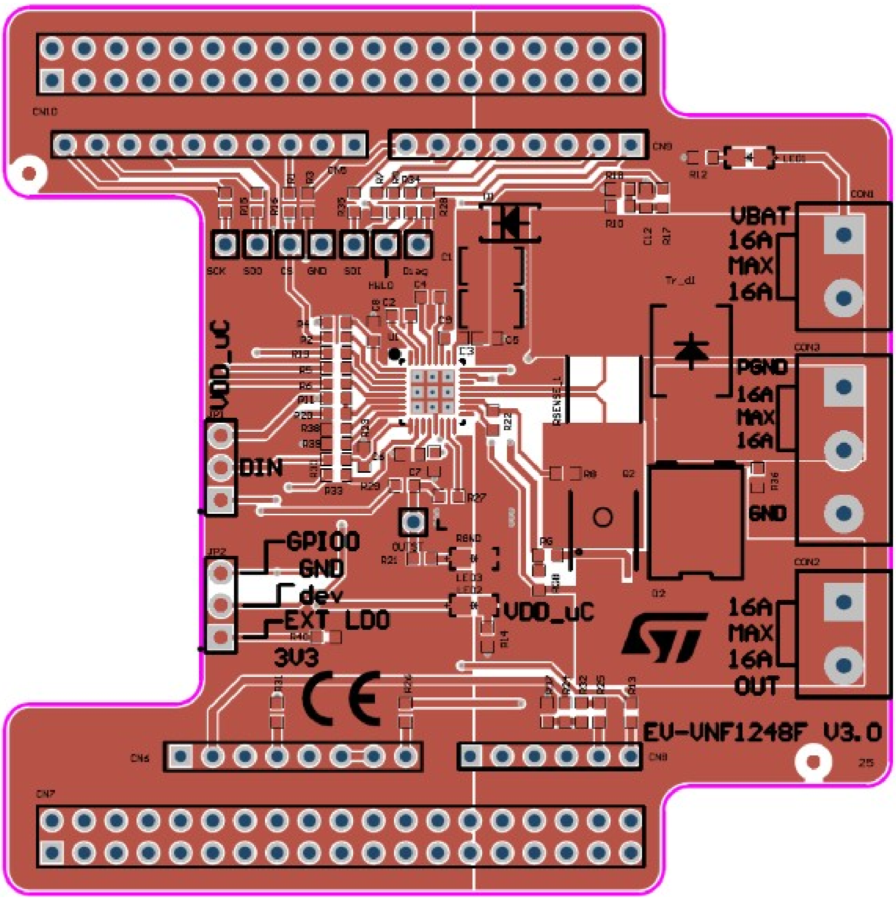


Figure 5. Layout of adopted VNF1248F application easy board



# 2 Capacitive Charging Mode – CCM

## 2.1 CCM and variables tuning application behavior

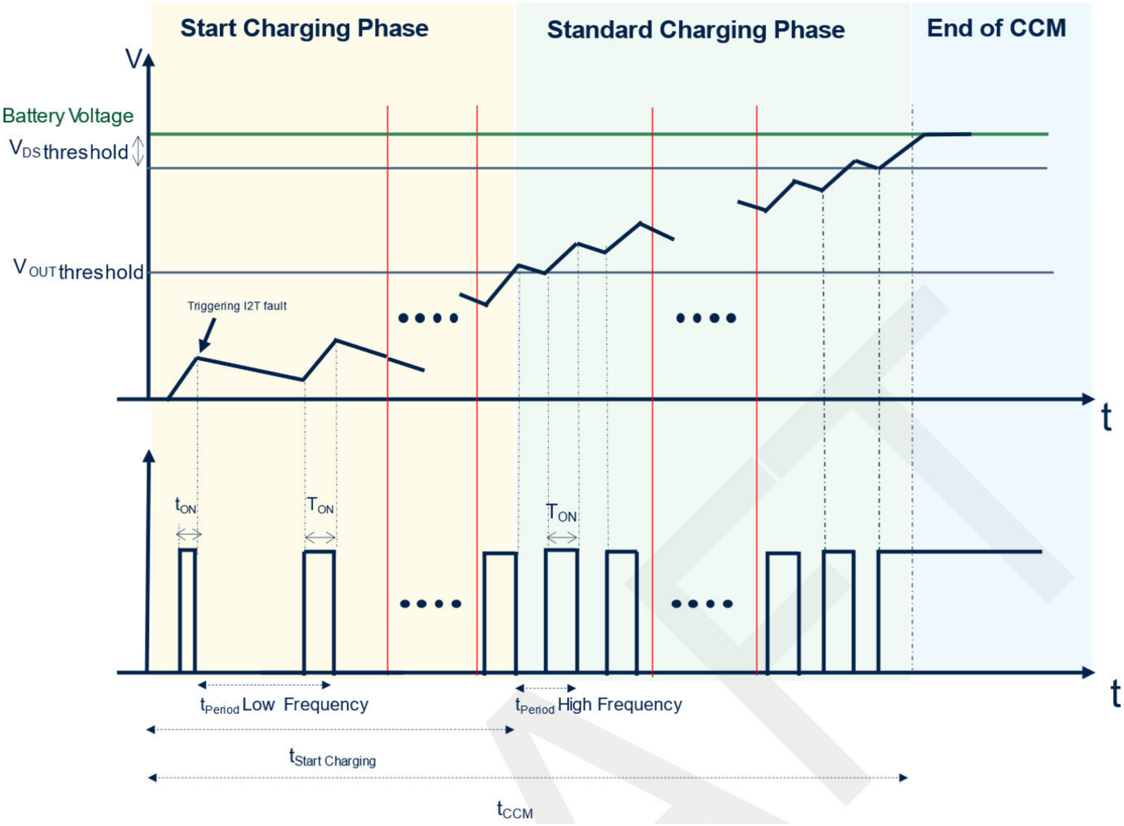
The device state machine implements a PWM-based control for the high-side driver controller to enable charging a capacitive load through the off-chip power MOSFET driven by the device.

The CCM feature is always available (for detailed information please refer to the flow charts available in "Capacity Charging Mode - CCM" chapter in the device datasheet, DS14109), and it can be triggered either in Unlocked/ Locked or in Fail-safe states.

The capacitive load charging sequence is split into two phases as shown in Figure 6:

1. **Start charging phase**: in this phase, the load is charged with a slower PWM period to check for a possible short circuit at the output; a maximum number of PWM pulses is allowed to reach a minimum $V_{OUT}$ value, otherwise CCM is aborted.
2. **Standard charging phase**: in this phase, the load is charged with a nominal PWM period until VDS reaches an internally defined threshold (100 mV), or a timeout limit is reached.

Figure 6. **CCM charging phases**



The register SR#1 (at address 0x11) reports the CCM status within the **CCM_STATUS** field, bits [23:22]. These two bits define four possible configurations:

- 00 → **IDLE:** CCM operation not started
- 01 → **RUN**: CCM operation running
- 10 → **CHARGED**: CCM operation completed successfully
- 11 → **CHARGE INCOMPLETE**: CCM operation aborted or stopped

Burst mode control for charging a capacitive load is configured by the following parameters, which must be programmed in dedicated registers:

Table 3. **CCM relevant fields**

| Parameter | Description | Field name | Field position in bits | Register number | Range |
|---|---|---|---|---|---|
| PWM period | ($t_{ON}$ + $t_{OFF}$) set during standard charging phase | CCM_PWM_T | 7:2 | CR#5 | From 50 to 4000 μs corresponding to frequency from 250 Hz to 20 KHz.<br>(refer to "CCM PWM $t_{ON}$ setting" table in DS14109) |
| PWM $t_{ON}$ time | PWM interval time with high-side driver turned on | CCM_PWM_TON | 13:8 | CR#5 | 1-50 μs (refer to "CCM PWM $t_{ON}$ setting" table in DS14109) |
| PWM $t_{ON}$ multiplying factor | to multiply by 1-2-4-8 Ton time defined by<br>CCM_PWM_TON setting, for duty cycle configuration | CCM_PWM_TON_MF | 19:18 | CR#3 | 1-2-4-8 |
| PWM start period | PWM period (Ton + Toff) set during starting phase (short<br>circuit check) | CCM_PWM_SC_T | 16:14 | CR#5 | 2.0-2.5-3.0-3.5-4.0 ms |
| PWM start pulses max number | Max number of PWM pulses during<br>starting phase (short circuit check) | CCM_PWM_SC_T_NB | 21:17 | CR#5 | From 5 to 50 pulses (refer to "CCM PWM max. start pulses number setting" table in DS14109) |
| CCM timeout | Maximum time allowed to charging phase | CCM_TIMEOUT | 23:22 | CR#5 | 200-250-300-400 ms |
| VOUT threshold | VOUT limit to be achieved to switch from starting phase to standard charging phase | CCM_VOUT_THR | 16:14 | CR#3 | 1-2-3-4-5 V |
| Hard short circuit latch-off threshold | It configures the Delta V reading at extremes of $R_{SHUNT}$ triggering the HSC protection | HSC_THR | 10:7 | CR#2 | From 20 to 160 mV (refer to "hard short circuit protection with integrated 10-bit ADC" table in DS14109) |
| Nominal overcurrent threshold | Value of the nominal overcurrent threshold for the eFuse emulation | OVC _THR | 15:11 | CR#2 | From 6 to 90 mV (refer to "overcurrent protection" table in DS14109) |
| Nominal time ON | Value of nominal time required for the eFuse emulation. It corresponds to the trip time obtained when the current is equal to the nominal overcurrent threshold | T_NOM | 23:16 | CR#2 | From 1 to 511 s (refer to "CCM PWM max. start pulses number setting" table in DS14109) |

Additional important variables affecting the CCM behavior are:

- $V_B$ battery supply voltage of entire application circuit
- $R_{SHUNT}$ dimension
- Ambient temperature
- $C_{LOAD}$ features and connection

## 2.2 Start Charging Phase

During this phase, the load is charged with a $T_{ON}$ (**CCM_PWM_TON**) and a PWM period (**CCM_PWM_SC_T**) to check for possible short circuit on output.

This phase ends when one of the following two conditions occurs:

- $V_{OUT}$ triggers the threshold as set in CR#3 (**CCM_VOUT_THR**) so that the standard phase can start
- The maximum number of PWM pulses has been reached as set in CR#5 (**CCM_PWM_SC_T_NB)** with $V_{OUT}$ below the threshold set by **CCM_VOUT_THR**

For the second condition, where the charging phase is interrupted, when the field **CCM_STATUS** (bits [23:22] of SR#1) sets to “11”, it means that the charging of the load has not succeeded. This event can occur in case of a setup not able to allow $V_{OUT}$ to reach the target threshold set by **CCM_VOUT_THR** (see Figure 63 below) or in case of short circuit between OUT and GND (see Figure 107 below).

## 2.3 Standard Charging Phase

Once the “Start Charging Phase” has been successfully completed (i. e.: $V_{OUT}$ triggers the target threshold), the load charging continues with a nominal PWM period (**CCM_PWM_T**).

The CCM ends when one of the following two conditions occurs:

- External power MOS VDS reaches an internally defined threshold (100 mV).
  The field **CCM_STATUS** (bits [23:22] of SR#1) sets to “10” meaning that the charging of the load is **completed successfully**
- $t_{CCM}$ timeout elapsed (**CCM_TIMEOUT**).
  The field **CCM_STATUS** (bits [23:22] of SR#1) sets to “11” indicating that the charging of the load is **aborted** (see Figure 113 below).

## 2.4 How to launch CCM

Capacitive charging mode can be launched with the device in Fail-safe, Unlocked or Locked state.

Please consider that with the device in Unlocked state, it is possible to configure all parameters reported in Table 5 by writing the related involved bits in the indicated fields while in case of the device in Fail-safe or Locked state, the mentioned parameters will follow the contents in the related CRs of NVM. For NVM operation, refer to AN6394 "NVM feature of VNF1248F"

Once the device is in Unlocked or Locked state, the CCM will be started or stopped by means of dedicated commands ON and OFF on bits 18 (CCM_CTRL_ON) and 19 (CCM_CTRL_OFF) inside CR#1.

Please refer to the trial setup A1 vs A2 below for the CCM with the device in Unlocked vs Locked state.

Refer to the trial setup Z1 vs Z3 below for the charge completed or aborted with device in Unlocked state.

Once the device is in Fail-safe state, capacitive load burst charging mode functionality can be enabled by proper DIN toggling sequence that ends with DIN high to maintain HS_GATE ON. In Fail-safe, the CCM can be stopped before charge completion by setting DIN low. Please refer to the trial setup Z2 vs Z4 below for the charge completed or aborted with device in Fail-safe state.

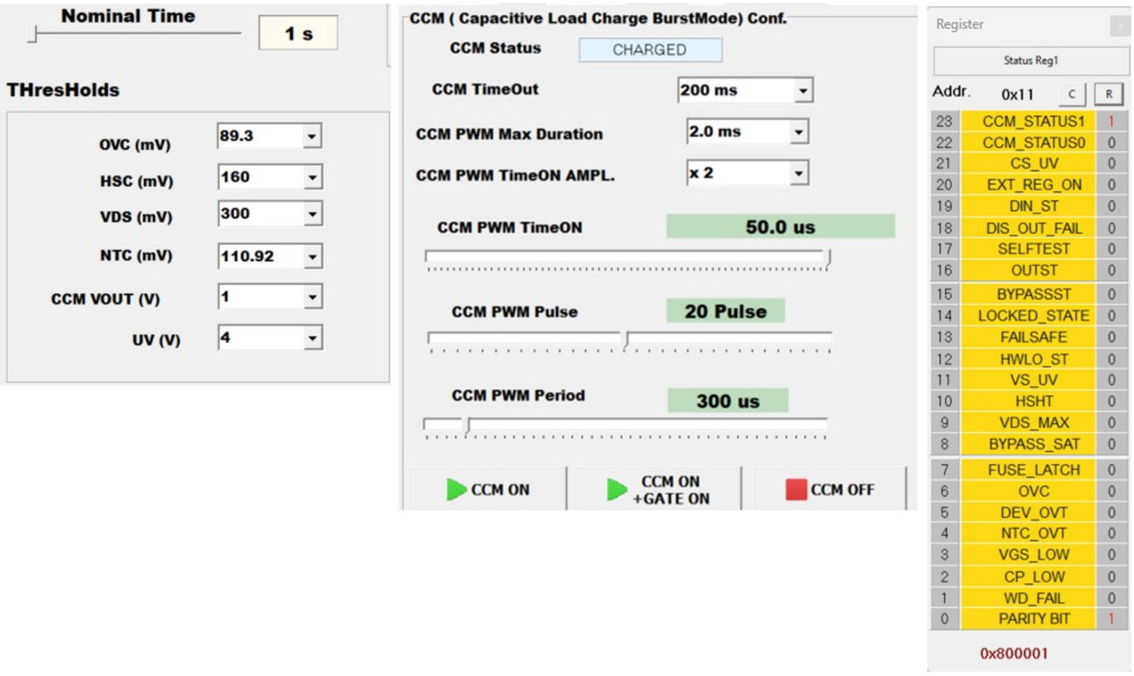
# 3 CCM test in Unlocked vs Locked vs Fail-safe state

This paragraph reports the examples of the charge of a capacitance working with the application circuit indicated in Figure 16, having $R_{SHUNT}$ = 5 mΩ and $C_S$ = 2 * 10 uF (100 V) and using the following setups.

## 3.1 Trial Setup A1

- $V_B$ = 13 V
- Ambient temperature = room temperature ~25°C generating TJ ~30°C
- $C_{LOAD}$ = 2.2 mF (measured 2.08 mF)
- Device in Unlocked state with following settings:
  - CCM_VOUT_THR → bits [16:14] of CR#5 set @ "000b" = 1 V
  - OVC_THR = VOC_THRS_31 → bits [15:11] of CR#2 set @ "11111b" = 89.3 mV
  - HSC_THR = VHSC_THRS_15 → bits [10:7] of CR#2 set @ "11111b" = 160 mV
  - T_NOM = $T\_NOM_{MIN}$ → bits [23:16] of CR#2 set @ "00000000b" = 1 s
  - CCM_PWM_TON → bits [13:8] of CR#5 set @ "111111b" = 50 µs
  - CCM_PWM_TON_MF → bits [19:18] of CR#3 set @ “01b” = 2 x
  - CCM_PWM_SC_T_NB → bits [21:17] of CR#5 set @ “01111b” = 20 pulses
  - CCM_PWM_T → bits [7:2] of CR#5 set @ “000100b” = 300 µs
  - CCM_TIMEOUT → bits [23:22] of CR#5 set @ “00b” = 200 ms
  - CCM_PWM_SC_T → bits [16:14] of CR#5 set @ “000b” = 2 ms
  - GUI settings as per Figure 7

Figure 7. CCM configuration and result from GUI for test setup A1



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

Register

Status Reg1

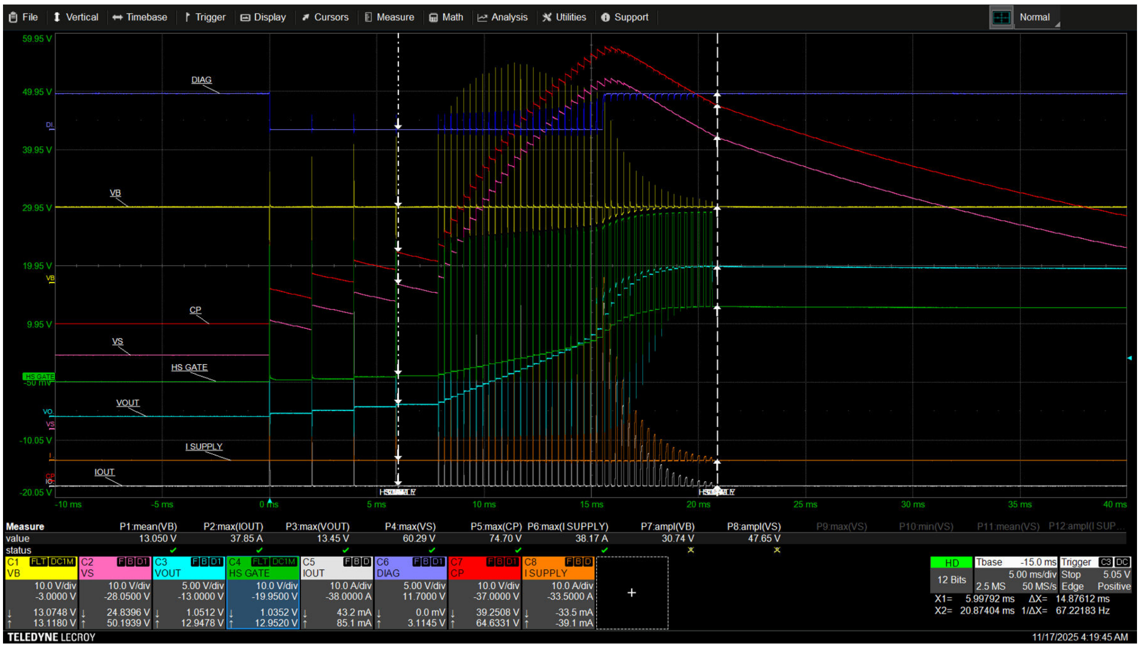
Addr. 0x11

| | | |
|---|---|---|
| 23 | CCM_STATUS1 | 1 |
| 22 | CCM_STATUS0 | 0 |
| 21 | CS_UV | 0 |
| 20 | EXT_REG_ON | 0 |
| 19 | DIN_ST | 0 |
| 18 | DIS_OUT_FAIL | 0 |
| 17 | SELFTEST | 0 |
| 16 | OUTST | 0 |
| 15 | BYPASSST | 0 |
| 14 | LOCKED_STATE | 0 |
| 13 | FAILSAFE | 0 |
| 12 | HWLO_ST | 0 |
| 11 | VS_UV | 0 |
| 10 | HSHT | 0 |
| 9 | VDS_MAX | 0 |
| 8 | BYPASS_SAT | 0 |
| 7 | FUSE_LATCH | 0 |
| 6 | OVC | 0 |
| 5 | DEV_OVT | 0 |
| 4 | NTC_OVT | 0 |
| 3 | VGS_LOW | 0 |
| 2 | CP_LOW | 0 |
| 1 | WD_FAIL | 0 |
| 0 | PARITY BIT | 1 |

0x800001

With the mentioned setup A1, the $C_{LOAD}$ is charged in 8 ms (start phase) + 12.9 ms (standard phase).

Figure 8. **Waveforms acquired during CCM with setup A1**



```
Measure  P1:mean(VB)  P2:max(IOUT)  P3:max(VOUT)  P4:max(VS)  P5:max(CP)  P6:max(I SUPPLY)  P7:ampl(VB)  P8:ampl(VS)  P9:max(VS)  P10:min(VS)  P11:mean(VS)  P12:ampl(I SUP
value    13.050 V     37.85 A       13.45 V       60.29 V     74.70 V     38.17 A           30.74 V      47.65 V
status   ✓            ✓             ✓             ✓           ✓           ✓                 ✗            ✗

C1 VB       C2 VS       C3 VOUT     C4 HS GATE  C5 IOUT     C6 DIAG     C7 CP       C8 I SUPPLY
10.0 V/div  10.0 V/div  5.00 V/div  10.0 V/div  10.0 A/div  5.00 V/div  10.0 V/div  10.0 A/div
-3.0000 V   -28.0500 V  -13.0000 V  -19.9500 V  -38.0000 A  11.7000 V   -37.0000 V  -33.5000 A
↓ 13.0748 V ↓ 24.8396 V ↓ 1.0512 V  ↓ 1.0352 V  ↓ 43.2 mA   ↓ 0.0 mV    ↓ 39.2508 V ↓ -33.5 mA
↑ 13.1180 V ↑ 50.1939 V ↑ 12.9478 V ↑ 12.9520 V ↑ 85.1 mA   ↑ 3.1145 V  ↑ 64.6331 V ↑ -39.1 mA

HD       Tbase  -15.0 ms   Trigger  C3 DC
12 Bits  5.00 ms/div       Stop     5.05 V
         2.5 MS  50 MS/s   Edge     Positive
X1=  5.99792 ms   ΔX=  14.87612 ms
X2=  20.87404 ms  1/ΔX=  67.22183 Hz

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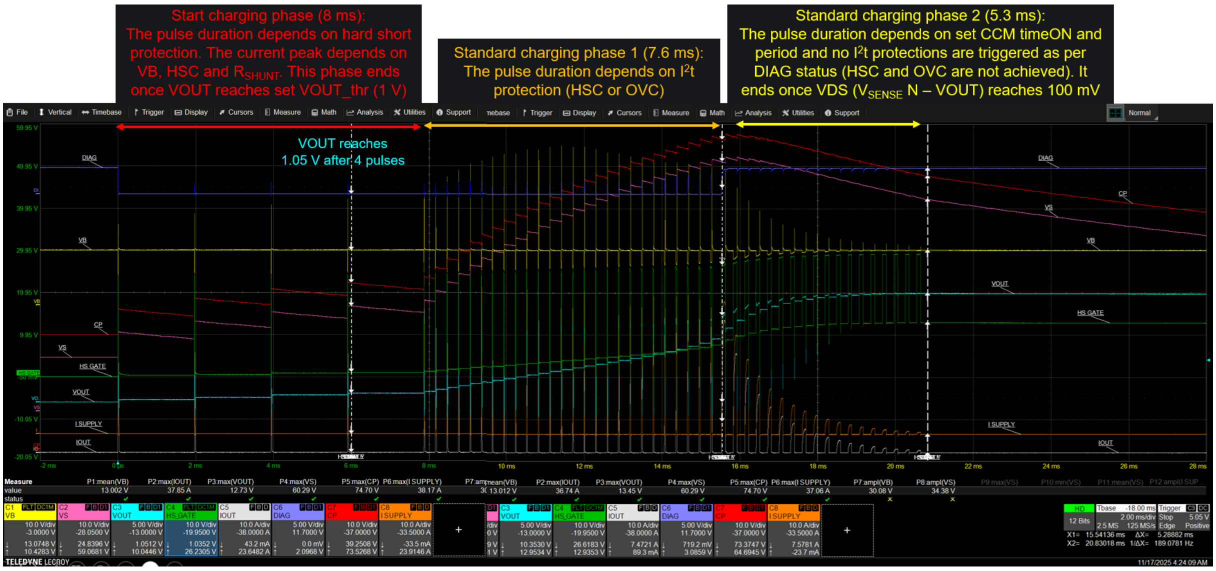
The image below highlights the two phases during the CCM and the I$^2$t - fuse protections triggering.

Figure 9. **Zoomed waveforms acquired during CCM with setup A1**



Start charging phase (8 ms):
The pulse duration depends on hard short protection. The current peak depends on VB, HSC and $R_{SHUNT}$. This phase ends once VOUT reaches set VOUT_thr (1 V)

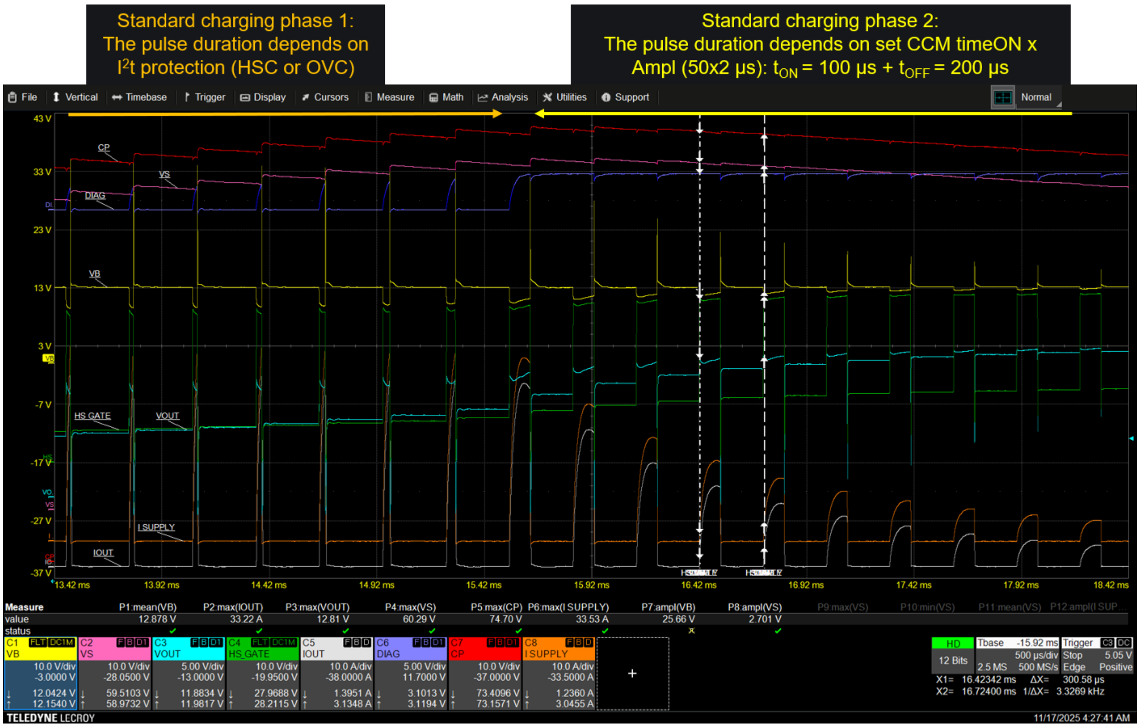
Standard charging phase 1 (7.6 ms):
The pulse duration depends on I$^2$t protection (HSC or OVC)

Standard charging phase 2 (5.3 ms):
The pulse duration depends on set CCM timeON and period and no I$^2$t protections are triggered as per DIAG status (HSC and OVC are not achieved). It ends once VDS ($V_{SENSE}$ N – VOUT) reaches 100 mV

VOUT reaches
1.05 V after 4 pulses

Figure 9 points out that the CCM time ON and time OFF configured in CR#5 are visible only when I$^2$t protection is no longer triggered.

Figure 10. **Zoomed waveforms acquired during CCM with setup A1**



Standard charging phase 1: The pulse duration depends on $I^2t$ protection (HSC or OVC)

Standard charging phase 2: The pulse duration depends on set CCM timeON x Ampl (50x2 µs): $t_{ON}$ = 100 µs + $t_{OFF}$ = 200 µs

| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.878 V | 33.22 A | 12.81 V | 60.29 V | 74.70 V | 33.53 A | 25.66 V | 2.701 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ | | | | |

| C1 FLT DC1M VB | C2 F B D1 VS | C3 F B D1 VOUT | C4 FLT DC1M HS_GATE | C5 F B D IOUT | C6 F B D1 DIAG | C7 F B D1 CP | C8 F B D I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 10.0 V/div | 5.00 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 10.0 V/div | 10.0 A/div |
| -3.0000 V | -28.0500 V | -13.0000 V | -19.9500 V | -38.0000 A | 11.7000 V | -37.0000 V | -33.5000 A |
| ↓ 12.0424 V | ↓ 59.5103 V | ↓ 11.8834 V | ↓ 27.9688 V | ↓ 1.3951 A | ↓ 3.1013 V | ↓ 73.4096 V | ↓ 1.2360 A |
| ↑ 12.1540 V | ↑ 58.9732 V | ↑ 11.9817 V | ↑ 28.2115 V | ↑ 3.1348 A | ↑ 3.1194 V | ↑ 73.1571 V | ↑ 3.0455 A |

| HD | Tbase -15.92 ms | Trigger C3 DC |
|---|---|---|
| 12 Bits | 500 µs/div | Stop 5.05 V |
| | 2.5 MS 500 MS/s | Edge Positive |

X1= 16.42342 ms ΔX= 300.58 µs
X2= 16.72400 ms 1/ΔX= 3.3269 kHz

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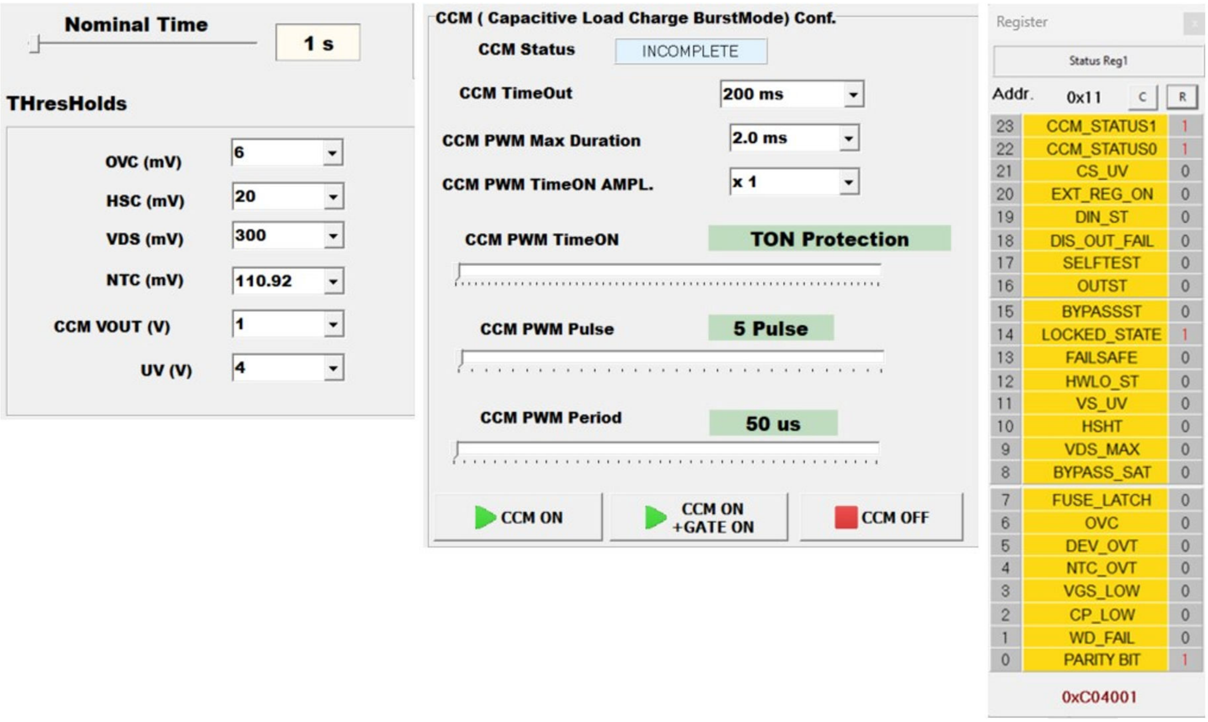
The CCM activation on the same circuit, $C_{LOAD}$ and $V_B$, but with the device in Locked mode, generates a different result because the device, once in Locked or Fail-safe modes, recovers the default setting written in the NVM.

In case of device in Locked state, the CCM operation is incomplete after 10 ms, with $V_{OUT}$ reaching 0.4 V after the five set pulses, as shown in trial A2 below.

## 3.2 Trial Setup A2

- $V_B$ = 13 V
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 2.2 mF (measured 2.08 mF)
- Device in Locked state recovering default NVM setting (the DUT was moved from Unlocked state with NVM_CFG_EN = 1b, bit 16 of CR#1, to Locked state):
  - CCM_VOUT_THR = 1 V
  - OVC_THR = VOC_THRS_0 → 6 mV
  - HSC_THR = VHSC_THRS_0 → 20 mV
  - T_NOM = $T\_NOM_{MIN}$ → 1 s
  - CCM_PWM_TON = $T_{ON}$ stopped by protection
  - CCM_PWM_SC_T_NB = 5 pulses
  - CCM_PWM_T = 50 µs
  - CCM_PWM_TON_MF = 1 x
  - CCM_TIMEOUT = 200 ms
  - CCM_PWM_SC_T = 2 ms
  - GUI settings collected at the end of CCM operations as shown in Figure 11

**Figure 11.** CCM configuration and result from GUI for test setup A2



**Nominal Time** 1 s

**THresHolds**

OVC (mV) 6
HSC (mV) 20
VDS (mV) 300
NTC (mV) 110.92
CCM VOUT (V) 1
UV (V) 4

**CCM ( Capacitive Load Charge BurstMode) Conf.**

CCM Status INCOMPLETE
CCM TimeOut 200 ms
CCM PWM Max Duration 2.0 ms
CCM PWM TimeON AMPL. x 1
CCM PWM TimeON TON Protection
CCM PWM Pulse 5 Pulse
CCM PWM Period 50 us

Register

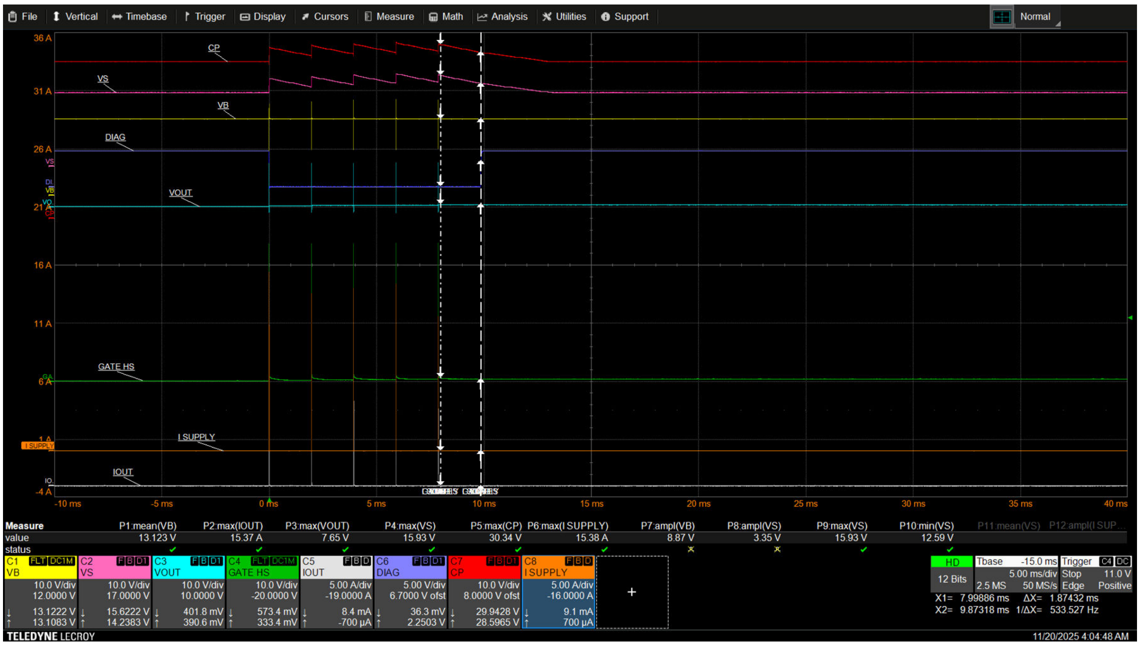
Status Reg1

Addr. 0x11

| | | |
|---|---|---|
| 23 | CCM_STATUS1 | 1 |
| 22 | CCM_STATUS0 | 1 |
| 21 | CS_UV | 0 |
| 20 | EXT_REG_ON | 0 |
| 19 | DIN_ST | 0 |
| 18 | DIS_OUT_FAIL | 0 |
| 17 | SELFTEST | 0 |
| 16 | OUTST | 0 |
| 15 | BYPASSST | 0 |
| 14 | LOCKED_STATE | 1 |
| 13 | FAILSAFE | 0 |
| 12 | HWLO_ST | 0 |
| 11 | VS_UV | 0 |
| 10 | HSHT | 0 |
| 9 | VDS_MAX | 0 |
| 8 | BYPASS_SAT | 0 |
| 7 | FUSE_LATCH | 0 |
| 6 | OVC | 0 |
| 5 | DEV_OVT | 0 |
| 4 | NTC_OVT | 0 |
| 3 | VGS_LOW | 0 |
| 2 | CP_LOW | 0 |
| 1 | WD_FAIL | 0 |
| 0 | PARITY BIT | 1 |

0xC04001

**Figure 12.** Waveforms acquired during CCM with test setup A2



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 13.123 V | 15.37 A | 7.65 V | 15.93 V | 30.34 V | 15.38 A | 8.87 V | 3.35 V | 15.93 V | 12.59 V | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✗ | ✓ | ✓ | | |

| C1 VB | C2 VS | C3 VOUT | C4 GATE HS | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 10.0 V/div | 10.0 V/div | 10.0 V/div | 5.00 A/div | 5.00 V/div | 10.0 V/div | 5.00 A/div |
| 12.0000 V | 17.0000 V | 10.0000 V | -20.0000 V | -19.0000 A | 6.7000 V ofst | 8.0000 V ofst | -16.0000 A |
| ↓ 13.1222 V | ↓ 15.6222 V | ↓ 401.8 mV | ↓ 573.4 mV | ↓ 8.4 mA | ↓ 36.3 mV | ↓ 29.9428 V | ↓ 9.1 mA |
| ↑ 13.1083 V | ↑ 14.2383 V | ↑ 390.6 mV | ↑ 333.4 mV | ↑ -700 µA | ↑ 2.2503 V | ↑ 28.5965 V | ↑ 700 µA |

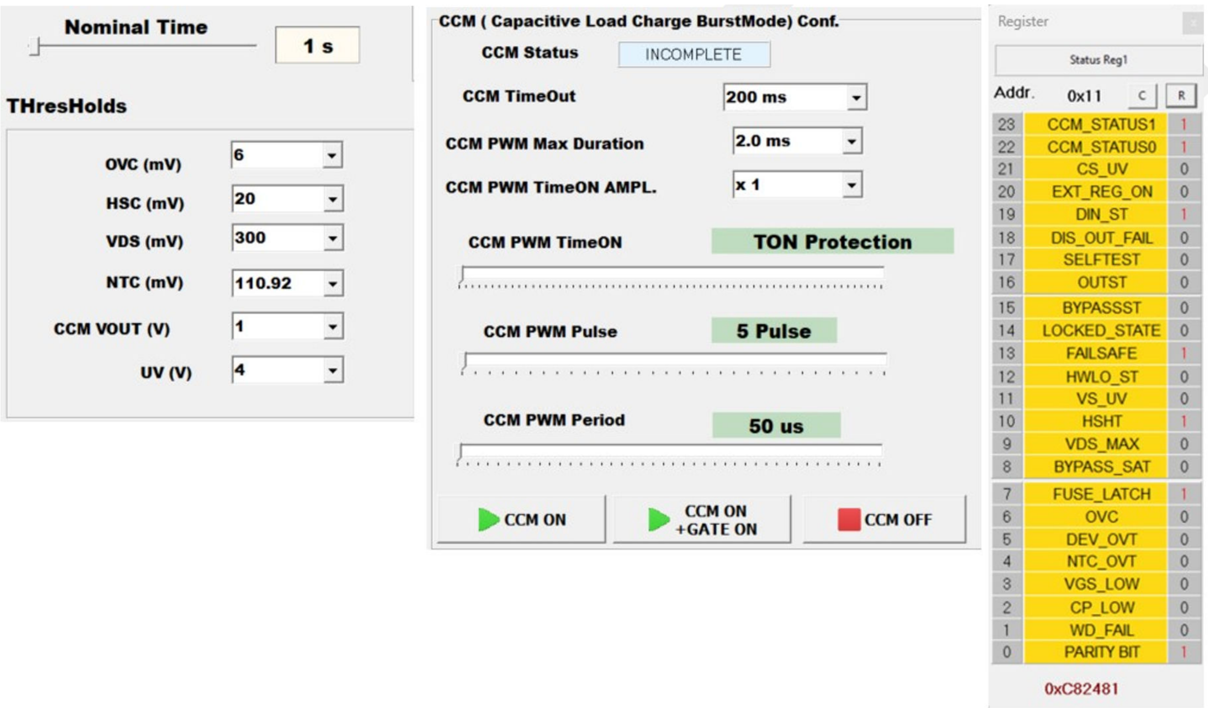
HD 12 Bits
Tbase -15.0 ms 5.00 ms/div 2.5 MS 50 MS/s
Trigger C4 DC Stop 11.0 V Edge Positive
X1= 7.99886 ms ΔX= 1.87432 ms
X2= 9.87318 ms 1/ΔX= 533.527 Hz

Also, in case of the device in Fail-safe state, the CCM operation is incomplete after 10 ms, with $V_{OUT}$ reaching 0.4 V after the five set pulses. Considering that CCM operations in Fail-safe are activated by DIN toggling ending with DIN high, the DIAG signal remains low and FUSE_LATCH + HSC are reported on SR#1 together with the CCM STATUS incomplete as shown in the images below related to trial A3.

## 3.3 Trial Setup A3

- $V_B$ = 13 V
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 2.2 mF (measured 2.08 mF)
- Device in Fail-safe state recovering default NVM setting:
  - CCM_VOUT_THR = 1 V
  - OVC_THR = OVC_THRS_0 → 6 mV
  - HSC_THR = VHSC_THRS_0 → 20 mV
  - T_NOM = $T\_NOM_{MIN}$ → 1 s
  - CCM_PWM_TON = $T_{ON}$ stopped by protection
  - CCM_PWM_SC_T_NB = 5 pulses
  - CCM_PWM_T = 50 µs
  - CCM_PWM_TON_MF = 1 x
  - CCM_TIMEOUT = 200 ms
  - CCM_PWM_SC_T = 2 ms
  - GUI settings collected at the end of CCM operations as shown in Figure 13

Figure 13. CCM configuration and result from GUI for test setup A3



**Nominal Time** 1 s

**THresHolds**

OVC (mV): 6
HSC (mV): 20
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

**CCM ( Capacitive Load Charge BurstMode) Conf.**

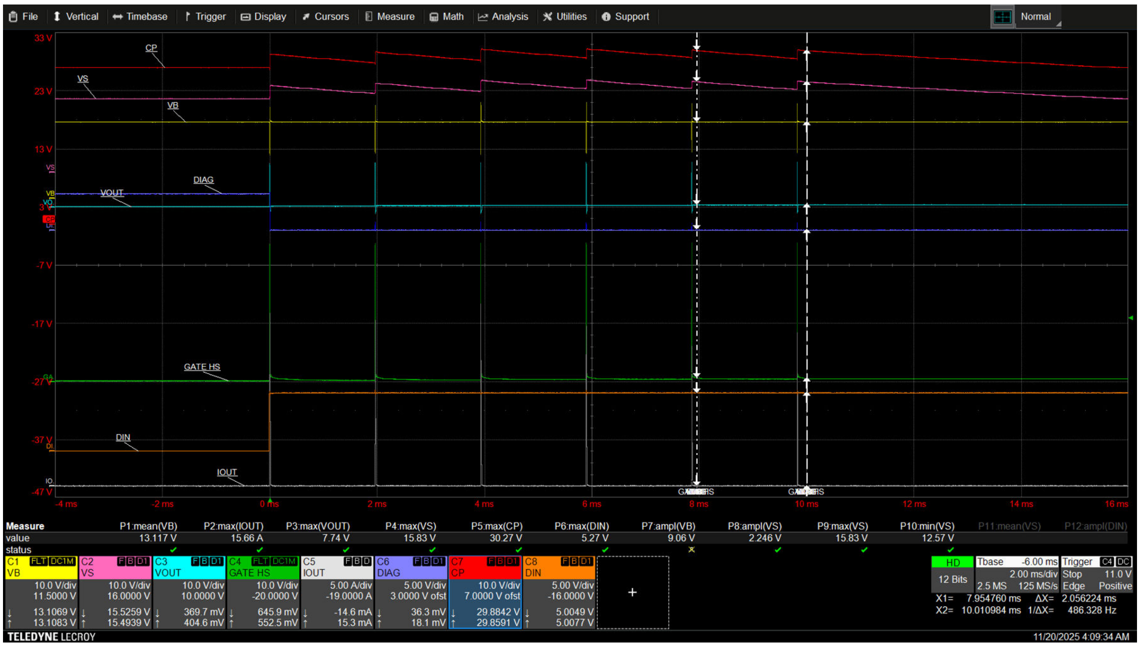
CCM Status: INCOMPLETE
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 1
CCM PWM TimeON: TON Protection
CCM PWM Pulse: 5 Pulse
CCM PWM Period: 50 us

Addr. 0x11

| | | |
|---|---|---|
| 23 | CCM_STATUS1 | 1 |
| 22 | CCM_STATUS0 | 1 |
| 21 | CS_UV | 0 |
| 20 | EXT_REG_ON | 0 |
| 19 | DIN_ST | 1 |
| 18 | DIS_OUT_FAIL | 0 |
| 17 | SELFTEST | 0 |
| 16 | OUTST | 0 |
| 15 | BYPASSST | 0 |
| 14 | LOCKED_STATE | 0 |
| 13 | FAILSAFE | 1 |
| 12 | HWLO_ST | 0 |
| 11 | VS_UV | 0 |
| 10 | HSHT | 1 |
| 9 | VDS_MAX | 0 |
| 8 | BYPASS_SAT | 0 |
| 7 | FUSE_LATCH | 1 |
| 6 | OVC | 0 |
| 5 | DEV_OVT | 0 |
| 4 | NTC_OVT | 0 |
| 3 | VGS_LOW | 0 |
| 2 | CP_LOW | 0 |
| 1 | WD_FAIL | 0 |
| 0 | PARITY BIT | 1 |

0xC82481

Figure 14. Waveforms acquired during CCM with test setup A3



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(DIN) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(DIN) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 13.117 V | 15.66 A | 7.74 V | 15.83 V | 30.27 V | 5.27 V | 9.06 V | 2.246 V | 15.83 V | 12.57 V | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ | ✓ | ✓ | | |

| C1 FLT DC1M VB | C2 F B D1 VS | C3 F B D1 VOUT | C4 FLT DC1M GATE HS | C5 F B D IOUT | C6 F B D1 DIAG | C7 F B D1 CP | C8 F B D1 DIN |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 10.0 V/div | 10.0 V/div | 10.0 V/div | 5.00 A/div | 5.00 V/div | 10.0 V/div | 5.00 V/div |
| 11.5000 V | 16.0000 V | 10.0000 V | -20.0000 V | -19.0000 A | 3.0000 V ofst | 7.0000 V ofst | -16.0000 V |
| ↓ 13.1069 V | ↓ 15.5259 V | ↓ 369.7 mV | ↓ 645.9 mV | ↓ -14.6 mA | ↓ 36.3 mV | ↓ 29.8842 V | ↓ 5.0049 V |
| ↑ 13.1083 V | ↑ 15.4939 V | ↑ 404.6 mV | ↑ 552.5 mV | ↑ 15.3 mA | ↑ 18.1 mV | ↑ 29.8591 V | ↑ 5.0077 V |

HD 12 Bits
Tbase -6.00 ms 2.00 ms/div 2.5 MS 125 MS/s
Trigger C4 DC Stop 11.0 V Edge Positive
X1= 7.954760 ms ΔX= 2.056224 ms
X2= 10.010984 ms 1/ΔX= 486.328 Hz
11/20/2025 4:09:34 AM

Figure 15. Zoomed view on DIN toggling activating CCM in Fail-safe with test setup A3

| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(DIN) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(DIN) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 13.068 V | 11.95 A | 8.44 V | 14.55 V | 28.82 V | 6.10 V | 8.29 V | 1.875 V | 14.55 V | 12.28 V | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ | ✓ | ✓ | | |

| C1 E F D1 VB | C2 E F B D1 VS | C3 E F B D1 VOUT | C4 E F D1 GATE HS | C5 E F B D IOUT | C6 E F B D1 DIAG | C7 E F B D1 CP | C8 E F B D1 DIN |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 10.0 V/div | 10.0 V/div | 10.0 V/div | 5.00 A/div | 5.00 V/div | 10.0 V/div | 5.00 V/div |
| 11.5000 V | 16.0000 V | 10.0000 V | -20.0000 V | -19.0000 A | 3.0000 V ofst | 7.0000 V ofst | -16.0000 V |
| ↓ 13.1543 V | ↓ 12.6381 V | ↓ 4.2 mV | ↓ 86.5 mV | ↓ 4.9 mA | ↓ 3.1264 V | ↓ 26.8987 V | ↓ 44.6 mV |
| ↑ 13.1236 V | ↑ 12.6172 V | ↑ 15.3 mV | ↑ 90.7 mV | ↑ 11.2 mA | ↑ 3.1124 V | ↑ 26.8903 V | ↑ 27.2 mV |

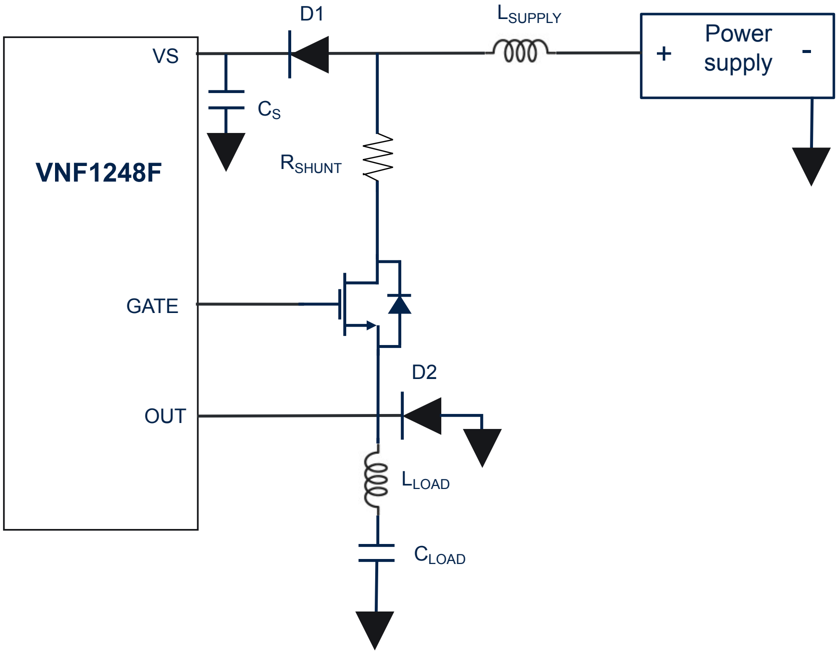
HD 12 Bits
Timebase -5.0 µs 5.00 µs/div 500 kS 10 GS/s
Trigger C4 DC Stop 11.0 V Edge Positive
X1= -12.2271 µs ΔX= 3.1975 µs
X2= -9.0296 µs 1/ΔX= 312.744 kHz
11/20/2025 4:11:23 AM

# 4 Application boost effects

An important aspect that the user must consider to correctly dimension the final application is that the combination of the circuit itself and the parasitic inductance of the surrounding connections leads results in a hidden boost architecture, potentially causing hazardous effects.

The hidden boost architecture is illustrated in Figure 16, where the inductance effect arises from the potentially long wire connecting the battery to the module on which the VNF1248F application is mounted.

Figure 16. **Hidden boost schematization**



The hazardous effects of the hidden boost architecture are evident in the setup analyzed in the previous chapters. In Figure 8, $V_S$ achieves a maximum value of 60.3 V.

During the standard charging phase, the voltage on the VS pin increases along with the output voltage. In addition to the VS pin, the ISNS_P and ISNS_N pins are also impacted by the side effects of the hidden boost. Of course, the CP voltage value also increases as a consequence of this effect.

The VNF1248F can withstand these side effects as long as the voltage of the affected pins remains below their absolute maximum rating (AMR) value, which is 70 V for the VS, ISNS_P, and ISNS_N pins and 90 V for the CP pin.

To mitigate the hazardous effects of the hidden boost, an additional capacitance $C_{IN}$ can be placed between the supply and ground connectors of the module.

This solution is suggested for 12 V applications, while it is absolutely needed for applications with a 24 V or 48 V battery to avoid reaching dangerous voltage values above AMR. In this case, a capacitance or a combination of caps, must fit with the required breakdown voltage (> 60 V) and provide a clamping voltage below the AMR (70 V).

To select the input capacitor $C_{IN}$, we performed several checks and calculations in our circuit using an energy-balance approach: the energy stored in the parasitic inductance $L_{SUPPLY}$ is transferred to the input capacitor $C_{IN}$, causing its voltage to rise from $V_{BATT}$ to $V_S$ (which must remain ≤ 70 V).

The schematic adding $C_{IN}$ and the schematic of the ST application circuit, showing the points in which the voltage and current measurements were performed, are reported below:

Figure 17. **Schematic of applicative circuit with the insertion of dedicated $C_{IN}$ to smooth boost effect**

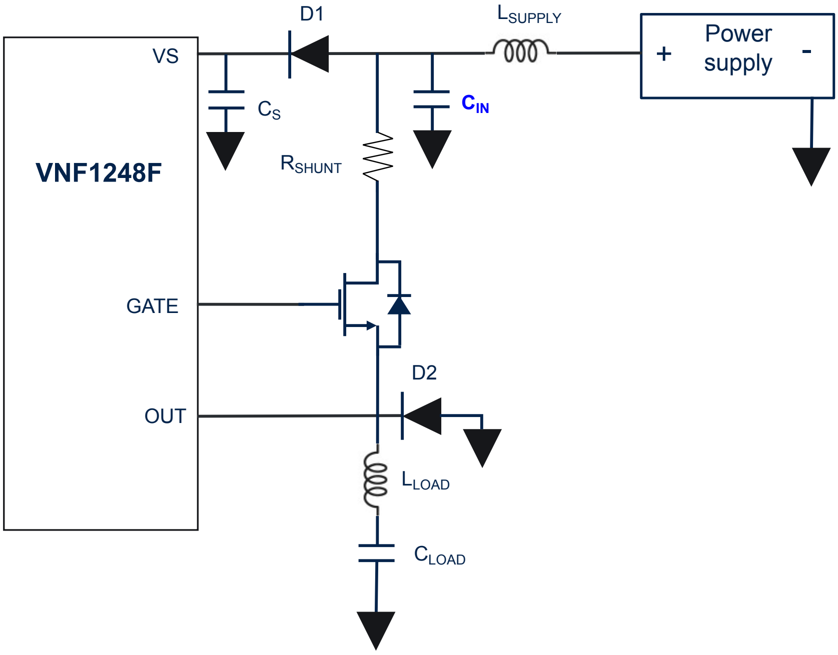
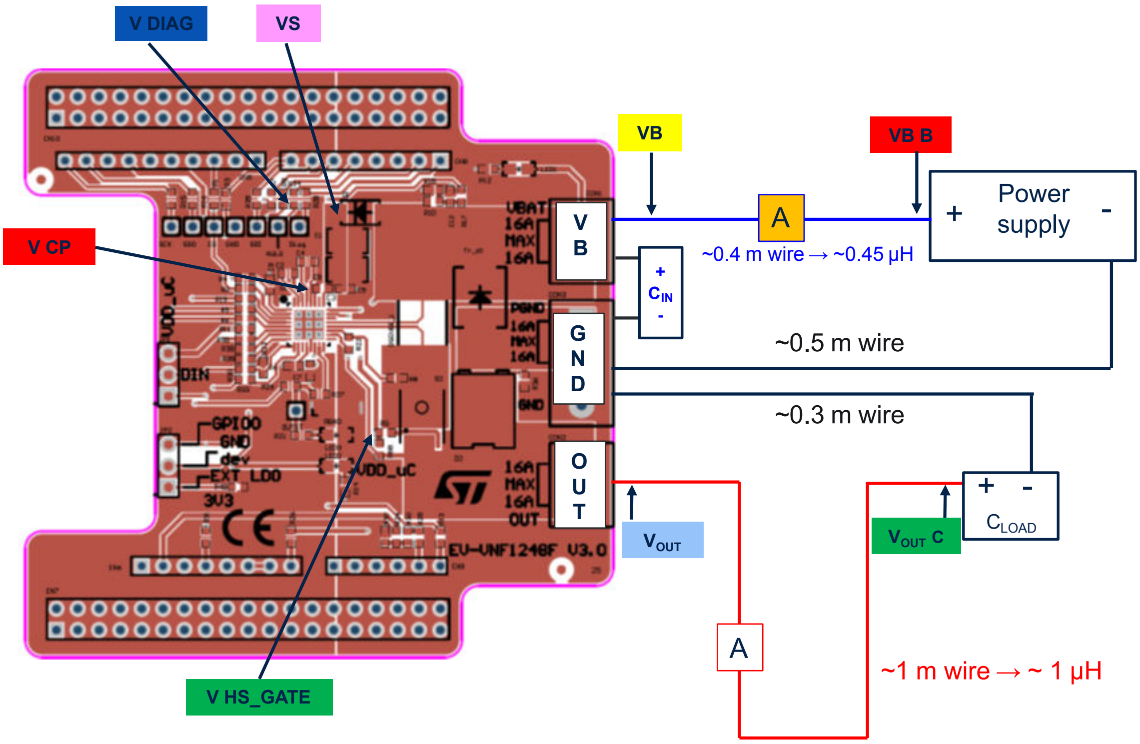
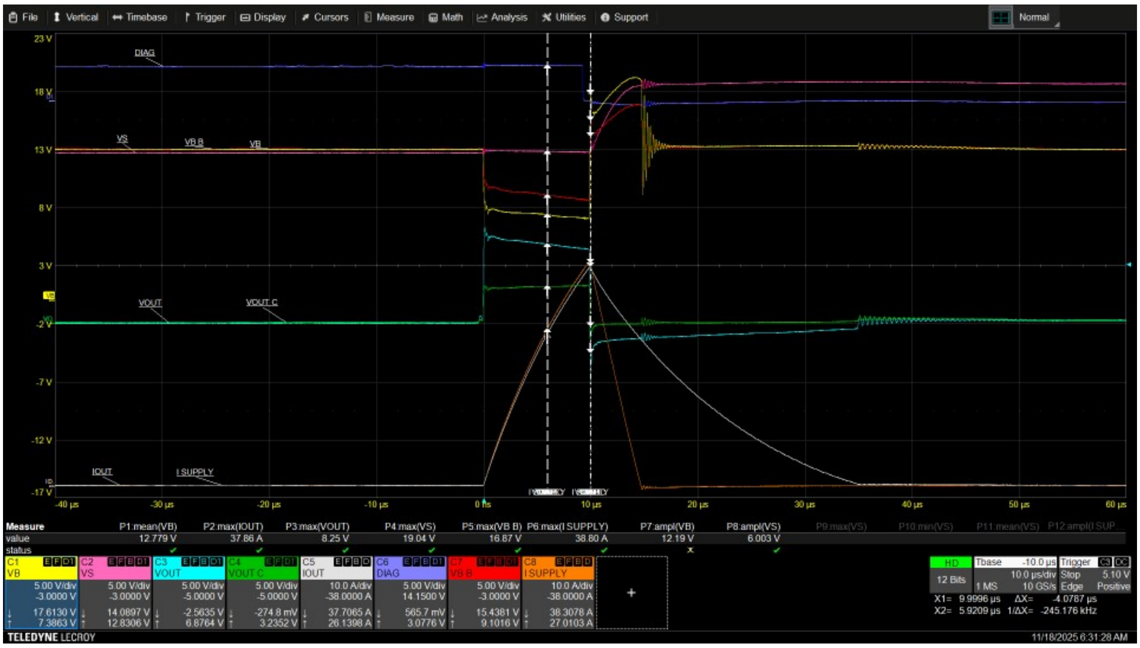


Figure 18. **Schematic of applicative circuit used to assess the dimension of $C_{IN}$**



First of all, we focused on the waveforms captured during the 1st pulse related to trial setup A1, in which no $C_{IN}$ was mounted, to assess the $L_{SUPPLY}$ value and develop a model able to relate the VS step to the adopted setups.

Figure 19. **Waveforms collected on 1st CCM pulse using setup A1**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(VB B) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.779 V | 37.86 A | 8.25 V | 19.04 V | 16.87 V | 38.80 A | 12.19 V | 6.003 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 VOUT C | C5 IOUT | C6 DIAG | C7 VB B | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 5.00 V/div | 5.00 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| -3.0000 V | -3.0000 V | -5.0000 V | -5.0000 V | -38.0000 A | 14.1500 V | -3.0000 V | -38.0000 A |
| ↓ 17.6130 V | ↓ 14.0897 V | ↓ -2.5635 V | ↓ -274.8 mV | ↓ 37.7065 A | ↓ 565.7 mV | ↓ 15.4381 V | ↓ 38.3078 A |
| ↑ 7.3863 V | ↑ 12.8306 V | ↑ 6.8764 V | ↑ 3.2352 V | ↑ 26.1398 A | ↑ 3.0776 V | ↑ 9.1016 V | ↑ 27.0103 A |

HD 12 Bits
Tbase -10.0 µs 10.0 µs/div 1 MS 10 GS/s
Trigger C3 DC Stop 5.10 V Edge Positive
X1= 9.9996 µs ΔX= -4.0787 µs
X2= 5.9209 µs 1/ΔX= -245.176 kHz
11/18/2025 6:31:28 AM

Once CCM is started, the power MOSFET is turned ON and the HS_GATE stays ON until hard short protection is triggered (in this case $T_{ON}$ = 11 µs). The two current peaks are very similar in the ramp up but differ in the ramp down due to the contribution of D2 connected to OUT. In ~4.9 µs after HS_GATE turns OFF, the current from the power supply (in orange) charges the $C_S$.

The $L_{SUPPLY}$ can be calculated by the formula:

$$L_{SUPPLY} = \mathrm{VL}_{SUPPLY} * \frac{\mathrm{dt}}{\mathrm{di}}$$

Considering that:

- $\Delta VL_{SUPPLY}$ = VB B - VB = 1.6 V
- dt = 11 µs
- di = $I_{PEAK\ SUPPLY}$ = 39.6 A

We have $L_{SUPPLY}$ = 444 nH

For the principle of energy conservation, we have that the energy stored in the parasitic inductance $L_{SUPPLY}$ is transferred to the input capacitor (only $C_S$ in this case) causing its voltage to rise from $V_B$ to $V_S$ (equal to ΔV on the extremes of the input capacitance):

$$E_{LSUPPLY} = \frac{1}{2} * L_{SUPPLY} * I_{PEAKSUPPLY}{}^{2} = E_C = \frac{1}{2} * C * \Delta V^2$$

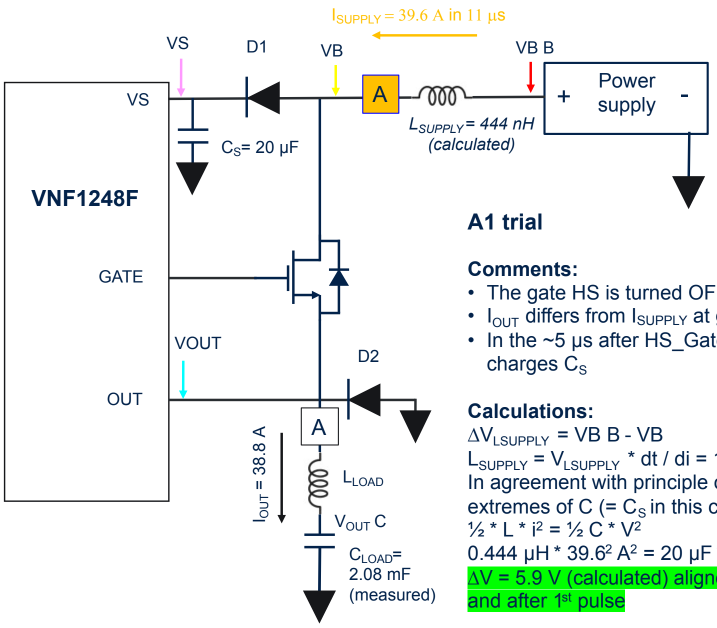
$$\Delta V^2 = \frac{L_{SUPPLY} * I_{PEAKSUPPLY}{}^{2}}{C}$$

Considering that C = $C_S$ + $C_{IN}$ = 20 µF

ΔV = 5.9 V that is fully aligned with the 6.0 V amplitude measured by the pink probe on the VS signal before and after the 1st pulse.

This calculation is summarized in the figure below.

**Figure 20.** Schematic and calculation adopted in setup A1



**A1 trial**

**Comments:**

- The gate HS is turned OFF due to HSC in 1st pulse that has a $t_{ON}$ = 11 µs
- $I_{OUT}$ differs from $I_{SUPPLY}$ at gate turn-on due to D2 contribution
- In the ~5 µs after HS_Gate turn-off, the $I_{PEAK}$ coming from the supply charges $C_S$

**Calculations:**

$\Delta V_{LSUPPLY}$ = VB B - VB

$L_{SUPPLY} = V_{LSUPPLY} * dt / di$ = 1.6 V * 11 µs / 39.6 A = 0.444 µH

In agreement with principle of energy conservation the Delta V at the extremes of C (= $C_S$ in this case) can be assessed as per below:

$½ * L * i^2 = ½ C * V^2$

0.444 µH * $39.6^2$ $A^2$ = 20 µF * $V^2$

$\Delta V$ = 5.9 V (calculated) aligned with the 6.0 V gap measured on VS before and after 1st pulse

To consolidate the above model and assess the dimension of $C_{IN}$ value to be added to $C_S$ to achieve the wanted safe $\Delta V$ on $V_S$, we repeated the charge of the same $C_{LOAD}$ with the same setup of trial A1 by inserting different $C_{IN}$ with measured value of 18.6 µF, 37.9 µF, and 42.6 µF and verifying the $\Delta V$ on $V_S$ generating trials B1, B2 and B3 with results summarized in table 4 below and detailed in the next paragraphs.

**Table 4.** Evaluations done to assess $L_{SUPPLY}$

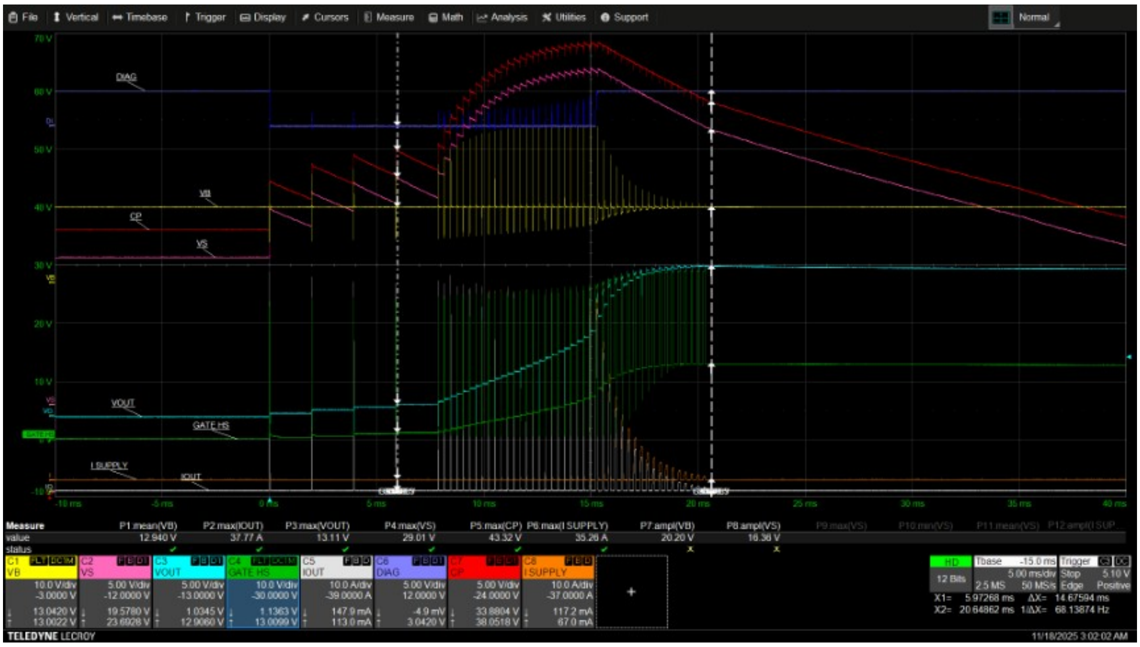
| Trial | C = $C_S$ + $C_{IN}$ (mounted) in µF | Max CP value in V | Max Vs value in V | $t_{CHARGE}$ of $C_{Load}$ in ms | $I_{PEAK}$ supply measured in A | HS_GATE $t_{ON}$ measured in µs | $\Delta V_{LSUPPLY}$ measured in V | $L_{SUPPPLY}$ calculated in µH | $\Delta V$ measured in V | $\Delta V$ calculated in V |
|---|---|---|---|---|---|---|---|---|---|---|
| **A1** | 20 | 74.7 | 60.3 | 20.9 | 39.6 | 11.0 | 1.60 | 0.444 | 6.00 | 5.90 |
| **B1** | 38.6 | 43.3 | 29.0 | 20.6 | 37.3 | 10.8 | 1.60 | 0.463 | 4.18 | 4.09 |
| **B2** | 58.6 | 34.8 | 20.4 | 20.9 | 31.1 | 9.3 | 1.50 | 0.448 | 2.70 | 2.70 |
| **B3** | 63.4 | 29.8 | 15.4 | 20.6 | 31.1 | 9.0 | 1.55 | 0.449 | 2.69 | 2.62 |

## 4.1 Trial Setup B1

Trial B1 uses the same setup as trial A1 (DUT in Unlocked state) with the only insertion of $C_{IN}$ of nominal 22 uF (measured 18.6 uF).

The $C_{LOAD}$ is charged in approximately the same time while the max achieved values on CP and VS appear smoother compared to trial A1 as shown in Figure 21.

Figure 21. Waveforms acquired during CCM with setup B1

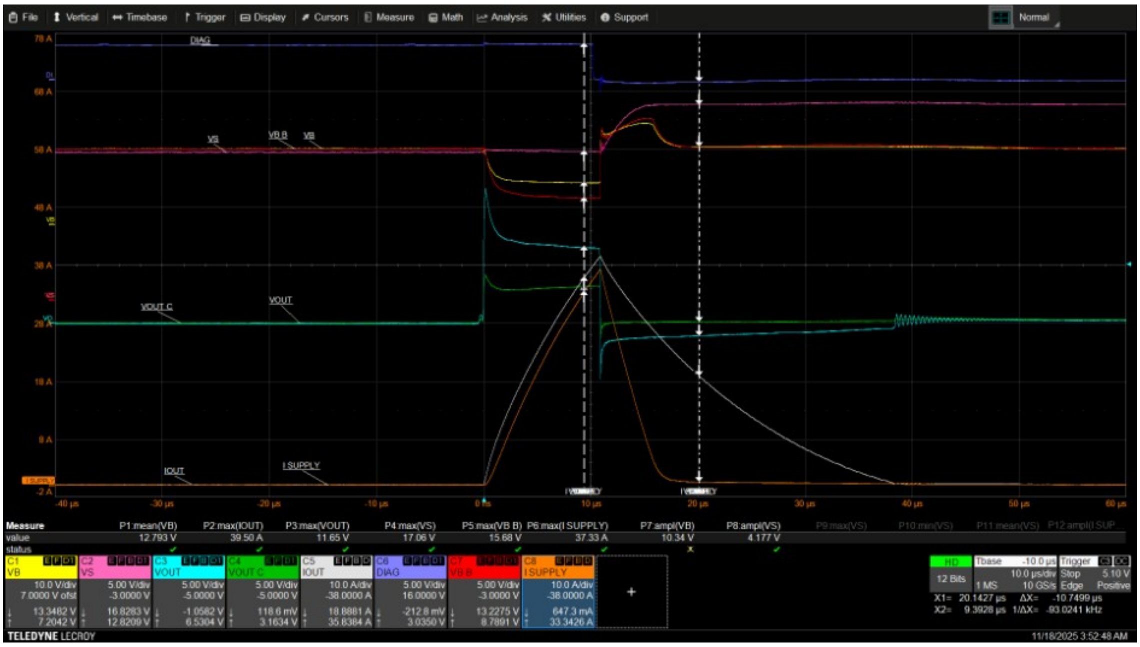


| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.940 V | 37.77 A | 13.11 V | 29.01 V | 43.32 V | 35.26 A | 20.20 V | 16.36 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✗ | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 GATE HS | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| -3.0000 V | -12.0000 V | -13.0000 V | -30.0000 V | -39.0000 A | 12.0000 V | -24.0000 V | -37.0000 A |
| ↓ 13.0420 V | ↓ 19.5780 V | ↓ 1.0345 V | ↓ 1.1363 V | ↓ 147.9 mA | ↓ -4.9 mV | ↓ 33.8804 V | ↓ 117.2 mA |
| ↑ 13.0022 V | ↑ 23.6928 V | ↑ 12.9060 V | ↑ 13.0099 V | ↑ 113.0 mA | ↑ 3.0420 V | ↑ 38.0518 V | ↑ 67.0 mA |

HD 12 Bits
Tbase -15.0 ms
5.00 ms/div
2.5 MS 50 MS/s
Trigger C3 DC
Stop 5.10 V
Edge Positive
X1= 5.97268 ms ΔX= 14.67594 ms
X2= 20.64862 ms 1/ΔX= 68.13874 Hz

Figure 22. Waveforms collected on 1st CCM pulse using setup B1

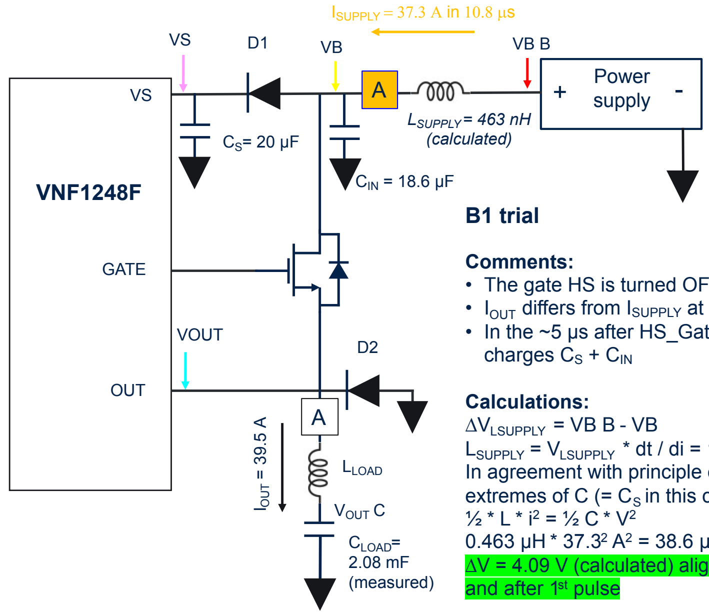


| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(VB B) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.793 V | 39.50 A | 11.65 V | 17.06 V | 15.68 V | 37.33 A | 10.34 V | 4.177 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 VOUT C | C5 IOUT | C6 DIAG | C7 VB B | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 5.00 V/div | 5.00 V/div | 5.00 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 7.0000 V ofst | -3.0000 V | -5.0000 V | -5.0000 V | -38.0000 A | 16.0000 V | -3.0000 V | -38.0000 A |
| ↓ 13.3482 V | ↓ 16.8283 V | ↓ -1.0582 V | ↓ 118.6 mV | ↓ 18.8881 A | ↓ -212.8 mV | ↓ 13.2275 V | ↓ 647.3 mA |
| ↑ 7.2042 V | ↑ 12.8209 V | ↑ 6.5304 V | ↑ 3.1634 V | ↑ 35.8384 A | ↑ 3.0350 V | ↑ 8.7891 V | ↑ 33.3426 A |

HD 12 Bits
Tbase -10.0 µs
10.0 µs/div
1 MS 10 GS/s
Trigger C3 DC
Stop 5.10 V
Edge Positive
X1= 20.1427 µs ΔX= -10.7499 µs
X2= 9.3928 µs 1/ΔX= -93.0241 kHz

Figure 23. **Schematic and calculation adopted in setup B1**



**B1 trial**

**Comments:**

- The gate HS is turned OFF due to HSC in 1st pulse that has a $t_{ON}$ = 10.8 µs
- $I_{OUT}$ differs from $I_{SUPPLY}$ at gate turn-on due to D2 and $C_{IN}$ contributions
- In the ~5 µs after HS_Gate turn-off, the $I_{PEAK}$ coming from the supply charges $C_S$ + $C_{IN}$

**Calculations:**

$\Delta V_{LSUPPLY}$ = VB B - VB

$L_{SUPPLY}$ = $V_{LSUPPLY}$ * dt / di = 1.6 V * 10.8 µs / 37.3 A = 0.463 µH

In agreement with principle of energy conservation the Delta V at the extremes of C (= $C_S$ in this case) can be assessed as per below:

½ * L * i² = ½ C * V²

0.463 µH * 37.3² A² = 38.6 µF * V²

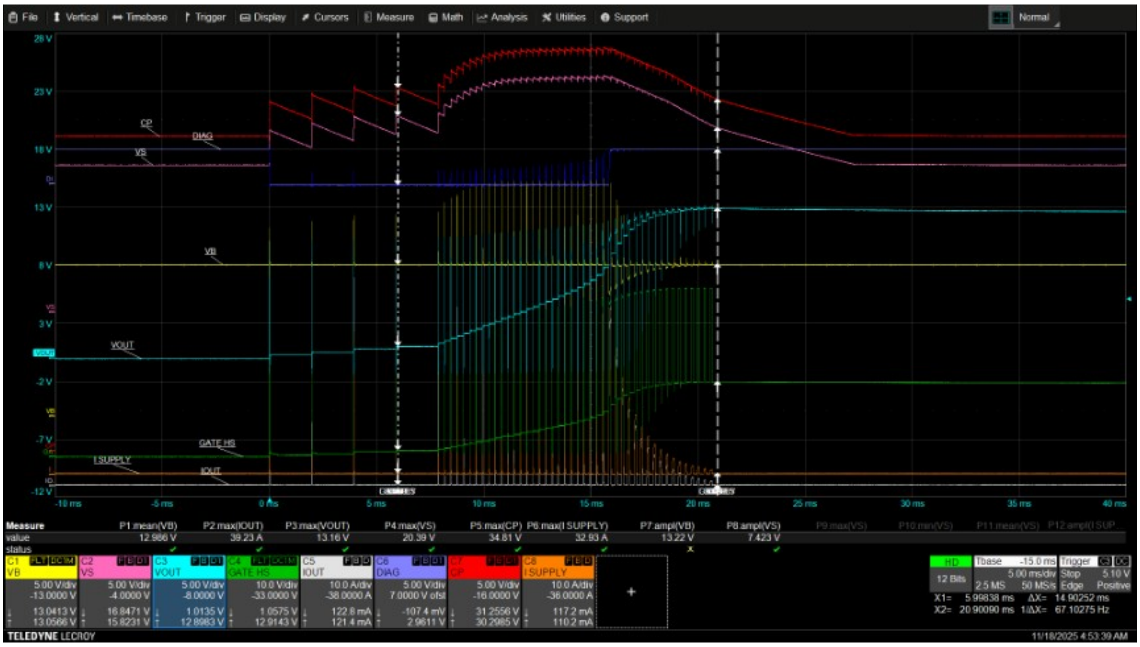
ΔV = 4.09 V (calculated) aligned with the 4.18 V gap measured on VS before and after 1st pulse

## 4.2 Trial Setup B2

Trial B2 uses the same setup as trial A1 (DUT in Unlocked state) with the only insertion of $C_{IN}$ of nominal 2 * 22 uF (measured 38.6 uF).

The $C_{LOAD}$ is charged in approximately the same time of trials A1 and B1 while the max achieved values on CP and VS appear even smoother.

Figure 24. **Waveforms acquired during CCM with setup B2**

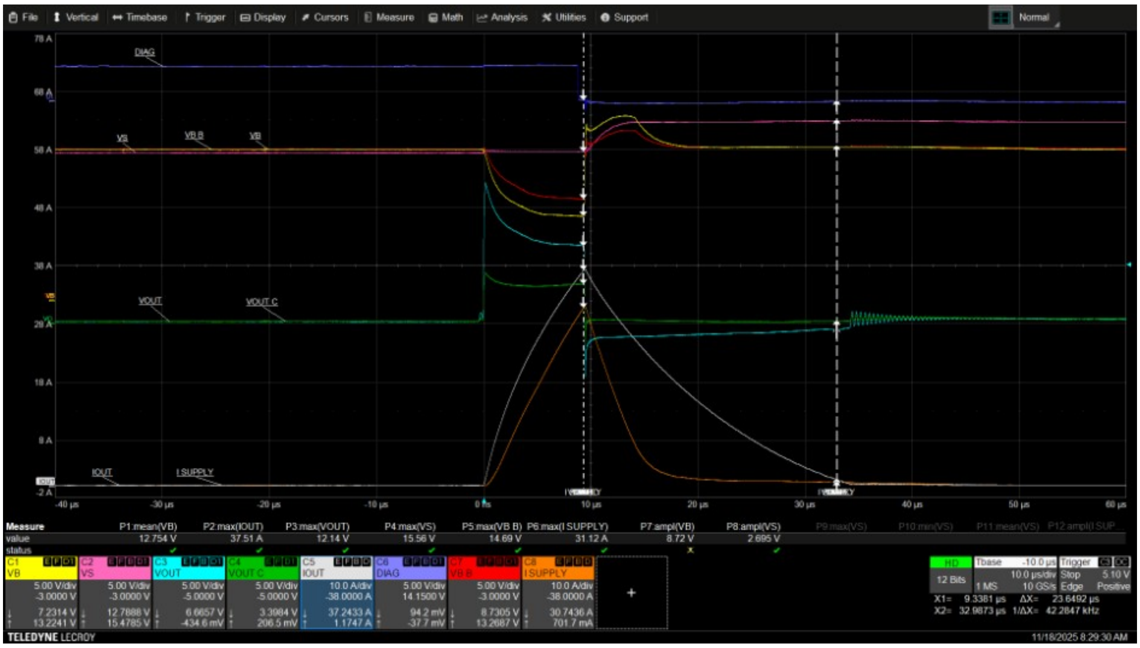


| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.986 V | 39.23 A | 13.16 V | 20.39 V | 34.81 V | 32.93 A | 13.22 V | 7.423 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 GATE HS | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| -13.0000 V | -4.0000 V | -8.0000 V | -33.0000 V | -38.0000 A | 7.0000 V ofst | -16.0000 V | -36.0000 A |
| ↓ 13.0413 V | ↓ 16.8471 V | ↓ 1.0135 V | ↓ 1.0575 V | ↓ 122.8 mA | ↓ -107.4 mV | ↓ 31.2556 V | ↓ 117.2 mA |
| ↑ 13.0566 V | ↑ 15.8231 V | ↑ 12.8983 V | ↑ 12.9143 V | ↑ 121.4 mA | ↑ 2.9611 V | ↑ 30.2985 V | ↑ 110.2 mA |

HD 12 Bits
Tbase -15.0 ms 5.00 ms/div 2.5 MS 50 MS/s
Trigger Stop 5.10 V Edge Positive
X1= 5.99838 ms ΔX= 14.90252 ms
X2= 20.90090 ms 1/ΔX= 67.10275 Hz

Figure 25. **Waveforms collected on 1st CCM pulse using setup B2**

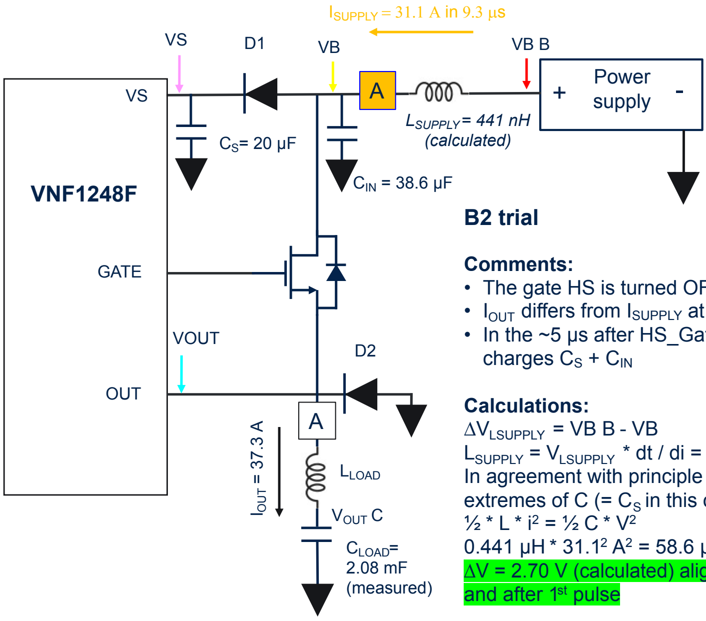


| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(VB B) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.754 V | 37.51 A | 12.14 V | 15.56 V | 14.69 V | 31.12 A | 8.72 V | 2.695 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | X | ✓ | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 VOUT C | C5 IOUT | C6 DIAG | C7 VB B | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 5.00 V/div | 5.00 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| -3.0000 V | -3.0000 V | -5.0000 V | -5.0000 V | -38.0000 A | 14.1500 V | -3.0000 V | -38.0000 A |
| ↓ 7.2314 V | ↓ 12.7888 V | ↓ 6.6657 V | ↓ 3.3984 V | ↓ 37.2433 A | ↓ 94.2 mV | ↓ 8.7305 V | 30.7436 A |
| ↑ 13.2241 V | ↑ 15.4785 V | ↑ -434.6 mV | ↑ 206.5 mV | ↑ 1.1747 A | ↑ -37.7 mV | ↑ 13.2687 V | 701.7 mA |

HD 12 Bits
Tbase -10.0 µs
10.0 µs/div
1 MS 10 GS/s
Trigger C3 DC
Stop 5.10 V
Edge Positive
X1= 9.3381 µs ΔX= 23.6492 µs
X2= 32.9873 µs 1/ΔX= 42.2847 kHz
11/18/2025 8:29:30 AM

Figure 26. **Schematic and calculation adopted in setup B2**



**B2 trial**

**Comments:**

- The gate HS is turned OFF due to HSC in 1st pulse that has a $t_{ON}$ = 9.3 µs
- $I_{OUT}$ differs from $I_{SUPPLY}$ at gate turn-on due to D2 and $C_{IN}$ contributions
- In the ~5 µs after HS_Gate turn-off, the $I_{PEAK}$ coming from the supply charges $C_S$ + $C_{IN}$

**Calculations:**

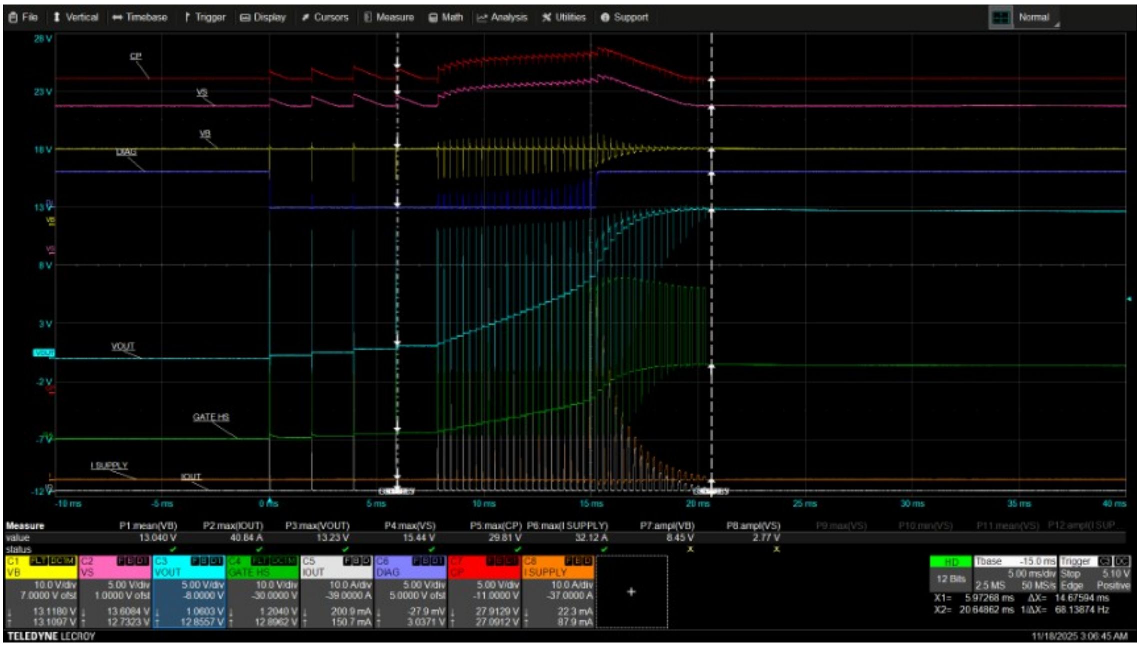
$\Delta V_{LSUPPLY}$ = VB B - VB
$L_{SUPPLY} = V_{LSUPPLY}$ * dt / di = 1.5 V * 9.3 µs / 31.1 A = 0.441 µH
In agreement with principle of energy conservation the Delta V at the extremes of C (= $C_S$ in this case) can be assessed as per below:
$\frac{1}{2} * L * i^2 = \frac{1}{2} C * V^2$
$0.441\ \mu H * 31.1^2\ A^2 = 58.6\ \mu F * V^2$
ΔV = 2.70 V (calculated) aligned with the 2.70 V gap measured on VS before and after 1st pulse

## 4.3 Trial Setup B3

Trial B3 uses the same setup as trial A1 (DUT in Unlocked state) with the only insertion of $C_{IN}$ of nominal 47 uF (measured 43.4 uF).

The $C_{LOAD}$ is charged in approximately the same time of previous trials A1, B1 and B2 while the max achieved values on CP and VS appear even smoother.

Figure 27. **Waveforms acquired during CCM with setup B3**

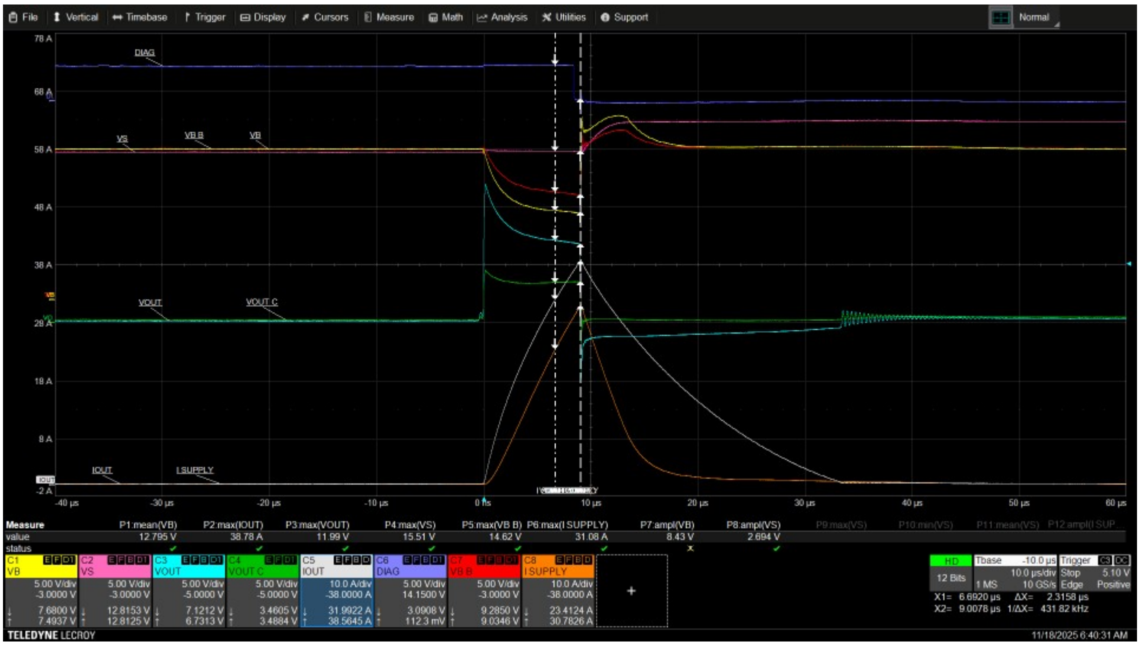


| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 13.040 V | 40.84 A | 13.23 V | 15.44 V | 29.81 V | 32.12 A | 8.45 V | 2.77 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✗ | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 GATE HS | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 7.0000 V ofst | 1.0000 V ofst | -8.0000 V | -30.0000 V | -39.0000 A | 5.0000 V ofst | -11.0000 V | -37.0000 A |
| ↓ 13.1180 V | ↓ 13.6084 V | ↓ 1.0603 V | ↓ 1.2040 V | ↓ 200.9 mA | ↓ -27.9 mV | ↓ 27.9129 V | ↓ 22.3 mA |
| ↑ 13.1097 V | ↑ 12.7323 V | ↑ 12.8557 V | ↑ 12.8962 V | ↑ 150.7 mA | ↑ 3.0371 V | ↑ 27.0912 V | ↑ 87.9 mA |

HD 12 Bits
Tbase -15.0 ms, 5.00 ms/div, 2.5 MS, 50 MS/s
Trigger C3 DC, Stop 5.10 V, Edge Positive
X1= 5.97268 ms ΔX= 14.67594 ms
X2= 20.64862 ms 1/ΔX= 68.13874 Hz
11/18/2025 3:06:45 AM

Figure 28. **Waveforms collected on 1st CCM pulse using setup B3**

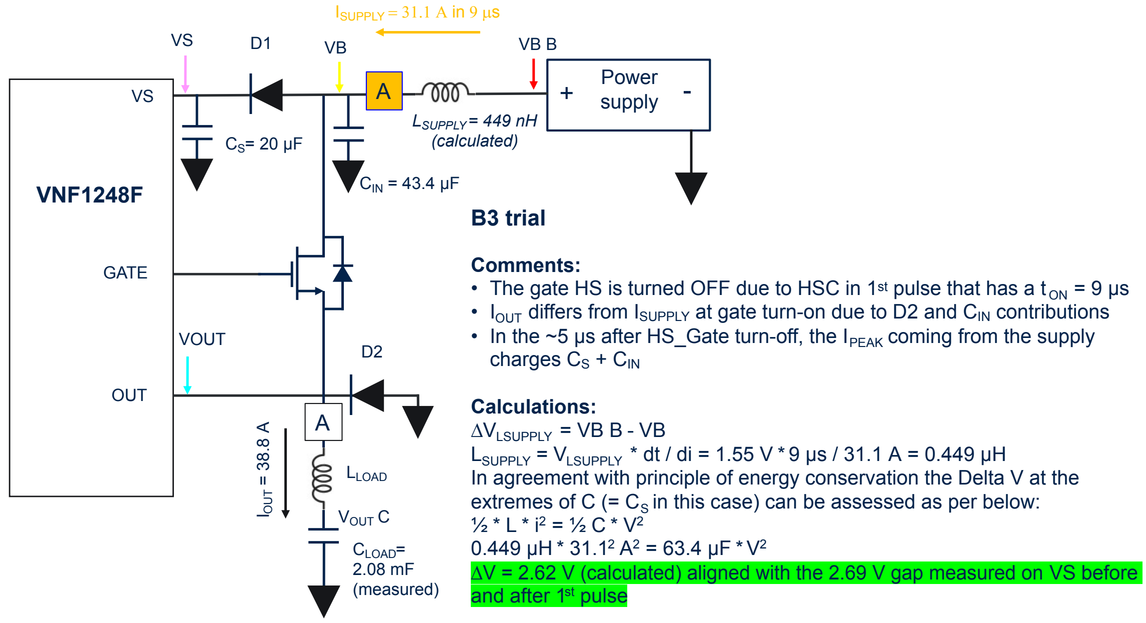


| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(VB B) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.795 V | 38.78 A | 11.99 V | 15.51 V | 14.62 V | 31.08 A | 8.43 V | 2.694 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 VOUT C | C5 IOUT | C6 DIAG | C7 VB B | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 5.00 V/div | 5.00 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| -3.0000 V | -3.0000 V | -5.0000 V | -5.0000 V | -38.0000 A | 14.1500 V | -3.0000 V | -38.0000 A |
| ↓ 7.6800 V | ↓ 12.8153 V | ↓ 7.1212 V | ↓ 3.4605 V | ↓ 31.9922 A | ↓ 3.0908 V | ↓ 9.2850 V | ↓ 23.4124 A |
| ↑ 7.4937 V | ↑ 12.8125 V | ↑ 6.7313 V | ↑ 3.4884 V | ↑ 38.5645 A | ↑ 112.3 mV | ↑ 9.0346 V | ↑ 30.7826 A |

HD 12 Bits
Tbase -10.0 µs, 10.0 µs/div, 1 MS, 10 GS/s
Trigger C3 DC, Stop 5.10 V, Edge Positive
X1= 6.6920 µs ΔX= 2.3158 µs
X2= 9.0078 µs 1/ΔX= 431.82 kHz
11/18/2025 6:40:31 AM

Figure 29. **Schematic and calculation adopted in setup B3**



**B3 trial**

**Comments:**
- The gate HS is turned OFF due to HSC in 1st pulse that has a $t_{ON}$ = 9 µs
- $I_{OUT}$ differs from $I_{SUPPLY}$ at gate turn-on due to D2 and $C_{IN}$ contributions
- In the ~5 µs after HS_Gate turn-off, the $I_{PEAK}$ coming from the supply charges $C_S$ + $C_{IN}$

**Calculations:**
$\Delta V_{LSUPPLY}$ = VB B - VB
$L_{SUPPLY}$ = $V_{LSUPPLY}$ * dt / di = 1.55 V * 9 µs / 31.1 A = 0.449 µH
In agreement with principle of energy conservation the Delta V at the extremes of C (= $C_S$ in this case) can be assessed as per below:
½ * L * $i^2$ = ½ C * $V^2$
0.449 µH * $31.1^2$ $A^2$ = 63.4 µF * $V^2$
ΔV = 2.62 V (calculated) aligned with the 2.69 V gap measured on VS before and after 1st pulse

Based on the results from above tests, we assessed that $L_{SUPPLY}$ ~450 nH. Assuming a peak current $I_{PEAK}$ ~10 A (due to the contribution of $C_S$ + $C_{IN}$), we estimated that the $C_{IN}$ value to be used to limit the ΔV on Vs to 0.4 V (a very safe value that strongly limits the boost effect):

½ * L * $i^2$ = ½ C * $V^2$

0.45 µH * $10^2$ $A^2$ = C µF * $0.4^2$

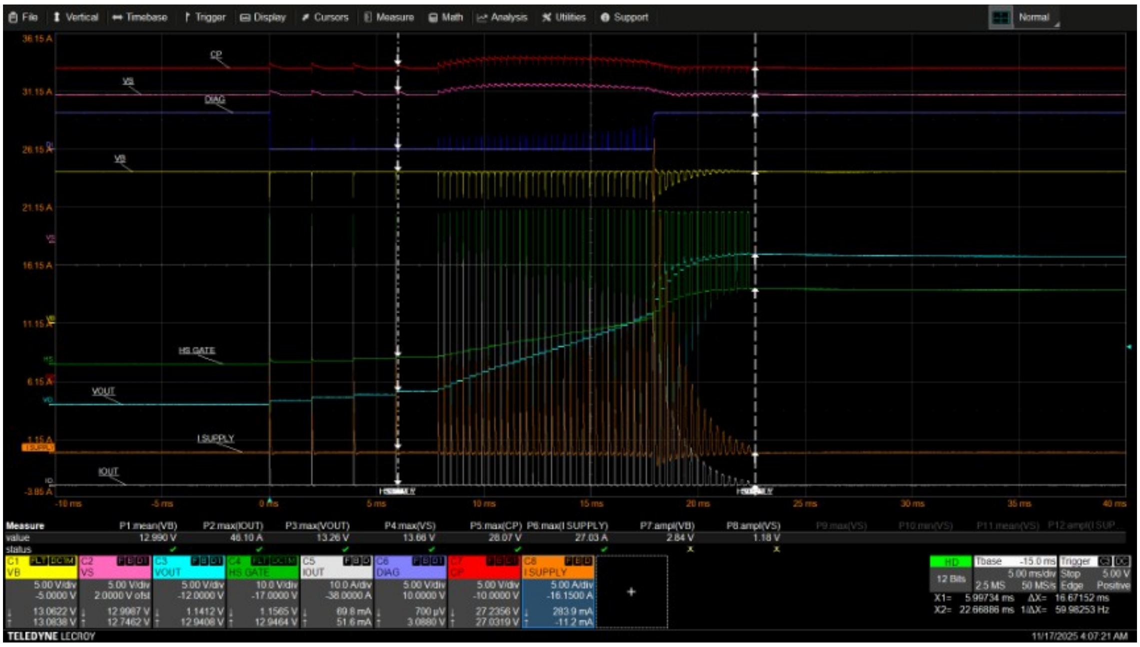
C = $C_S$ + $C_{IN}$ = 281 µF

$C_{IN}$ = 261 µF

## 4.4 Trial Setup B4

Below is the results of the CCM test using the same setup of trial A1 with insertion of $C_{IN}$ of nominal 300 µF (measured 314 µF) generating trial B4.

Figure 30. **Waveforms acquired during CCM with setup B4**

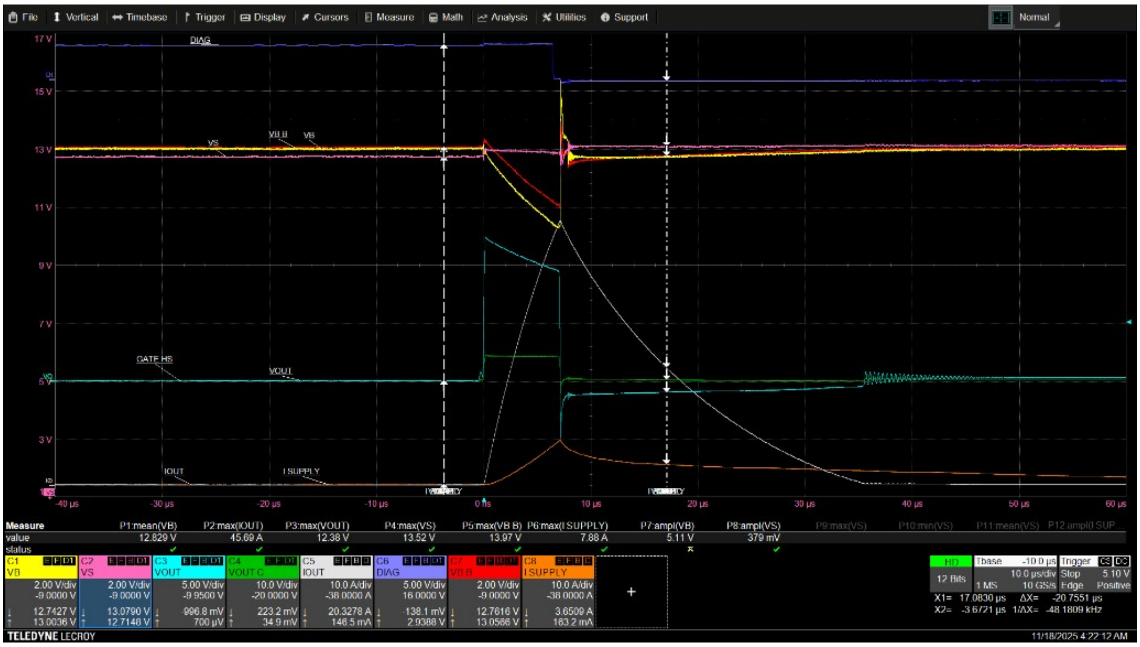


| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.990 V | 46.10 A | 13.26 V | 13.66 V | 28.07 V | 27.03 A | 2.84 V | 1.18 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | x | x | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 5.00 A/div |
| -5.0000 V | 2.0000 V ofst | -12.0000 V | -17.0000 V | -38.0000 A | 10.0000 V | -10.0000 V | -16.1500 A |
| ↓ 13.0622 V | ↓ 12.9087 V | ↓ 1.1412 V | ↓ 1.1565 V | ↓ 69.8 mA | ↓ 700 µV | ↓ 27.2356 V | ↓ 283.9 mA |
| ↑ 13.0838 V | ↑ 12.7462 V | ↑ 12.9408 V | ↑ 12.9464 V | ↑ 51.6 mA | ↑ 3.0880 V | ↑ 27.0319 V | ↑ -11.2 mA |

HD 12 Bits
Tbase -15.0 ms 5.00 ms/div 2.5 MS 50 MS/s
Trigger C3 DC Stop 5.00 V Edge Positive
X1= 5.99734 ms ΔX= 16.67152 ms
X2= 22.66886 ms 1/ΔX= 59.98253 Hz
11/17/2025 4:07:21 AM

Figure 31. **Waveforms collected on 1$^{st}$ CCM pulse using setup B4**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(VB B) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.829 V | 45.69 A | 12.38 V | 13.52 V | 13.97 V | 7.88 A | 5.11 V | 379 mV | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | x | ✓ | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 VOUT C | C5 IOUT | C6 DIAG | C7 VB B | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 2.00 V/div | 2.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 2.00 V/div | 10.0 A/div |
| -9.0000 V | -9.0000 V | -9.9500 V | -20.0000 V | -38.0000 A | 16.0000 V | -9.0000 V | -38.0000 A |
| ↓ 12.7427 V | ↓ 13.0790 V | ↓ 996.8 mV | ↓ 223.2 mV | ↓ 20.3278 A | ↓ 138.1 mV | ↓ 12.7616 V | ↓ 3.6509 A |
| ↑ 13.0036 V | ↑ 12.7148 V | ↑ 700 µV | ↑ 34.9 mV | ↑ 146.5 mA | ↑ 2.9388 V | ↑ 13.0586 V | ↑ 163.2 mA |

HD 12 Bits
Tbase -10.0 µs 10.0 µs/div 1 MS 10 GS/s
Trigger C3 DC Stop 5.10 V Edge Positive
X1= 17.0830 µs ΔX= -20.7551 µs
X2= -3.6721 µs 1/ΔX= -48.1809 kHz
11/18/2025 4:22:12 AM

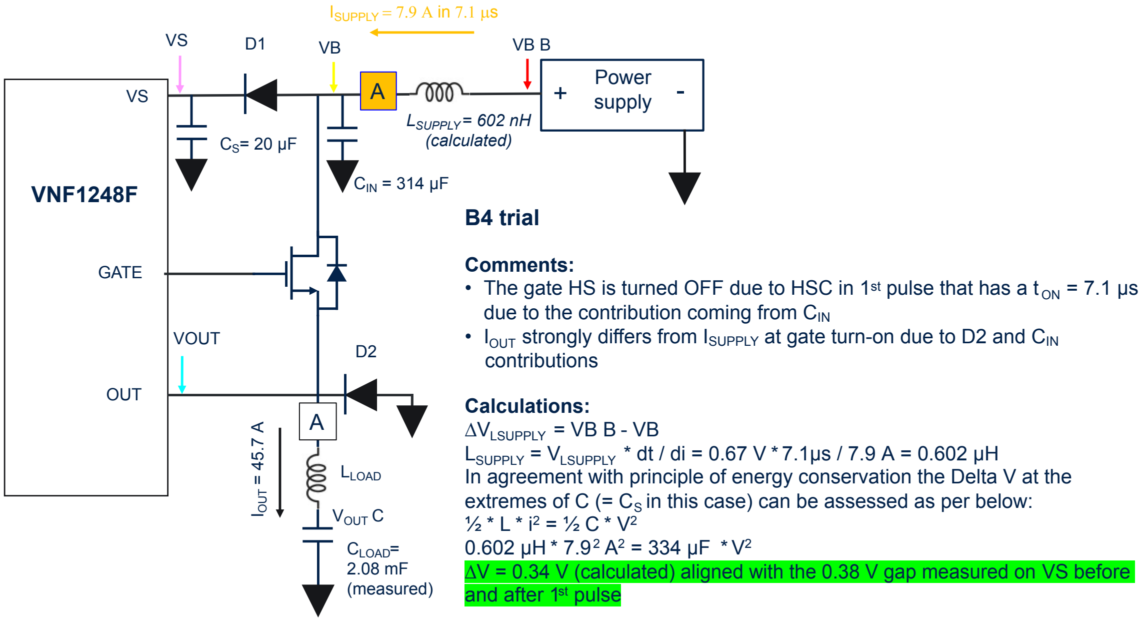
The usage of $C_{IN}$ = 314 µF generates the following results:

- $t_{CHARGE}$ = 22.7 ms
- $I_{PEAK}$ = 7.9 A
- $\Delta V_{LSUPPLY}$ = VB B – VB = 0.67 V
- HS_GATE $t_{ON}$ = 7.1 µs
- ΔV = 0.38 V

The $C_{LOAD}$ is charged in a time slightly longer than in the previous cases (20.8 ms vs 22.7 ms) due to the impact of the greater $C_{IN}$ in the standard phase (in each pulse, the supply must charge both $C_{LOAD}$ and $C_{IN}$).

The measured gap on VS is close to the estimated 0.4 V, even if the $I_{PEAK}$ resulted lower than assessed (7.9 A vs 10 A) due to the contribution of $C_{IN}$. Reusing the same model adopted for the previous cases A1, B1, B2 and B3, we estimate for $L_{SUPPLY}$ a value greater than the previously assessed one (602 μF vs 450 μF).

Of course, these little errors are consequences of the adopted simplified model, but the safe wanted gap on VS was achieved, close to expectations.



**B4 trial**

**Comments:**

- The gate HS is turned OFF due to HSC in 1st pulse that has a $t_{ON}$ = 7.1 μs due to the contribution coming from $C_{IN}$
- $I_{OUT}$ strongly differs from $I_{SUPPLY}$ at gate turn-on due to D2 and $C_{IN}$ contributions

**Calculations:**

$\Delta V_{LSUPPLY}$ = VB B - VB
$L_{SUPPLY} = V_{LSUPPLY}$ * dt / di = 0.67 V * 7.1μs / 7.9 A = 0.602 μH
In agreement with principle of energy conservation the Delta V at the extremes of C (= $C_S$ in this case) can be assessed as per below:
$½ * L * i^2 = ½ C * V^2$
$0.602\ \mu H * 7.9^2\ A^2 = 334\ \mu F * V^2$
ΔV = 0.34 V (calculated) aligned with the 0.38 V gap measured on VS before and after 1st pulse

Figure 32. **Schematic and calculation adopted in setup B4**

The need for a careful $C_{IN}$ value definition explained in this paragraph is more evident in case of the usage of greater $C_{LOAD}$ or higher VB that will involve a greater number of pulses in both phases, strongly impacting the max value achievable by VS.

Two examples are reported below using the same setup of trial A1, but differing in the following conditions:

- Trial A4: for the usage as $C_{LOAD}$ of 3.3 mF nominal capacitance (measured 3.17 mF)
- Trial A5: for the usage of VB = 20 V

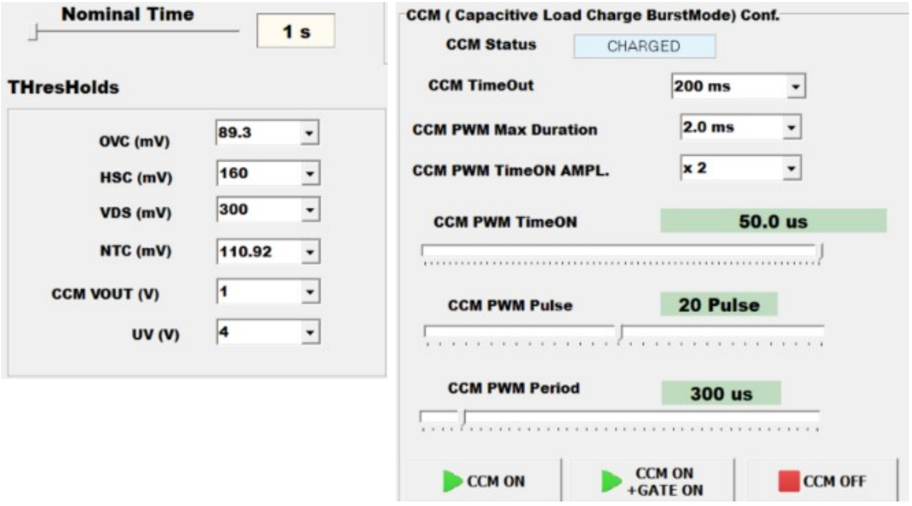
## 4.5 Trial Setup A4

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = 3.3 mF (measured 3.17 mF)**
- No $C_{IN}$ mounted, $C_S$ = 20 μF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = T_NOM$_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 33

Figure 33. **CCM configuration and result from GUI for test setup A4**



**Nominal Time** 1 s

**THresHolds**

OVC (mV) 89.3
HSC (mV) 160
VDS (mV) 300
NTC (mV) 110.92
CCM VOUT (V) 1
UV (V) 4

**CCM ( Capacitive Load Charge BurstMode) Conf.**

CCM Status CHARGED
CCM TimeOut 200 ms
CCM PWM Max Duration 2.0 ms
CCM PWM TimeON AMPL. x 2
CCM PWM TimeON 50.0 us
CCM PWM Pulse 20 Pulse
CCM PWM Period 300 us

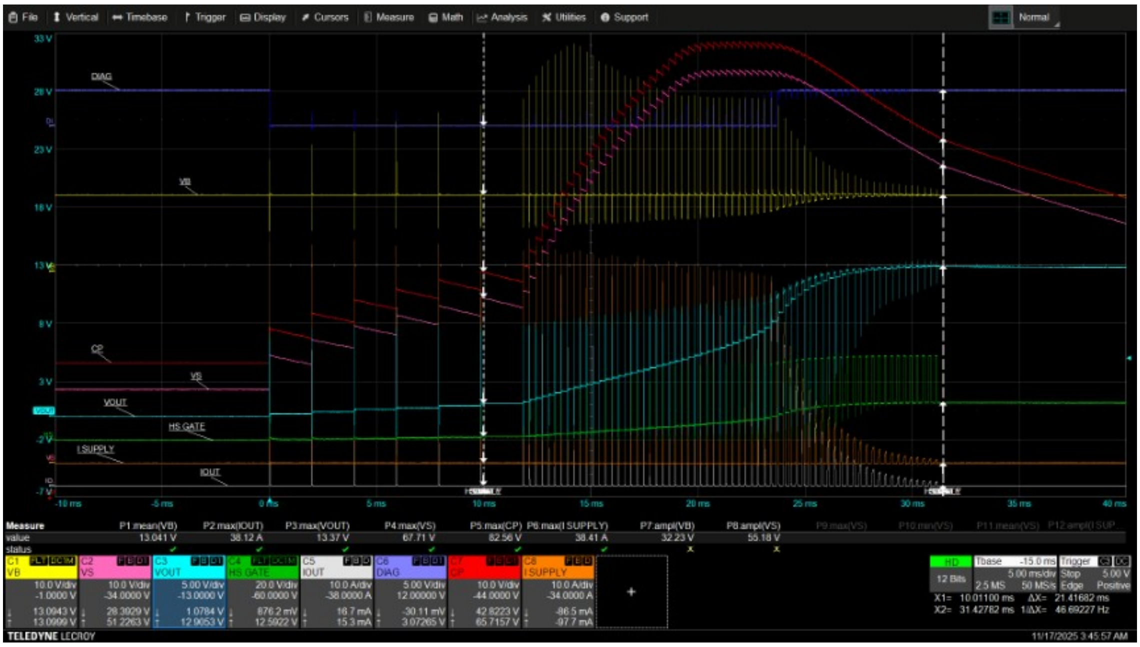
**Result A4:**

With the mentioned setup A4, the $C_{LOAD}$ is charged in 12 ms (start phase) + 19.4 ms (standard phase).

In this case, a strong boost effect is visible due to the $C_{LOAD}$ of 3.3 mF vs 2.2 mF adopted in trial A1. VS reached a maximum value of 67.7 V very close to the AMR that is not violated thanks to the contribution coming from the component Tr_d1 (SM15T68CAY).

The gap on VS after 1$^{st}$ pulse was 6.08 V.

Figure 34. Waveforms acquired during CCM with setup A4



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 13.041 V | 38.12 A | 13.37 V | 67.71 V | 82.56 V | 38.41 A | 32.23 V | 55.18 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | x | x | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 10.0 V/div | 5.00 V/div | 20.0 V/div | 10.0 A/div | 5.00 V/div | 10.0 V/div | 10.0 A/div |
| -1.0000 V | -34.0000 V | -13.0000 V | -60.0000 V | -38.0000 A | 12.00000 V | -44.0000 V | -34.0000 A |
| ↓ 13.0943 V | ↓ 28.3929 V | ↓ 1.0784 V | ↓ 876.2 mV | ↓ 16.7 mA | ↓ -30.11 mV | ↓ 42.8223 V | ↓ -86.5 mA |
| ↑ 13.0999 V | ↑ 51.2263 V | ↑ 12.9053 V | ↑ 12.5922 V | ↑ 15.3 mA | ↑ 3.07265 V | ↑ 65.7157 V | ↑ -97.7 mA |

HD 12 Bits
Tbase -15.0 ms 5.00 ms/div 2.5 MS 50 MS/s
Trigger Stop 5.00 V Edge Positive
X1= 10.01100 ms ΔX= 21.41682 ms
X2= 31.42782 ms 1/ΔX= 46.69227 Hz
11/17/2025 3:45:57 AM

Figure 35. Zoomed view of waveforms acquired at 1st pulse during CCM with setup A4

| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.870 V | 36.81 A | 8.13 V | 19.05 V | 33.55 V | 37.67 A | 12.63 V | 6.084 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | x | ✓ | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| -3.0000 V | -3.5000 V | -12.0000 V | -17.0000 V | -38.0000 A | 14.0000 V | -15.0000 V | -34.0000 A |
| ↓ 13.1334 V | ↓ 12.5977 V | ↓ 5.6 mV | ↓ -34.9 mV | ↓ 79.5 mA | ↓ 3.0336 V | ↓ 27.0536 V | ↓ 27.9 mA |
| ↑ 13.4794 V | ↑ 18.7319 V | ↑ -156.2 mV | ↑ 1.0645 V | ↑ 288.8 mA | ↑ 16.0 mV | ↑ 33.2785 V | ↑ -20.9 mA |

HD 12 Bits
Tbase -10.0 µs 10.0 µs/div 1 MS 10 GS/s
Trigger Stop 5.00 V Edge Positive
X1= -5.0497 µs ΔX= 43.9911 µs
X2= 38.9414 µs 1/ΔX= 22.73187 kHz
11/17/2025 3:49:13 AM

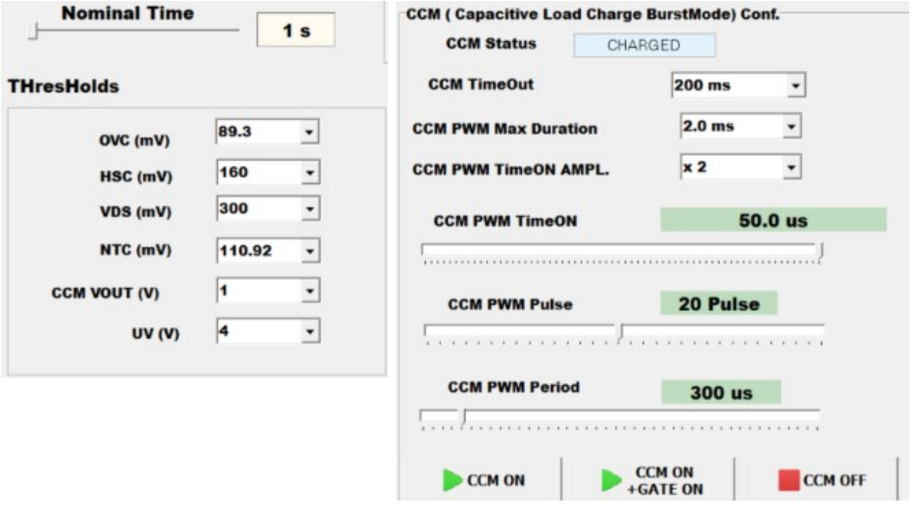
## 4.6 Trial Setup A5

- **VB = 20 V**
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = 2.2 mF (measured 2.08 mF)**
- No $C_{IN}$ mounted, $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = T_NOM$_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 36

Figure 36. **CCM configuration and result from GUI for test setup A5**



Nominal Time 1 s

THresHolds

OVC (mV) 89.3
HSC (mV) 160
VDS (mV) 300
NTC (mV) 110.92
CCM VOUT (V) 1
UV (V) 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status CHARGED
CCM TimeOut 200 ms
CCM PWM Max Duration 2.0 ms
CCM PWM TimeON AMPL. x 2
CCM PWM TimeON 50.0 us
CCM PWM Pulse 20 Pulse
CCM PWM Period 300 us

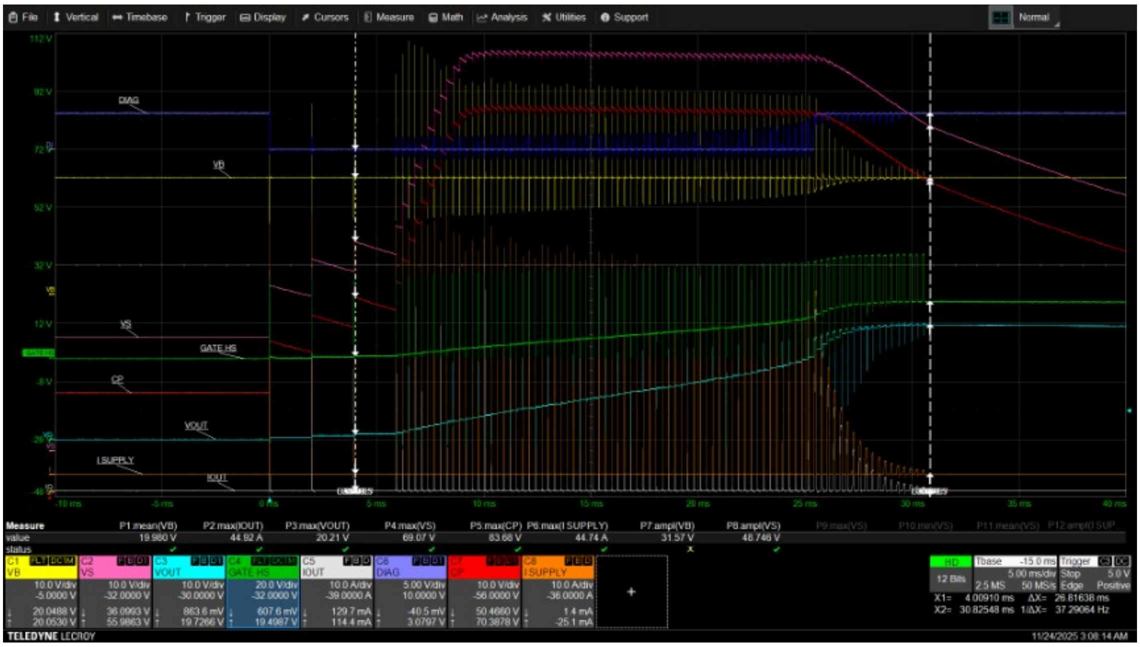
**Result A5:**

With the mentioned setup A5, the C$_{LOAD}$ is charged in 6 ms (start phase) + 24.8 ms (standard phase).

In this case, a strong boost effect is visible due to the VB set at 20 V vs 13 V adopted in trial A1. VS reached a maximum value of 69.1 V very close to the AMR that is not violated thanks to the contribution coming from the component Tr_d1 SM15T68CAY.

The gap on VS after 1$^{st}$ pulse was 9.15 V.

Figure 37. **Waveforms acquired during CCM with setup A5**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) |
|---|---|---|---|---|---|---|---|---|
| value | 19.980 V | 44.92 A | 20.21 V | 69.07 V | 83.68 V | 44.74 A | 31.57 V | 48.746 V |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ |

| C1 VB | C2 VS | C3 VOUT | C4 GATE HS | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 10.0 V/div | 10.0 V/div | 20.0 V/div | 10.0 A/div | 5.00 V/div | 10.0 V/div | 10.0 A/div |
| -5.0000 V | -32.0000 V | -30.0000 V | -32.0000 V | -39.0000 A | 10.0000 V | -56.0000 V | -36.0000 A |
| ↓ 20.0488 V | ↓ 36.0093 V | ↓ 863.6 mV | ↓ 607.6 mV | ↓ 129.7 mA | ↓ -40.5 mV | ↓ 50.4680 V | ↓ 1.4 mA |
| ↑ 20.0530 V | ↑ 55.9863 V | ↑ 19.7266 V | ↑ 19.4987 V | ↑ 114.4 mA | ↑ 3.0797 V | ↑ 70.3878 V | ↑ -25.1 mA |

HD 12 Bits
Tbase -15.0 ms
5.00 ms/div
2.5 MS 50 MS/s
Trigger
Stop 5.0 V
Edge Positive
X1= 4.00910 ms ΔX= 26.81638 ms
X2= 30.82548 ms 1/ΔX= 37.29064 Hz
11/24/2025 3:08:14 AM

Figure 38. **Zoomed view of waveforms acquired at 1st pulse during CCM with setup A5**

| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(VB B) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) |
|---|---|---|---|---|---|---|---|---|
| value | 19.838 V | 45.26 A | 12.93 V | 29.38 V | 25.83 V | 46.08 A | 17.20 V | 9.147 V |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ |

| C1 VB | C2 VS | C3 VOUT | C4 GATE HS | C5 IOUT | C6 DIAG | C7 VB B | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 10.0 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 10.0 V/div | 10.0 A/div |
| 0.0 mV offset | 0.0 mV offset | -20.0000 V | -20.0500 V | -35.0000 A | 16.0000 V | 0.0 mV offset | -35.0000 A |
| ↓ 12.2028 V | ↓ 19.8703 V | ↓ 11.1579 V | ↓ 17.3354 V | ↓ 44.6791 A | ↓ 190.4 mV | ↓ 14.2090 V | ↓ 45.4855 A |
| ↑ 12.2070 V | ↑ 19.9372 V | ↑ 11.4607 V | ↑ 27.7302 V | ↑ 27.5042 A | ↑ 3.1717 V | ↑ 14.3973 V | ↑ 27.9889 A |

HD 12 Bits
Tbase -10.0 µs
10.0 µs/div
1 MS 10 GS/s
Trigger
Stop 5.0 V
Edge Positive
X1= 7.5188 µs ΔX= -3.3625 µs
X2= 4.1563 µs 1/ΔX= -297.398 kHz
11/24/2025 3:18:18 AM

Based on this analysis, we recommend the end user to perform a careful assessment of the setup conditions including VB, $C_{LOAD}$, $L_{SUPPLY}$, and $C_{IN}$ to perform CCM activities in safe conditions.

In this document, we continued the CCM tests by always adopting $C_{IN}$ = 314 μF to verify the impact of various parameters including verifications with VB set at 24 V and 48 V and using greater $C_{LOAD}$ of 4.7 mF and 6.9 mF.

As visible in the results reported in the next chapter, the adoption of this $C_{IN}$ always ensures a safe condition for the VNF1248F. In fact, in all cases a VS max well below the AMR was observed.

# 5 CCM application measurements tuning various parameters

This chapter shows several CCM measurements carried out on the EV-VNF1248F easy board, modifying one or more variables listed in Section 2.1.

The overall effects of each parameter are summarized in Table 5.

Table 5. **CCM relevant fields**

| Parameter | Description | Comment | Reference trials |
|---|---|---|---|
| **VB** | Battery supply voltage of the entire application circuit (range from 6 to 60 V) | It affects the duration of the charge because the greater the VB is, the greater the VOUT value that must to be achieved.<br>Fixing all parameters, **higher value of VB involves longer charging time** | B5 vs C vs D and E vs F vs G |
| **$V_{OUT}$ threshold** | OUT pin voltage to be reached during the first charging phase at low frequency in ton protection (range from 1 to 5 V) | Due to the low frequency of the start charging phase, the higher the CCM_VOUT_THR, the longer the duration of the 1st phase in case of a high PWM pulse number setting.<br>Fixing all parameters **a greater CCM_VOUT_THR involves a longer time to charge** | C vs F |
| **PWM start period** | Period used in the first charging phase at low frequency in ton protection (range from 2 to 4 ms) | Fixing all parameters **a greater CCM_PWM_SC_T duration involves a longer time to charge** | C vs G |
| **PWM period** | It refers to the period of standard charging phase (range from 0.2 to 4 ms) | Fixing all parameters, **the higher the CCM_PWM_T, the longer the charging time** because it reduces the GATE turn ON frequency | E vs H |
| **PWM $t_{ON}$ multiplying factor** | It is an amplifier of the PWM Time ON duration in the standard charging phase (range from 1 to 8 x) | Fixing all parameters, **the higher CM_PWM_TON_MF, the shorter the charging time** because it increases the duty cycle and GATE turn ON duration | K vs L |
| **PWM $t_{ON}$ time** | It defines the CCM PWM time ON duration in standard charging phase in combination with PWM ton multiplying factor (range from 1 to 50 µs in case of multiplying factor=1x arriving at 400us in case of multiplying factor = 8x or ton protection) | Fixing all parameters, **the higher the CM_PWM_TON, the shorter the charging time**. Once $t_{ON}$ protection is selected, the high-side driver is controlled by protection only (hard short, fuse latch) so that this configuration assures the maximum ton value limited only by i2t algorithm | E vs K vs L vs M |
| **OVC** | Nominal overcurrent threshold for the eFuse emulation (VOVC_THRS range from 6 to 89.3 mv) | It affects the duration of the charge only in the portion of the standard charging phase in which hard short (HSC) is not triggered.<br>Fixing all parameters, **the higher this value, the lower the charging time** | E vs O vs Q vs R |
| **HSC** | It configures the Delta V reading at extremes of $R_{SHUNT}$ triggering the hard short protection threshold (VHSC_THRS, range from 20 mV to 160 mV) | It affects the duration of the charge because it has a direct impact on the amplitude in current of each pulse triggered by the HSC protection (start phase) and i2t or fuse protection (standard phase).<br>Fixing all parameters, **the higher the HSC threshold, the lower the charging time** | E vs P vs Q vs R |
| **$R_{SHUNT}$** | high precision sense resistance connected between sense P and sense N | It affects the duration of the charge because it has a direct impact on the current sense voltage drop at its extremes influencing HSC and OVC currents. **Greater $R_{SHUNT}$ involves longer charging time**. | E vs W |

| Parameter | Description | Comment | Reference trials |
|---|---|---|---|
| **Ambient temperature** | Operative temperature of the device | **The Tj of VNF1248 device has a negligible impact on charging time.**<br>The heating of the entire circuit also affects MOSFET, which has very little effect on reducing the charging time. | U vs W |
| **TNOM** | Value of nominal time required for the fuse emulation. | **It has a little effect** in time to charge affects the duration of standard charging phase where i2t protection is triggered after a longer time, assuring a longer HS_GATE time ON. **The greater tnom is, the shorter the charging time** | X1 vs X2 |
| **PWM start pulses max number** | It refers to the max number of attempts allowed in start charging phase at low frequency to achieve the set CCM VOUT (CCM_PWM_SC_T_NB range from 5 to 50 pulses) | Higher value is suggested in case of a higher CCM_VOUT_THR value to avoid CHARGE INCOMPLETE due to CCM_VOUT_THR not achieved or short circuit on OUT | H vs H-bis and Y |
| **CCM timeout** | Maximum time allowed to start + standard charging phases (CCM_TIMEOUT range from 200 to 400 ms) independently of the successful charge of the cload | Higher values are suggested in case of a higher VB, $R_{SHUNT}$, CCM_VOUT_THR, the longer the CCM_PWM_SC_T duration, the greater capacitance and lower values of CCM PWM duty cycle in start phase and standard phase, OVC, HSC | J vs J-bis |

The overall collected results are summarized in Table 6.

Table 6. **Summary of all performed trials**

| Trial | VB | VOUT (V) | PWM start period (ms) | PWM Period (us) | PWM Time ON (us) | PWM Time ON Ampl. | OVC (mV) | HSC (mV) | TNOM (s) | TJ (°C) | $R_{SHUNT}$ (mΩ) | $C_{LOAD}$[1] (mF) Measured - nominal | MAX Vs (V) | Number of pulses in start phase – duration in ms | Duration of charging phase (ms) | Time to charge (ms) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B4 | 13 | 1 | 2 | 300 | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | **2.08 - 2.2** | 13.7 | 4 – 8 | 14.7 | 22.7 |
| B5 | 13 | 1 | 2 | **50** | **3** | **1** | 89.3 | 160 | 1 | 35 | 5 | **2.08 - 2.2** | 13.7 | 13 - 26 | 169 | 195 |
| B6 | 13 | 1 | 2 | 300 | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | **3.17 - 3.3** | 13.9 | 5 -10 | 22.3 | 32.3 |
| C | **24** | 1 | 2 | 300 | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | **3.17 - 3.3** | 26.7 | 3 – 6 | 53.6 | 59.6 |
| D | **48** | 1 | 2 | 300 | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | **3.17 - 3.3** | 52.2 | 2 – 4 | 131 | 135 |
| *E1*[2] | *13* | *1* | *2* | *300* | *50* | *2* | *89.3* | *160* | *1* | *35* | *5* | *4.52 – 4.7* | *13.8* | *7 - 14* | *30* | *44.0* |
| F | **24** | 1 | 2 | 300 | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 27 | 4 -8 | 77.7 | 85.7 |
| G | **48** | 1 | 2 | 300 | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 52.2 | 2 -4 | 220.6 | 224.6 |
| H | 13 | **5** | 2 | 300 | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 13.3 | 48 – 95 | 18.4 | 113 |
| I | 13 | 1 | **4** | 300 | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 13.7 | 7 -28 | 31.8 | 57.8 |
| J | 13 | 1 | 2 | **3000** | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 13.0 | 7 -14 | 321.6 | 335.6 |
| K | 13 | 1 | 2 | 300 | **10** | 2 | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 13.7 | 7 -14 | 111.8 | 125.8 |
| L | 13 | 1 | 2 | 300 | **30** | **8** | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 13.7 | 6 -12 | 24.3 | 36.3 |
| M | 13 | 1 | 2 | 300 | **Ton Prot** | 2 | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 13.7 | 6 -12 | 21.6 | 33.6 |
| N | 13 | 1 | 2 | **50** | **Ton Prot** | 2 | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 16.1 | 7 – 14 | 3.9 | 17.9 |
| O | 13 | 1 | 2 | 300 | 50 | 2 | **6** | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 13.8 | 7 -14 | 39.8 | 53.8 |
| P | 13 | 1 | 2 | 300 | 50 | 2 | 89.3 | **80** | 1 | 35 | 5 | 4.52 – 4.7 | 13.0 | 14 -28 | 87.2 | 115.1 |
| Q1 | 13 | 1 | 2 | 300 | 50 | 2 | **6** | **20** | 1 | 35 | 5 | 4.52 – 4.7 | 12.8 | 26 – 52 | 348 | incomplete |
| Q2 | 13 | 1 | 2 | 300 | 50 | 2 | **44.5** | **60.6** | 1 | 35 | 5 | 4.52 – 4.7 | 13.0 | 16 -32 | 127 | 159 |
| R1 | **48** | 1 | 2 | 300 | 50 | 2 | **44.5** | **60.6** | 1 | 35 | 5 | 4.52 – 4.7 | 51.7 | 1-2 | 398 | incomplete |

| Trial | VB | VOUT (V) | PWM start period (ms) | PWM Period (us) | PWM Time ON (us) | PWM Time ON Ampl. | OVC (mV) | HSC (mV) | TNOM (s) | TJ (°C) | $R_{SHUNT}$ (mΩ) | $C_{LOAD}$[1] (mF) Measured - nominal | MAX Vs (V) | Number of pulses in start phase – duration in ms | Duration of charging phase (ms) | Time to charge (ms) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R2 | **48** | 1 | 2 | 300 | 50 | 2 | **69.5** | **91.9** | 1 | 35 | 5 | 4.52 – 4.7 | 51.9 | 3 -6 | 359 | 365 |
| S | 13 | 1 | 2 | 300 | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | **6.69 – 6.9** | 14.1 | 9 -18 | 45.5 | 63.5 |
| T | 13 | 1 | 2 | 300 | **Ton Prot** | 2 | 89.3 | 160 | 1 | 35 | 5 | **6.69 – 6.9** | 14.1 | 8 -16 | 33.4 | 49.4 |
| U | 13 | **3** | 2 | 300 | 50 | 2 | 89.3 | **91.9** | 1 | 35 | 5 | 4.52 – 4.7 | 13.2 | 12 -24 | 70.1 | 94.1 |
| V | 13 | **3** | 2 | 300 | 50 | 2 | 89.3 | **91.9** | 1 | **100** | 5 | 4.52 – 4.7 | 13.4 | 10 -20 | 70 | 90 |
| W | 13 | 1 | 2 | 300 | 50 | 2 | 89.3 | 160 | 1 | 35 | **20** | 4.52 – 4.7 | 12.9 | 17 -34 | 219.5 | 253.5 |
| X1 | 13 | 1 | 2 | **500** | 50 | **8** | **10.4** | **80** | 1 | 35 | 5 | 4.52 – 4.7 | 13.0 | 12 -24 | 144.4 | 168.4 |
| Y2 | 13 | 1 | 2 | **500** | 50 | **8** | **10.4** | **80** | **511** | 35 | 5 | 4.52 – 4.7 | 13.0 | 12 -24 | 135.1 | 159.1 |
| Y | 13 | 1 | 2 | 300 | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | **Short circuit** | 13.1 | 20 - 40 | NA | incomplete |
| Z1 | 13 | **4** | 2 | **1000** | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 13.0 | 37 - 74 | 41.4 | 115.4 |
| Z2 [3] | 13 | **4** | 2 | **1000** | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 13.0 | 38 - 76 | 44.4 | 120.4 |
| Z3 | 13 | **4** | 2 | **1000** | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 13.0 | NA | NA | **Stopped after 46.8 ms** |
| Z4 [3] | 13 | **4** | 2 | **1000** | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 13.0 | 37 - 74 | NA | **Stopped after 85.6 ms** |
| E2 [4] | 13 | 1 | 2 | 300 | 50 | 2 | 89.3 | 160 | 1 | 35 | 5 | 4.52 – 4.7 | 13.8 | 7 - 14 | 31 | 45 |

1. *$C_{LOAD}$ is connected to OUT through 1 m wire*
2. *Trial-Setup E1 was verified with device both in Unlocked and Fail-safe states*
3. *Z2 and Z4 trials were performed with DUT in Fail-safe state while all other trials were verified with DUT in Unlocked state*
4. *E2 is the only trial performed in Unlocked state sending CCM ON + HS_GATE ON*

Note: *The values modified with respect to the reference setup adopted in Trial E1 are shown in bold (reference values are in italic)*

Note: *314 µF (3 x 100 uF – 100 V) is connected as $C_{IN}$ on VB vs GND connectors of the evaluation board*

## 5.1 Effect of CCM_PWM_TON before hard short protection triggering

### 5.1.1 Trial Setup B5

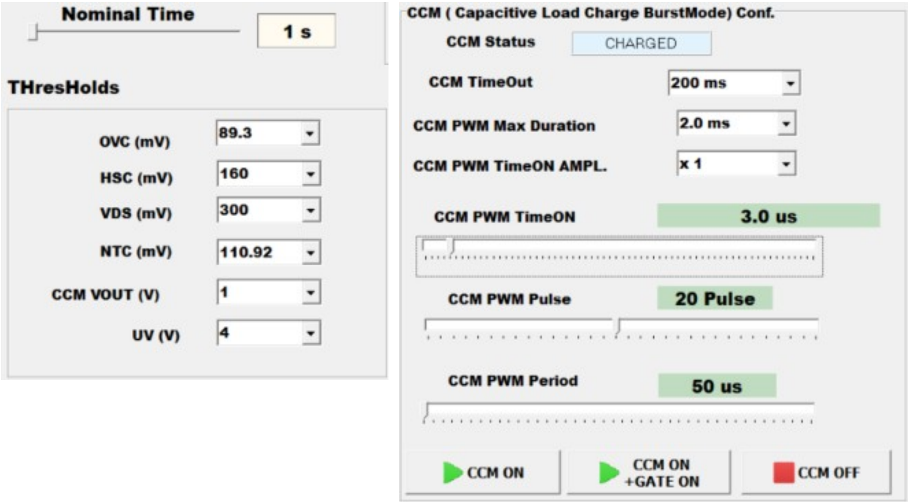
It adopts the same setup as trial B4 modifying the CCM_PWM_TON at 3 µs vs 100 µs and CCM_PWM_T at 50 µs vs 300 µs to highlight the possibility of interrupting the pulse before the hard short protection triggering.

- **VB = 13 V**
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = 2.2 mF (measured 2.08 mF)**
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = T_NOM$_{MIN}$ → 1 s
- **CCM_PWM_TON = 3 µs**
- **CCM_PWM_TON_MF = 1 x**
- CCM_PWM_SC_T_NB = 20 pulses
- **CCM_PWM_T = 50 µs**
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 39

Figure 39. **CCM configuration and result from GUI for test setup B5**



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

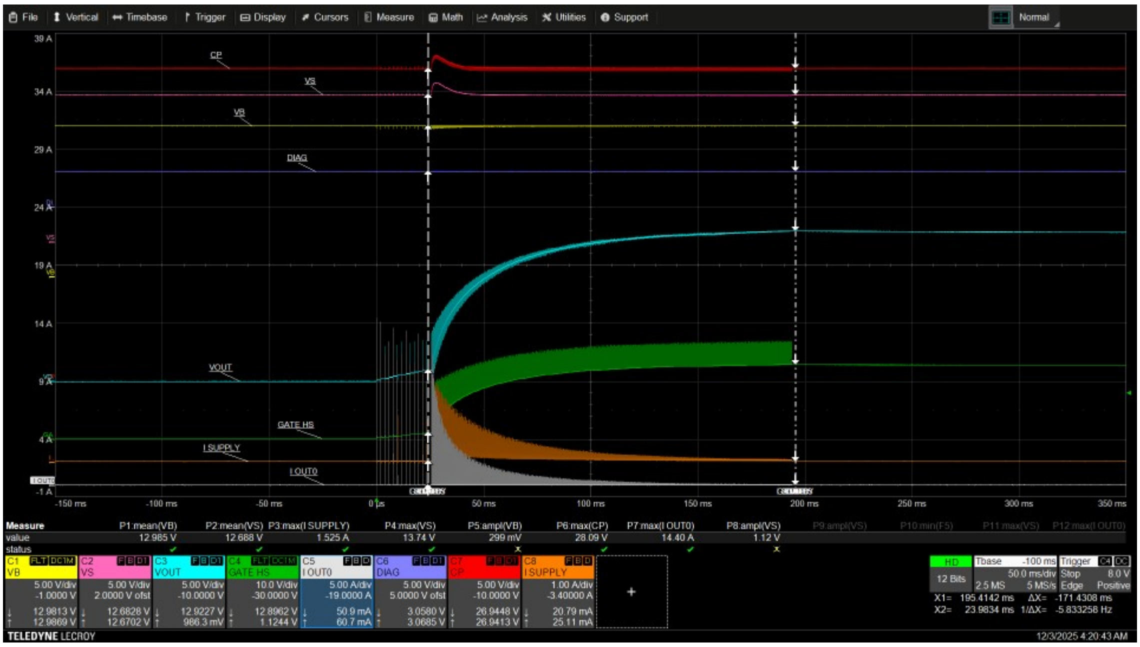
CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 1
CCM PWM TimeON: 3.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 50 us

**Result B5:**

With setup B5, the C$_{LOAD}$ is charged in 26 ms (start phase) + 169 ms (standard phase).

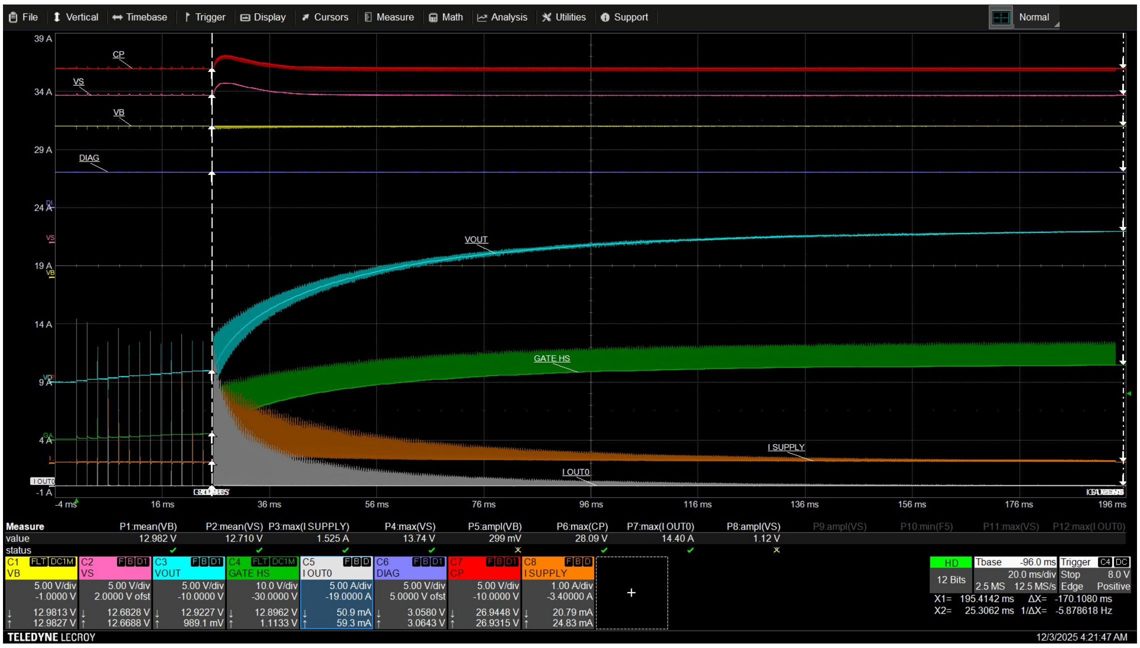
The CIN strongly limits the boost effect so that VS max = 13.7 V.

The reduction of CCM_PWM_TON at 3 µs has a strong impact on the t$_{CHARGE}$ because it interrupts each gate HS pulse (both in start and standard phase) before the triggering of I$^2$t protection so that the DIAG signal remains high along the charge of the C$_{LOAD}$.



| Measure | P1:mean(VB) | P2:mean(VS) | P3:max(I SUPPLY) | P4:max(VS) | P5:ampl(VB) | P6:max(CP) | P7:max(I OUT0) | P8:ampl(VS) | P9:ampl(VS) | P10:min(F5) | P11:max(VS) | P12:max(I OUT0) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.985 V | 12.688 V | 1.525 A | 13.74 V | 299 mV | 28.09 V | 14.40 A | 1.12 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ | ✓ | ✗ | | | | |

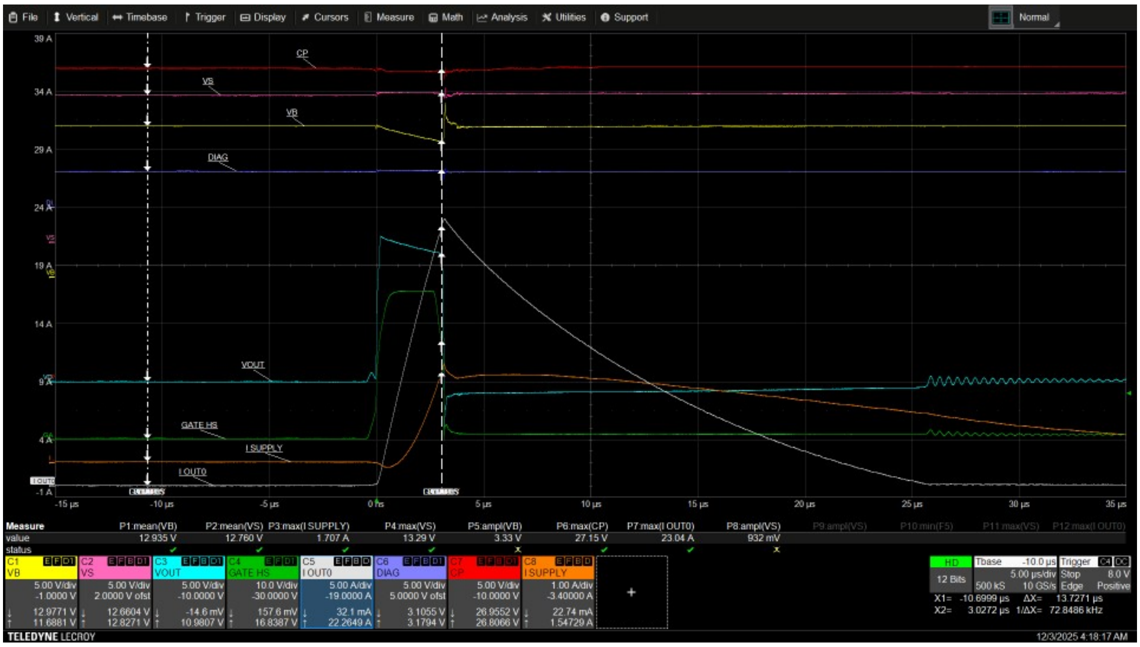
Figure 40. Waveforms acquired during CCM with setup B5



| Measure | P1:mean(VB) | P2:mean(VS) | P3:max(I SUPPLY) | P4:max(VS) | P5:ampl(VB) | P6:max(CP) | P7:max(I OUT0) | P8:ampl(VS) | P9:ampl(VS) | P10:min(F5) | P11:max(VS) | P12:max(I OUT0) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.982 V | 12.710 V | 1.525 A | 13.74 V | 299 mV | 28.09 V | 14.40 A | 1.12 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ | ✓ | ✗ | | | | |

Figure 41. Zoomed view of waveforms acquired during CCM with setup B5

Figure 42. Zoomed view of waveforms acquired at 1st pulse during CCM with setup B5 (TON is 3 µs and TOFF is ~1997 µs)



| Measure | P1:mean(VB) | P2:mean(VS) | P3:max(I SUPPLY) | P4:max(VS) | P5:ampl(VB) | P6:max(CP) | P7:max(I OUT0) | P8:ampl(VS) | P9:ampl(VS) | P10:min(F5) | P11:max(VS) | P12:max(I OUT0) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.935 V | 12.760 V | 1.707 A | 13.29 V | 3.33 V | 27.15 V | 23.04 A | 932 mV | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ | ✓ | ✗ | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 GATE HS | C5 I OUT0 | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| E F D1 | E F B D1 | E F B D1 | E F D1 | E F B D | E F B D1 | E F B D1 | E F B D |
| 5.00 V/div | 5.00 V/div | 5.00 V/div | 10.0 V/div | 5.00 A/div | 5.00 V/div | 5.00 V/div | 1.00 A/div |
| -1.0000 V | 2.0000 V ofst | -10.0000 V | -30.0000 V | -19.0000 A | 5.0000 V ofst | -10.0000 V | -3.40000 A |
| ↓ 12.9771 V | ↓ 12.6604 V | ↓ -14.6 mV | ↓ 157.6 mV | ↓ 32.1 mA | ↓ 3.1055 V | ↓ 26.9552 V | ↓ 22.74 mA |
| ↑ 11.6881 V | ↑ 12.8271 V | ↑ 10.9807 V | ↑ 16.8387 V | ↑ 22.2649 A | ↑ 3.1794 V | ↑ 26.8066 V | ↑ 1.54729 A |

| HD | Tbase -10.0 µs | Trigger C4 DC |
|---|---|---|
| 12 Bits | 5.00 µs/div | Stop 8.0 V |
| | 500 kS 10 GS/s | Edge Positive |

X1= -10.6999 µs ΔX= 13.7271 µs
X2= 3.0272 µs 1/ΔX= 72.8486 kHz

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Figure 43. Zoomed view of waveforms acquired on first 2 pulses during CCM with setup B5 showing a period of 2 ms

| Measure | P1:mean(VB) | P2:mean(VS) | P3:max(I SUPPLY) | P4:max(VS) | P5:ampl(VB) | P6:max(CP) | P7:max(I OUT0) | P8:ampl(VS) | P9:ampl(VS) | P10:min(F5) | P11:max(VS) | P12:max(I OUT0) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.988 V | 12.665 V | 1.829 A | 12.87 V | 2.51 V | 27.17 V | 24.00 A | 315 mV | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ | ✓ | ✗ | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 GATE HS | C5 I OUT0 | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| FLT DC1M | F B D1 | F B D1 | FLT DC1M | F B D | F B D1 | F B D1 | F B D |
| 5.00 V/div | 5.00 V/div | 5.00 V/div | 10.0 V/div | 5.00 A/div | 5.00 V/div | 5.00 V/div | 500 mA/div |
| -1.0000 V | 2.0000 V ofst | -10.0000 V | -30.0000 V | -18.1500 A | 5.0000 V ofst | -10.0000 V | -1.70000 A |
| ↓ 12.9946 V | ↓ 12.6521 V | ↓ 185.5 mV | ↓ 457.6 mV | ↓ 69.8 mA | ↓ 3.0434 V | ↓ 26.9245 V | ↓ 6.42 mA |
| ↑ 12.9897 V | ↑ 12.6737 V | ↑ 97.7 mV | ↑ 378.1 mV | ↑ 67.7 mA | ↑ 3.0699 V | ↑ 26.9273 V | ↑ 5.37 mA |

| HD | Tbase -1.00 ms | Trigger C4 DC |
|---|---|---|
| 12 Bits | 500 µs/div | Stop 8.0 V |
| | 2.5 MS 500 MS/s | Edge Positive |

X1= 2.372658 ms ΔX= -1.769574 ms
X2= 603.084 µs 1/ΔX= -565.1078 Hz

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Figure 44. Zoomed view of waveforms acquired at last 3 pulses during CCM with setup B5 (PWM period is 50 µs with TON = 3 µs and TOFF = 47 µs)

| Measure | P1:mean(VB) | P2:mean(VS) | P3:max(I SUPPLY) | P4:max(VS) | P5:ampl(VB) | P6:max(CP) | P7:max(I OUT0) | P8:ampl(VS) | P9:ampl(VS) | P10:min(F5) | P11:max(VS) | P12:max(I OUT0) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.993 V | 12.646 V | 44 mA | 12.68 V | 52 mV | 27.00 V | 266 mA | 87 mV | | | | |
| status | ✓ | ✓ | ✓ | ✓ | x | ✓ | ✓ | x | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 GATE HS | C5 I OUT0 | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 5.00 V/div | 10.0 V/div | 1.00 A/div | 5.00 V/div | 5.00 V/div | 500 mA/div |
| -1.0000 V | 2.0000 V ofst | -10.0000 V | -30.0000 V | -3.80000 A | 5.0000 V ofst | -10.0000 V | -1.70000 A |
| ↓ 13.0029 V | ↓ 12.6374 V | ↓ 13.3573 V | ↓ 14.2425 V | ↓ 31.67 mA | ↓ 3.0706 V | ↓ 26.9468 V | ↓ 5.16 mA |
| ↑ 13.0071 V | ↑ 12.6737 V | ↑ 13.4494 V | ↑ 14.9163 V | ↑ 50.08 mA | ↑ 3.0699 V | ↑ 26.9148 V | ↑ 3.28 mA |

HD 12 Bits
Tb -192.0356 ms 20.0 µs/div 2 MS 10 GS/s
Trigger C4 DC Stop 8.0 V Edge Positive
X1= 191.955222 ms ΔX= 50.612 µs
X2= 192.005834 ms 1/ΔX= 19.7582 kHz

## 5.2 Effect of CLOAD (3.3 mF vs 4.7 mF) and VB (13 V vs 24 V vs 48 V) on CCM

### 5.2.1 Trial Setup B6

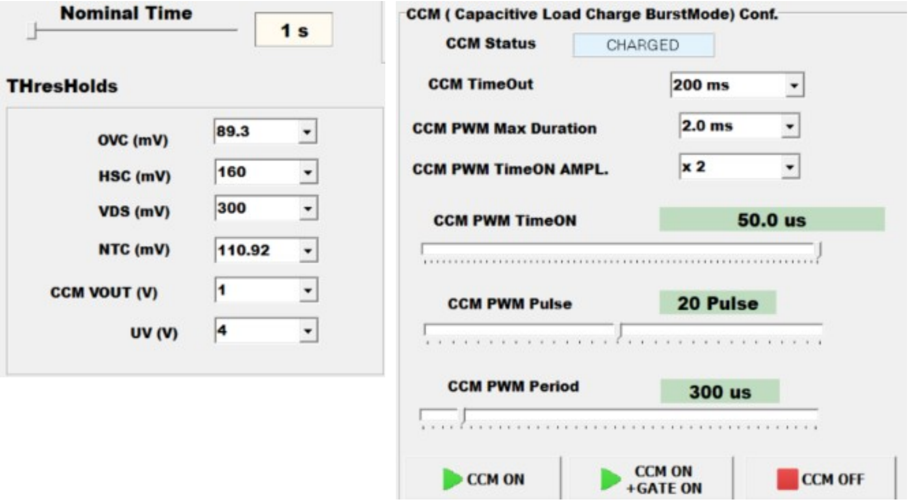
It adopts the same setup as trial B4 with $C_{LOAD}$ increased at 3.3 mF.

- **VB = 13 V**
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = 3.3 mF (measured 3.17 mF)**
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 45

Figure 45. **CCM configuration and result from GUI for test setup B6**



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

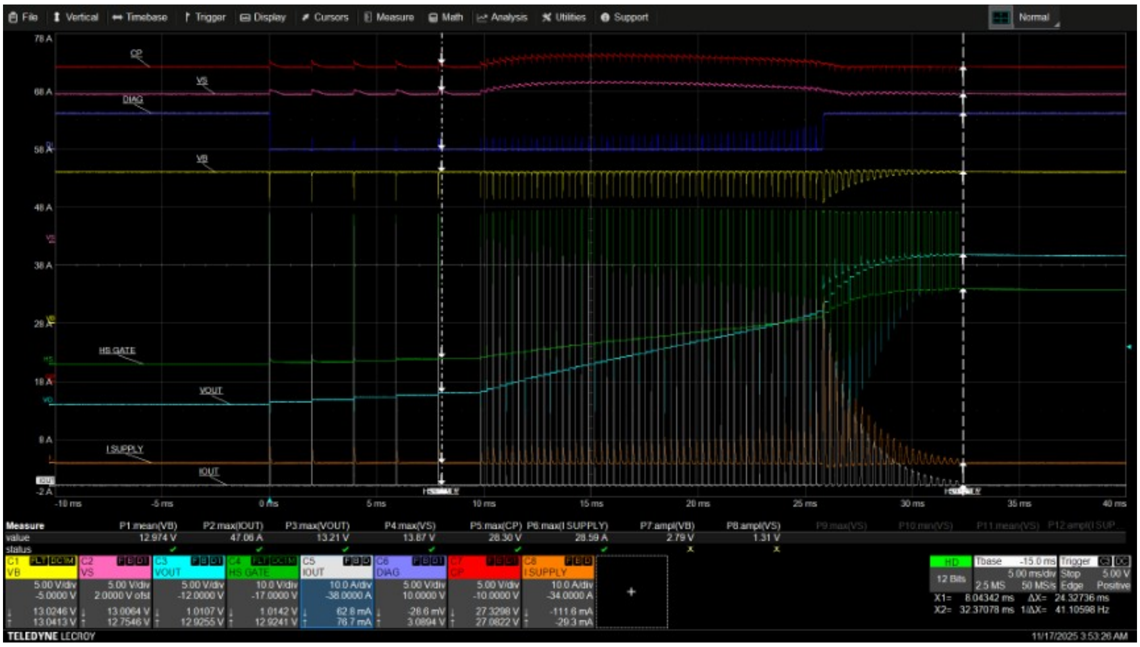
**Result B6:**

With setup B6, the $C_{LOAD}$ is charged in 10 ms (start phase) + 22.3 ms (standard phase).

The $C_{IN}$ strongly limits the boost effect so that VS max = 13.9 V, and it helps the start phase, which requires only five pulses vs the six observed without $C_{IN}$ in trial A4. The $C_{IN}$ allows higher current peaks to be achieved in the start phase; in fact, on the 1st pulse we reach 45.5 A on setup B6 vs 36.8 A on setup A4, helping to reach the set CCM_VOUT_THR with five instead of six pulses.

The overall $t_{CHARGE}$ of trial B6 is slightly longer than A4 due to the impact of $C_{IN}$ in the portion of standard phase limited by $I^2t$ fuse protection. The duration of standard phase is 22.3 ms with setup B6 vs 19.4 ms with setup A4, because a greater achieved current leads to faster $I^2t$ protection triggering. As a consequence, HS_GATE stays on for shorter timing, increasing the duration of the standard charging phase.

Figure 46. **Waveforms acquired during CCM with setup B6**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) |
|---|---|---|---|---|---|---|---|---|
| value | 12.974 V | 47.06 A | 13.21 V | 13.87 V | 28.30 V | 28.59 A | 2.79 V | 1.31 V |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | X | X |

Figure 47. Zoomed view of waveforms acquired at 1st pulse during CCM with setup B6

| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) |
|---|---|---|---|---|---|---|---|---|
| value | 12.852 V | 45.52 A | 12.42 V | 13.44 V | 27.49 V | 7.93 A | 4.42 V | 357 mV |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ⌅ | ✓ |

## 5.2.2 Trial Setup C

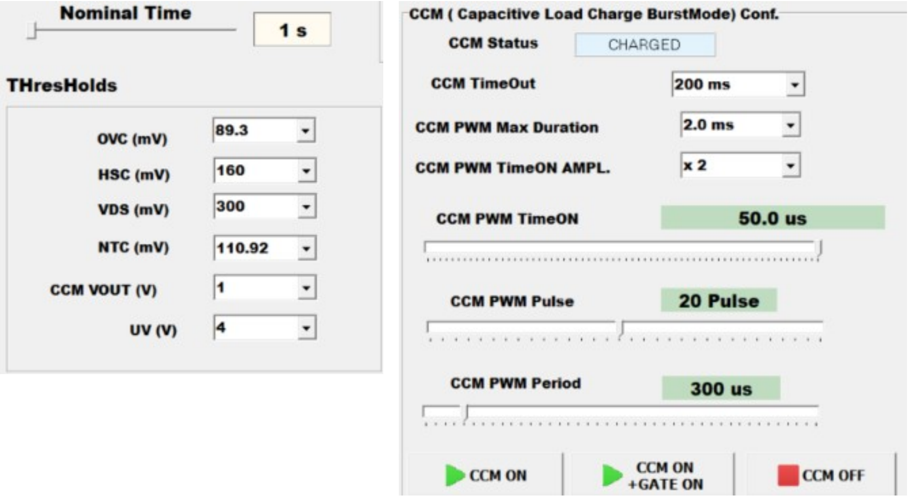
It adopts the same setup as trial B6 with VB increased at 24 V vs 13 V.

- **VB = 24 V**
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = 3.3 mF (measured 3.17 mF)**
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 48

Figure 48. **CCM configuration and result from GUI for test setup C**



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

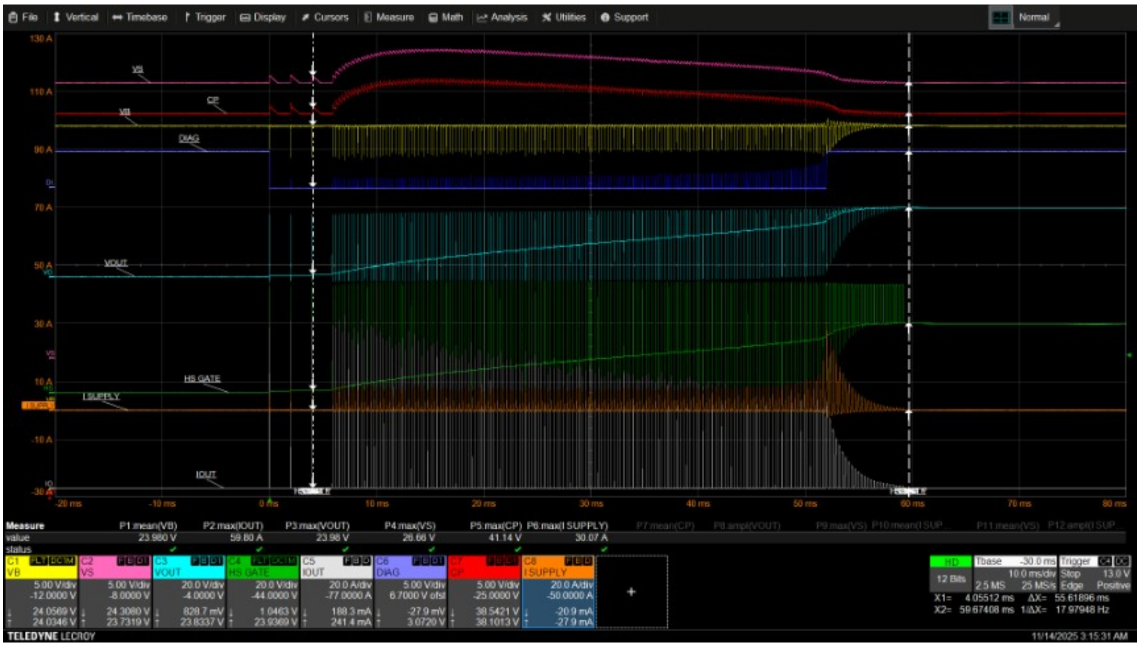
CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

**Result C:**

With setup C, the $C_{LOAD}$ is charged in 6 ms (start phase) + 53.6 ms (standard phase).

A higher VB involves a higher VOUT to be achieved by increasing the $t_{CHARGE}$ vs the adoption of a lower VB.

Figure 49. **Waveforms acquired during CCM with setup C**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:mean(CP) | P8:ampl(VOUT) | P9:max(VS) | P10:mean(I SUP... | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 23.980 V | 59.80 A | 23.98 V | 26.66 V | 41.14 V | 30.07 A | | | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 20.0 V/div | 20.0 V/div | 20.0 A/div | 5.00 V/div | 5.00 V/div | 20.0 A/div |
| -12.0000 V | -8.0000 V | -4.0000 V | -44.0000 V | -77.0000 A | 6.7000 V ofst | -25.0000 V | -50.0000 A |
| ↓ 24.0569 V | ↓ 24.3080 V | ↓ 828.7 mV | ↓ 1.0463 V | ↓ 188.3 mA | ↓ -27.9 mV | ↓ 38.5421 V | ↓ -20.9 mA |
| ↑ 24.0346 V | ↑ 23.7319 V | ↑ 23.8337 V | ↑ 23.9369 V | ↑ 241.4 mA | ↑ 3.0720 V | ↑ 38.1013 V | ↑ -27.9 mA |

HD 12 Bits
Tbase -30.0 ms 10.0 ms/div 2.5 MS 25 MS/s
Trigger C4 DC Stop 13.0 V Edge Positive
X1= 4.05512 ms ΔX= 55.61896 ms
X2= 59.67408 ms 1/ΔX= 17.97948 Hz

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## 5.2.3 Trial Setup D

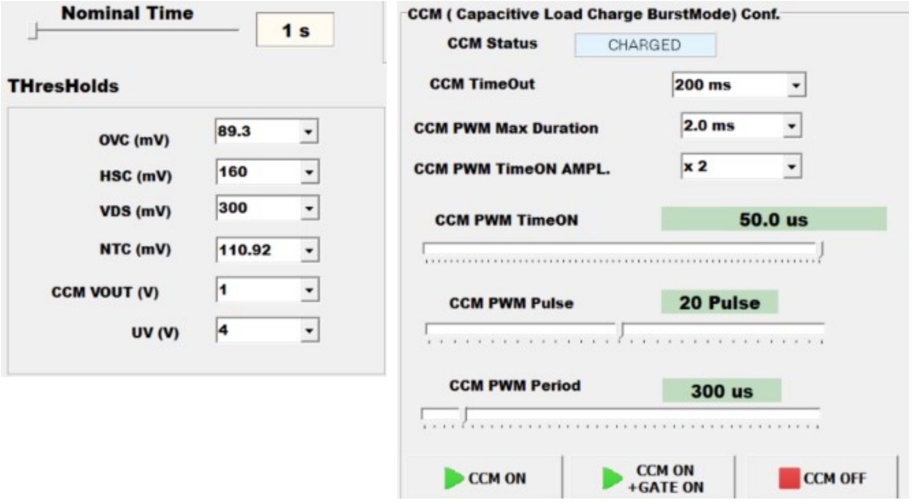
It adopts the same setup as trials B6 with VB increased at 48 V vs 13 V.

- **VB = 48 V**
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = 3.3 mF (measured 3.17 mF)**
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = T_NOM$_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 50

**Figure 50.** **CCM configuration and result from GUI for test setup D**



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

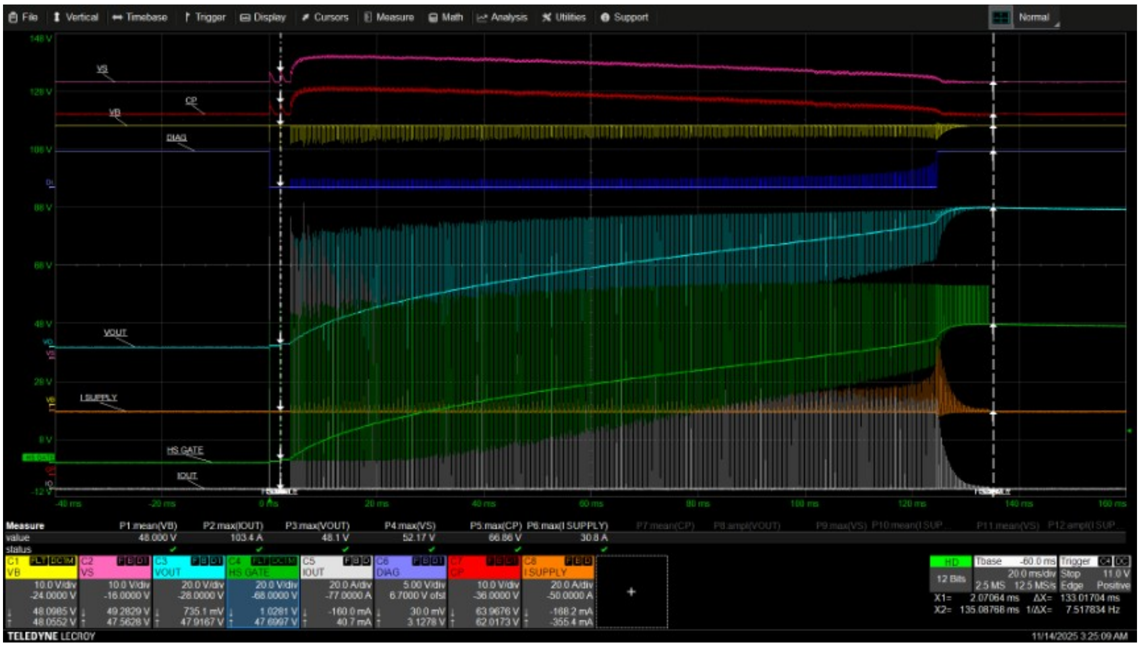
CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

**Result D:**

With setup D, the $C_{LOAD}$ is charged in 4 ms (start phase) + 131 ms (standard phase).

Thanks to $C_{IN}$, the max value achieved by VS is 52.2 V and the gap of VS after $1^{st}$ pulse is 1.79 V.

Figure 51. **Waveforms acquired during CCM with setup D**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:mean(CP) | P8:ampl(VOUT) | P9:max(VS) | P10:mean(I SUP... | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 48.000 V | 103.4 A | 48.1 V | 52.17 V | 66.86 V | 30.8 A | | | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 10.0 V/div | 20.0 V/div | 20.0 V/div | 20.0 A/div | 5.00 V/div | 10.0 V/div | 20.0 A/div |
| -24.0000 V | -16.0000 V | -28.0000 V | -68.0000 V | -77.0000 A | 6.7000 V ofst | -36.0000 V | -50.0000 A |
| ↓ 48.0985 V | ↓ 49.2829 V | ↓ 735.1 mV | ↓ 1.0281 V | ↓ -160.0 mA | ↓ 30.0 mV | ↓ 63.9676 V | ↓ -168.2 mA |
| ↑ 48.0552 V | ↑ 47.5628 V | ↑ 47.9167 V | ↑ 47.6997 V | ↑ 40.7 mA | ↑ 3.1278 V | ↑ 62.0173 V | ↑ -355.4 mA |

HD 12 Bits
Tbase -60.0 ms
20.0 ms/div
2.5 MS 12.5 MS/s
Trigger C4 DC
Stop 11.0 V
Edge Positive
X1= 2.07064 ms ΔX= 133.01704 ms
X2= 135.08768 ms 1/ΔX= 7.517834 Hz

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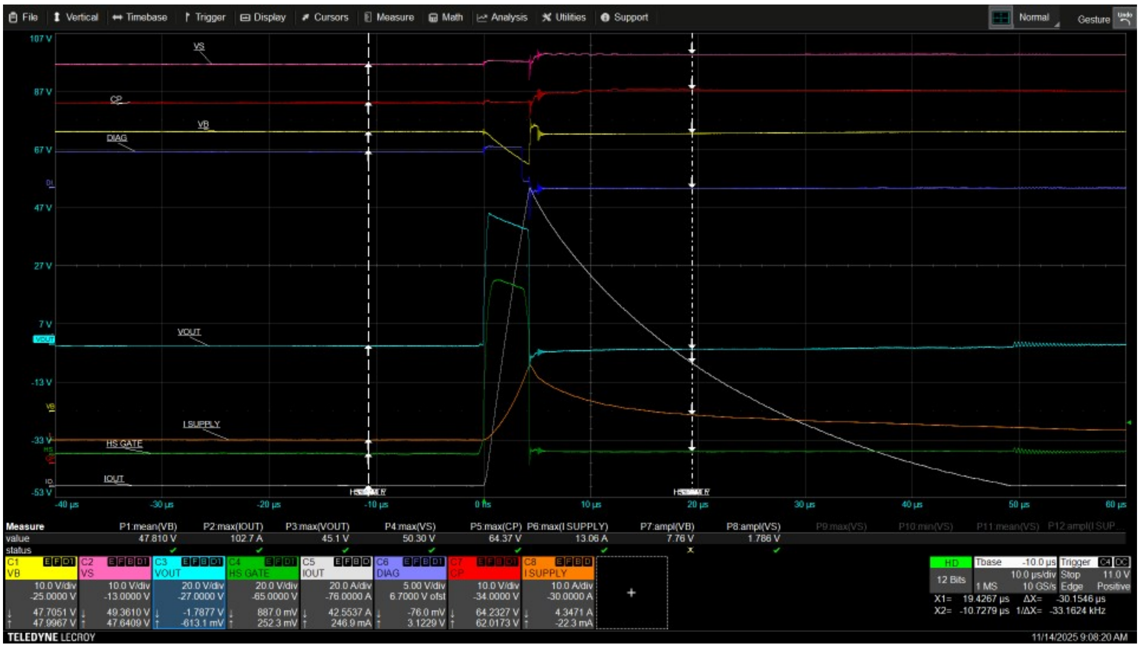
Figure 52. **Zoomed view of waveforms acquired at 1st pulse during CCM with setup D**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 47.810 V | 102.7 A | 45.1 V | 50.30 V | 64.37 V | 13.06 A | 7.76 V | 1.786 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 10.0 V/div | 20.0 V/div | 20.0 V/div | 20.0 A/div | 5.00 V/div | 10.0 V/div | 10.0 A/div |
| -25.0000 V | -13.0000 V | -27.0000 V | -65.0000 V | -76.0000 A | 6.7000 V ofst | -34.0000 V | -30.0000 A |
| ↓ 47.7051 V | ↓ 49.3610 V | ↓ -1.7877 V | ↓ 887.0 mV | ↓ 42.5537 A | ↓ -76.0 mV | ↓ 64.2327 V | ↓ 4.3471 A |
| ↑ 47.9967 V | ↑ 47.6409 V | ↑ -613.1 mV | ↑ 252.3 mV | ↑ 246.9 mA | ↑ 3.1229 V | ↑ 62.0173 V | ↑ -22.3 mA |

HD 12 Bits
Tbase -10.0 µs
10.0 µs/div
1 MS 10 GS/s
Trigger C4 DC
Stop 11.0 V
Edge Positive
X1= 19.4267 µs ΔX= -30.1546 µs
X2= -10.7279 µs 1/ΔX= -33.1624 kHz

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### 5.2.4 Trial Setup E1

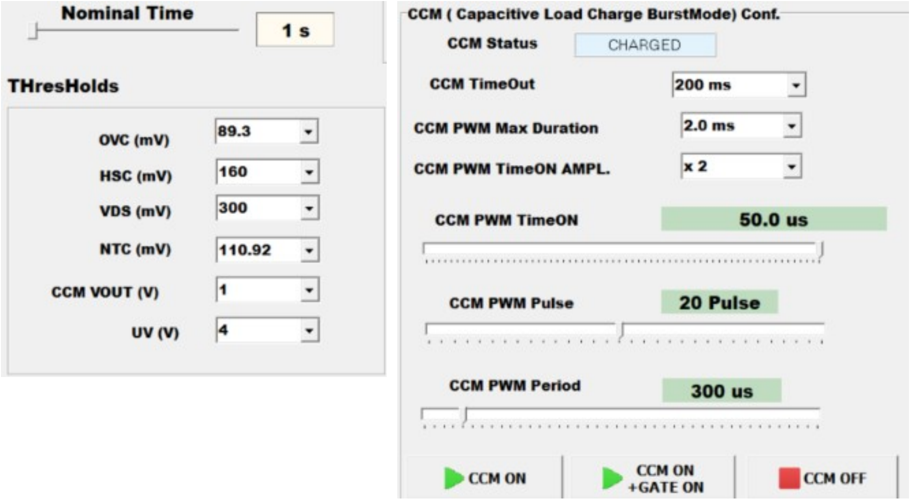
It adopts the same setup as trial B6 with $C_{LOAD}$ increased at 4.7 mF vs 3.3 mF.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = 4.7 mF (measured 4.52 mF)**
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 53

Figure 53. CCM configuration and result from GUI for test setup E1



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

**Result E1:**

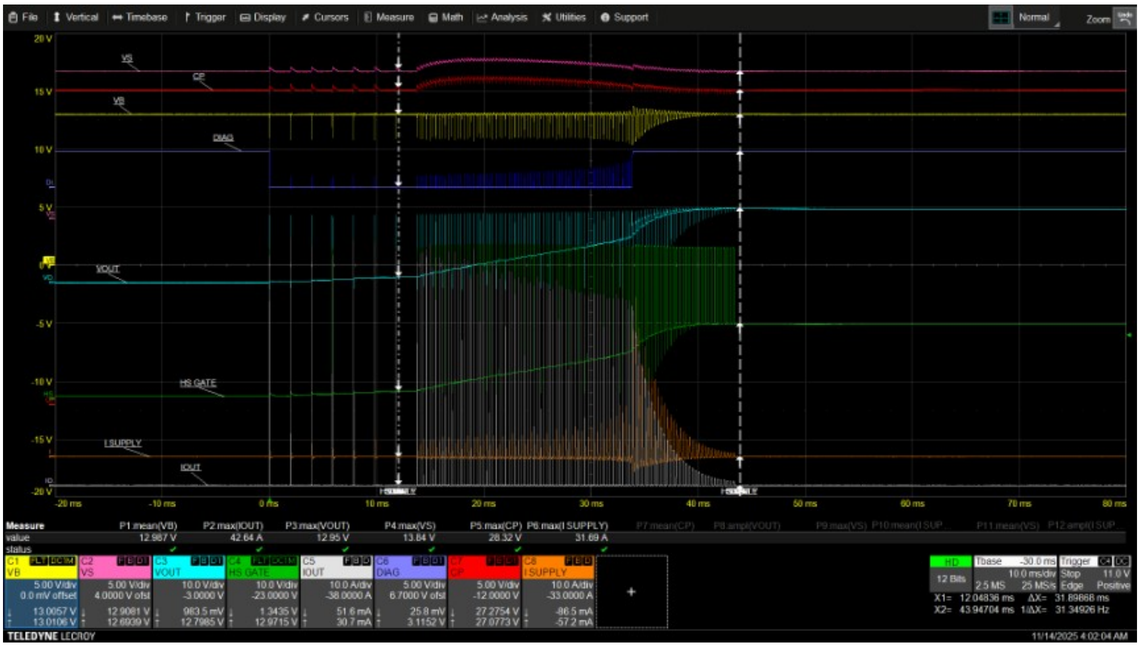
With the mentioned setup E1, the $C_{LOAD}$ is charged in 4 ms (start phase) + 30 ms (standard phase).

This setup is verified both in Unlocked and Fail-safe modes with negligible difference in terms of $t_{CHARGE}$.

The setting of various parameters is written in NVM to maintain in Fail-safe state with the same setup adopted on the device in Unlocked state.

The CCM mode is activated in Fail-safe state by four pulses on DIN. Due to DIN remaining high at the end of the $C_{LOAD}$ charge, the HS_GATE remains ON differently on the trials done in Unlocked state in which the gate was turned OFF at the end of the CCM.

Figure 54. Waveforms acquired during CCM with setup E1 with device in Unlocked mode



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 12.987 V | 42.64 A | 12.95 V | 13.84 V | 28.32 V | 31.69 A |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 0.0 mV offset | 4.0000 V ofst | -3.0000 V | -23.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -33.0000 A |
| ↓ 13.0057 V | ↓ 12.9081 V | ↓ 983.5 mV | ↓ 1.3435 V | ↓ 51.6 mA | ↓ 25.8 mV | ↓ 27.2754 V | ↓ -86.5 mA |
| ↑ 13.0106 V | ↑ 12.6939 V | ↑ 12.7985 V | ↑ 12.9715 V | ↑ 30.7 mA | ↑ 3.1152 V | ↑ 27.0773 V | ↑ -57.2 mA |

HD 12 Bits
Tbase -30.0 ms 10.0 ms/div 2.5 MS 25 MS/s
Trigger C4 DC Stop 11.0 V Edge Positive
X1= 12.04836 ms ΔX= 31.89868 ms
X2= 43.94704 ms 1/ΔX= 31.34926 Hz
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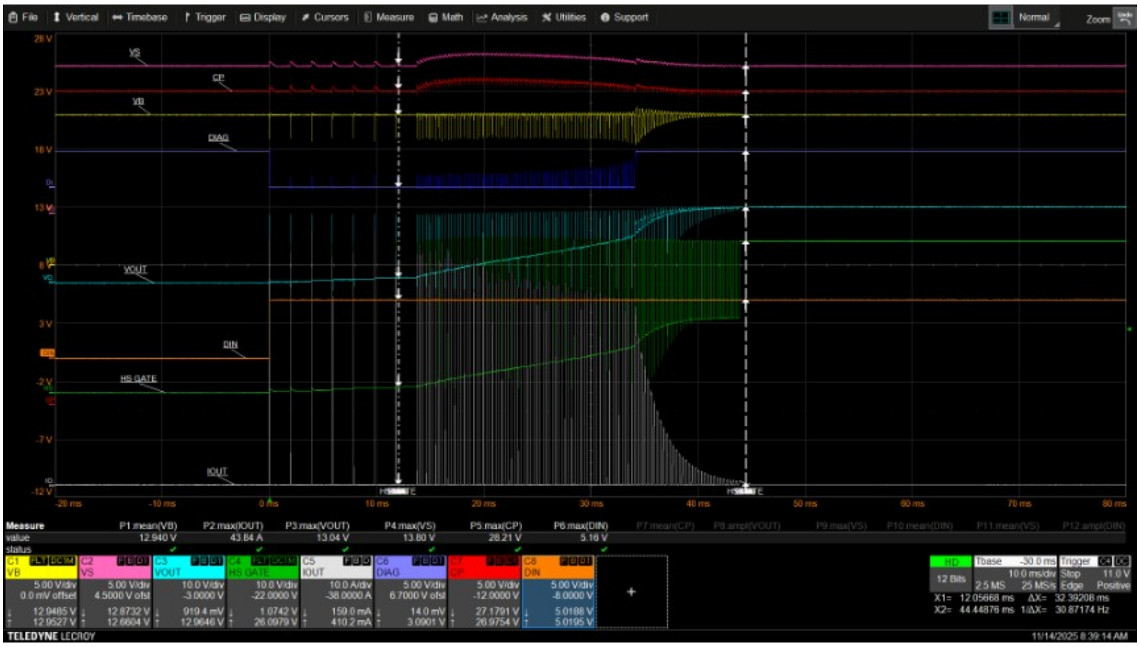
Figure 55. Waveforms acquired during CCM with setup E1 with device in Fail-safe mode

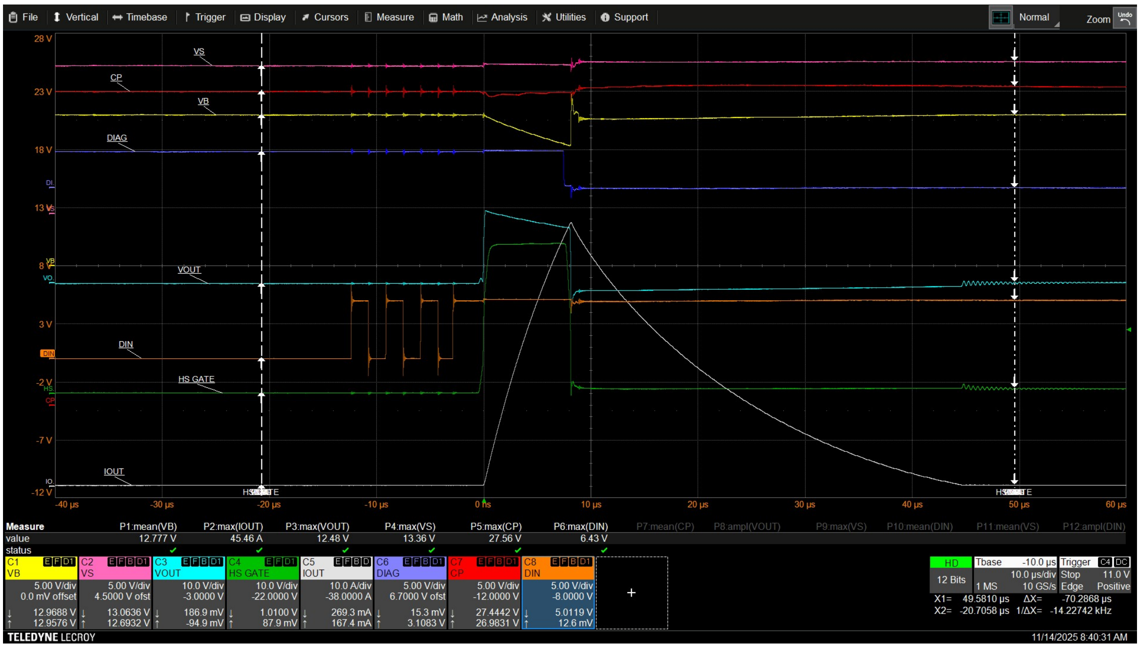


| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(DIN) |
|---|---|---|---|---|---|---|
| value | 12.940 V | 43.84 A | 13.04 V | 13.80 V | 28.21 V | 5.16 V |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 DIN |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 5.00 V/div |
| 0.0 mV offset | 4.5000 V ofst | -3.0000 V | -22.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -8.0000 V |
| ↓ 12.9485 V | ↓ 12.8732 V | ↓ 919.4 mV | ↓ 1.0742 V | ↓ 150.0 mA | ↓ 14.0 mV | ↓ 27.1791 V | ↓ 5.0188 V |
| ↑ 12.9527 V | ↑ 12.6604 V | ↑ 12.9646 V | ↑ 26.0979 V | ↑ 410.2 mA | ↑ 3.0901 V | ↑ 26.9754 V | ↑ 5.0195 V |

HD 12 Bits
Tbase -30.0 ms 10.0 ms/div 2.5 MS 25 MS/s
Trigger C4 DC Stop 11.0 V Edge Positive
X1= 12.05668 ms ΔX= 32.39208 ms
X2= 44.44876 ms 1/ΔX= 30.87174 Hz
11/14/2025 8:39:14 AM

Figure 56. Zoomed waveforms acquired at CCM start with setup E1 with device in Fail-safe mode



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(DIN) | P7:mean(CP) | P8:ampl(VOUT) | P9:max(VS) | P10:mean(DIN) | P11:mean(VS) | P12:ampl(DIN) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.777 V | 45.46 A | 12.48 V | 13.36 V | 27.56 V | 6.43 V | | | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 DIN |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 5.00 V/div |
| 0.0 mV offset | 4.5000 V ofst | -3.0000 V | -22.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -8.0000 V |
| ↓ 12.9688 V | ↓ 13.0636 V | ↓ 186.9 mV | ↓ 1.0100 V | ↓ 269.3 mA | ↓ 15.3 mV | ↓ 27.4442 V | ↓ 5.0119 V |
| ↑ 12.9576 V | ↑ 12.6932 V | ↑ -94.9 mV | ↑ 87.9 mV | ↑ 167.4 mA | ↑ 3.1083 V | ↑ 26.9831 V | ↑ 12.6 mV |

HD 12 Bits
Tbase -10.0 µs
10.0 µs/div
1 MS 10 GS/s
Trigger C4 DC
Stop 11.0 V
Edge Positive
X1= 49.5810 µs ΔX= -70.2868 µs
X2= -20.7058 µs 1/ΔX= -14.22742 kHz
11/14/2025 8:40:31 AM

## 5.2.5 Trial Setup F

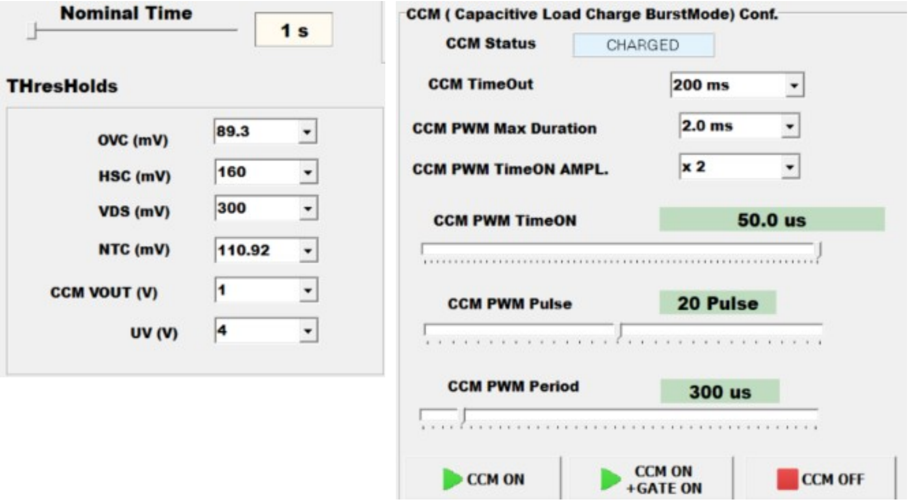
It adopts the same setup as trial E1 with VB increased at 24 V vs 13 V.

- **VB = 24 V**
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = 4.7 mF (measured 4.52 mF)**
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 57

Figure 57. **CCM configuration and result from GUI for test setup F**



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

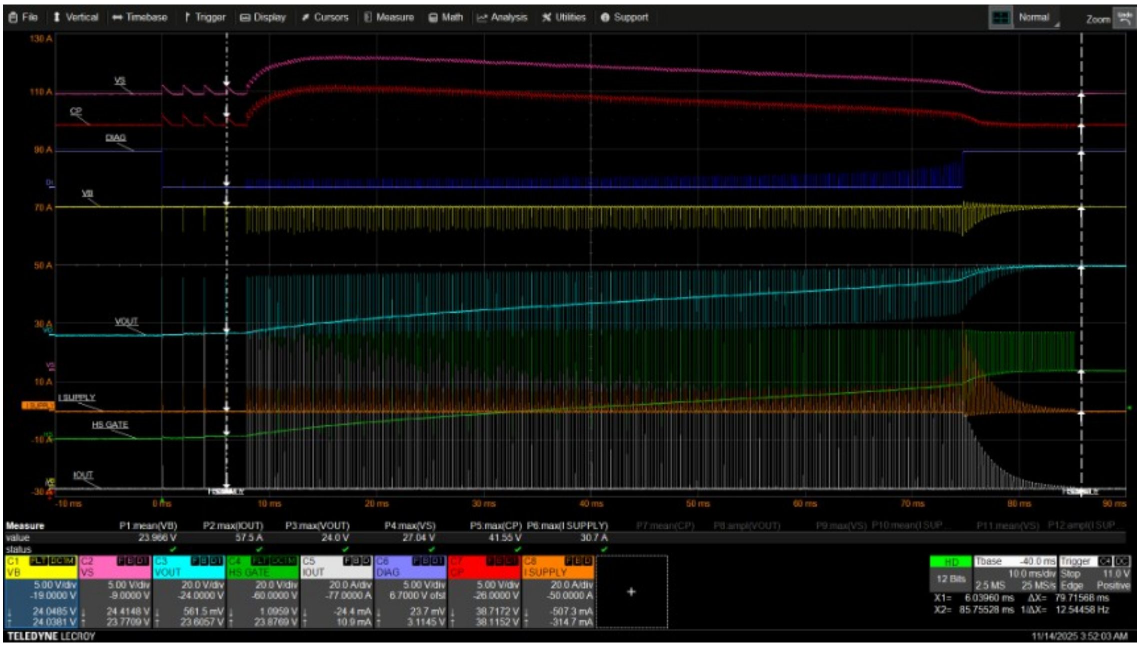
CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

**Result F:**

With the mentioned setup F, the $C_{LOAD}$ is charged in 8 ms (start phase) + 77.7 ms (standard phase).

Working with 4.7 mF as $C_{LOAD}$ and VB at 24 V, the maximum value achieved by VS was 27 V.

Figure 58. **Waveforms acquired during CCM with setup F**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 23.966 V | 57.5 A | 24.0 V | 27.04 V | 41.55 V | 30.7 A |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

| | C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|---|
| Scale | 5.00 V/div | 5.00 V/div | 20.0 V/div | 20.0 V/div | 20.0 A/div | 5.00 V/div | 5.00 V/div | 20.0 A/div |
| Offset | -19.0000 V | -9.0000 V | -24.0000 V | -60.0000 V | -77.0000 A | 6.7000 V ofst | -26.0000 V | -50.0000 A |
| ↓ | 24.0485 V | 24.4148 V | 561.5 mV | 1.0959 V | -24.4 mA | 23.7 mV | 38.7172 V | -507.3 mA |
| ↑ | 24.0381 V | 23.7709 V | 23.6057 V | 23.8769 V | 10.9 mA | 3.1145 V | 38.1152 V | -314.7 mA |

Tbase -40.0 ms, 10.0 ms/div, 2.5 MS, 25 MS/s
Trigger C4 DC, Stop 11.0 V, Edge Positive
X1= 6.03960 ms ΔX= 79.71568 ms
X2= 85.75528 ms 1/ΔX= 12.54458 Hz

## 5.2.6 Trial Setup G

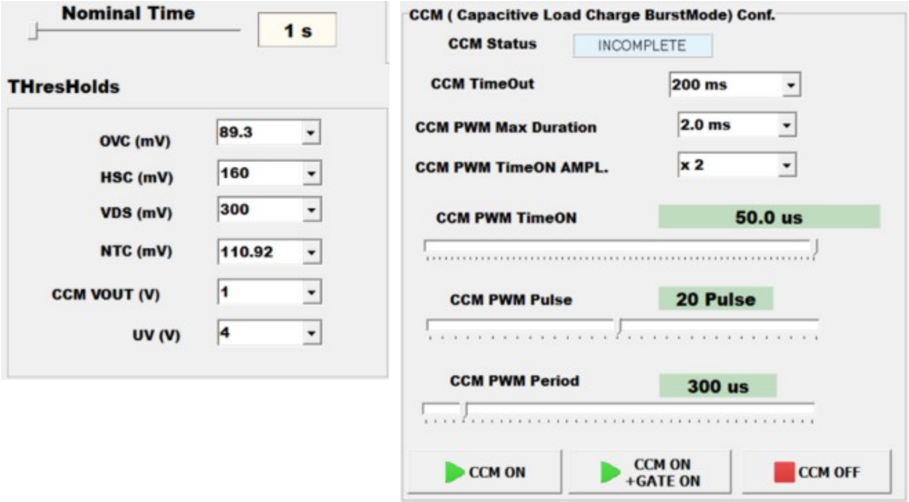
It adopts the same setup as trial E1 with VB increased at 48 V vs 13 V.

- **VB = 48 V**
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = 4.7 mF (measured 4.52 mF)**
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = T_NOM$_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 59

Figure 59. **CCM configuration and result from GUI for test setup G**



**Nominal Time** 1 s

**THresHolds**

| | |
|---|---|
| OVC (mV) | 89.3 |
| HSC (mV) | 160 |
| VDS (mV) | 300 |
| NTC (mV) | 110.92 |
| CCM VOUT (V) | 1 |
| UV (V) | 4 |

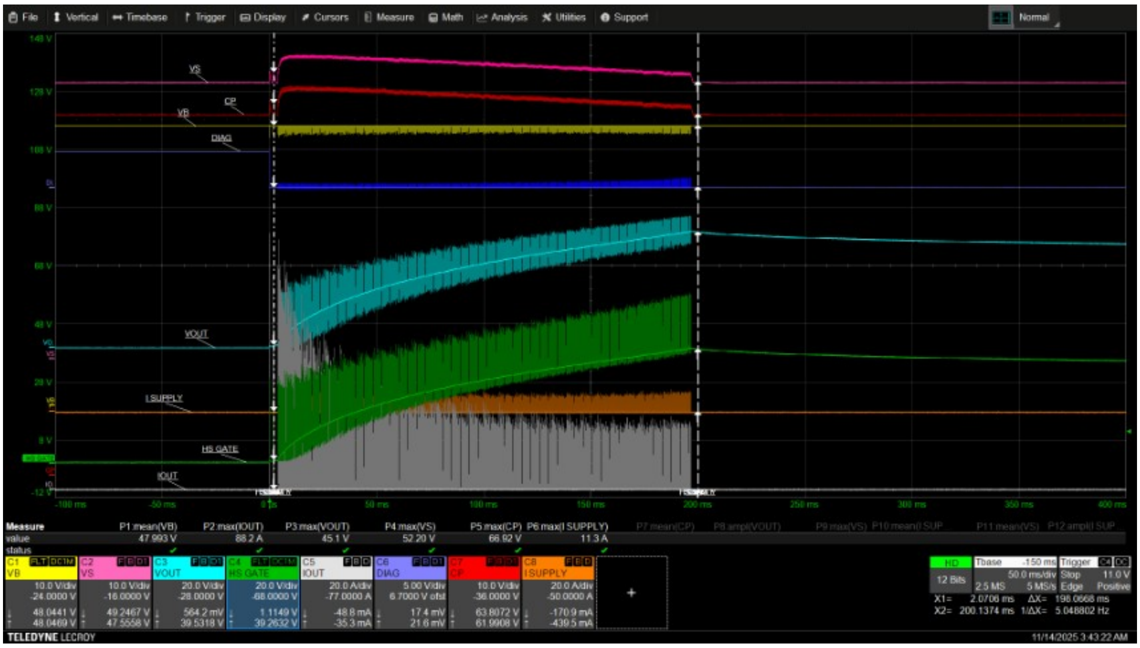
**CCM ( Capacitive Load Charge BurstMode) Conf.**

| | |
|---|---|
| CCM Status | INCOMPLETE |
| CCM TimeOut | 200 ms |
| CCM PWM Max Duration | 2.0 ms |
| CCM PWM TimeON AMPL. | x 2 |
| CCM PWM TimeON | 50.0 us |
| CCM PWM Pulse | 20 Pulse |
| CCM PWM Period | 300 us |

**Result G:**

With the mentioned setup G, the 4.7 mF C$_{LOAD}$ charge results incomplete in 2 ms (start phase) + 198 ms (standard phase) as shown in Figure 60 so that the trial was repeated increasing CCM timeout from 200 ms to 300 ms.

Figure 60. Waveforms acquired during CCM with setup G

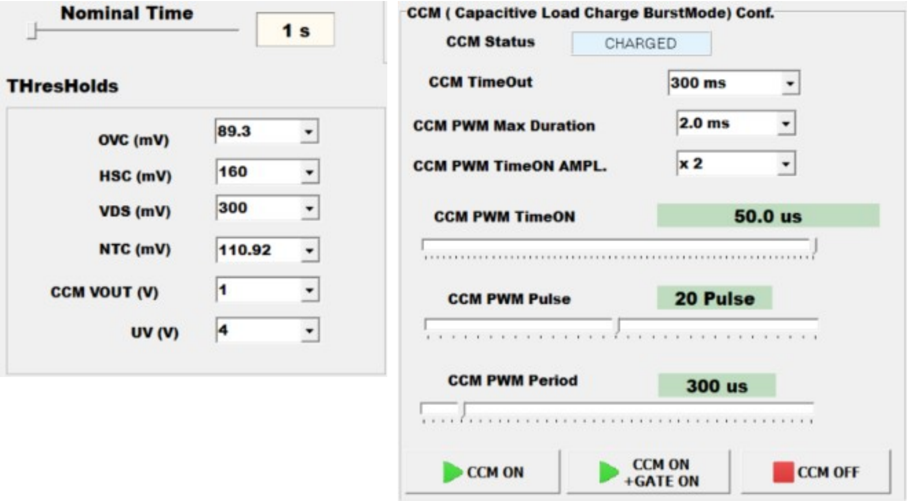


| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 47.993 V | 88.2 A | 45.1 V | 52.20 V | 66.92 V | 11.3 A |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 10.0 V/div | 20.0 V/div | 20.0 V/div | 20.0 A/div | 5.00 V/div | 10.0 V/div | 20.0 A/div |
| -24.0000 V | -16.0000 V | -28.0000 V | -68.0000 V | -77.0000 A | 6.7000 V ofst | -36.0000 V | -50.0000 A |
| 48.0441 V | 49.2467 V | 564.2 mV | 1.1149 V | -48.8 mA | 17.4 mV | 63.8072 V | -170.9 mA |
| 48.0469 V | 47.5558 V | 39.5318 V | 39.2632 V | -35.3 mA | 21.6 mV | 61.9908 V | -439.5 mA |

Tbase -150 ms 50.0 ms/div 2.5 MS 5 MS/s
Trigger C4 DC Stop 11.0 V Edge Positive
X1= 2.0706 ms ΔX= 198.0668 ms
X2= 200.1374 ms 1/ΔX= 5.048802 Hz

Figure 61. CCM configuration and result from GUI for test setup G-bis with CCM timeout at 300 ms



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 300 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

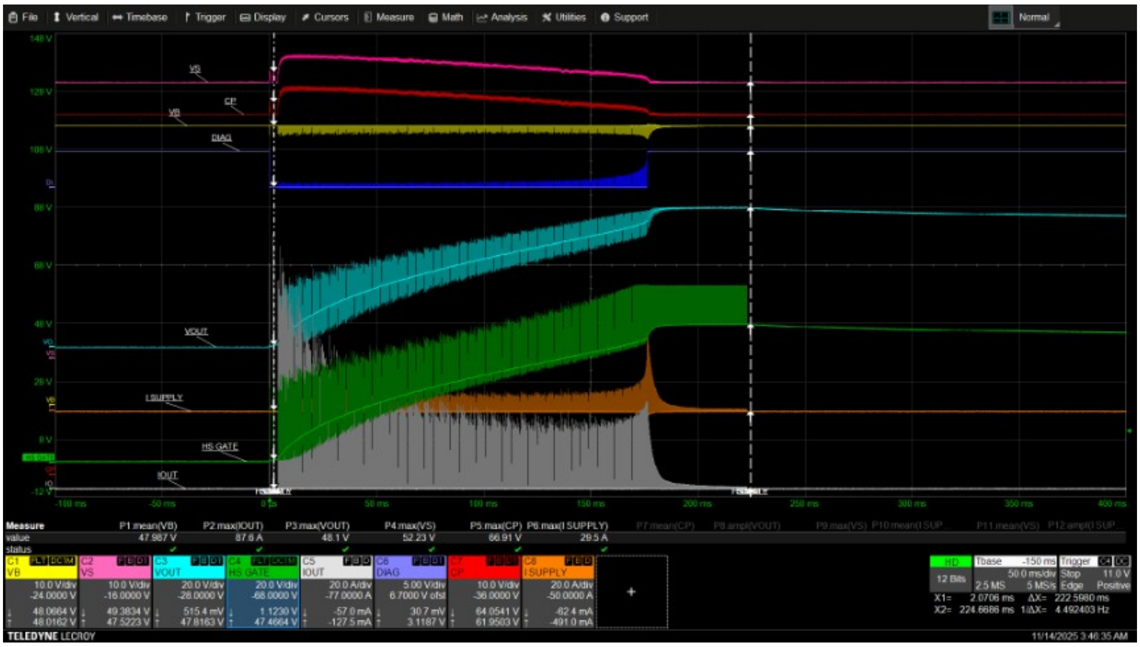
**Result G-bis:**

With the mentioned setup G-bis, the 4.7 mF $C_{LOAD}$ charge is completed in 2 ms (start phase) + 222.6 ms (standard phase).

An impact of VB at 48 V vs 13 V is visible on IOUT max and VS max:

- IOUT max reached 87.6 A on trial G-bis vs 42.6 A on trial E1
- VS max reached 52.2 V on trial G-bis vs 13.8 V on trial E1

Figure 62. **Waveforms acquired during CCM with setup G-bis**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:mean(CP) | P8:ampl(VOUT) | P9:max(VS) | P10:mean(I SUP... | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 47.987 V | 87.6 A | 48.1 V | 52.23 V | 66.91 V | 29.5 A | | | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 10.0 V/div | 20.0 V/div | 20.0 V/div | 20.0 A/div | 5.00 V/div | 10.0 V/div | 20.0 A/div |
| -24.0000 V | -16.0000 V | -28.0000 V | -68.0000 V | -77.0000 A | 6.7000 V ofst | -36.0000 V | -50.0000 A |
| ↓ 48.0664 V | ↓ 49.3834 V | ↓ 515.4 mV | ↓ 1.1230 V | ↓ -57.0 mA | ↓ 30.7 mV | ↓ 64.0541 V | ↓ -62.4 mA |
| ↑ 48.0162 V | ↑ 47.5223 V | ↑ 47.8163 V | ↑ 47.4664 V | ↑ -127.5 mA | ↑ 3.1187 V | ↑ 61.9503 V | ↑ -491.0 mA |

HD 12 Bits
Tbase -150 ms 50.0 ms/div 2.5 MS 5 MS/s
Trigger C4 DC Stop 11.0 V Edge Positive
X1= 2.0706 ms ΔX= 222.5980 ms
X2= 224.6686 ms 1/ΔX= 4.492403 Hz
11/14/2025 3:46:35 AM

## 5.3 Effect of CCM_VOUT_THR

### 5.3.1 Trial Setup H

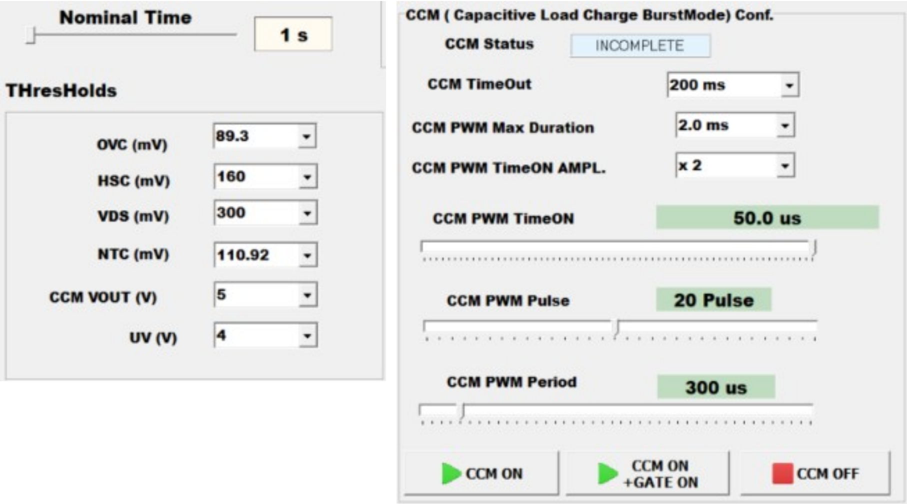
It adopts the same setup as trial E1 with the CCM_VOUT_THR increased at 5 V (max) vs 1 V (min).

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 μF and $C_S$ = 20 μF

Device in Unlocked state with the following settings:

- **CCM_VOUT_THR = 5 V**
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 μs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 μs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 63

Figure 63. CCM configuration and result from GUI for test setup H



Nominal Time: 1 s

**THresHolds**

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 5
UV (V): 4

**CCM ( Capacitive Load Charge BurstMode) Conf.**

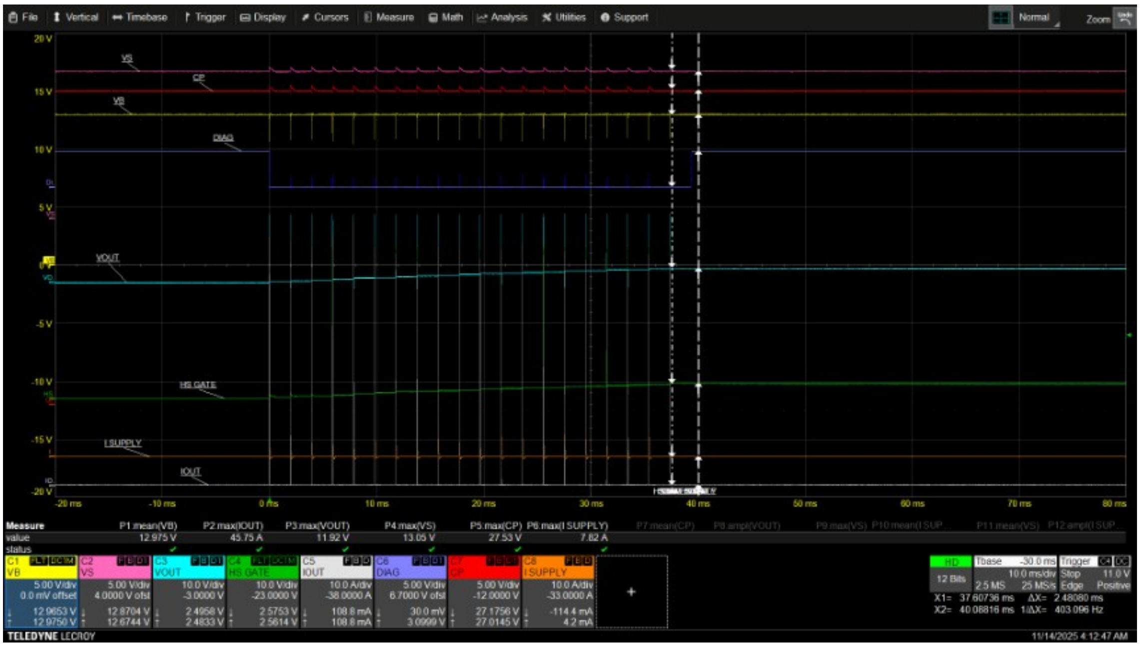
CCM Status: INCOMPLETE
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

**Result H:**

With the mentioned setup G, the 4.7 mF $C_{LOAD}$ charge results incomplete in 40 ms - 20 pulses (start phase) with VOUT reaching 2.5 V because the number of pulses is not enough to successfully complete the start phase as shown in Figure 64.

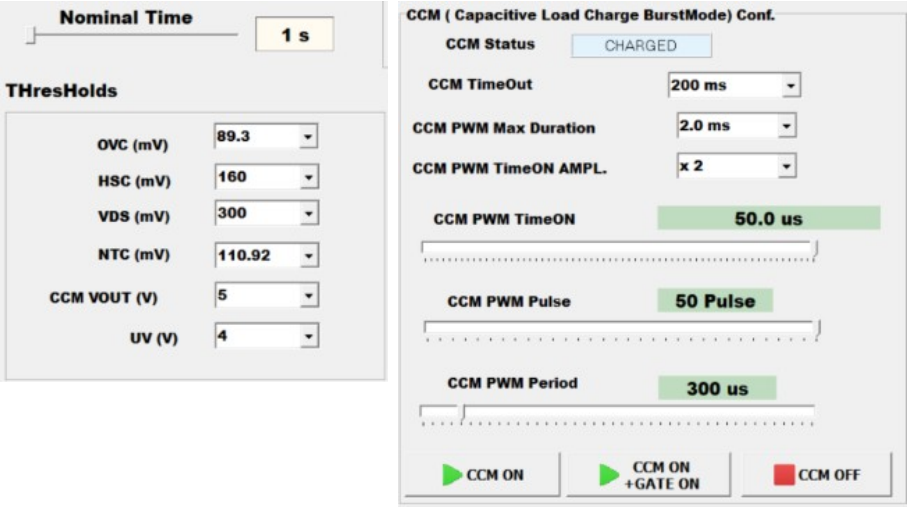
The trial was repeated by increasing the CCM PWM pulses from 20 to 50.

Figure 64. Waveforms acquired during CCM with setup H



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 12.975 V | 45.75 A | 11.92 V | 13.05 V | 27.53 V | 7.82 A |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Figure 65. CCM configuration and result from GUI for test setup H-bis with CCM PWM pulses set at 50



**Nominal Time**: 1 s

**THresHolds**

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 5
UV (V): 4

**CCM ( Capacitive Load Charge BurstMode) Conf.**

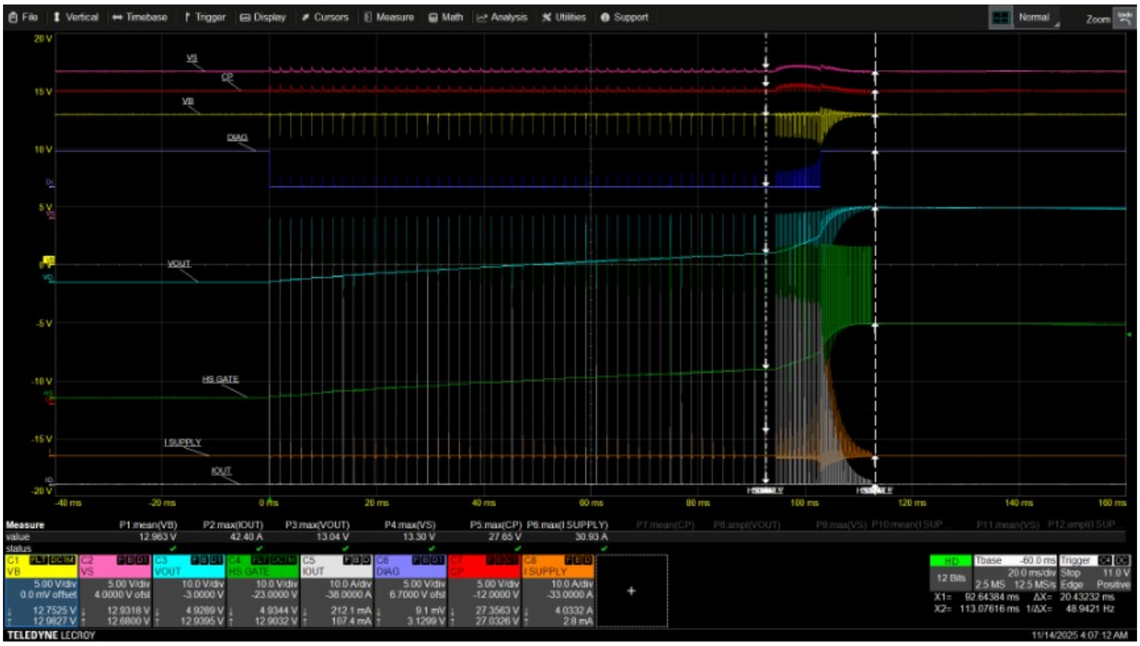
CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 50 Pulse
CCM PWM Period: 300 us

**Result H-bis:**

With the mentioned setup H-bis, the 4.7 mF $C_{LOAD}$ charge results incomplete in 94.6 ms (start phase) + 20.4 ms (standard phase).

The CCM_VOUT_THR set at maximum value involves a longer charging time, strongly affecting the duration of the start phase.

Figure 66. Waveforms acquired during CCM with setup H-bis



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 12.963 V | 42.40 A | 13.04 V | 13.30 V | 27.65 V | 30.93 A |

## 5.4 Effect of CCM_PWM_SC_T

### 5.4.1 Trial Setup I

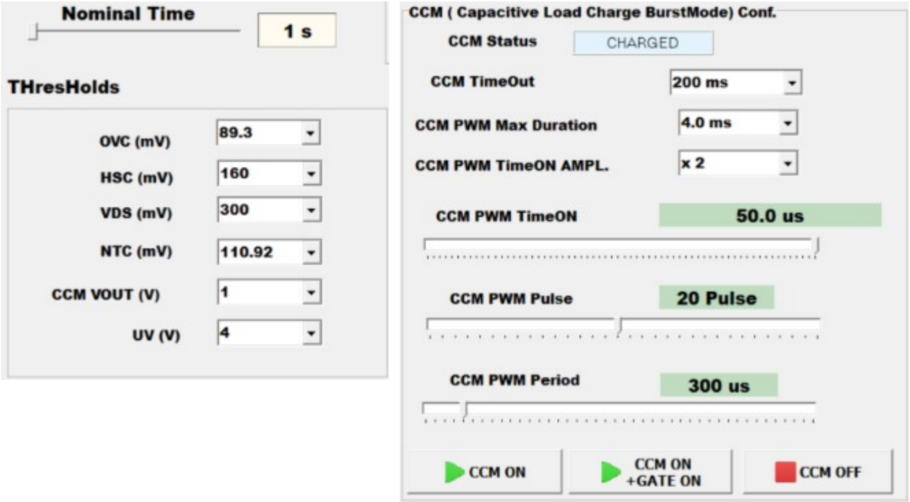
It adopts the same setup as trial E1 with the CCM_PWM_SC_T increased at 4 ms vs 2 ms.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $\text{T\_NOM}_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- **CCM_PWM_SC_T = 4 ms**
- GUI settings at the end of CCM operations as shown in Figure 67

Figure 67. **CCM configuration and result from GUI for test setup I**



Nominal Time 1 s

THresHolds

OVC (mV) 89.3
HSC (mV) 160
VDS (mV) 300
NTC (mV) 110.92
CCM VOUT (V) 1
UV (V) 4

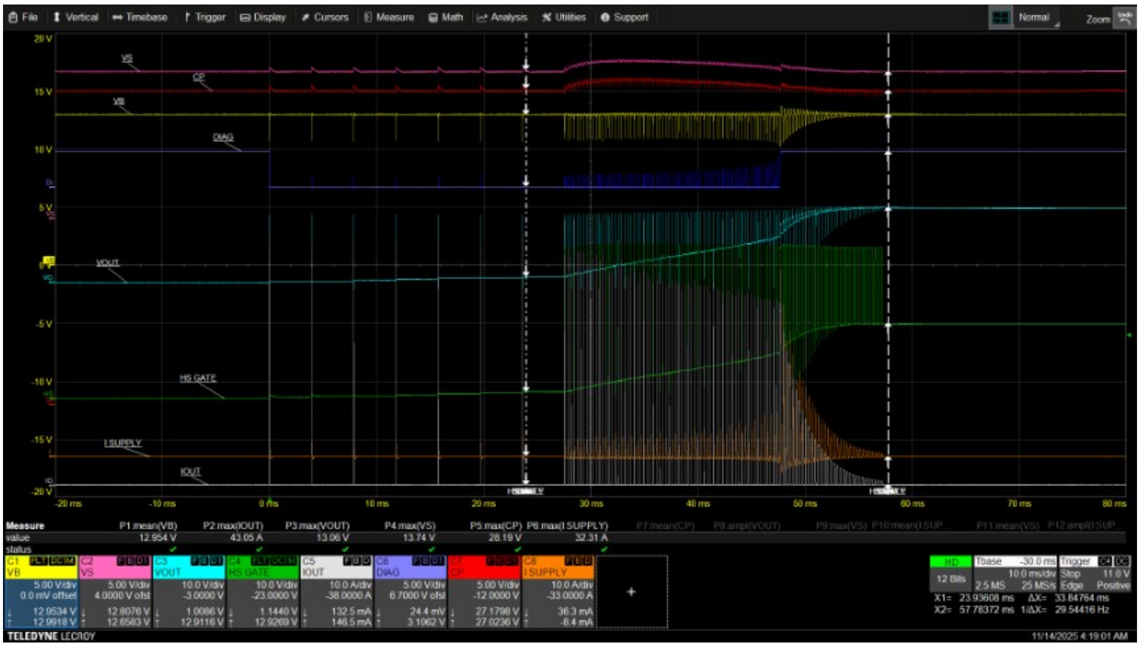
CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status CHARGED
CCM TimeOut 200 ms
CCM PWM Max Duration 4.0 ms
CCM PWM TimeON AMPL. x 2
CCM PWM TimeON 50.0 us
CCM PWM Pulse 20 Pulse
CCM PWM Period 300 us

**Result I:**

With the mentioned setup I, the $C_{LOAD}$ is charged in 26 ms (start phase) + 31.8 ms (standard phase). A longer CCM_PWM_SC_T leads to a longer charging time, affecting the duration of the start phase.

Figure 68. **Waveforms acquired during CCM with setup I**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 12.954 V | 43.05 A | 13.06 V | 13.74 V | 28.19 V | 32.31 A |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 0.0 mV offset | 4.0000 V ofst | -3.0000 V | -23.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -33.0000 A |
| ↓ 12.9534 V | ↓ 12.8076 V | ↓ 1.0086 V | ↓ 1.1440 V | ↓ 132.5 mA | ↓ 24.4 mV | ↓ 27.1798 V | ↓ 36.3 mA |
| ↑ 12.9918 V | ↑ 12.6583 V | ↑ 12.9116 V | ↑ 12.9269 V | ↑ 146.5 mA | ↑ 3.1062 V | ↑ 27.0236 V | ↑ -8.4 mA |

HD 12 Bits
Tbase -30.0 ms 10.0 ms/div 2.5 MS 25 MS/s
Trigger C4 DC Stop 11.0 V Edge Positive
X1= 23.93608 ms ΔX= 33.84764 ms
X2= 57.78372 ms 1/ΔX= 29.54416 Hz
11/14/2025 4:19:01 AM

## 5.5 Effect of CCM_PWM_T

### 5.5.1 Trial Setup J

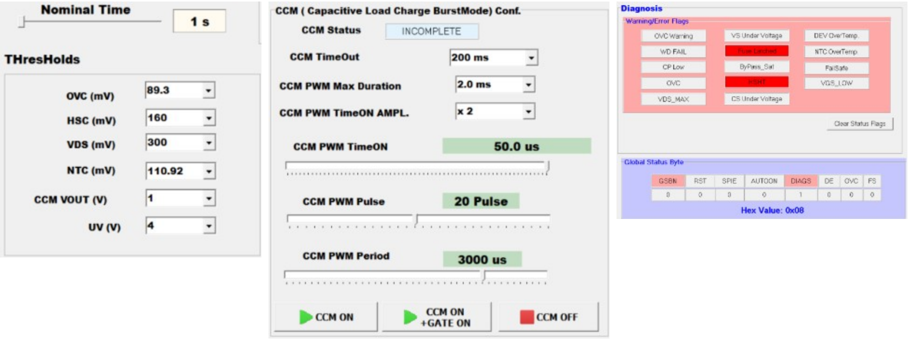
It adopts the same setup as trial E1 with the CCM_PWM_T increased at 3000 μs vs 300 μs.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 μF and $C_S$ = 20 μF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 5 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 μs
- CCM_PWM_TON_MF = 2 x
- **CCM_PWM_SC_T_NB = 20 pulses**
- **CCM_PWM_T = 3000 μs**
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 69

Figure 69. **CCM configuration and result from GUI for test setup J**



Nominal Time: 1 s

THresHolds
- OVC (mV): 89.3
- HSC (mV): 160
- VDS (mV): 300
- NTC (mV): 110.92
- CCM VOUT (V): 1
- UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.
- CCM Status: INCOMPLETE
- CCM TimeOut: 200 ms
- CCM PWM Max Duration: 2.0 ms
- CCM PWM TimeON AMPL.: x 2
- CCM PWM TimeON: 50.0 us
- CCM PWM Pulse: 20 Pulse
- CCM PWM Period: 3000 us

Global Status Byte

| GSBN | RST | SPIE | AUTOON | DIAGS | DE | OVC | FS |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

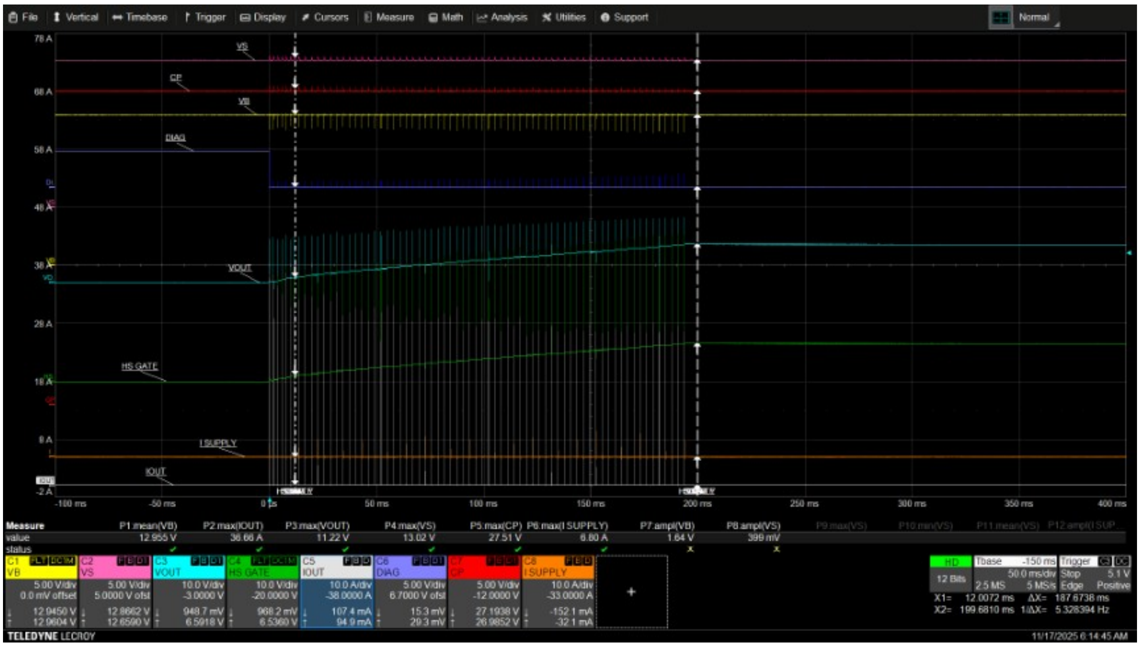
Hex Value: 0x08

### Result J:

With the mentioned setup J, the 4.7 mF $C_{LOAD}$ charge results incomplete in 14 ms (start phase) + 186 ms (standard phase) with VOUT reaching 6.6 V because a longer PWM period with a very small duty cycle are not enough to successfully complete the start phase as shown in Figure 70. The diagnosis reported DIAGS flag due to eFuse + hard short protections being triggered.

The trial was repeated by increasing the CCM timeout from 200 ms to 400 ms.

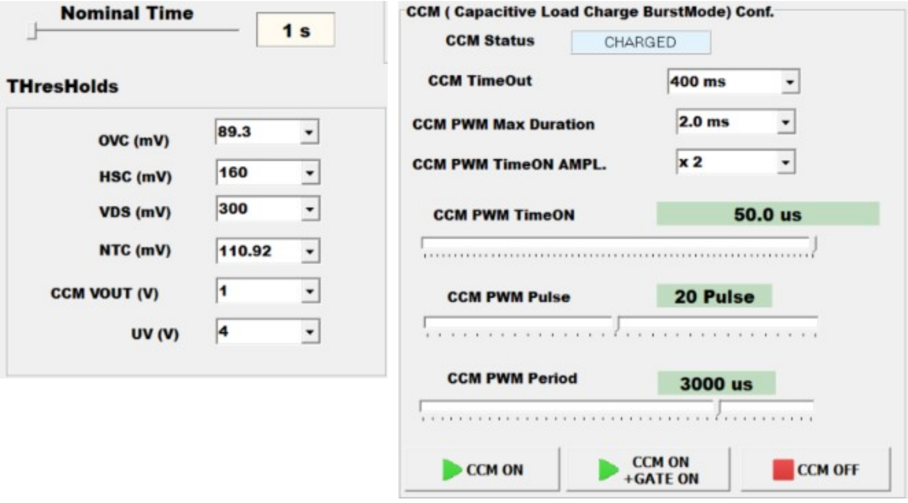
Figure 70. **Waveforms acquired during CCM with setup J**



```
Measure  P1:mean(VB)  P2:max(IOUT)  P3:max(VOUT)  P4:max(VS)  P5:max(CP)  P6:max(I SUPPLY)  P7:ampl(VB)  P8:ampl(VS)
value    12.955 V     36.66 A       11.22 V       13.02 V     27.51 V     6.80 A            1.64 V       399 mV
status   ✓            ✓             ✓             ✓           ✓           ✓                 x            x
```

```
C1 VB        5.00 V/div   0.0 mV offset    ↓ 12.9450 V   ↑ 12.9604 V
C2 VS        5.00 V/div   5.0000 V ofst    ↓ 12.8662 V   ↑ 12.6590 V
C3 VOUT      10.0 V/div   -3.0000 V        ↓ 948.7 mV    ↑ 6.5918 V
C4 HS GATE   10.0 V/div   -20.0000 V       ↓ 968.2 mV    ↑ 6.5360 V
C5 IOUT      10.0 A/div   -38.0000 A       ↓ 107.4 mA    ↑ 94.9 mA
C6 DIAG      5.00 V/div   6.7000 V ofst    ↓ 15.3 mV     ↑ 29.3 mV
C7 CP        5.00 V/div   -12.0000 V       ↓ 27.1938 V   ↑ 26.9852 V
C8 I SUPPLY  10.0 A/div   -33.0000 A       ↓ -152.1 mA   ↑ -32.1 mA
Tbase -150 ms  50.0 ms/div  2.5 MS  5 MS/s   Trigger  Stop  5.1 V  Edge  Positive
X1= 12.0072 ms   ΔX= 187.6738 ms
X2= 199.6810 ms  1/ΔX= 5.328394 Hz
```

Figure 71. CCM configuration and result from GUI for test setup J-bis with CCM timeout set at 400 ms



**Nominal Time** 1 s

**THresHolds**

| | |
|---|---|
| OVC (mV) | 89.3 |
| HSC (mV) | 160 |
| VDS (mV) | 300 |
| NTC (mV) | 110.92 |
| CCM VOUT (V) | 1 |
| UV (V) | 4 |

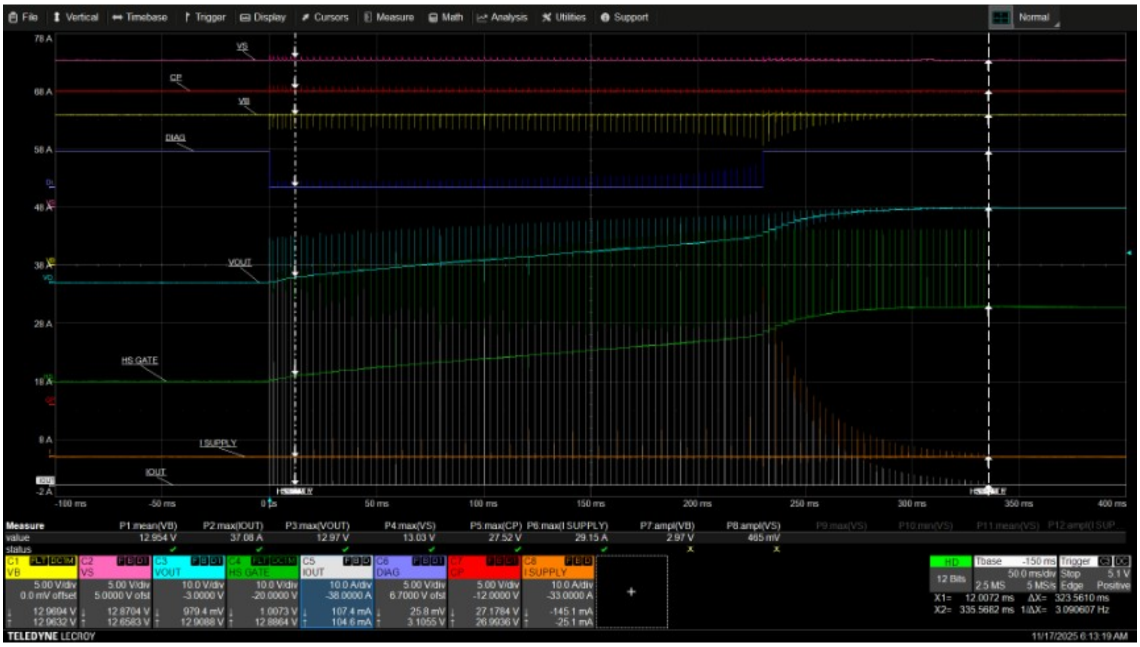
**CCM ( Capacitive Load Charge BurstMode) Conf.**

| | |
|---|---|
| CCM Status | CHARGED |
| CCM TimeOut | 400 ms |
| CCM PWM Max Duration | 2.0 ms |
| CCM PWM TimeON AMPL. | x 2 |
| CCM PWM TimeON | 50.0 us |
| CCM PWM Pulse | 20 Pulse |
| CCM PWM Period | 3000 us |

**Result J-bis:**

With the mentioned setup J-bis, the 4.7 mF $C_{LOAD}$ charge results incomplete in 14 ms (start phase) + 321.6 ms (standard phase).

Figure 72. Waveforms acquired during CCM with setup J-bis



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.954 V | 37.08 A | 12.97 V | 13.03 V | 27.52 V | 29.15 A | 2.97 V | 465 mV | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | x | x | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 0.0 mV offset | 5.0000 V ofst | -3.0000 V | -20.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -33.0000 A |
| ↓ 12.9694 V | ↓ 12.8704 V | ↓ 979.4 mV | ↓ 1.0073 V | ↓ 107.4 mA | ↓ 25.8 mV | ↓ 27.1784 V | ↓ -145.1 mA |
| ↑ 12.9632 V | ↑ 12.6583 V | ↑ 12.9088 V | ↑ 12.8864 V | ↑ 104.6 mA | ↑ 3.1055 V | ↑ 26.9936 V | ↑ -25.1 mA |

Tbase -150 ms Trigger
50.0 ms/div Stop 5.1 V
12 Bits 2.5 MS 5 MS/s Edge Positive
X1= 12.0072 ms ΔX= 323.5610 ms
X2= 335.5682 ms 1/ΔX= 3.090607 Hz

## 5.6 Effect of CCM_PWM_TON

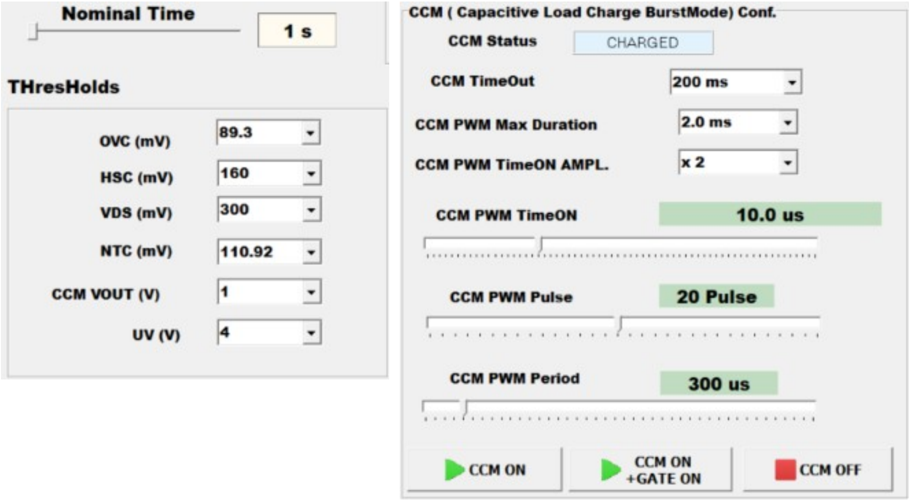
### 5.6.1 Trial Setup K

It adopts the same setup as trial E1 with the CCM_PWM_TON decreased at 10 μ vs 50 μs.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:
- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- **CCM_PWM_TON = 10 µs**
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 73

Figure 73. **CCM configuration and result from GUI for test setup K**



Nominal Time 1 s

THresHolds

OVC (mV) 89.3
HSC (mV) 160
VDS (mV) 300
NTC (mV) 110.92
CCM VOUT (V) 1
UV (V) 4

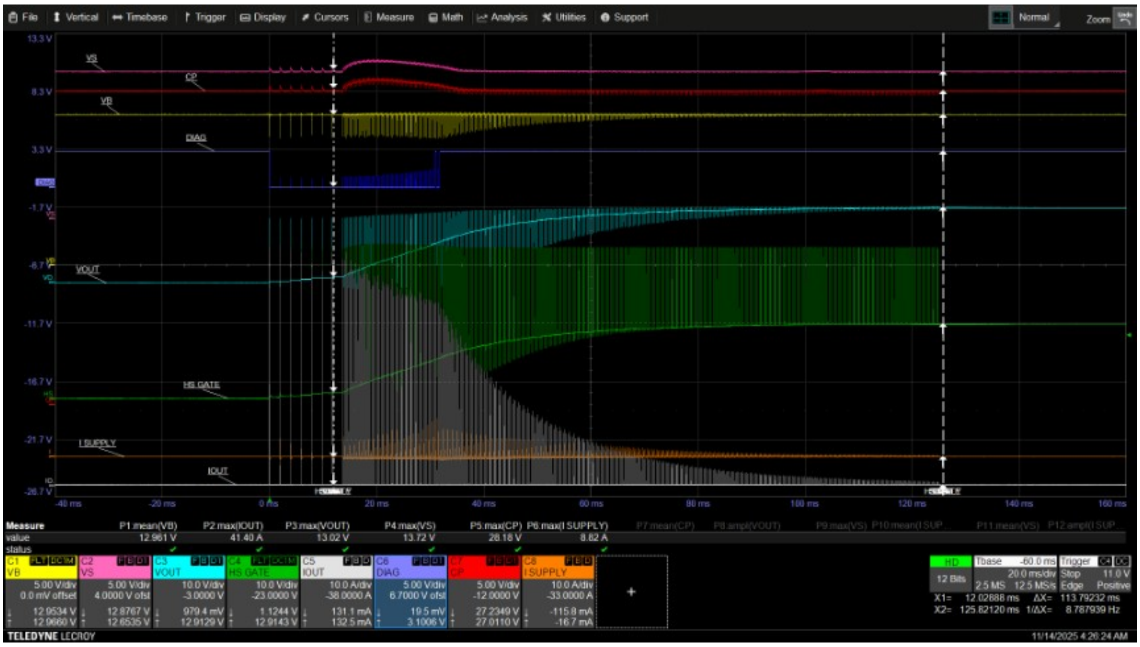
CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status CHARGED
CCM TimeOut 200 ms
CCM PWM Max Duration 2.0 ms
CCM PWM TimeON AMPL. x 2
CCM PWM TimeON 10.0 us
CCM PWM Pulse 20 Pulse
CCM PWM Period 300 us

**Result K:**

With the mentioned setup K, the $C_{LOAD}$ is charged in 14 ms (start phase) + 111.8 ms (standard phase).

Figure 74. **Waveforms acquired during CCM with setup K**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:mean(CP) | P8:ampl(VOUT) | P9:max(VS) | P10:mean(I SUP... | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.961 V | 41.40 A | 13.02 V | 13.72 V | 28.18 V | 8.82 A | | | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | | |

## 5.7 Effect of PWM Ton Multiplying Factor

### 5.7.1 Trial Setup L

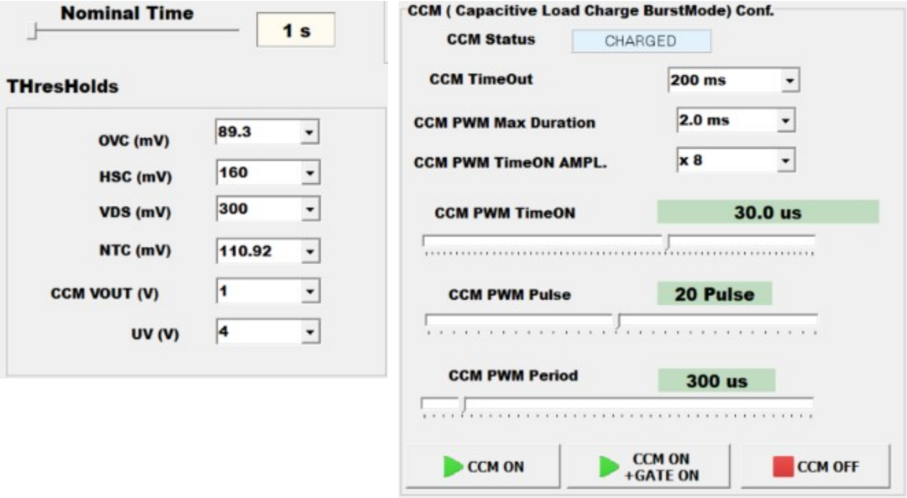
It adopts the same setup as trial E1 with the CCM_PWM_TON at 30 µs vs 50 µs and CCM_PWM_TON_MF multiplying factor at 8 x vs 2 x (duty cycle moved from 33.3% to 80%).

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- **CCM_PWM_TON = 30 µs**
- **CCM_PWM_TON_MF = 8 x**
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 75

Figure 75. **CCM configuration and result from GUI for test setup L**



**Nominal Time**: 1 s

**THresHolds**

| | |
|---|---|
| OVC (mV) | 89.3 |
| HSC (mV) | 160 |
| VDS (mV) | 300 |
| NTC (mV) | 110.92 |
| CCM VOUT (V) | 1 |
| UV (V) | 4 |

**CCM ( Capacitive Load Charge BurstMode) Conf.**

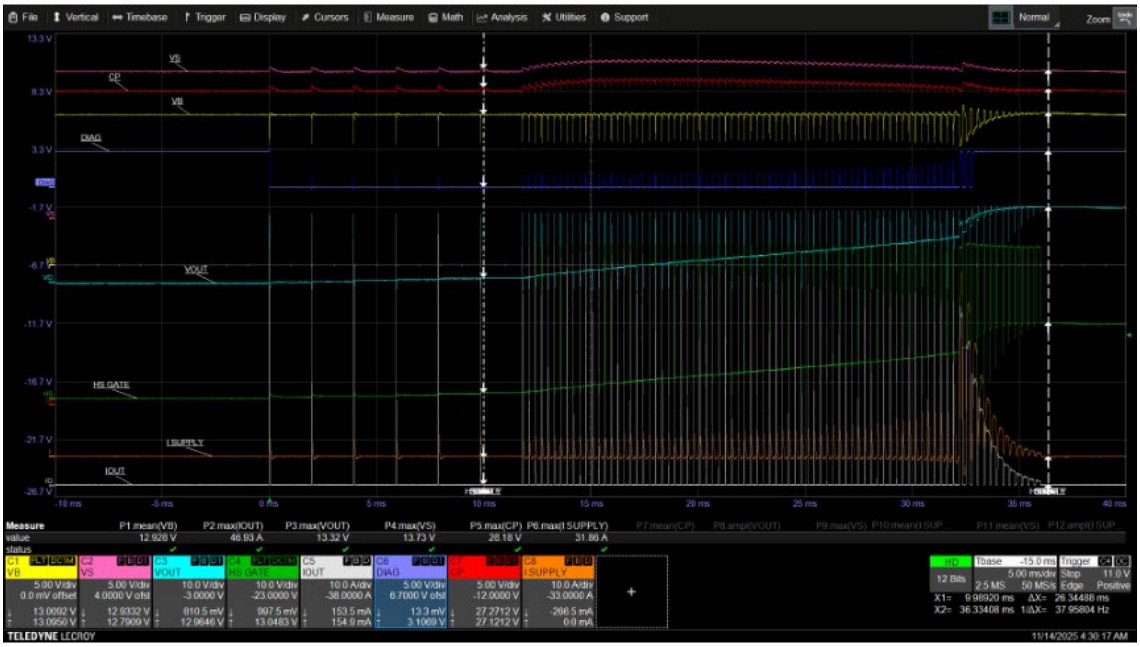
| | |
|---|---|
| CCM Status | CHARGED |
| CCM TimeOut | 200 ms |
| CCM PWM Max Duration | 2.0 ms |
| CCM PWM TimeON AMPL. | x 8 |
| CCM PWM TimeON | 30.0 us |
| CCM PWM Pulse | 20 Pulse |
| CCM PWM Period | 300 us |

**Result L:**

With the mentioned setup L, the $C_{LOAD}$ is charged in 12 ms (start phase) + 24.3 ms (standard phase).

An increase of CCM PWM Time ON decreases the duration of the CCM standard phase due to a greater PWM duty cycle at 80% (TON = 240 µs and TOFF = 300 µs)

Figure 76. **Waveforms acquired during CCM with setup L**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 12.928 V | 46.93 A | 13.32 V | 13.73 V | 28.18 V | 31.86 A |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

## 5.8 Effect of TON protection mode

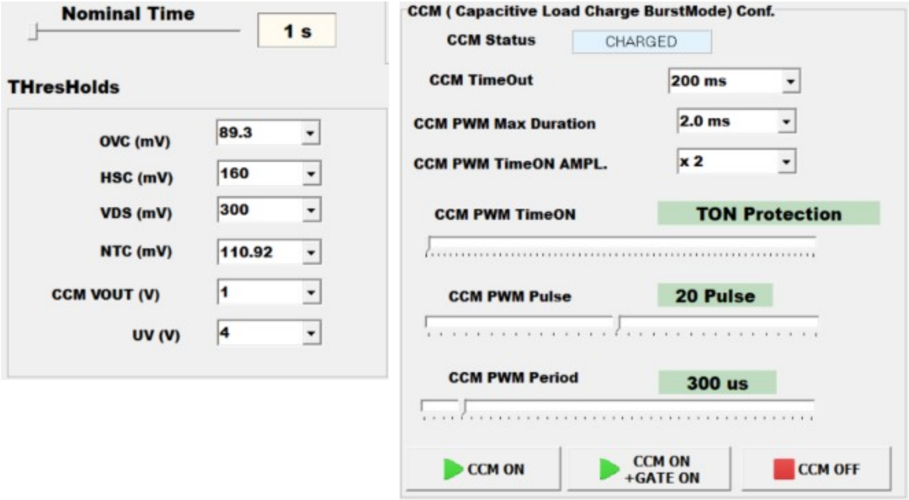
### 5.8.1 Trial Setup M

It adopts the same setup as trial E with the CCM_PWM_TON set in TON protection vs 50 us.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:
- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- **CCM_PWM_TON = TON protection**
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 77

Figure 77. **CCM configuration and result from GUI for test setup M**



Nominal Time: 1 s

THresHolds
OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

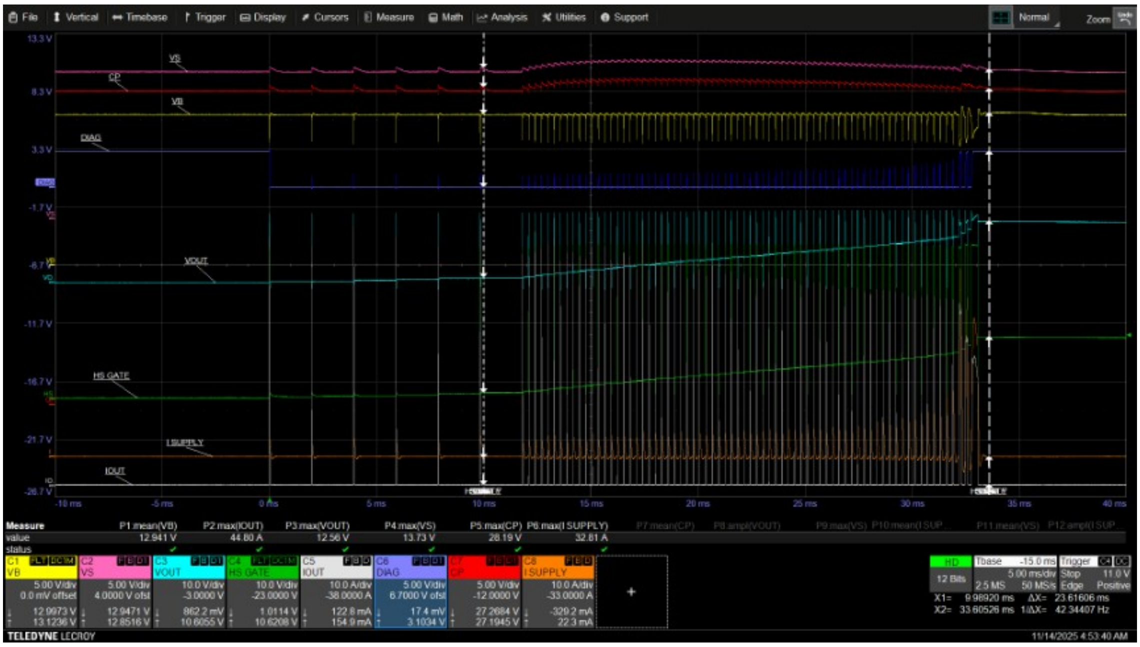
CCM ( Capacitive Load Charge BurstMode) Conf.
CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: TON Protection
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

**Result M:**

With the mentioned setup M, the $C_{LOAD}$ is charged in 12 ms (start phase) + 21.6 ms (standard phase).

The selection of TON protection as CCM PWM Time ON brings the duration of the CCM standard phase to the minimum value because the HS_GATE stays ON until $I^2t$ protection is triggered within the selected CCM PWM period.

Figure 78. **Waveforms acquired during CCM with setup M**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 12.941 V | 44.80 A | 12.56 V | 13.73 V | 28.19 V | 32.81 A |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 0.0 mV offset | 4.0000 V ofst | -3.0000 V | -23.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -33.0000 A |
| ↓ 12.0973 V | ↓ 12.9471 V | ↓ 862.2 mV | ↓ 1.0114 V | ↓ 122.8 mA | ↓ 17.4 mV | ↓ 27.2684 V | ↓ -329.2 mA |
| ↑ 13.1236 V | ↑ 12.8516 V | ↑ 10.6055 V | ↑ 10.6208 V | ↑ 154.9 mA | ↑ 3.1034 V | ↑ 27.1945 V | ↑ 22.3 mA |

HD 12 Bits
Tbase -15.0 ms
5.00 ms/div
2.5 MS 50 MS/s
Trigger C4 DC
Stop 11.0 V
Edge Positive
X1= 9.98920 ms ΔX= 23.61606 ms
X2= 33.60526 ms 1/ΔX= 42.34407 Hz
11/14/2025 4:53:40 AM

### 5.8.2 Trial Setup N

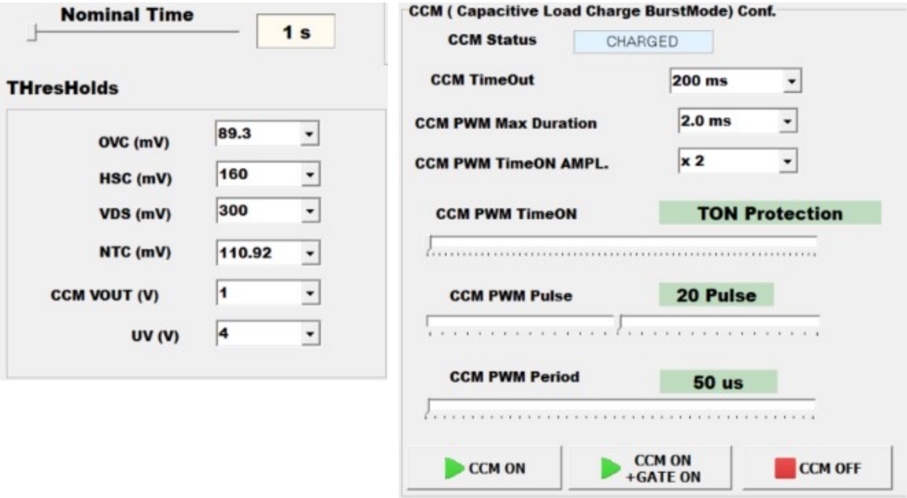
It adopts the same setup as trial M with the CCM_PWM_TON in TON protection but CCM_PWM_T (PWM Period) set at 50 µs vs 300 µs.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- **CCM_PWM_TON = TON protection**
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- **CCM_PWM_T = 50 µs**
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 79

Figure 79. **CCM configuration and result from GUI for test setup N**



**Nominal Time**: 1 s

**THresHolds**

| | |
|---|---|
| OVC (mV) | 89.3 |
| HSC (mV) | 160 |
| VDS (mV) | 300 |
| NTC (mV) | 110.92 |
| CCM VOUT (V) | 1 |
| UV (V) | 4 |

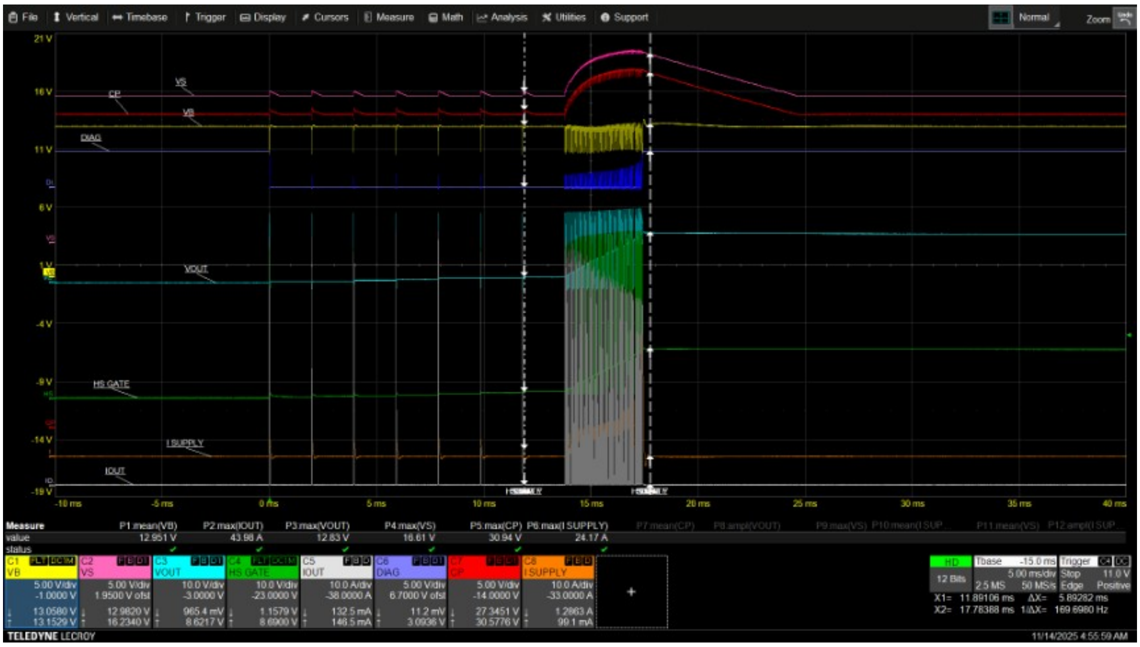
**CCM ( Capacitive Load Charge BurstMode) Conf.**

| | |
|---|---|
| CCM Status | CHARGED |
| CCM TimeOut | 200 ms |
| CCM PWM Max Duration | 2.0 ms |
| CCM PWM TimeON AMPL. | x 2 |
| CCM PWM TimeON | TON Protection |
| CCM PWM Pulse | 20 Pulse |
| CCM PWM Period | 50 us |

**Result N:**

With the mentioned setup N, the 4.7 mF $C_{LOAD}$ is charged in 14 ms (start phase) + 3.9 ms (standard phase). This setup allows us to achieve the fastest charge of the selected $C_{LOAD}$ at 13 V.

Figure 80. **Waveforms acquired during CCM with setup N**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 12.951 V | 43.98 A | 12.83 V | 16.61 V | 30.94 V | 24.17 A |

## 5.9 Effect of OVC_THR and HSC_THR

### 5.9.1 Trial Setup O

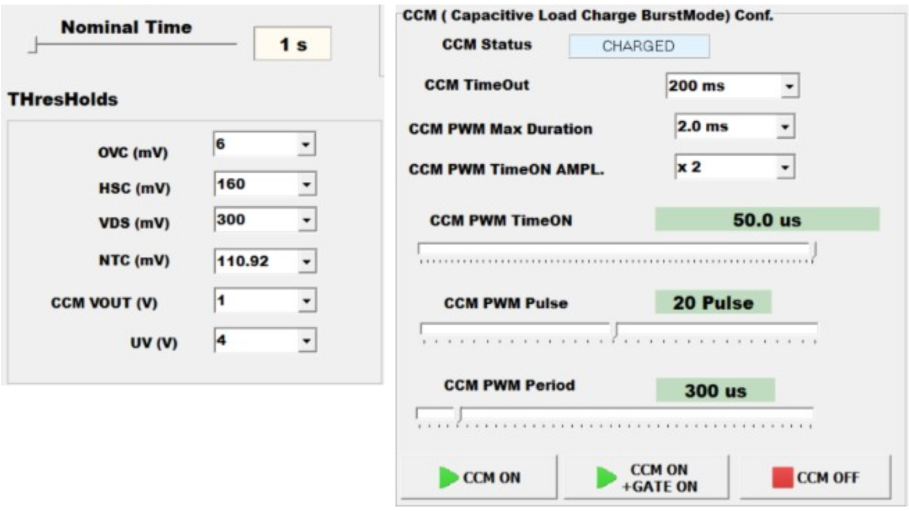
It adopts the same setup as trial E1 with OVC_THR set at 6 mV (min) vs 89.3 mV (max).

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 μF and $C_S$ = 20 μF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- **OVC_THR = VOC_THRS_0 → 6 mV**
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 μs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 μs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 81

Figure 81. **CCM configuration and result from GUI for test setup O**



Nominal Time: 1 s

THresHolds

OVC (mV): 6

HSC (mV): 160

VDS (mV): 300

NTC (mV): 110.92

CCM VOUT (V): 1

UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED

CCM TimeOut: 200 ms

CCM PWM Max Duration: 2.0 ms

CCM PWM TimeON AMPL.: x 2

CCM PWM TimeON: 50.0 us

CCM PWM Pulse: 20 Pulse

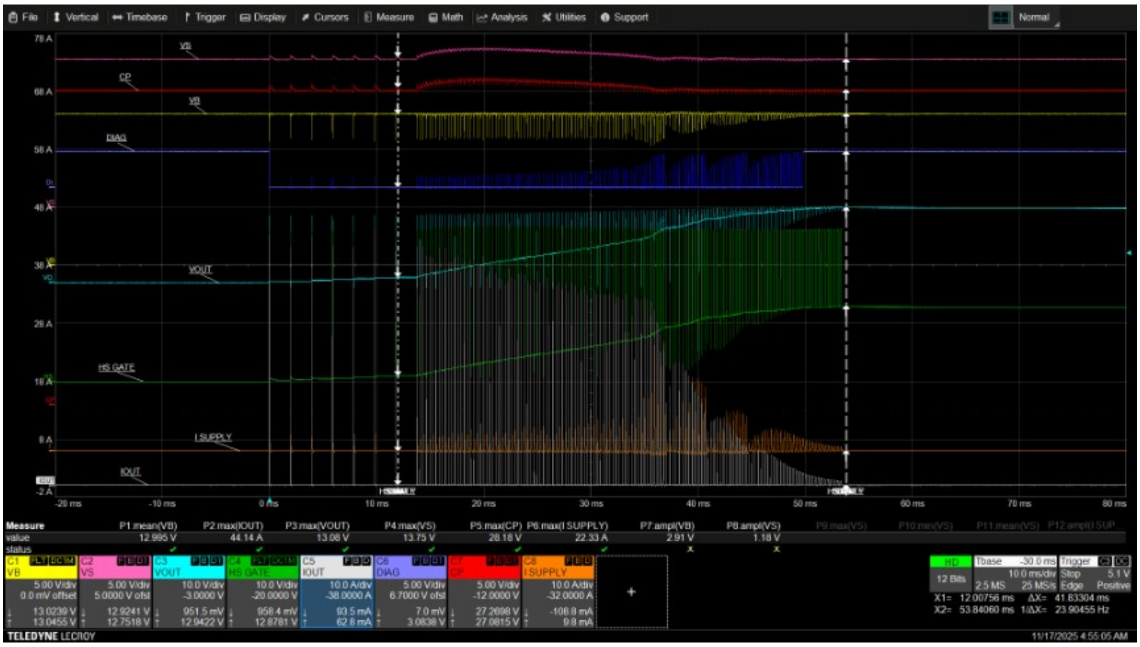
CCM PWM Period: 300 us

**Result O:**

With the mentioned setup O, the 4.7 mF $C_{LOAD}$ is charged in 14 ms (start phase) + 39.8 ms (standard phase).

This setup involves a slower speed in the standard charging phase due to the min OVC threshold strongly affecting the standard phase duration.

Figure 82. Waveforms acquired during CCM with setup O



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.995 V | 44.14 A | 13.08 V | 13.75 V | 28.18 V | 22.33 A | 2.91 V | 1.18 V | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | x | x | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 0.0 mV offset | 5.0000 V ofst | -3.0000 V | -20.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -32.0000 A |
| ↓ 13.0239 V | ↓ 12.9241 V | ↓ 951.5 mV | ↓ 958.4 mV | ↓ 93.5 mA | ↓ 7.0 mV | ↓ 27.2698 V | ↓ -108.8 mA |
| ↑ 13.0455 V | ↑ 12.7518 V | ↑ 12.9422 V | ↑ 12.8781 V | ↑ 62.8 mA | ↑ 3.0838 V | ↑ 27.0815 V | ↑ 9.8 mA |

HD 12 Bits
Tbase -30.0 ms 10.0 ms/div 2.5 MS 25 MS/s
Trigger Stop 5.1 V Edge Positive
X1= 12.00756 ms ΔX= 41.83304 ms
X2= 53.84060 ms 1/ΔX= 23.90455 Hz
11/17/2025 4:55:05 AM

## 5.9.2 Trial Setup P

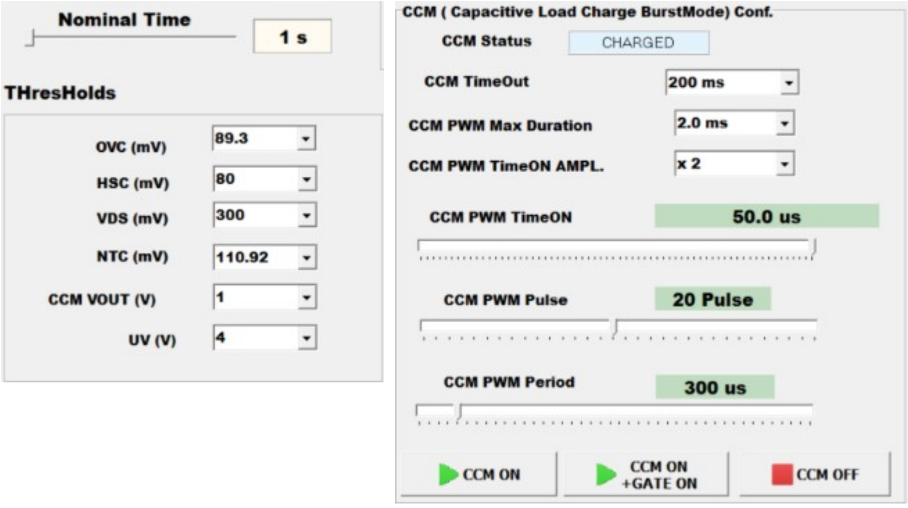
It adopts the same setup as trial E1 with HSC_THR set at 80 mV vs 160 mV (max).

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- **HSC_THR = VHSC_THRS_10 → 80 mV**
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 83

Figure 83. **CCM configuration and result from GUI for test setup P**



**Nominal Time**: 1 s

**THresHolds**

OVC (mV): 89.3
HSC (mV): 80
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

**CCM ( Capacitive Load Charge BurstMode) Conf.**

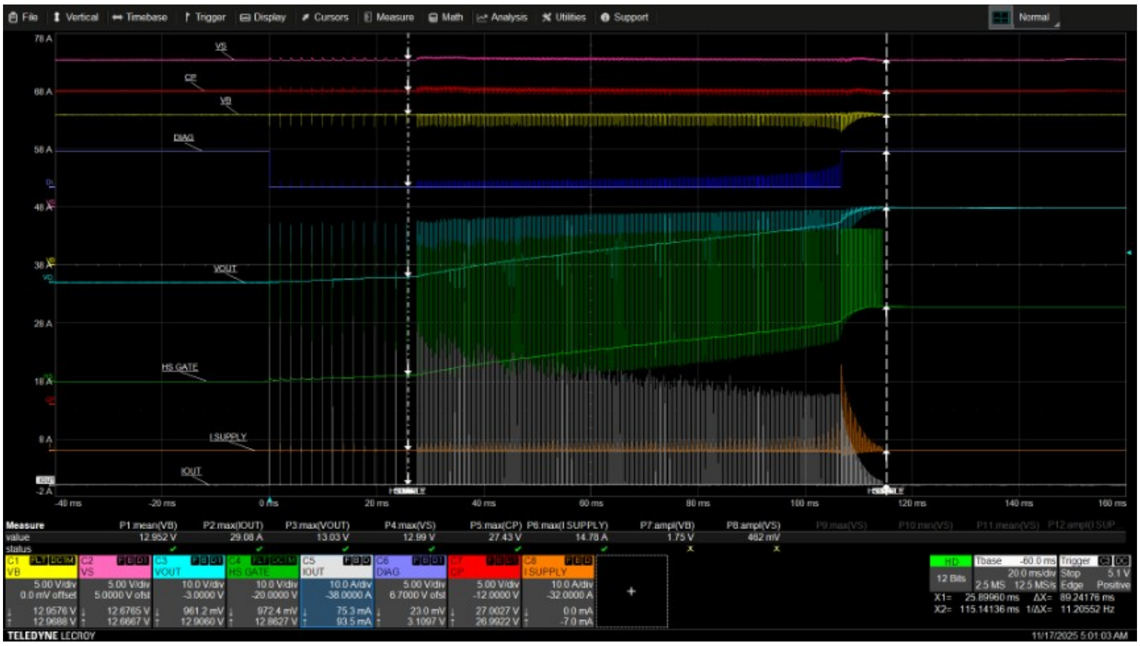
CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

**Result P:**

With the mentioned setup P, the 4.7 mF $C_{LOAD}$ is charged in 28 ms (start phase) + 87.1 ms (standard phase).

This setup involves a slower speed to charge due to a lower HSC threshold affecting the current peaks of both start and standard charging phases.

Figure 84. **Waveforms acquired during CCM with setup P**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) |
|---|---|---|---|---|---|---|---|---|
| value | 12.952 V | 29.08 A | 13.03 V | 12.99 V | 27.43 V | 14.78 A | 1.75 V | 482 mV |

X1= 25.89960 ms ΔX= 89.24176 ms
X2= 115.14136 ms 1/ΔX= 11.20552 Hz

### 5.9.3 Trial Setup Q1

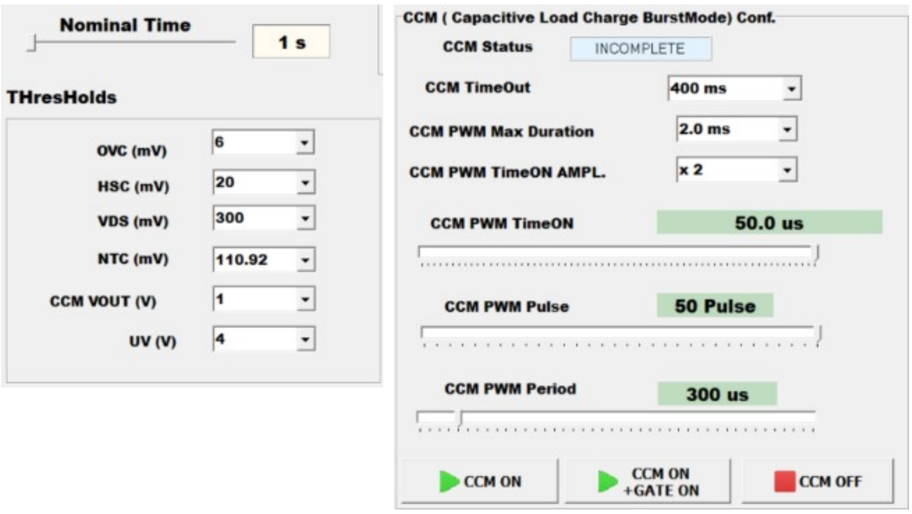
It adopts the same setup as trial E1 with OVC_THR set at 6 mV (min) vs 89.3 mV (max) and HSC_THR set at 20 mV (min) vs 160 mV (max).

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- **OVC_THR = VOC_THRS_0 → 6 mV**
- **HSC_THR = VHSC_THRS_0 → 20 mV**
- T_NOM = T_NOM$_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- **CCM_PWM_SC_T_NB = 50 pulses**
- CCM_PWM_T = 300 µs
- **CCM_TIMEOUT = 400 ms**
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 85

Figure 85. **CCM configuration and result from GUI for test setup Q1**



Nominal Time: 1 s

THresHolds

OVC (mV): 6
HSC (mV): 20
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: INCOMPLETE
CCM TimeOut: 400 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 50 Pulse
CCM PWM Period: 300 us

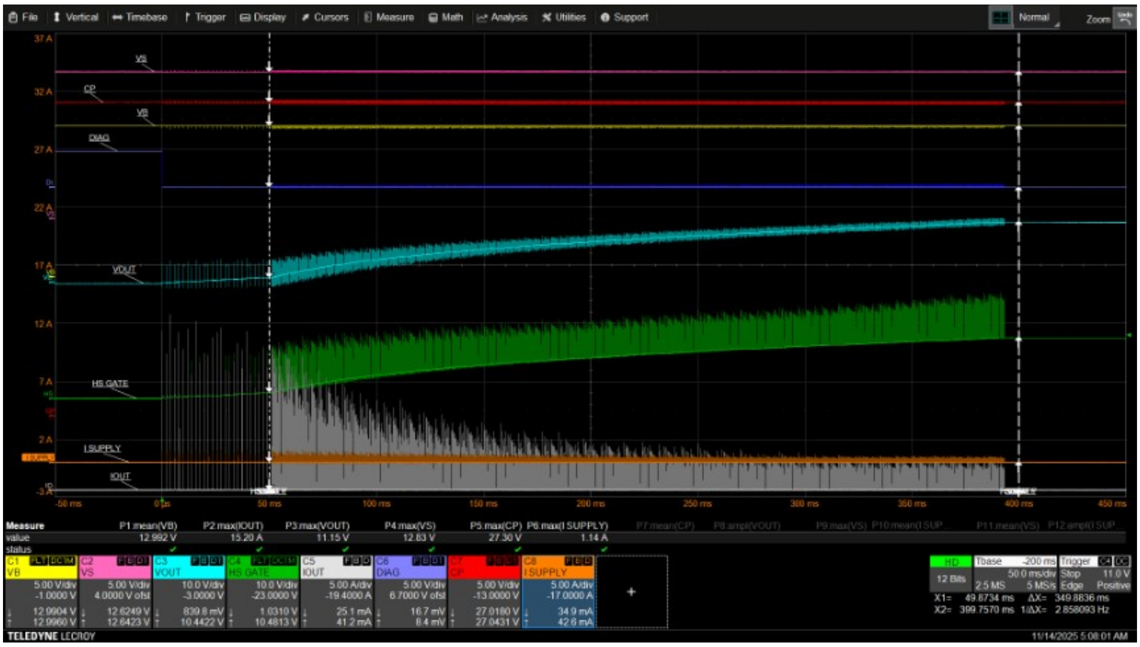
**Result Q1:**

Even if the CCM pulses are increased to 50 and CCM timeout is set at 400 ms, with the mentioned setup Q1, the 4.7 mF C$_{LOAD}$ is not charged in 50 ms (start phase) + 350 ms (standard phase). VOUT reaches 10.4 V after 400 ms.

This setup cannot charge the C$_{LOAD}$ because the usage of minimum value for OVC and HSC thresholds involves peak with minimum current during both charging phases. IOUT max results only 15.2 A vs 42.6 A of trial E1 in which both OVC and HSC were set at maximum levels.

To successfully complete the charge of the mentioned C$_{LOAD}$, fixing other parameters, the minimum OVC and HSC levels are the ones used in trial Q2.

Figure 86. Waveforms acquired during CCM with setup Q1



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 12.992 V | 15.20 A | 11.15 V | 12.83 V | 27.30 V | 1.14 A |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 5.00 A/div | 5.00 V/div | 5.00 V/div | 5.00 A/div |
| -1.0000 V | 4.0000 V ofst | -3.0000 V | -23.0000 V | -19.4000 A | 6.7000 V ofst | -13.0000 V | -17.0000 A |
| 12.9904 V | 12.6249 V | 830.8 mV | 1.0310 V | 25.1 mA | 16.7 mV | 27.0180 V | 34.9 mA |
| 12.9960 V | 12.6423 V | 10.4422 V | 10.4813 V | 41.2 mA | 8.4 mV | 27.0431 V | 42.6 mA |

HD 12 Bits
Tbase -200 ms
50.0 ms/div
2.5 MS 5 MS/s
Trigger Stop 11.0 V
Edge Positive
X1= 49.8734 ms ΔX= 349.8836 ms
X2= 399.7570 ms 1/ΔX= 2.858093 Hz

### 5.9.4 Trial Setup Q2

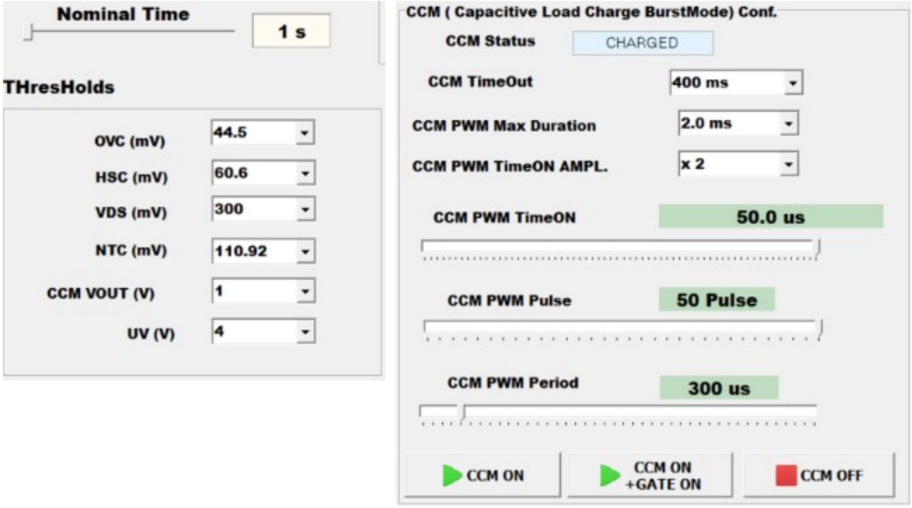
It adopts the same setup as trial E1 with OVC_THR set at 44.5 mV vs 89.3 mV (max) and HSC_THR set at 60.6 mV vs 160 mV (max).

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- **OVC_THR = VOC_THRS_24 → 44.5 mV**
- **HSC_THR = VHSC_THRS_8 → 60.6 mV**
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- **CCM_PWM_SC_T_NB = 50 pulses**
- CCM_PWM_T = 300 µs
- **CCM_TIMEOUT = 400 ms**
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 87

Figure 87. CCM configuration and result from GUI for test setup Q2



Nominal Time 1 s

THresHolds

OVC (mV) 44.5
HSC (mV) 60.6
VDS (mV) 300
NTC (mV) 110.92
CCM VOUT (V) 1
UV (V) 4

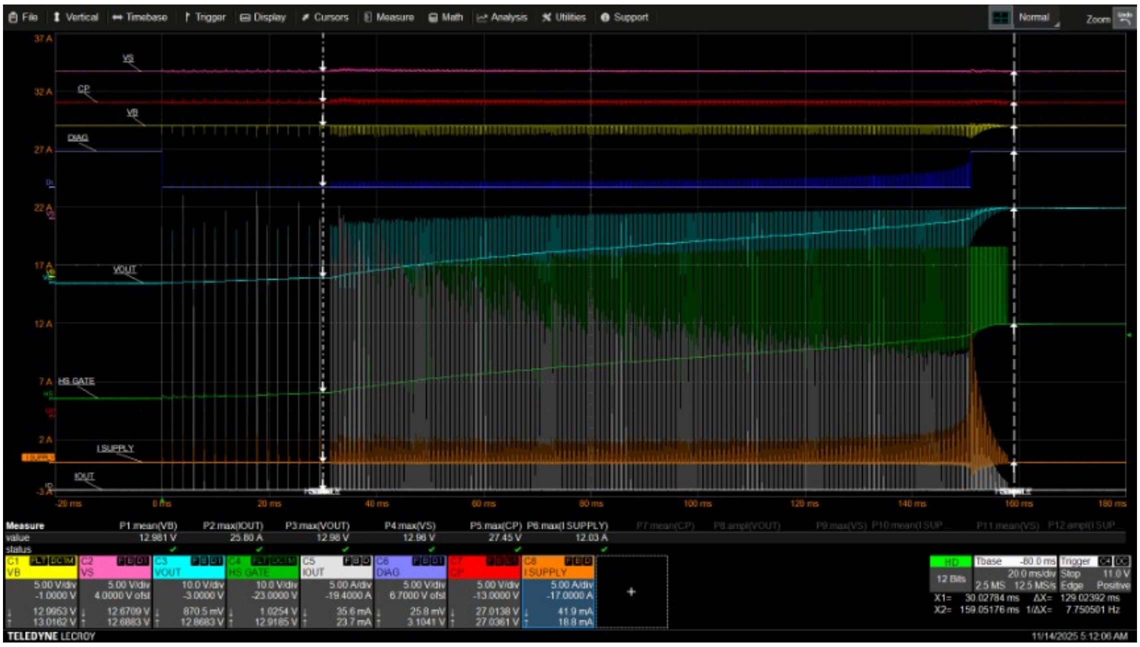
CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status CHARGED
CCM TimeOut 400 ms
CCM PWM Max Duration 2.0 ms
CCM PWM TimeON AMPL. x 2
CCM PWM TimeON 50.0 us
CCM PWM Pulse 50 Pulse
CCM PWM Period 300 us

**Result Q2:**

With the mentioned setup Q2, the 4.7 mF $C_{LOAD}$ is charged in 32 (start phase) + 127 ms (standard phase). E1 vs Q1 vs Q2 trials show the strong contribution of OVC and HSC setting in $t_{CHARGE}$.

Figure 88. Waveforms acquired during CCM with setup Q2



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 12.981 V | 25.80 A | 12.98 V | 12.96 V | 27.45 V | 12.03 A |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 5.00 A/div | 5.00 V/div | 5.00 V/div | 5.00 A/div |
| -1.0000 V | 4.0000 V ofst | -3.0000 V | -23.0000 V | -19.4000 A | 6.7000 V ofst | -13.0000 V | -17.0000 A |
| 12.9953 V | 12.6709 V | 870.5 mV | 1.0254 V | 35.6 mA | 25.8 mV | 27.0138 V | 41.9 mA |
| 13.0162 V | 12.6883 V | 12.8683 V | 12.9185 V | 23.7 mA | 3.1041 V | 27.0361 V | 18.8 mA |

Tbase -80.0 ms, 20.0 ms/div, 2.5 MS, 12.5 MS/s
Trigger C4 DC, Stop 11.0 V, Edge Positive
X1= 30.02784 ms ΔX= 129.02392 ms
X2= 159.05176 ms 1/ΔX= 7.750501 Hz

## 5.9.5 Trial Setup R1

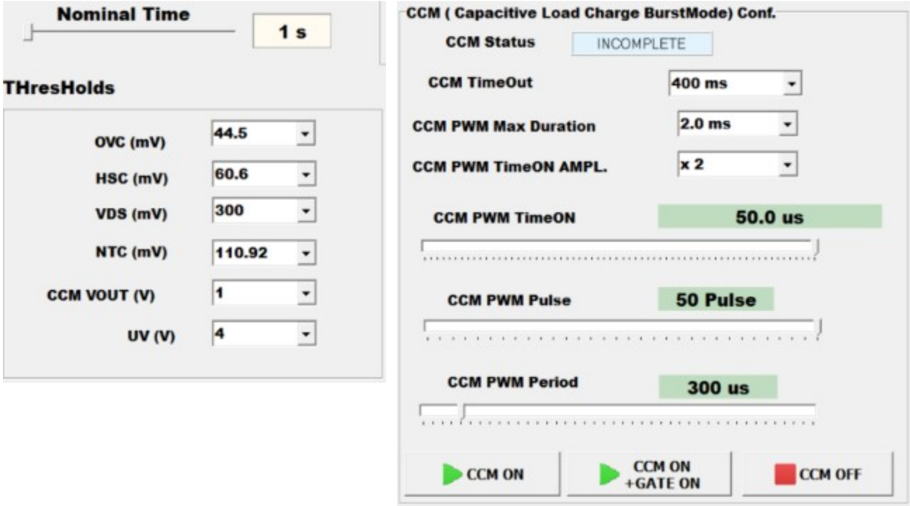
It adopts the same setup as trial Q2 but VB is set at 48 V.

- **VB = 48 V**
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- **OVC_THR = VOC_THRS_24 → 44.5 mV**
- **HSC_THR = VHSC_THRS_8 → 60.6 mV**
- T_NOM = T_NOM$_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- **CCM_PWM_SC_T_NB = 50 pulses**
- CCM_PWM_T = 300 µs
- **CCM_TIMEOUT = 400 ms**
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 89

Figure 89. **CCM configuration and result from GUI for test setup R1**



Nominal Time: 1 s

THresHolds
OVC (mV): 44.5
HSC (mV): 60.6
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

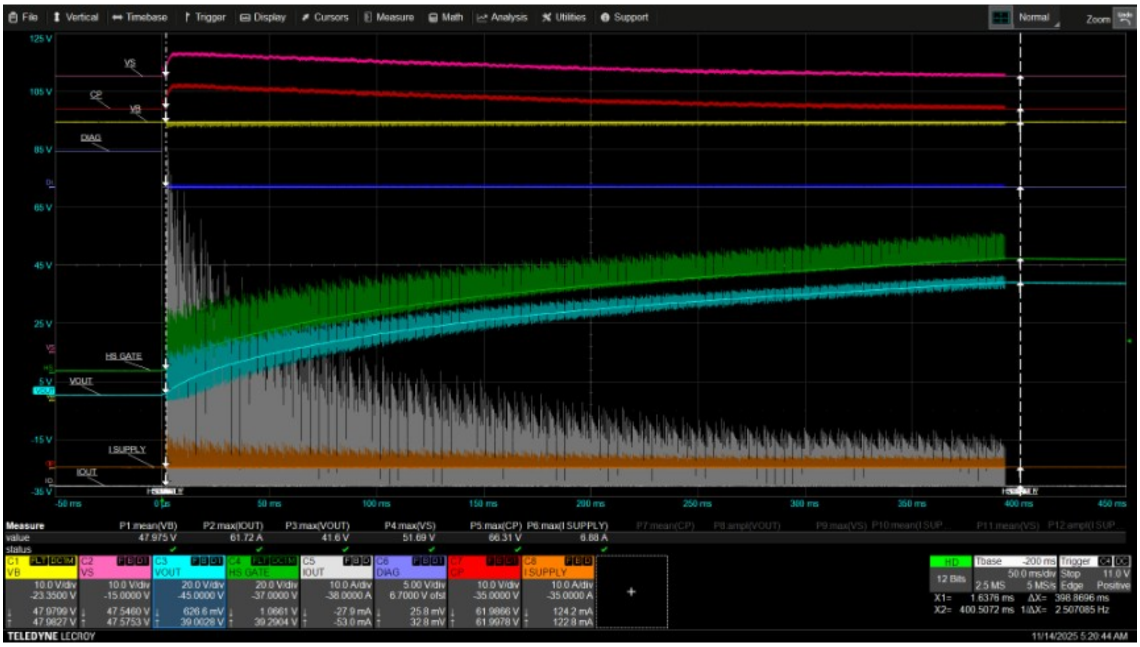
CCM ( Capacitive Load Charge BurstMode) Conf.
CCM Status: INCOMPLETE
CCM TimeOut: 400 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 50 Pulse
CCM PWM Period: 300 us

**Result R1:**

With the mentioned setup R1, the 4.7 mF C$_{LOAD}$ is not charged in 2 ms (start phase) + 398 ms (standard phase). VOUT reaches only 39 V after 400 ms due to the VB set at 48 V vs the 13 V used in trial Q2.

Please note that the usage of VB = 48 V involves IOUT max at 61.7 A and VS max at 51.7 V.

Figure 90. Waveforms acquired during CCM with setup R1



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:mean(CP) | P8:ampl(VOUT) | P9:max(VS) | P10:mean(I SUP... | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 47.975 V | 61.72 A | 41.6 V | 51.69 V | 66.31 V | 6.88 A | | | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 10.0 V/div | 10.0 V/div | 20.0 V/div | 20.0 V/div | 10.0 A/div | 5.00 V/div | 10.0 V/div | 10.0 A/div |
| -23.3500 V | -15.0000 V | -45.0000 V | -37.0000 V | -38.0000 A | 6.7000 V ofst | -35.0000 V | -35.0000 A |
| ↓ 47.9799 V | ↓ 47.5460 V | ↓ 626.6 mV | ↓ 1.0661 V | ↓ -27.9 mA | ↓ 25.8 mV | ↓ 61.9866 V | ↓ 124.2 mA |
| ↑ 47.9827 V | ↑ 47.5753 V | ↑ 39.0028 V | ↑ 39.2904 V | ↑ -53.0 mA | ↑ 32.8 mV | ↑ 61.9978 V | ↑ 122.8 mA |

HD 12 Bits
Tbase -200 ms 50.0 ms/div 2.5 MS 5 MS/s
Trigger C4 DC Stop 11.0 V Edge Positive
X1= 1.6376 ms ΔX= 398.8696 ms
X2= 400.5072 ms 1/ΔX= 2.507085 Hz
11/14/2025 5:20:44 AM

## 5.9.6 Trial Setup R2

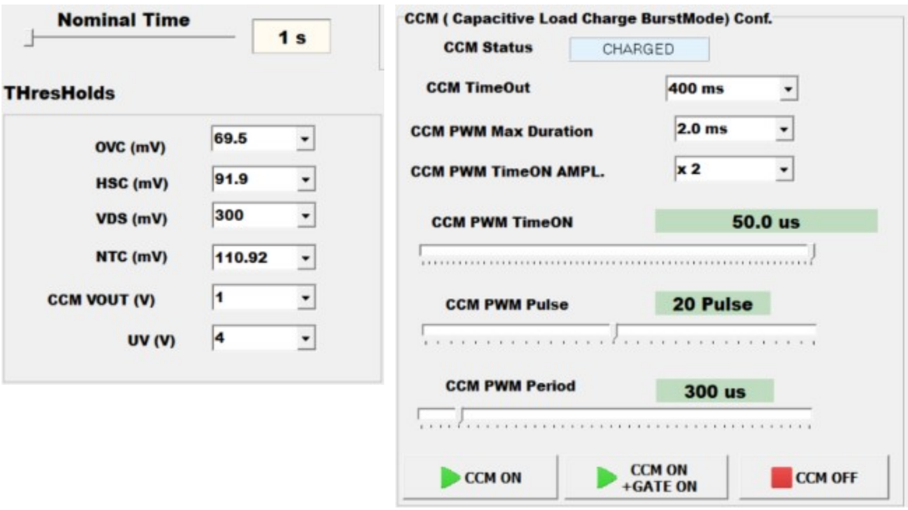
It adopts the same setup as trial R1, but the OVC and HSC thresholds are set at higher levels, allowing the $C_{LOAD}$ charge to be successfully completed.

- **VB = 48 V**
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 μF and $C_S$ = 20 μF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- **OVC_THR = VOC_THRS_29 → 69.5 mV**
- **HSC_THR = VHSC_THRS_11 → 91.9 mV**
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 μs
- CCM_PWM_TON_MF = 2 x
- **CCM_PWM_SC_T_NB = 50 pulses**
- CCM_PWM_T = 300 μs
- **CCM_TIMEOUT = 400 ms**
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 91

Figure 91. **CCM configuration and result from GUI for Test setup R2**



Nominal Time: 1 s

THresHolds

OVC (mV): 69.5
HSC (mV): 91.9
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

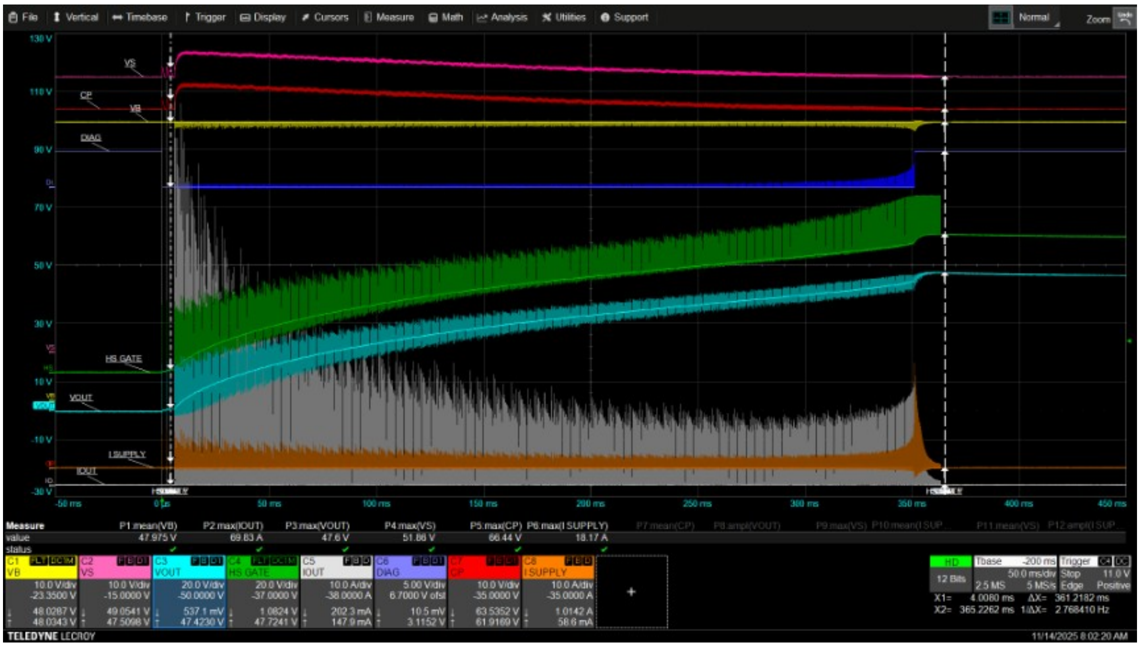
CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 400 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

**Result R2:**

With the mentioned setup R2, the 4.7 mF $C_{LOAD}$ is charged in 6 ms (start phase) + 359 ms (standard phase). Please note that this setup involves IOUT max at 69.8 A and VS max at 51.8 V confirming that selected $C_{IN}$ is also very safe in this heavy setup to limit the boost effect.

Figure 92. **Waveforms acquired during CCM with setup R2**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 47.975 V | 69.83 A | 47.6 V | 51.86 V | 66.44 V | 18.17 A |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

## 5.10 Effect of CLOAD = 6.9 mF

### 5.10.1 Trial Setup S

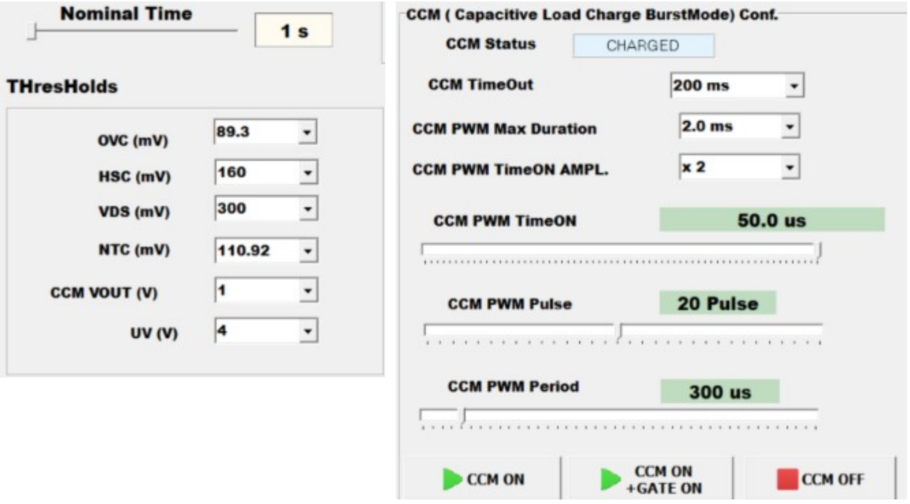
It adopts the same setup as trial E1 with the $C_{LOAD}$ increased at 6.9 mF vs 4.7 mF.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = 6.9 mF (measured 6.69 mF)**
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 93

Figure 93. **CCM configuration and result from GUI for test setup S**



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

**Result S:**

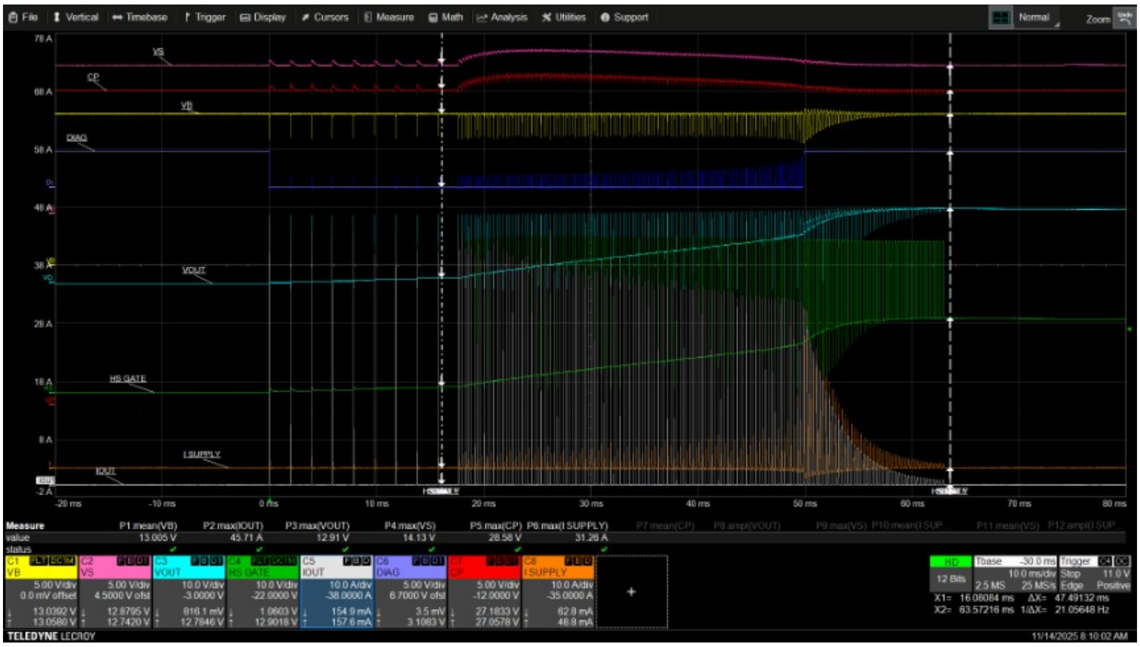
With the mentioned setup S, the 6.9 mF $C_{LOAD}$ is charged in 18 ms (start phase) + 48.5 ms (standard phase).

Using the same setup of trial E1, the overall $t_{CHARGE}$ moves from 43.9 ms to 63.5 ms due to the $C_{LOAD}$ that was increased from 4.7 mF to 6.9 mF.

Also, IOUT max and VS max are impacted:

- IOUT max at 45.7 A (trial S) vs 42.6 A (trial E1)
- VS max at 14.1 V (trial S) vs 13.8 V (trial E1)

Figure 94. **Waveforms acquired during CCM with setup S**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:mean(CP) | P8:ampl(VOUT) | P9:max(VS) | P10:mean(I SUP... | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 13.005 V | 45.71 A | 12.91 V | 14.13 V | 28.58 V | 31.28 A | | | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 0.0 mV offset | 4.5000 V ofst | -3.0000 V | -22.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -35.0000 A |
| ↓ 13.0302 V | ↓ 12.8795 V | ↓ 816.1 mV | ↓ 1.0603 V | ↓ 154.9 mA | ↓ 3.5 mV | ↓ 27.1833 V | ↓ 62.8 mA |
| ↑ 13.0580 V | ↑ 12.7420 V | ↑ 12.7846 V | ↑ 12.9018 V | ↑ 157.6 mA | ↑ 3.1083 V | ↑ 27.0578 V | ↑ 48.8 mA |

HD 12 Bits
Tbase -30.0 ms
10.0 ms/div
2.5 MS 25 MS/s
Trigger C4 DC
Stop 11.0 V
Edge Positive
X1= 16.08084 ms ΔX= 47.49132 ms
X2= 63.57216 ms 1/ΔX= 21.05648 Hz
11/14/2025 8:10:02 AM

## 5.10.2 Trial Setup T

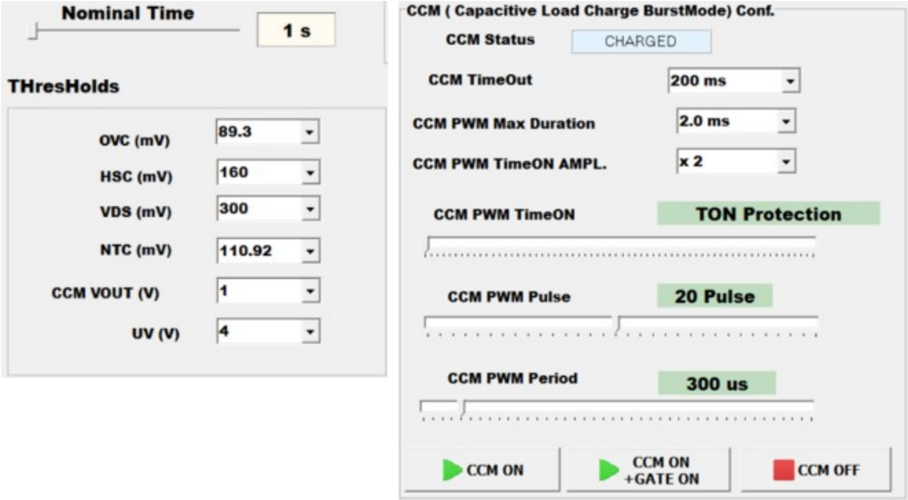
It adopts the same setup as trial S with the CCM_PWM_TON set in TON protection to reduce $t_{CHARGE}$.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = 6.9 mF (measured 6.69 mF)**
- $C_{IN}$ = 314 μF and $C_S$ = 20 μF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- **CCM_PWM_TON = TON protection**
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 μs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 95

Figure 95. CCM configuration and result from GUI for test setup T



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: TON Protection
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

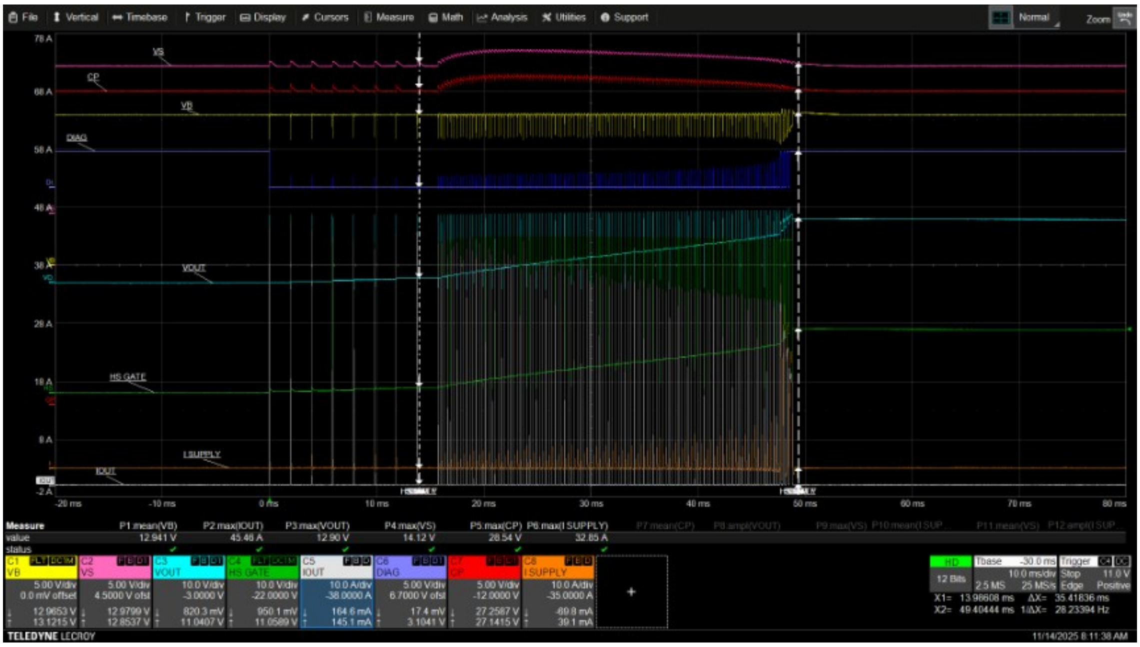
**Result T:**

With the mentioned setup T, the 6.9 mF $C_{LOAD}$ is charged in 16 ms (start phase) + 33.4 ms (standard phase).

The setting of TON protection allows the overall $t_{CHARGE}$ from 63.5 ms (trial S) to 49.4 ms (trial T).

Using the same setup of trial M, the overall $t_{CHARGE}$ moves from 33.6 ms to 49.4 ms due to the increase of $C_{LOAD}$ from 4.7 mF (trial M) to 6.9 mF (trial T).

Figure 96. Waveforms acquired during CCM with setup T



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 12.941 V | 45.46 A | 12.90 V | 14.12 V | 28.54 V | 32.85 A |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 0.0 mV offset | 4.5000 V ofst | -3.0000 V | -22.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -35.0000 A |
| ↓ 12.9653 V | ↓ 12.9799 V | ↓ 820.3 mV | ↓ 950.1 mV | ↓ 164.6 mA | ↓ 17.4 mV | ↓ 27.2587 V | ↓ -69.8 mA |
| ↑ 13.1215 V | ↑ 12.8537 V | ↑ 11.0407 V | ↑ 11.0589 V | ↑ 145.1 mA | ↑ 3.1041 V | ↑ 27.1415 V | ↑ 39.1 mA |

HD 12 Bits
Tbase -30.0 ms, 10.0 ms/div, 2.5 MS, 25 MS/s
Trigger C4 DC, Stop 11.0 V, Edge Positive
X1= 13.98608 ms ΔX= 35.41836 ms
X2= 49.40444 ms 1/ΔX= 28.23394 Hz

## 5.11 Effect of Junction Temperature on CCM

### 5.11.1 Trial Setup U

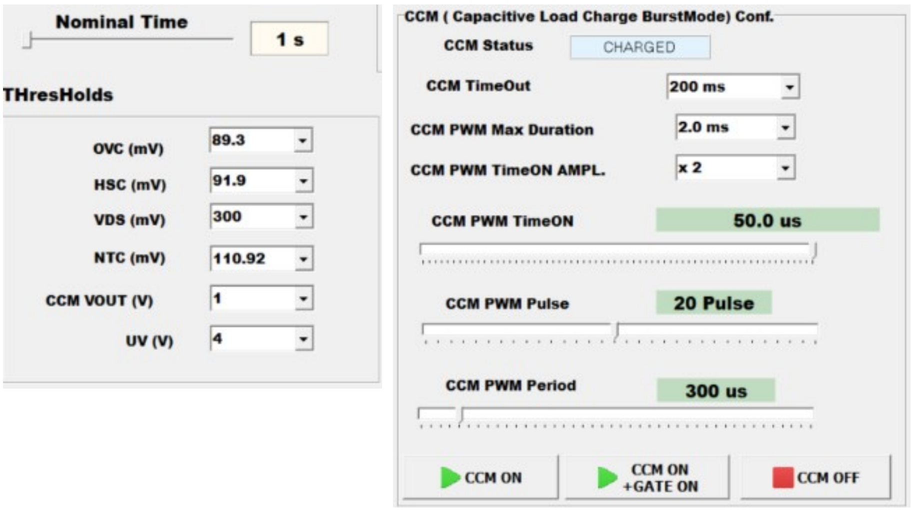
It adopts the same setup as trial E1, with HSC_THR modified from the max level 160 mV to 91.9 mV.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = 4.7 mF (measured 4.52 mF)**
- $C_{IN}$ = 314 μF and $C_S$ = 20 μF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- **HSC_THR = VHSC_THRS_11 → 91.9 mV**
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 μs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 μs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 97

Figure 97. **CCM configuration and result from GUI for test setup U**



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 91.9
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

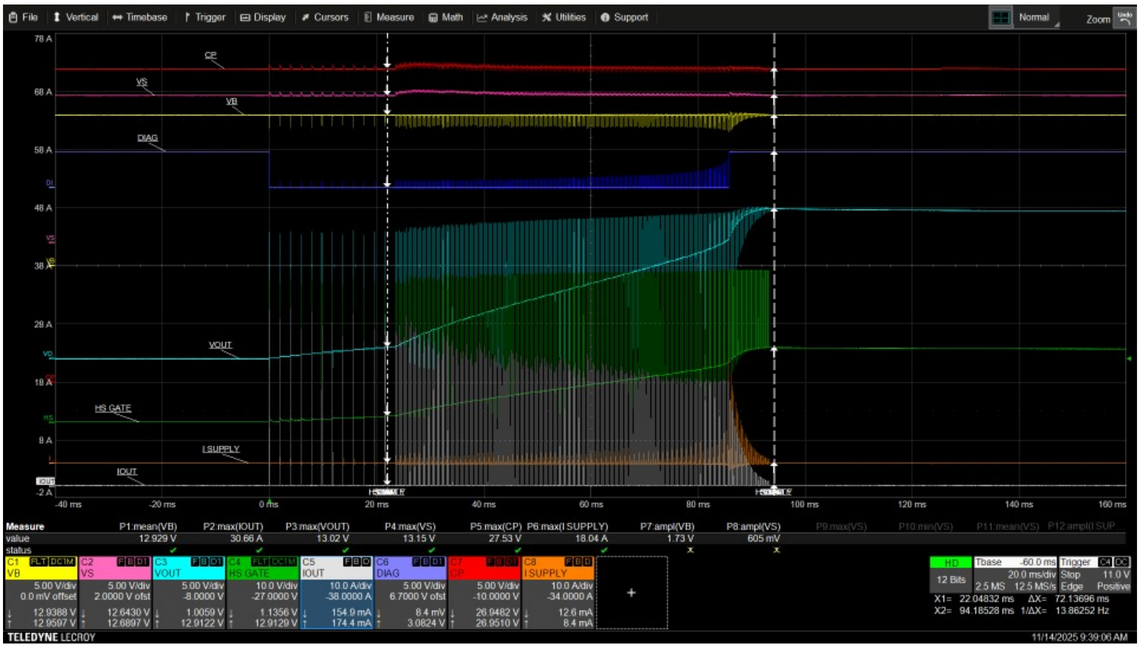
CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

**Result U:**

With the mentioned setup U, the 4.7 mF $C_{LOAD}$ is charged in 24 ms (start phase) + 70.1 ms (standard phase).

Figure 98. Waveforms acquired during CCM with setup U



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.929 V | 30.66 A | 13.02 V | 13.15 V | 27.53 V | 18.04 A | 1.73 V | 605 mV | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✗ | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| FLT DC1M | F B D1 | F B D1 | FLT DC1M | F B D | F B D1 | F B D1 | F B D |
| 5.00 V/div | 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 0.0 mV offset | 2.0000 V ofst | -8.0000 V | -27.0000 V | -38.0000 A | 6.7000 V ofst | -10.0000 V | -34.0000 A |
| ↓ 12.9388 V | ↓ 12.6430 V | ↓ 1.0059 V | ↓ 1.1356 V | ↓ 154.9 mA | ↓ 8.4 mV | ↓ 26.9482 V | ↓ 12.6 mA |
| ↑ 12.9597 V | ↑ 12.6897 V | ↑ 12.9122 V | ↑ 12.9129 V | ↑ 174.4 mA | ↑ 3.0824 V | ↑ 26.9510 V | ↑ 8.4 mA |

HD 12 Bits
Tbase -60.0 ms
20.0 ms/div
2.5 MS 12.5 MS/s
Trigger C4 DC
Stop 11.0 V
Edge Positive
X1= 22.04832 ms ΔX= 72.13696 ms
X2= 94.18528 ms 1/ΔX= 13.86252 Hz
11/14/2025 9:39:06 AM

## 5.11.2 Trial Setup V

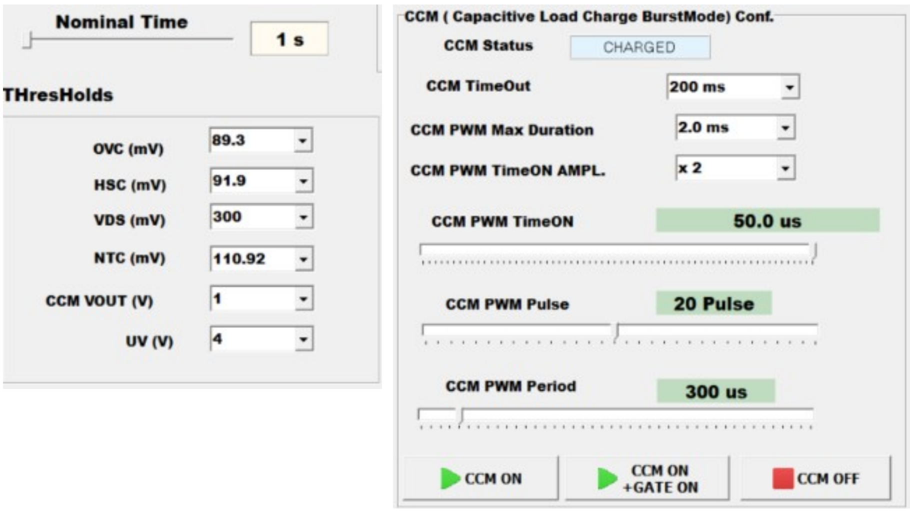
It adopts the same setup as trial U, with the ambient temperature modified to hot.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~90°C generating TJ ~100°C
- **$C_{LOAD}$ = 4.7 mF (measured 4.52 mF)**
- $C_{IN}$ = 314 μF and $C_S$ = 20 μF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- **HSC_THR = VHSC_THRS_11 → 91.9 mV**
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 μs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 μs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 99

Figure 99. **CCM configuration and result from GUI for test setup V**



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 91.9
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

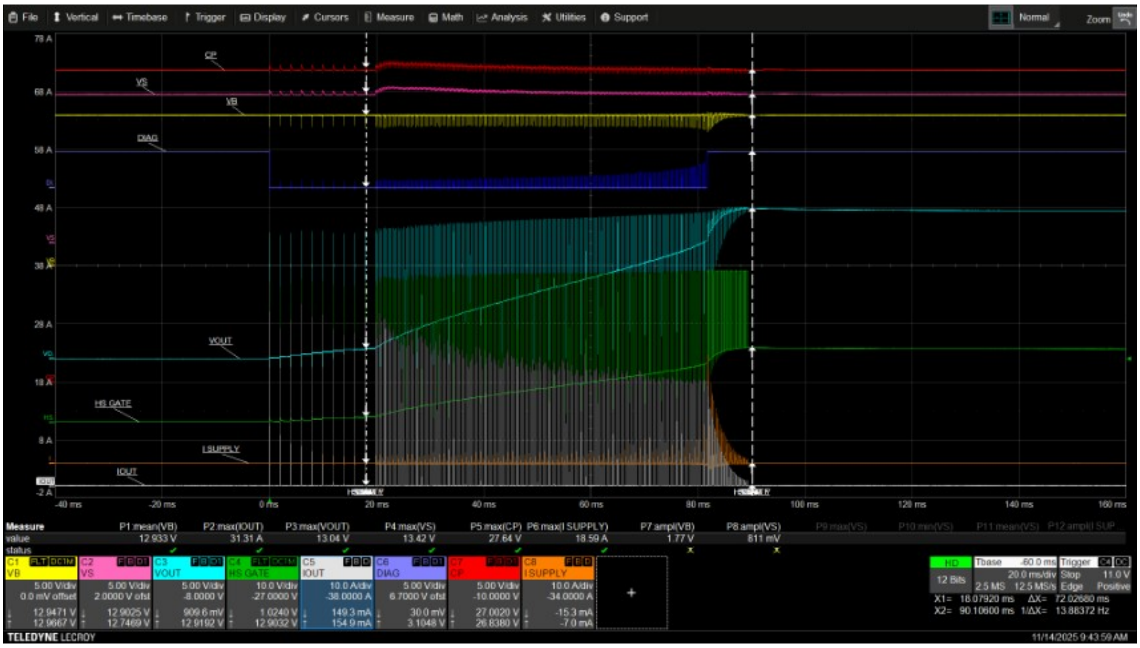
**Result V:**

With the mentioned setup V, the 4.7 mF $C_{LOAD}$ is charged in 20 ms (start phase) + 70 ms (standard phase).

The temperature of gate controller device has a negligible effect on $t_{CHARGE}$ that can be affected by the temperature of the $C_{LOAD}$ and the temperature of the external MOSFET.

In the reported examples U vs V, the VNF1248F device was heated by the hot air flow over the device that is very close to the MOSFET while the $C_{LOAD}$ is far from the used circuit. In this specific example, the trial V involves a slightly faster $t_{CHARGE}$ vs trial U because the impact of a higher current peak in the start phase; in fact, we observed ten pulses with max IOUT = 31.3 A in trial V vs 12 pulses with max IOUT = 30.6 A in trial U.

Figure 100. **Waveforms acquired during CCM with setup V**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.933 V | 31.31 A | 13.04 V | 13.42 V | 27.64 V | 18.59 A | 1.77 V | 811 mV | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | x | x | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 0.0 mV offset | 2.0000 V ofst | -8.0000 V | -27.0000 V | -38.0000 A | 6.7000 V ofst | -10.0000 V | -34.0000 A |
| ↓ 12.9471 V | ↓ 12.9025 V | ↓ 909.6 mV | ↓ 1.0240 V | ↓ 149.3 mA | ↓ 30.0 mV | ↓ 27.0020 V | ↓ -15.3 mA |
| ↑ 12.9667 V | ↑ 12.7469 V | ↑ 12.9192 V | ↑ 12.9032 V | ↑ 154.9 mA | ↑ 3.1048 V | ↑ 26.8380 V | ↑ -7.0 mA |

HD 12 Bits
Tbase -60.0 ms, 20.0 ms/div, 2.5 MS, 12.5 MS/s
Trigger C4 DC, Stop 11.0 V, Edge Positive
X1= 18.07920 ms ΔX= 72.02680 ms
X2= 90.10600 ms 1/ΔX= 13.88372 Hz
11/14/2025 9:43:59 AM

## 5.12 Effect of $R_{SHUNT}$ on CCM

### 5.12.1 Trial Setup W

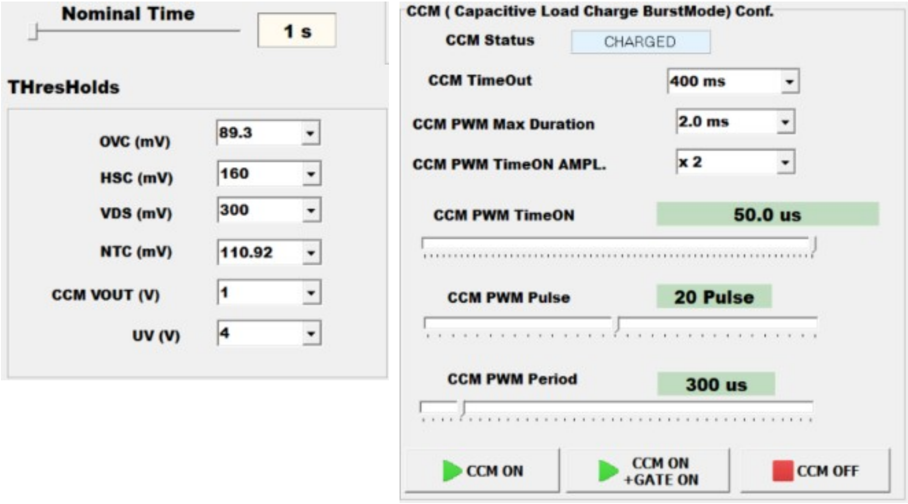
It adopts the same setup as trial E1 with the $R_{SHUNT}$ increased at 20 mΩ vs 5 mΩ and the CCM timeout increased at 400 ms vs 200 ms.

- VB = 13 V
- **$R_{SHUNT}$ = 20 mΩ**
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 μF and $C_S$ = 20 μF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 μs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 μs
- **CCM_TIMEOUT = 400 ms**
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 101

Figure 101. CCM configuration and result from GUI for test setup W



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 400 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

**Result W:**

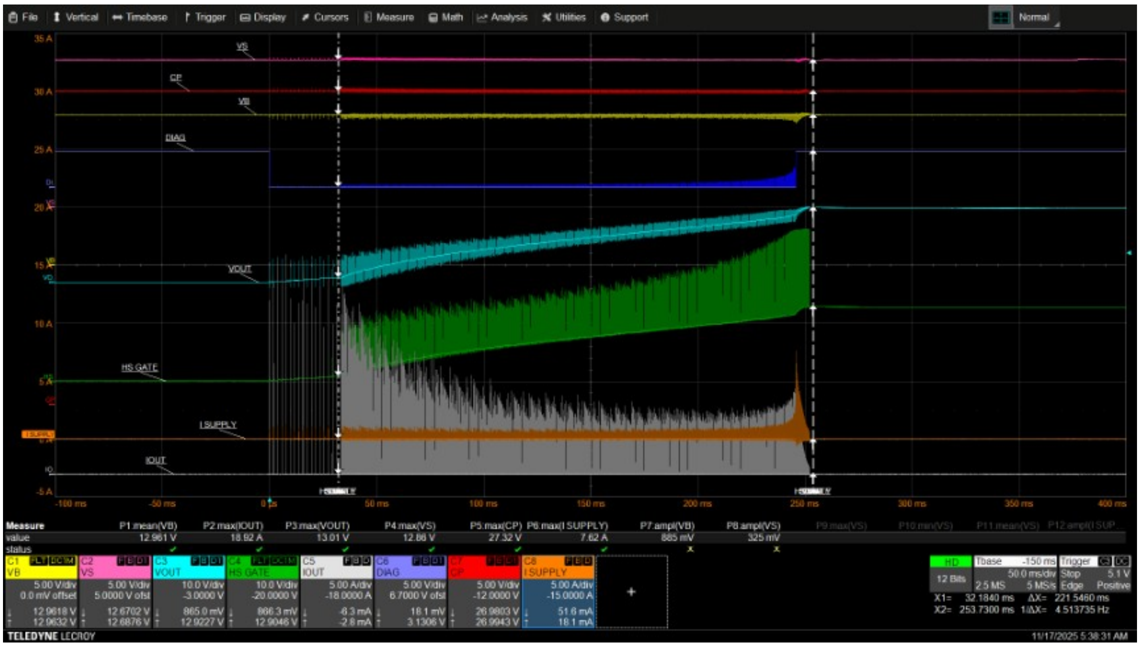
With the mentioned setup W, the 4.7 mF $C_{LOAD}$ is charged in 34 ms (start phase) + 219.5 ms (standard phase).

The CCM timeout is increased at 400 ms to complete the charge.

The increase of $R_{SHUNT}$ from 5 mΩ to 20 mΩ involves reading from the ADC of current level four times greater.

Considering that the setup is the same as the one adopted in trial E1, we see IOUT max moving from 42.6 A with $R_{SHUNT}$ = 5 mΩ to 18.9 A with $R_{SHUNT}$ = 20 mΩ. The $t_{CHARGE}$ time increases from 43.9 ms to 253.5 ms.

Figure 102. Waveforms acquired during CCM with setup W



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP… |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.961 V | 18.92 A | 13.01 V | 12.86 V | 27.32 V | 7.62 A | 885 mV | 325 mV | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | x | x | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 5.00 A/div | 5.00 V/div | 5.00 V/div | 5.00 A/div |
| 0.0 mV offset | 5.0000 V ofst | -3.0000 V | -20.0000 V | -18.0000 A | 6.7000 V ofst | -12.0000 V | -15.0000 A |
| ↓ 12.9618 V | ↓ 12.6702 V | ↓ 865.0 mV | ↓ 866.3 mV | ↓ -6.3 mA | ↓ 18.1 mV | ↓ 26.9803 V | ↓ 51.6 mA |
| ↑ 12.9632 V | ↑ 12.6876 V | ↑ 12.9227 V | ↑ 12.9046 V | ↑ -2.8 mA | ↑ 3.1306 V | ↑ 26.9943 V | ↑ 18.1 mA |

HD 12 Bits
Tbase -150 ms
50.0 ms/div
2.5 MS 5 MS/s
Trigger DC
Stop 5.1 V
Edge Positive
X1= 32.1840 ms ΔX= 221.5460 ms
X2= 253.7300 ms 1/ΔX= 4.513735 Hz

11/17/2025 5:38:31 AM

## 5.13 Effect of TNOM on CCM

### 5.13.1 Trial Setup X1

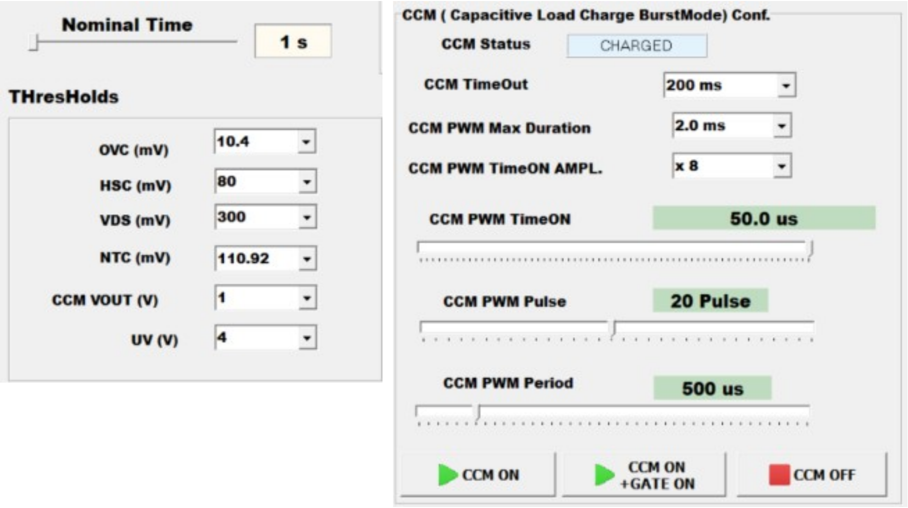
It adopts a dedicated setup to point out the effect of $T_{NOM}$ set at 1 s (min value).

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_3 → 10.4 mV
- HSC_THR = VHSC_THRS_10 → 80 mV
- **T_NOM = T_NOM$_{MIN}$ → 1 s**
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 8 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 500 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 103

Figure 103. **CCM configuration and result from GUI for test setup X1**



Nominal Time: 1 s

THresHolds

OVC (mV): 10.4
HSC (mV): 80
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

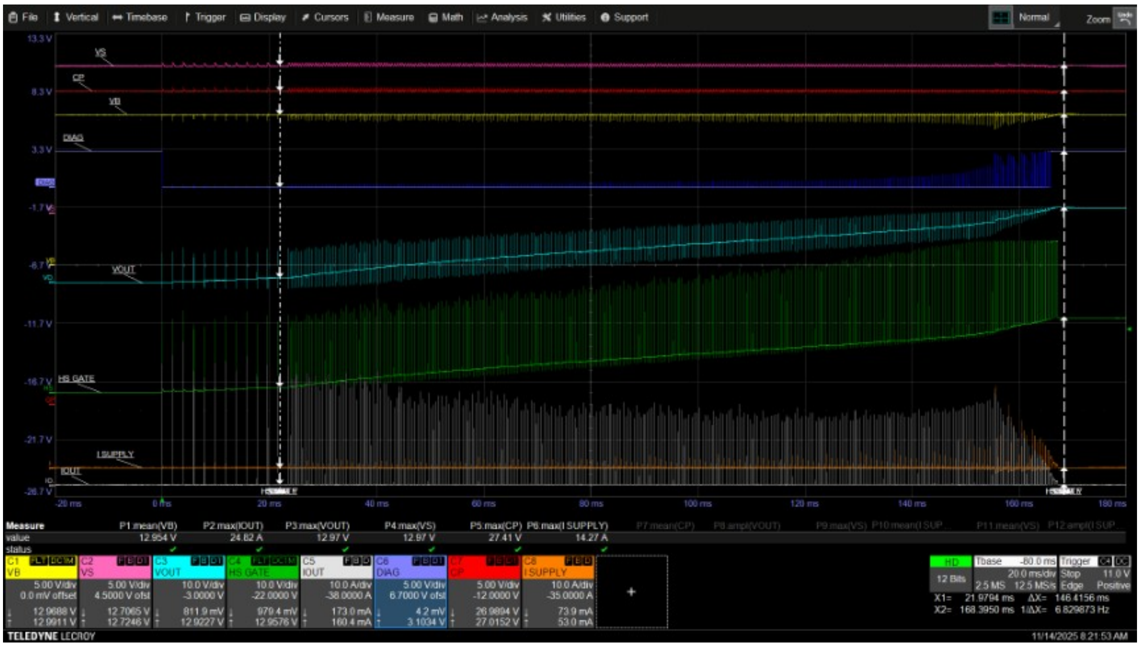
CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 8
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 500 us

**Result X1:**

With setup X1, the 4.7 mF $C_{LOAD}$ is charged in 24 ms (start phase) + 144.4 ms (standard phase).

Figure 104. **Waveforms acquired during CCM with setup X1**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) |
|---|---|---|---|---|---|---|
| value | 12.954 V | 24.82 A | 12.97 V | 12.97 V | 27.41 V | 14.27 A |

Tbase -80.0 ms, 20.0 ms/div, 2.5 MS, 12.5 MS/s
Trigger Stop, 11.0 V, Edge, Positive
X1= 21.9794 ms ΔX= 146.4156 ms
X2= 168.3950 ms 1/ΔX= 6.829873 Hz

## 5.13.2 Trial Setup X2

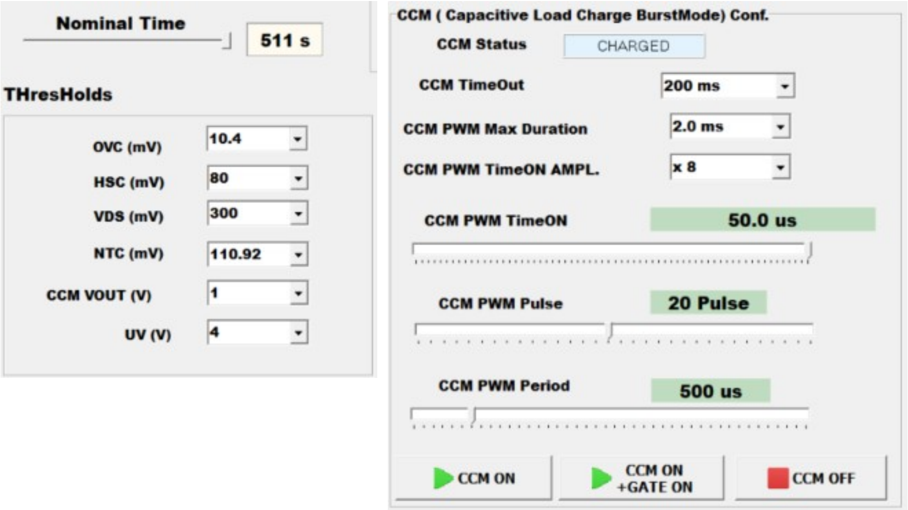
It adopts the the same setup as trial X1 with $T_{NOM}$ set at 511 s (max value) vs 1 s (min value).

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_3 → 10.4 mV
- HSC_THR = VHSC_THRS_10 → 80 mV
- **T_NOM = T_NOM$_{MAX}$ → 511 s**
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 8 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 500 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 105

Figure 105. **CCM configuration and result from GUI for test setup X2**



Nominal Time: 511 s

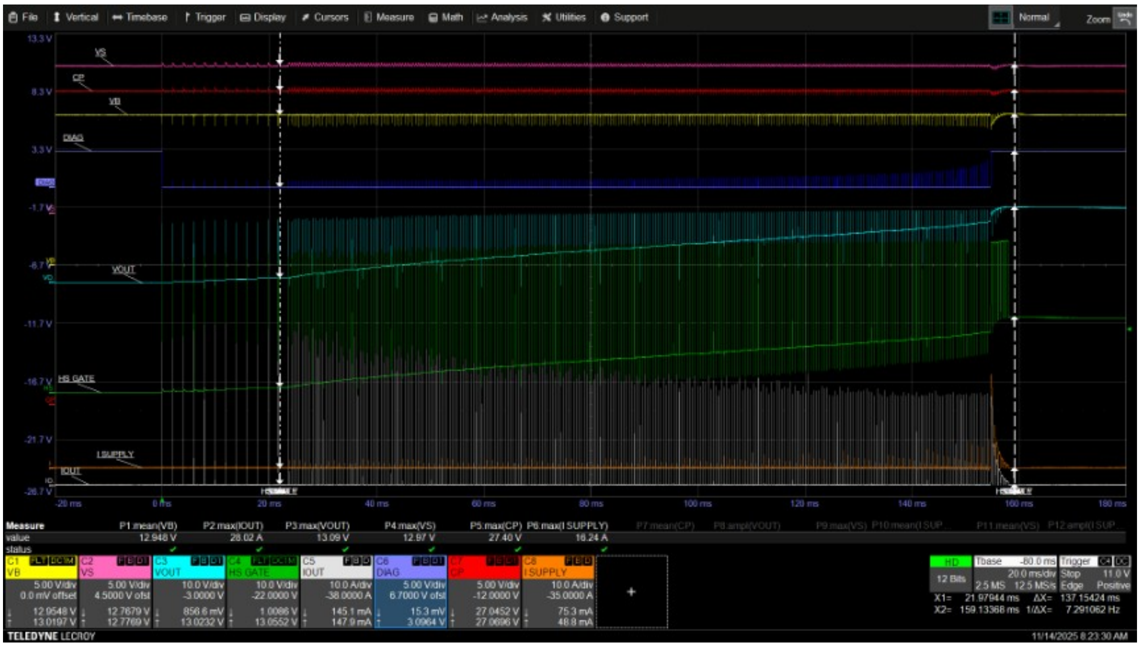
THresHolds
OVC (mV): 10.4
HSC (mV): 80
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.
CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 8
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 500 us

**Result X2:**

With the mentioned setup X2, the 4.7 mF C$_{LOAD}$ is charged in 24 ms (start phase) + 135.1 ms (standard phase). The T$_{NOM}$ set at max (trial X2 at 511 s) vs min (trial X1 at 1 s) value involves a faster t$_{CHARGE}$ due to its contribution in I$^2$t fuse protection triggering in the standard charging phase. Max T$_{NOM}$ involves a longer time ON of HS_GATE because a longer time is needed to trigger I$^2$t protection. In any case, the impact on the overall t$_{CHARGE}$ is very little and it is visible by the slopes of the VOUT signal during the standard phase and by the final portion highlighted in yellow in the below image where the I$^2$t protection is triggered by OVC assuring longer time ON of HS_GATE.

Figure 106. **Waveforms acquired during CCM with setup X2**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:mean(CP) | P8:ampl(VOUT) | P9:max(VS) | P10:mean(I SUP... | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.948 V | 28.02 A | 13.09 V | 12.97 V | 27.40 V | 16.24 A | | | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 0.0 mV offset | 4.5000 V ofst | -3.0000 V | -22.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -35.0000 A |
| ↓ 12.9548 V | ↓ 12.7679 V | ↓ 856.6 mV | ↓ 1.0086 V | ↓ 145.1 mA | ↓ 15.3 mV | ↓ 27.0452 V | ↓ 75.3 mA |
| ↑ 13.0197 V | ↑ 12.7769 V | ↑ 13.0232 V | ↑ 13.0552 V | ↑ 147.9 mA | ↑ 3.0964 V | ↑ 27.0696 V | ↑ 48.8 mA |

HD 12 Bits
Tbase -80.0 ms 20.0 ms/div 2.5 MS 12.5 MS/s
Trigger C4 DC Stop 11.0 V Edge Positive
X1= 21.97944 ms ΔX= 137.15424 ms
X2= 159.13368 ms 1/ΔX= 7.291062 Hz
11/14/2025 8:23:30 AM

## 5.14 CCM attempt on OUT shorted to GND

### 5.14.1 Trial Setup Y

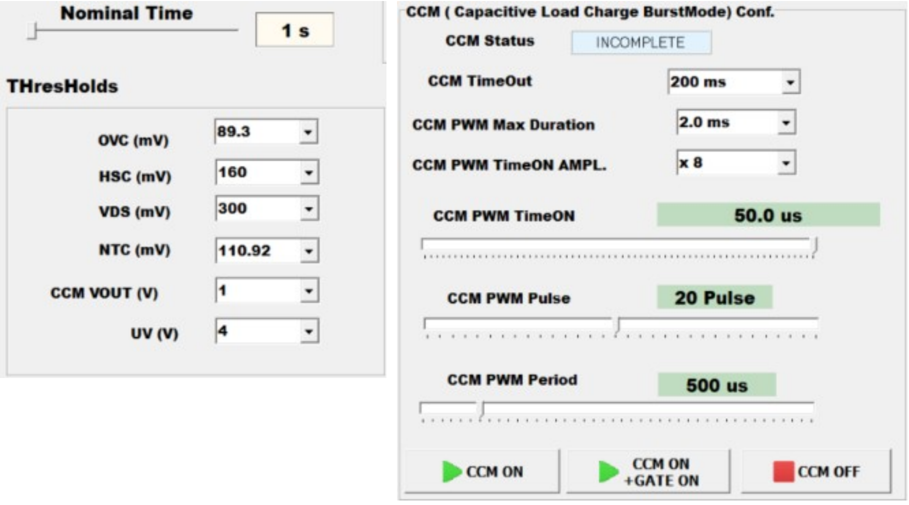
It adopts a dedicated setup to point out the consequences of a capacitive charging mode launched with OUT shorted to GND.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = short circuit between OUT and GND**
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 8 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 500 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 107

Figure 107. CCM configuration and result from GUI for test setup Y



**Nominal Time**: 1 s

**THresHolds**

| | |
|---|---|
| OVC (mV) | 89.3 |
| HSC (mV) | 160 |
| VDS (mV) | 300 |
| NTC (mV) | 110.92 |
| CCM VOUT (V) | 1 |
| UV (V) | 4 |

**CCM ( Capacitive Load Charge BurstMode) Conf.**

| | |
|---|---|
| CCM Status | INCOMPLETE |
| CCM TimeOut | 200 ms |
| CCM PWM Max Duration | 2.0 ms |
| CCM PWM TimeON AMPL. | x 8 |
| CCM PWM TimeON | 50.0 us |
| CCM PWM Pulse | 20 Pulse |
| CCM PWM Period | 500 us |

**Result Y:**
With the mentioned setup Y, the CCM is aborted after 20 pulses corresponding to 40 ms of the start phase because VOUT remained at 0 V so that no transition to the standard phase is allowed.

Figure 108. Waveforms acquired during CCM with setup Y

| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:mean(CP) | P8:ampl(VOUT) | P9:max(VS) | P10:mean(I SUP... | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.957 V | 48.79 A | 11.99 V | 13.10 V | 27.65 V | 8.56 A | | | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 HS GATE | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 0.0 mV offset | 4.5000 V ofst | -3.0000 V | -22.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -35.0000 A |
| ↓ 13.0232 V | ↓ 13.0350 V | ↓ -170.2 mV | ↓ 615.2 mV | ↓ 147.9 mA | ↓ 21.6 mV | ↓ 27.2642 V | ↓ -40.5 mA |
| ↑ 12.9715 V | ↑ 12.6821 V | ↑ -152.1 mV | ↑ 8.4 mV | ↑ 173.0 mA | ↑ 3.0685 V | ↑ 26.9985 V | ↑ 86.5 mA |

HD 12 Bits
Tbase -20.0 ms 5.00 ms/div 2.5 MS 50 MS/s
Trigger C4 DC Stop 11.0 V Edge Positive
X1= 37.52514 ms ΔX= 2.51340 ms
X2= 40.03854 ms 1/ΔX= 397.867 Hz
11/14/2025 8:30:40 AM

## 5.15 Examples of CCM completed or stopped before capacitance charge completion

### 5.15.1 Trial Setup Z1

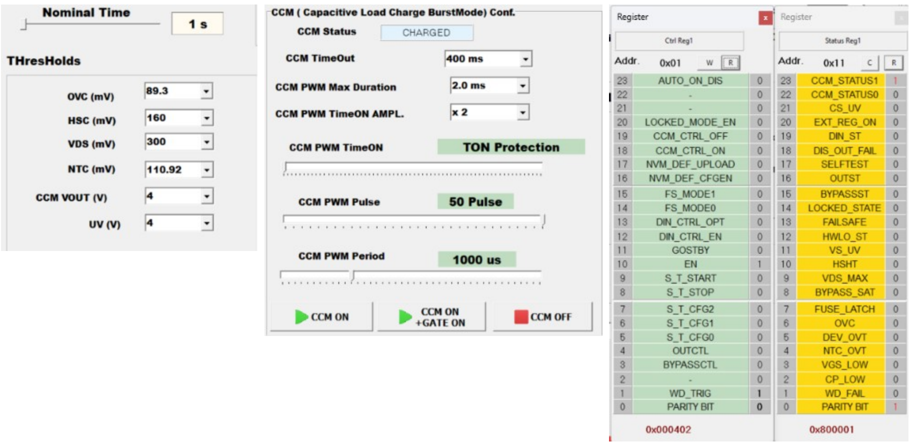
It adopts a dedicated setup.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- **CCM_VOUT_THR = 4 V**
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = TON protection
- CCM_PWM_TON_MF = 2 x
- **CCM_PWM_SC_T_NB = 50 pulses**
- **CCM_PWM_T = 1000 µs**
- **CCM_TIMEOUT = 400 ms**
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 109

Figure 109. **CCM configuration and result from GUI for test setup Z1**



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 4
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 400 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: TON Protection
CCM PWM Pulse: 50 Pulse
CCM PWM Period: 1000 us

Ctrl Reg1 — Addr. 0x01

| Bit | Name | Value |
|---|---|---|
| 23 | AUTO_ON_DIS | 0 |
| 22 | - | 0 |
| 21 | - | 0 |
| 20 | LOCKED_MODE_EN | 0 |
| 19 | CCM_CTRL_OFF | 0 |
| 18 | CCM_CTRL_ON | 0 |
| 17 | NVM_DEF_UPLOAD | 0 |
| 16 | NVM_DEF_CFGEN | 0 |
| 15 | FS_MODE1 | 0 |
| 14 | FS_MODE0 | 0 |
| 13 | DIN_CTRL_OPT | 0 |
| 12 | DIN_CTRL_EN | 0 |
| 11 | GOSTBY | 0 |
| 10 | EN | 1 |
| 9 | S_T_START | 0 |
| 8 | S_T_STOP | 0 |
| 7 | S_T_CFG2 | 0 |
| 6 | S_T_CFG1 | 0 |
| 5 | S_T_CFG0 | 0 |
| 4 | OUTCTL | 0 |
| 3 | BYPASSCTL | 0 |
| 2 | - | 0 |
| 1 | WD_TRIG | 1 |
| 0 | PARITY BIT | 0 |

0x000402

Status Reg1 — Addr. 0x11

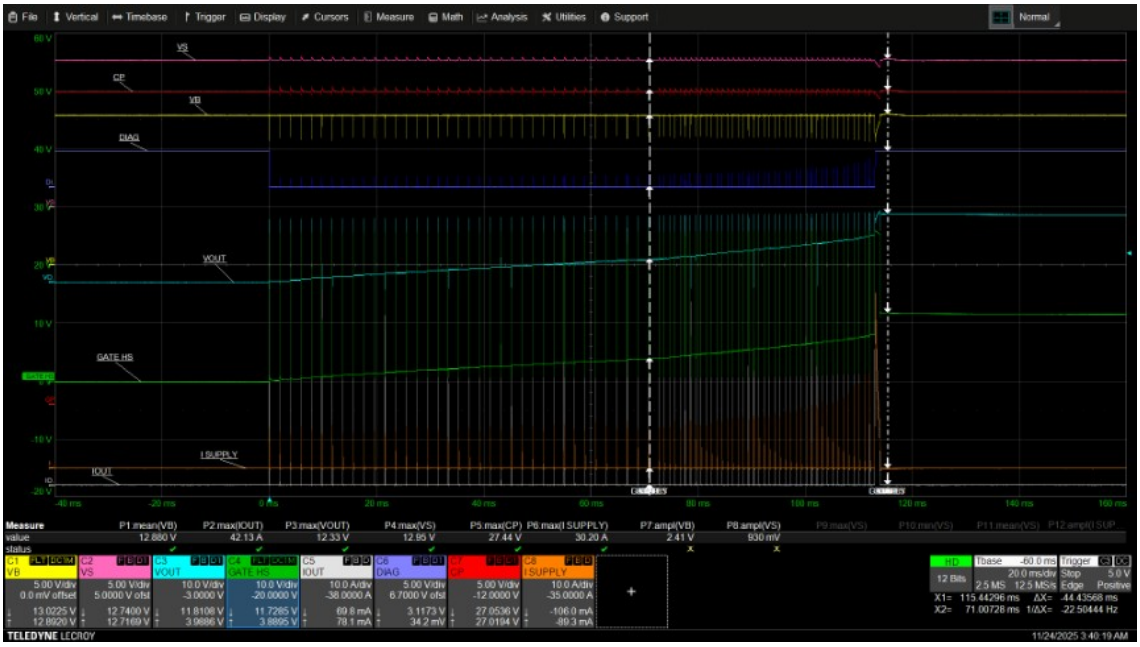
| Bit | Name | Value |
|---|---|---|
| 23 | CCM_STATUS1 | 1 |
| 22 | CCM_STATUS0 | 0 |
| 21 | CS_UV | 0 |
| 20 | EXT_REG_ON | 0 |
| 19 | DIN_ST | 0 |
| 18 | DIS_OUT_FAIL | 0 |
| 17 | SELFTEST | 0 |
| 16 | OUTST | 0 |
| 15 | BYPASSST | 0 |
| 14 | LOCKED_STATE | 0 |
| 13 | FAILSAFE | 0 |
| 12 | HWLO_ST | 0 |
| 11 | VS_UV | 0 |
| 10 | HSHT | 0 |
| 9 | VDS_MAX | 0 |
| 8 | BYPASS_SAT | 0 |
| 7 | FUSE_LATCH | 0 |
| 6 | OVC | 0 |
| 5 | DEV_OVT | 0 |
| 4 | NTC_OVT | 0 |
| 3 | VGS_LOW | 0 |
| 2 | CP_LOW | 0 |
| 1 | WD_FAIL | 0 |
| 0 | PARITY BIT | 1 |

0x800001

**Result Z1:**

With the mentioned setup Z1, the 4.7 mF $C_{LOAD}$ is charged in 74 ms (start phase) + 41.4 ms (standard phase).

Figure 110. **Waveforms acquired during CCM with setup Z1**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.880 V | 42.13 A | 12.33 V | 12.95 V | 27.44 V | 30.20 A | 2.41 V | 930 mV | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | x | x | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 GATE HS | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 0.0 mV offset | 5.0000 V ofst | -3.0000 V | -20.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -35.0000 A |
| ↓ 13.0225 V | ↓ 12.7400 V | ↓ 11.8108 V | ↓ 11.7285 V | ↓ 69.8 mA | ↓ 3.1173 V | ↓ 27.0536 V | ↓ -106.0 mA |
| ↑ 12.8920 V | ↑ 12.7169 V | ↑ 3.9886 V | ↑ 3.8895 V | ↑ 78.1 mA | ↑ 34.2 mV | ↑ 27.0194 V | ↑ -89.3 mA |

HD 12 Bits
Tbase -60.0 ms
20.0 ms/div
2.5 MS 12.5 MS/s
Trigger DC
Stop 5.0 V
Edge Positive
X1= 115.44296 ms ΔX= -44.43568 ms
X2= 71.00728 ms 1/ΔX= -22.50444 Hz
11/24/2025 3:40:19 AM

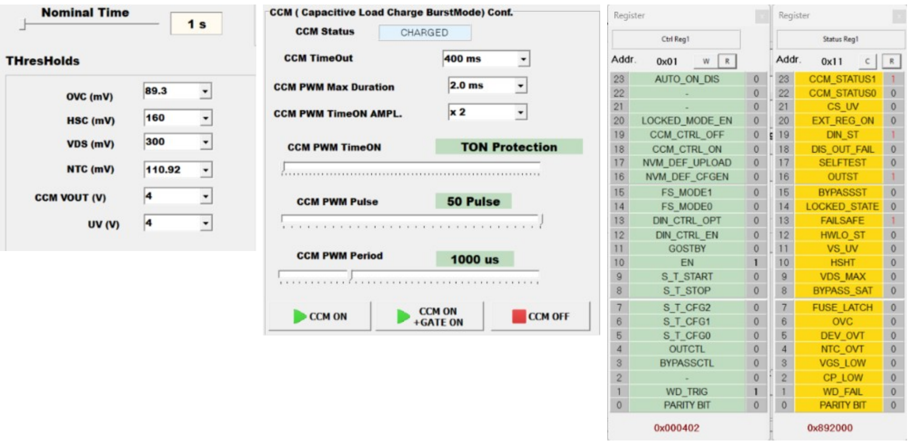
## 5.15.2 Trial Setup Z2

It adopts the same setup as trial Z1, but the device is in Fail-safe.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 μF and $C_S$ = 20 μF

Device in Fail-safe state with the following settings:

- **CCM_VOUT_THR = 4 V**
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = TON protection
- CCM_PWM_TON_MF = 2 x
- **CCM_PWM_SC_T_NB = 50 pulses**
- **CCM_PWM_T = 1000 μs**
- **CCM_TIMEOUT = 400 ms**
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 111



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 4
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 400 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: TON Protection
CCM PWM Pulse: 50 Pulse
CCM PWM Period: 1000 us

Ctrl Reg1 — Addr. 0x01

| | | |
|---|---|---|
| 23 | AUTO_ON_DIS | 0 |
| 22 | - | 0 |
| 21 | - | 0 |
| 20 | LOCKED_MODE_EN | 0 |
| 19 | CCM_CTRL_OFF | 0 |
| 18 | CCM_CTRL_ON | 0 |
| 17 | NVM_DEF_UPLOAD | 0 |
| 16 | NVM_DEF_CFGEN | 0 |
| 15 | FS_MODE1 | 0 |
| 14 | FS_MODE0 | 0 |
| 13 | DIN_CTRL_OPT | 0 |
| 12 | DIN_CTRL_EN | 0 |
| 11 | GOSTBY | 0 |
| 10 | EN | 1 |
| 9 | S_T_START | 0 |
| 8 | S_T_STOP | 0 |
| 7 | S_T_CFG2 | 0 |
| 6 | S_T_CFG1 | 0 |
| 5 | S_T_CFG0 | 0 |
| 4 | OUTCTL | 0 |
| 3 | BYPASSCTL | 0 |
| 2 | - | 0 |
| 1 | WD_TRIG | 1 |
| 0 | PARITY BIT | 0 |

0x000402

Status Reg1 — Addr. 0x11

| | | |
|---|---|---|
| 23 | CCM_STATUS1 | 1 |
| 22 | CCM_STATUS0 | 0 |
| 21 | CS_UV | 0 |
| 20 | EXT_REG_ON | 0 |
| 19 | DIN_ST | 1 |
| 18 | DIS_OUT_FAIL | 0 |
| 17 | SELFTEST | 0 |
| 16 | OUTST | 1 |
| 15 | BYPASSST | 0 |
| 14 | LOCKED_STATE | 0 |
| 13 | FAILSAFE | 1 |
| 12 | HWLO_ST | 0 |
| 11 | VS_UV | 0 |
| 10 | HSHT | 0 |
| 9 | VDS_MAX | 0 |
| 8 | BYPASS_SAT | 0 |
| 7 | FUSE_LATCH | 0 |
| 6 | OVC | 0 |
| 5 | DEV_OVT | 0 |
| 4 | NTC_OVT | 0 |
| 3 | VGS_LOW | 0 |
| 2 | CP_LOW | 0 |
| 1 | WD_FAIL | 0 |
| 0 | PARITY BIT | 0 |

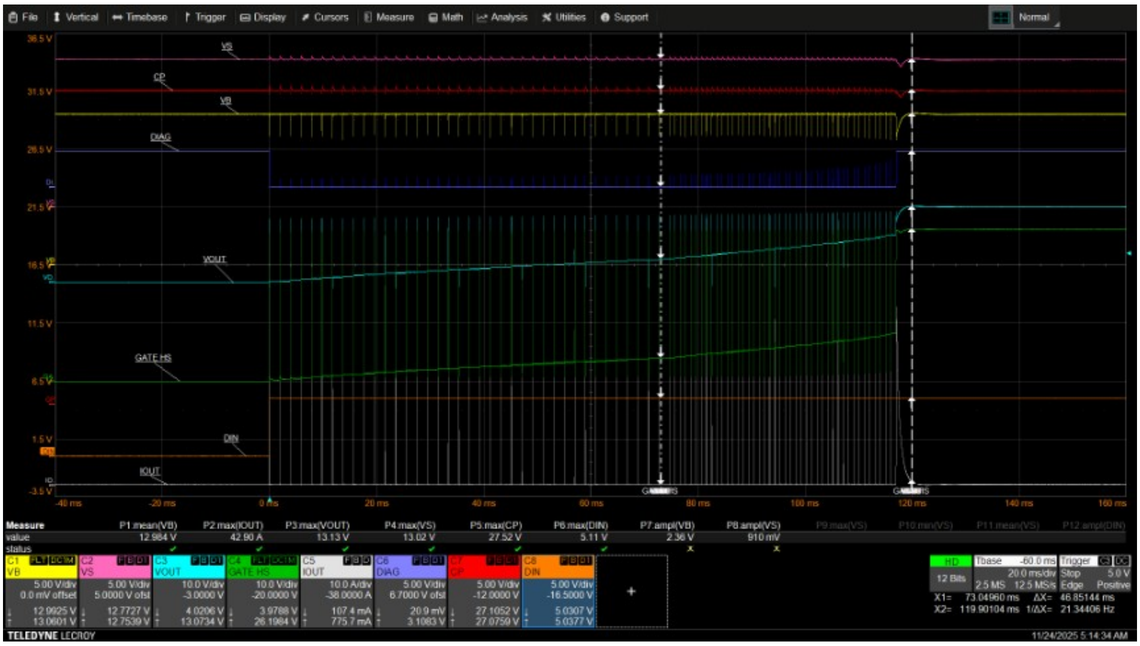
0x892000

Figure 111. CCM configuration and result from GUI for test setup Z2

**Result Z2:**

With the mentioned setup Z1, the 4.7 mF $C_{LOAD}$ is charged in 76 ms (start phase) + 44.4 ms (standard phase).

The slight longer $t_{CHARGE}$ vs trial A1 is due to one additional pulse present in the start phase and a longer duration in the standard phase due to VOUT reaching 13.1 V vs 11.7 V.



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(DIN) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(DIN) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.984 V | 42.90 A | 13.13 V | 13.02 V | 27.52 V | 5.11 V | 2.36 V | 910 mV | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | X | X | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 GATE HS | C5 IOUT | C6 DIAG | C7 CP | C8 DIN |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 5.00 V/div |
| 0.0 mV offset | 5.0000 V ofst | -3.0000 V | -20.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -16.5000 V |
| 12.9925 V | 12.7727 V | 4.0206 V | 3.9788 V | 107.4 mA | 20.9 mV | 27.1052 V | 5.0307 V |
| 13.0601 V | 12.7539 V | 13.0734 V | 26.1984 V | 775.7 mA | 3.1083 V | 27.0759 V | 5.0377 V |

HD 12 Bits
Tbase -60.0 ms 20.0 ms/div 2.5 MS 12.5 MS/s
Trigger Stop 5.0 V Edge Positive
X1= 73.04960 ms ΔX= 46.85144 ms
X2= 119.90104 ms 1/ΔX= 21.34406 Hz

11/24/2025 5:14:34 AM

Figure 112. Waveforms acquired during CCM with setup Z2

## 5.15.3 Trial Setup Z3

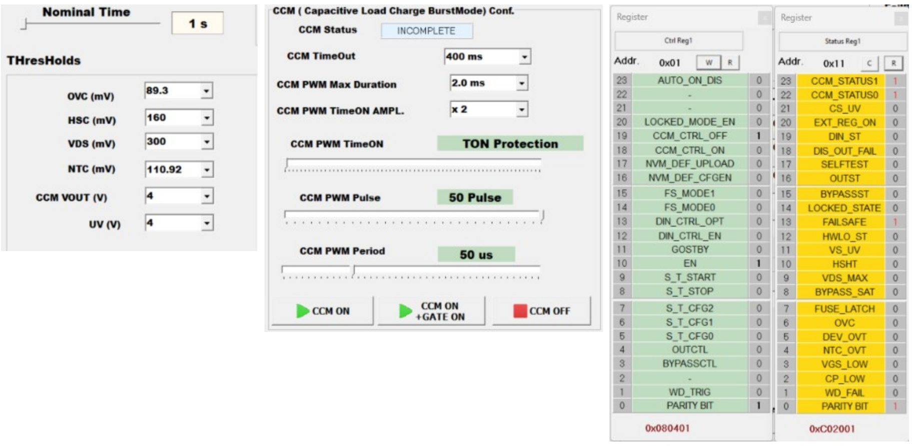
It adopts the same setup as trial Z1 but the CCM is purposely aborted after ~47 ms by means of a dedicated SPI frame in CR#1 where bit 18 (CCM_CTRL_ON) is set at “0” and bit 19 (CCM_CTRL_OFF) is set at “1”.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Fail-safe state with the following settings:

- **CCM_VOUT_THR = 4 V**
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = TON protection
- CCM_PWM_TON_MF = 2 x
- **CCM_PWM_SC_T_NB = 50 pulses**
- **CCM_PWM_T = 1000 µs**
- **CCM_TIMEOUT = 400 ms**
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 113

**Figure 113. CCM configuration and result from GUI for test setup Z3**



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 4
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: INCOMPLETE
CCM TimeOut: 400 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: TON Protection
CCM PWM Pulse: 50 Pulse
CCM PWM Period: 50 us

Ctrl Reg1 — Addr. 0x01

| | | |
|---|---|---|
| 23 | AUTO_ON_DIS | 0 |
| 22 | - | 0 |
| 21 | - | 0 |
| 20 | LOCKED_MODE_EN | 0 |
| 19 | CCM_CTRL_OFF | 1 |
| 18 | CCM_CTRL_ON | 0 |
| 17 | NVM_DEF_UPLOAD | 0 |
| 16 | NVM_DEF_CFGEN | 0 |
| 15 | FS_MODE1 | 0 |
| 14 | FS_MODE0 | 0 |
| 13 | DIN_CTRL_OPT | 0 |
| 12 | DIN_CTRL_EN | 0 |
| 11 | GOSTBY | 0 |
| 10 | EN | 1 |
| 9 | S_T_START | 0 |
| 8 | S_T_STOP | 0 |
| 7 | S_T_CFG2 | 0 |
| 6 | S_T_CFG1 | 0 |
| 5 | S_T_CFG0 | 0 |
| 4 | OUTCTL | 0 |
| 3 | BYPASSCTL | 0 |
| 2 | - | 0 |
| 1 | WD_TRIG | 0 |
| 0 | PARITY BIT | 1 |

0x080401

Status Reg1 — Addr. 0x11

| | | |
|---|---|---|
| 23 | CCM_STATUS1 | 1 |
| 22 | CCM_STATUS0 | 1 |
| 21 | CS_UV | 0 |
| 20 | EXT_REG_ON | 0 |
| 19 | DIN_ST | 0 |
| 18 | DIS_OUT_FAIL | 0 |
| 17 | SELFTEST | 0 |
| 16 | OUTST | 0 |
| 15 | BYPASSST | 0 |
| 14 | LOCKED_STATE | 0 |
| 13 | FAILSAFE | 1 |
| 12 | HWLO_ST | 0 |
| 11 | VS_UV | 0 |
| 10 | HSHT | 0 |
| 9 | VDS_MAX | 0 |
| 8 | BYPASS_SAT | 0 |
| 7 | FUSE_LATCH | 0 |
| 6 | OVC | 0 |
| 5 | DEV_OVT | 0 |
| 4 | NTC_OVT | 0 |
| 3 | VGS_LOW | 0 |
| 2 | CP_LOW | 0 |
| 1 | WD_FAIL | 0 |
| 0 | PARITY BIT | 1 |

0xC02001

Please note that the CCM_CTRL_OFF (bit19 in CR#1) is refreshed after the CCM is aborted.

**Result Z3:**

With the mentioned setup Z3, the 4.7 mF $C_{LOAD}$ is aborted after 46.8 ms during the start phase due to a dedicated command on CR# 1. The VOUT reaches 2.8 V once the CCM is stopped.

Figure 114. Waveforms acquired during CCM with setup Z3

| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(I SUPPLY) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(I SUP... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.983 V | 41.78 A | 11.36 V | 13.03 V | 27.54 V | 7.66 A | 2.30 V | 369 mV | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | x | x | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 GATE HS | C5 IOUT | C6 DIAG | C7 CP | C8 I SUPPLY |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 10.0 A/div |
| 0.0 mV offset | 5.0000 V ofst | -3.0000 V | -20.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -35.0000 A |
| ↓ 12.9806 V | ↓ 12.7121 V | ↓ 2.8348 V | ↓ 2.7246 V | ↓ 76.7 mA | ↓ 3.0246 V | ↓ 27.0326 V | ↓ -82.3 mA |
| ↑ 12.9736 V | ↑ 12.7134 V | ↑ -65.6 mV | ↑ -96.3 mV | ↑ 101.8 mA | ↑ 3.1194 V | ↑ 27.0306 V | ↑ -78.1 mA |

HD 12 Bits
Tbase -30.0 ms
10.0 ms/div
2.5 MS 25 MS/s
Trigger C3 DC
Stop 5.0 V
Edge Positive
X1= 46.80960 ms ΔX= -49.72872 ms
X2= -2.91912 ms 1/ΔX= -20.10910 Hz
11/24/2025 4:01:06 AM

## 5.15.4 Trial Setup Z4

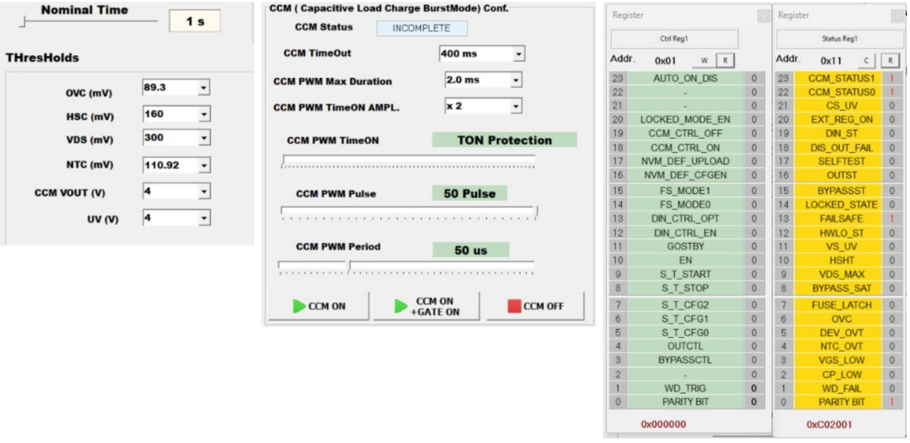
It adopts the same setup as trial Z3 with the device in Fail-safe mode and the CCM purposely aborted after 85.6 ms by means of a dedicated DIN set from high to low.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- $C_{LOAD}$ = 4.7 mF (measured 4.52 mF)
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Fail-safe state with the following settings (written in NVM):

- **CCM_VOUT_THR = 4 V**
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = TON protection
- CCM_PWM_TON_MF = 2 x
- **CCM_PWM_SC_T_NB = 50 pulses**
- **CCM_PWM_T = 1000 µs**
- **CCM_TIMEOUT = 400 ms**
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 115

Figure 115. **CCM configuration and result from GUI for test setup Z4**



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 4
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: INCOMPLETE
CCM TimeOut: 400 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: TON Protection
CCM PWM Pulse: 50 Pulse
CCM PWM Period: 50 us

Register: Ctrl Reg1, Addr. 0x01

| | | |
|---|---|---|
| 23 | AUTO_ON_DIS | 0 |
| 22 | - | 0 |
| 21 | - | 0 |
| 20 | LOCKED_MODE_EN | 0 |
| 19 | CCM_CTRL_OFF | 0 |
| 18 | CCM_CTRL_ON | 0 |
| 17 | NVM_DEF_UPLOAD | 0 |
| 16 | NVM_DEF_CFGEN | 0 |
| 15 | FS_MODE1 | 0 |
| 14 | FS_MODE0 | 0 |
| 13 | DIN_CTRL_OPT | 0 |
| 12 | DIN_CTRL_EN | 0 |
| 11 | GOSTBY | 0 |
| 10 | EN | 0 |
| 9 | S_T_START | 0 |
| 8 | S_T_STOP | 0 |
| 7 | S_T_CFG2 | 0 |
| 6 | S_T_CFG1 | 0 |
| 5 | S_T_CFG0 | 0 |
| 4 | OUTCTL | 0 |
| 3 | BYPASSCTL | 0 |
| 2 | - | 0 |
| 1 | WD_TRIG | 0 |
| 0 | PARITY BIT | 0 |

0x000000

Register: Status Reg1, Addr. 0x11

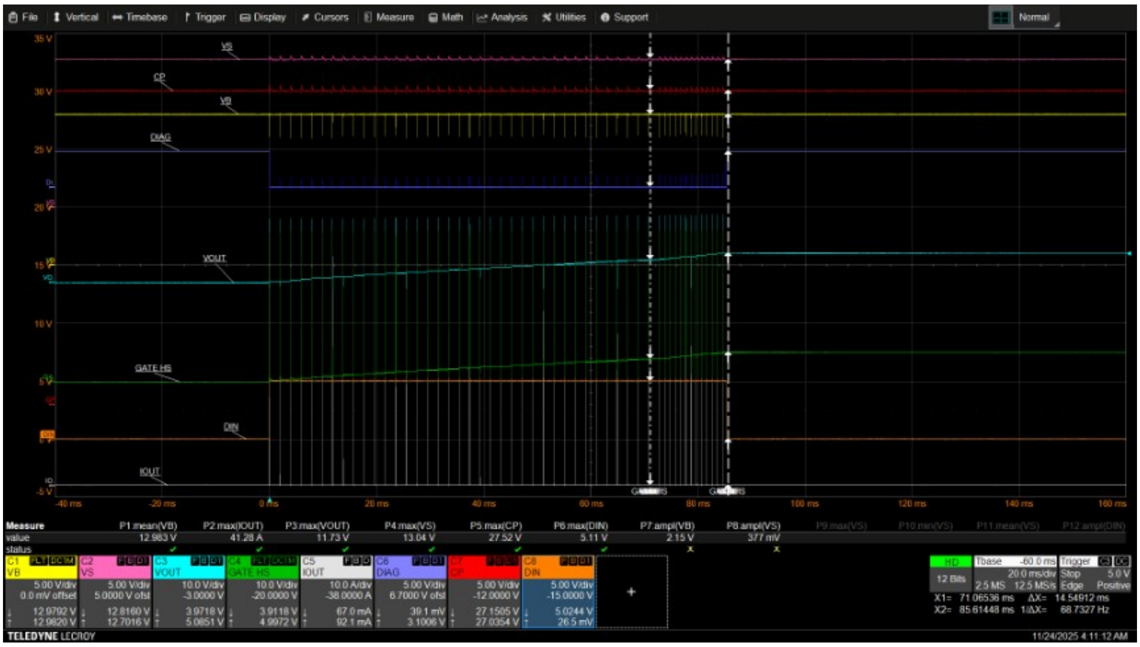
| | | |
|---|---|---|
| 23 | CCM_STATUS1 | 1 |
| 22 | CCM_STATUS0 | 1 |
| 21 | CS_UV | 0 |
| 20 | EXT_REG_ON | 0 |
| 19 | DIN_ST | 0 |
| 18 | DIS_OUT_FAIL | 0 |
| 17 | SELFTEST | 0 |
| 16 | OUTST | 0 |
| 15 | BYPASSST | 0 |
| 14 | LOCKED_STATE | 0 |
| 13 | FAILSAFE | 1 |
| 12 | HWLO_ST | 0 |
| 11 | VS_UV | 0 |
| 10 | HSHT | 0 |
| 9 | VDS_MAX | 0 |
| 8 | BYPASS_SAT | 0 |
| 7 | FUSE_LATCH | 0 |
| 6 | OVC | 0 |
| 5 | DEV_OVT | 0 |
| 4 | NTC_OVT | 0 |
| 3 | VGS_LOW | 0 |
| 2 | CP_LOW | 0 |
| 1 | WD_FAIL | 0 |
| 0 | PARITY BIT | 1 |

0xC02001

**Result Z4:**

With the mentioned setup Z4, the 4.7 mF $C_{LOAD}$ is aborted after 74 ms (start phase) + 11.6 ms (standard phase) due to DIN moving from high to low. The VOUT reaches 5.1 V once the CCM is stopped.

Figure 116. **Waveforms acquired during CCM with setup Z4**



| Measure | P1:mean(VB) | P2:max(IOUT) | P3:max(VOUT) | P4:max(VS) | P5:max(CP) | P6:max(DIN) | P7:ampl(VB) | P8:ampl(VS) | P9:max(VS) | P10:min(VS) | P11:mean(VS) | P12:ampl(DIN) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 12.983 V | 41.28 A | 11.73 V | 13.04 V | 27.52 V | 5.11 V | 2.15 V | 377 mV | | | | |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | x | x | | | | |

| C1 VB | C2 VS | C3 VOUT | C4 GATE HS | C5 IOUT | C6 DIAG | C7 CP | C8 DIN |
|---|---|---|---|---|---|---|---|
| 5.00 V/div | 5.00 V/div | 10.0 V/div | 10.0 V/div | 10.0 A/div | 5.00 V/div | 5.00 V/div | 5.00 V/div |
| 0.0 mV offset | 5.0000 V ofst | -3.0000 V | -20.0000 V | -38.0000 A | 6.7000 V ofst | -12.0000 V | -15.0000 V |
| ↓ 12.9792 V | ↓ 12.8160 V | ↓ 3.9718 V | ↓ 3.9118 V | ↓ 67.0 mA | ↓ 39.1 mV | ↓ 27.1505 V | ↓ 5.0244 V |
| ↑ 12.9820 V | ↑ 12.7016 V | ↑ 5.0851 V | ↑ 4.9972 V | ↑ 92.1 mA | ↑ 3.1006 V | ↑ 27.0354 V | ↑ 26.5 mV |

HD 12 Bits
Tbase -60.0 ms 20.0 ms/div 2.5 MS 12.5 MS/s
Trigger Stop 5.0 V Edge Positive
X1= 71.06536 ms ΔX= 14.54912 ms
X2= 85.61448 ms 1/ΔX= 68.7327 Hz
11/24/2025 4:11:12 AM

## 5.16 Examples of CCM + GATE ON

### 5.16.1 Trial Setup E2

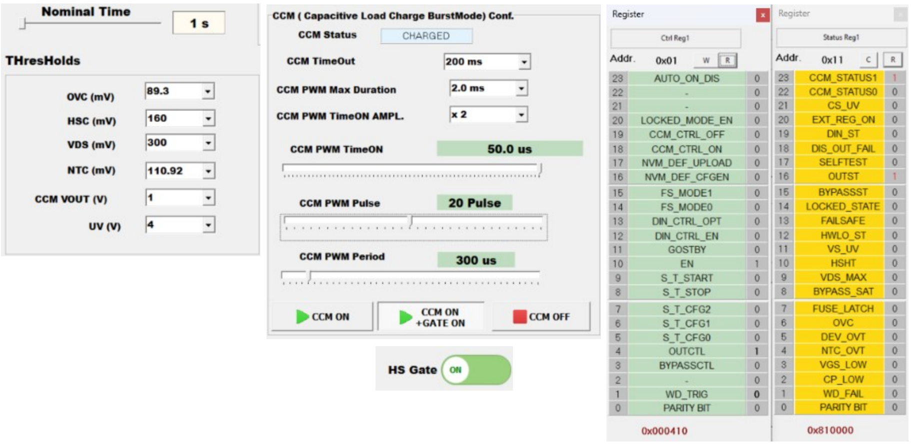
It adopts the same setup as trial E1 with $C_{LOAD}$ at 4.7 mF but in this case we launched CCM + GATE ON.

- VB = 13 V
- $R_{SHUNT}$ = 5 mΩ
- Ambient temperature = room temperature ~25°C generating TJ ~35°C
- **$C_{LOAD}$ = 4.7 mF (measured 4.52 mF)**
- $C_{IN}$ = 314 µF and $C_S$ = 20 µF

Device in Unlocked state with the following settings:

- CCM_VOUT_THR = 1 V
- OVC_THR = VOC_THRS_31 → 89.3 mV
- HSC_THR = VHSC_THRS_15 → 160 mV
- T_NOM = $T\_NOM_{MIN}$ → 1 s
- CCM_PWM_TON = 50 µs
- CCM_PWM_TON_MF = 2 x
- CCM_PWM_SC_T_NB = 20 pulses
- CCM_PWM_T = 300 µs
- CCM_TIMEOUT = 200 ms
- CCM_PWM_SC_T = 2 ms
- GUI settings at the end of CCM operations as shown in Figure 117
- In the same frame on CR#1 set CCM_CTRL_ON (bit 18) = 1b AND OUTCTL (bit 4) = 1b

Figure 117. **CCM configuration and result from GUI for test setup E2. At the end of charge the HS_GATE is turned again ON to sustain OUT voltage**



Nominal Time: 1 s

THresHolds

OVC (mV): 89.3
HSC (mV): 160
VDS (mV): 300
NTC (mV): 110.92
CCM VOUT (V): 1
UV (V): 4

CCM ( Capacitive Load Charge BurstMode) Conf.

CCM Status: CHARGED
CCM TimeOut: 200 ms
CCM PWM Max Duration: 2.0 ms
CCM PWM TimeON AMPL.: x 2
CCM PWM TimeON: 50.0 us
CCM PWM Pulse: 20 Pulse
CCM PWM Period: 300 us

HS Gate: ON

Ctrl Reg1 — Addr. 0x01

| | | |
|---|---|---|
| 23 | AUTO_ON_DIS | 0 |
| 22 | - | 0 |
| 21 | - | 0 |
| 20 | LOCKED_MODE_EN | 0 |
| 19 | CCM_CTRL_OFF | 0 |
| 18 | CCM_CTRL_ON | 0 |
| 17 | NVM_DEF_UPLOAD | 0 |
| 16 | NVM_DEF_CFGEN | 0 |
| 15 | FS_MODE1 | 0 |
| 14 | FS_MODE0 | 0 |
| 13 | DIN_CTRL_OPT | 0 |
| 12 | DIN_CTRL_EN | 0 |
| 11 | GOSTBY | 0 |
| 10 | EN | 1 |
| 9 | S_T_START | 0 |
| 8 | S_T_STOP | 0 |
| 7 | S_T_CFG2 | 0 |
| 6 | S_T_CFG1 | 0 |
| 5 | S_T_CFG0 | 0 |
| 4 | OUTCTL | 1 |
| 3 | BYPASSCTL | 0 |
| 2 | - | 0 |
| 1 | WD_TRIG | 0 |
| 0 | PARITY BIT | 0 |

0x000410

Status Reg1 — Addr. 0x11

| | | |
|---|---|---|
| 23 | CCM_STATUS1 | 1 |
| 22 | CCM_STATUS0 | 0 |
| 21 | CS_UV | 0 |
| 20 | EXT_REG_ON | 0 |
| 19 | DIN_ST | 0 |
| 18 | DIS_OUT_FAIL | 0 |
| 17 | SELFTEST | 0 |
| 16 | OUTST | 1 |
| 15 | BYPASSST | 0 |
| 14 | LOCKED_STATE | 0 |
| 13 | FAILSAFE | 0 |
| 12 | HWLO_ST | 0 |
| 11 | VS_UV | 0 |
| 10 | HSHT | 0 |
| 9 | VDS_MAX | 0 |
| 8 | BYPASS_SAT | 0 |
| 7 | FUSE_LATCH | 0 |
| 6 | OVC | 0 |
| 5 | DEV_OVT | 0 |
| 4 | NTC_OVT | 0 |
| 3 | VGS_LOW | 0 |
| 2 | CP_LOW | 0 |
| 1 | WD_FAIL | 0 |
| 0 | PARITY BIT | 0 |

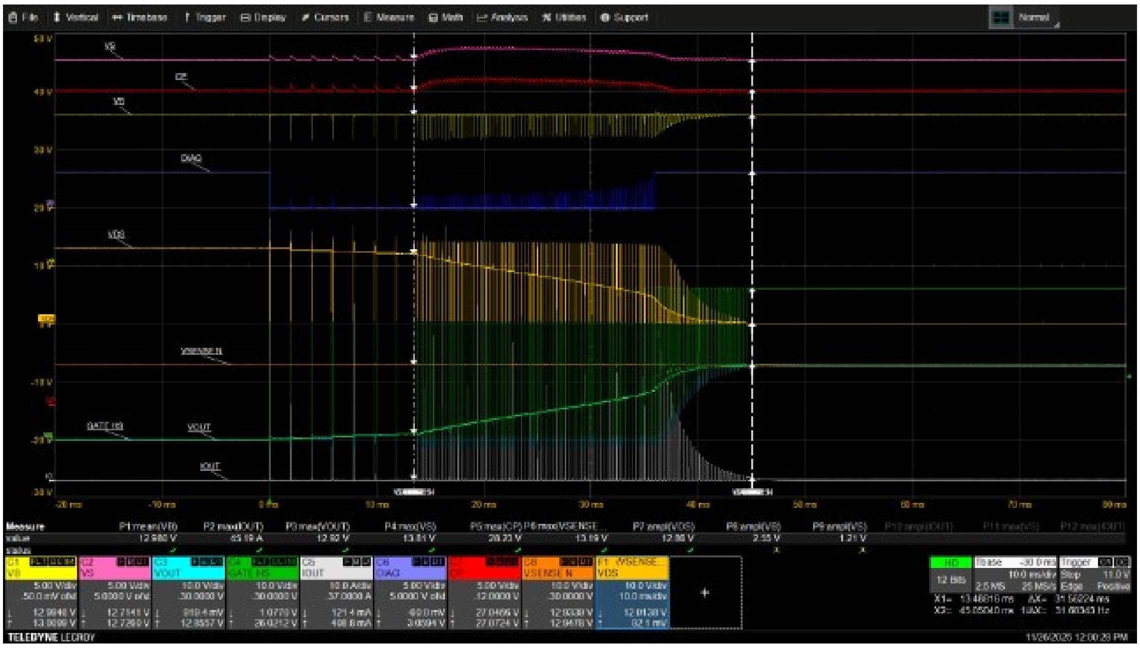
0x810000

**Result E2:**

With the mentioned setup E2, the $C_{LOAD}$ is charged in 4 ms (start phase) + 31 ms (standard phase).

In this case, once $C_{LOAD}$ is charged, OUTCTL (bit4) = 1b in CR#1 maintain ON the MOS (OUTST bit 16 in SR#1 is at “1”) to maintain VOUT value close to VB.

**Figure 118.** Waveforms including VDS acquired during CCM with setup E2 with device in Unlocked state



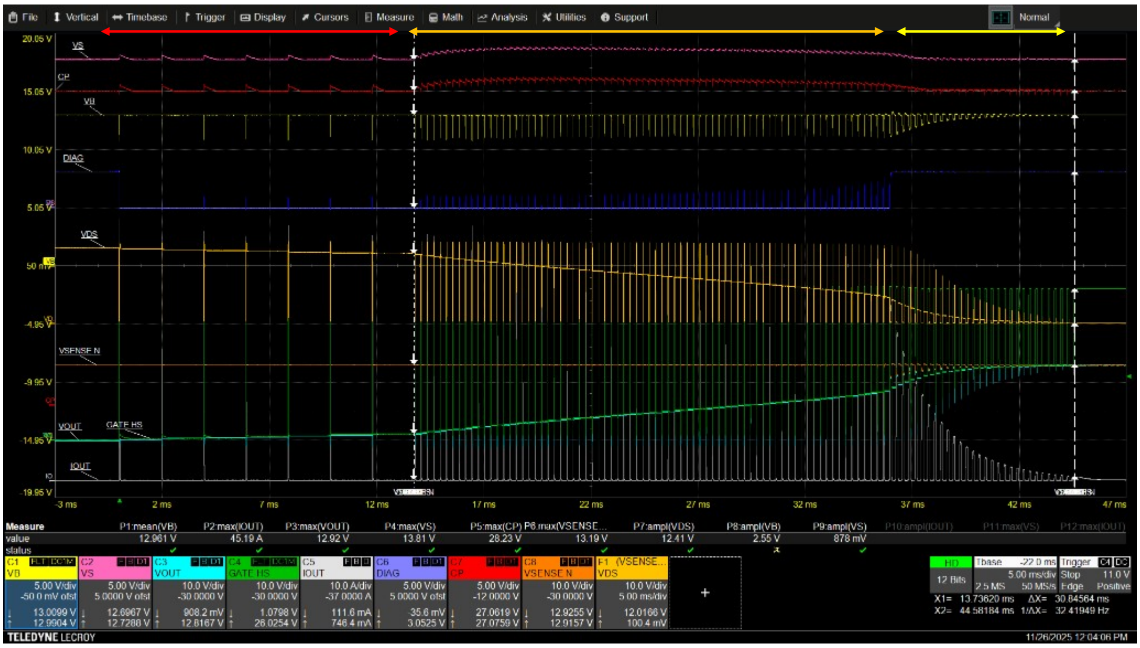
Below is the zoomed image focused on the CCM step, with HS_GATE maintained ON at the end of the $C_{LOAD}$ charge.

**Figure 119.** Zoomed waveforms including VDS focused on CCM step with setup E2 with device in Unlocked state

Start charging phase (14ms):
The pulse duration depends on hard short protection. The current peak depends on VB, HSC and $R_{SHUNT}$. This phase ends once VOUT reaches set target threshold (1V)

Standard charging phase 1 (22ms):
The pulse duration depends on I²t protection (HSC or OVC)

Standard charging phase 2 (9ms):
The pulse duration depends on set CCM timeON and period and no I²t protections are triggered as per DIAG status (HSC and OVC are not achieved). It ends once VDS (Vsense N – VOUT) reaches 100mV



# 6 Conclusions

As shown in the examples verified in this document, the VNF1248F device can sustain, through the CCM feature, the charging of a wide range of capacitive loads operating at supply voltages of 12 V, 24 V, and 48 V. For 48 V applications, while CCM is active, the parasitic elements combined with the application circuitry of VNF1248F can cause a voltage boost effect that is potentially critical.

In this document, all hazardous conditions are avoided by varying the value of $C_{IN}$ capacitors and, where necessary, by using a transient voltage suppressor (TVS) SM15T68CAY.

Similarly, end users must select the application components to prevent dangerous voltage levels that could exceed the absolute maximum ratings of the VNF1248F device.

# Revision history

Table 7. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 12-Mar-2026 | 1 | First release. |

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