Non-volatile Memory (NVM) feature of VNF1248F

Introduction

The purpose of this document is to demonstrate the functionality of the Non-volatile Memory (NVM) feature of VNF1248F, high-side switch controller with STi^{2}Fuse protection for 12 V, 24 V, and 48 V automotive applications, in an application environment using the EV-VNF1248F evaluation board.

Typical application diagrams for 3.3 V and 5.0 V applications are reported in the datasheet of VNF1248F (see DS14109).

For the schematic of the EV-VNF1248F refer to the related data brief (DB5511) and user manual (UM3487).

All tests were conducted on a typical sample representative of the standard population.

1 System Overview

1.1 VNF1248F Description

The VNF1248F device is an advanced controller for a power MOSFET in high-side configuration, designed for the implementation of an intelligent high-side switch for 12 V, 24 V, and 48 V automotive applications. The control IC is interfaced to a host microcontroller through a 3.3 V and 5 V CMOS-compatible SPI interface and provides protection and diagnostics to the system.

1.2 Block diagram and pin description

Figure 1. Block diagram

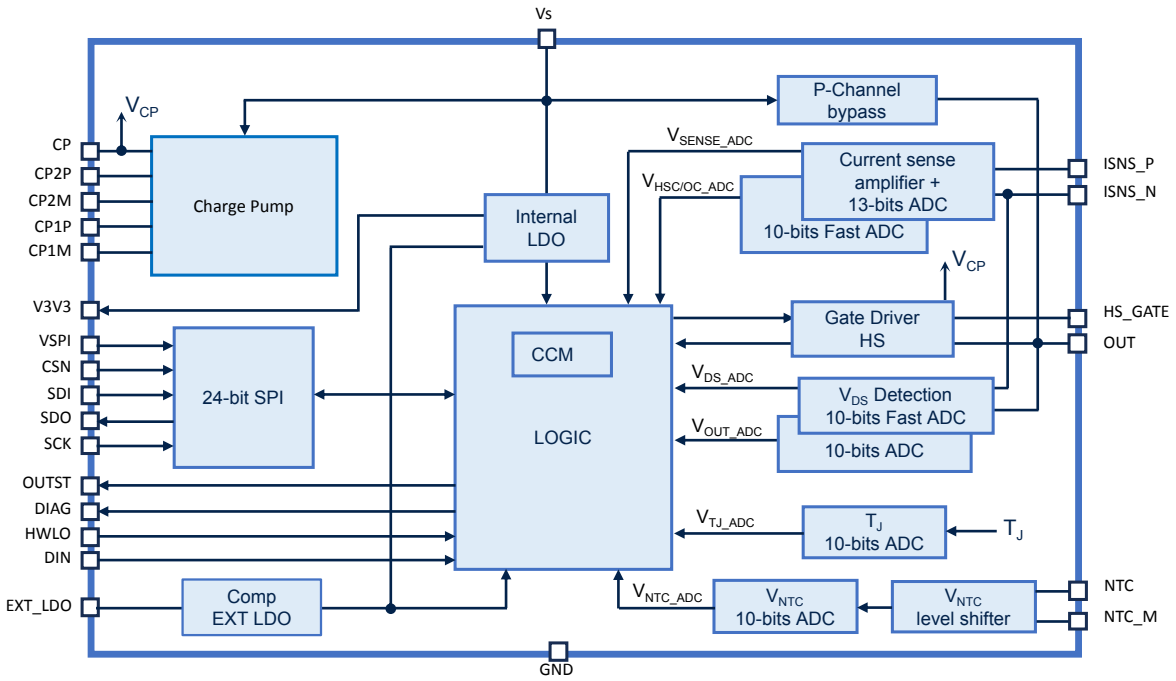
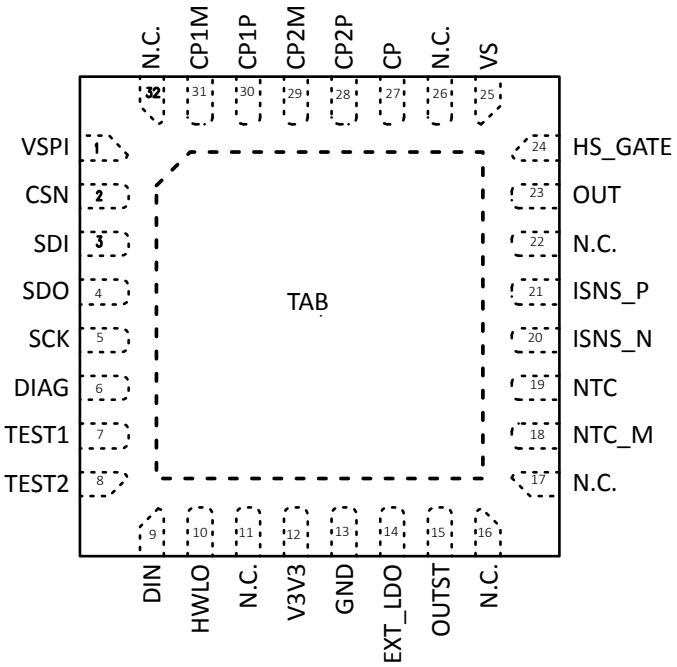


Figure 2. Configuration diagram (top through view)



Note: TAB connection must be connected to the ground. TAB is not intended as the device reference ground (a dedicated pin shall be used).

Table 1. Pin functions

Pin #	Name	Function
TAB		GND
1	VSPI	DC supply input for the SPI interface. 3.3 V and 5 V are compatible.
2	CSN	Chip select (active low) for SPI communication. It is the selection pin of the device. CMOS compatible input.
3	SDI	Serial data input for SPI communication. Data is transferred serially into the device and sampled on SCK rising edge.
4	SDO	Serial data output for SPI communication. Data is transferred serially out of the device on the SCK falling edge.
5	SCK	Serial clock for SPI communication. It is a CMOS compatible input.
6	DIAG	Open drain logic output. Diagnostic feedback. DIAG = '0' if ((SR1.FAILSAFE_ST='1' or (CR1.AUTO_ON_DIS='1') and BYPASS_SAT='1') or (GSB.DIAGS = '1') or (GSB.DE = '1') or "internal oscillator fault event" else '1'
7	TEST1	Test mode pin 1 - It must be connected to the ground through a 1 kΩ resistor.
8	TEST2	Test mode pin 2 - It must be connected to the ground through a 1 kΩ resistor.
9	DIN	Direct input to wake-up device from standby and to control gate turn-on/ turn-off directly. If not used, must be connected to the ground through a 1 kΩ resistor.
10	HWLO	Active high input pin compatible with 3.3 V and 5 V CMOS. If not used, must be connected to the ground through a 1 kΩ resistor.
11, 16, 17, 22,	N.C	Not connected.

Pin #	Name	Function
26, 32		
12	V3V3	Output of the 3.3 V internal LDO voltage regulator (logic and I/O supply). Connect a low ESR capacitor (1 µF) close to this pin.
13	GND	Ground connection.
14	EXT_LDO	External V3V3 supply. If not used, must be connected to the ground through a 1 kΩ resistor.
15	OUTST	Gate status monitor.
18	NTC_M	Negative input pin for external NTC resistor.
19	NTC	Positive input pin for external NTC resistor.
20	ISNS_N	Current sense amplifier negative input.
21	ISNS_P	Current sense amplifier positive input.
23	OUT	External FET source connection.
24	HS_GATE	Output of the gate driver for the external FET.
25	VS	Input supply pin. Connect to the 12 V, 24 V, 48 V battery voltage.
27	CP	Charge pump output.
28	CP2P	Charge pump–positive terminal of the flying capacitor C_{P2}.
29	CP2M	Charge pump–negative terminal of the flying capacitor C_{P2}.
30	CP1P	Charge pump–positive terminal of the flying capacitor C_{P1}.
31	CP1M	Charge pump–negative terminal of the flying capacitor C_{P1}.

2 Non-volatile memory (NVM) customer programming

The control logic unit implemented in the device enables users to program a portion of the non-volatile memory (NVM) embedded in the device. This functionality allows users to test and store specific settings for key parameters used during operations.

The customer has free access to one sector (sector 5) out of the six available to read or write the contents that influence the behavior of the device. Write and read operations are possible through an appropriate command sequence that ensures secure and protected access. This prevents unexpected or unwanted write operations from corrupting the content of the NVM.

Each NVM operation (write or read) is enabled by the sequence:

1. SPI write frame to set UNLOCK bit to 1 (CR#3)
2. SPI write frame to write customer access key (CR#4)

Both steps must be performed by means of atomic frames (sequentially not interleaved by any other command, such as watchdog frames or diagnostic frames).

After having properly completed the sequence, CR#4 changes its function, making it available the following fields to control NVM Write/Read operations (enabled only if write customer access key is executed successfully):

- NVM_ADDR (bits [11:8]): address of the NVM sector to be read/written (0x5)
- NVM_WR_EN (bit 3): NVM operation type (1 → write, 0 → read)
- NVM_OP_START (bit 2): trigger bit to start the selected NVM operation

All control register fields mapped on the NVM sector 0x5 are listed in Table 2 below. Detailed descriptions of the fields can be found in the device datasheet.

Table 2. NVM mapped configuration parameters

Name	Description	Register field	Use
DIN_CTRL_EN_DEF	Direct input control enable	CR#1→DIN_CTRL_EN	Locked
DIN_CTRL_OPT_DEF	Direct input control behavior selection (AND/OR modes)	CR#1→DIN_CTRL_OPT	Locked
BYPASS_CTL_DEF	Internal bypass control	CR#1→BYPASS_CTL	Fail-safe/Standby
FS_MODE_DEF	Output behavior configuration in fail-safe	CR#1→FS_MODE	Fail-safe
NVM_DEF_CFG_EN	Fail-safe default configuration enable	CR#1→NVM_DEF_CFG_EN	Fail-safe/Locked
T_NOM_FS_DEF	I2t fuse emulation nominal timescale	CR#2→TNOM	Fail-safe/Locked
OVC_THR_FS_DEF	I2t fuse emulation nominal overcurrent protection threshold selection	CR#2→OVC_THR	Fail-safe/Locked
HSC_THR_FS_DEF	Hard short protection threshold selection	CR#2 →HSC_THR	Fail-safe/Locked
VDS_THRS_FS_DEF	V_{DS} protection threshold selection	CR#2→VDS_THRS	Fail-safe/Locked
NTC_THR_FS_DEF	NTC thermal protection threshold selection	CR#3→NTC_THR	Fail-safe/Locked
WD_TIME_DEF	Watchdog monitor timeout selection	CR#3→WD_TIME	Fail-safe/Locked
UV_THR_DEF	Vs undervoltage threshold selection	CR#3→UV_THR	Fail-safe/Locked
CS_UV_RETRY_T_DEF	Current sense undervoltage protection retry time	CR#3→CS_UV_RETRY_T	Fail-safe/Locked
CCM_VOUT_THR_DEF	Capacitive load charge (burst mode) V_{OUT} threshold selection	CR#3→CCM_VOUT_THR	Fail-safe/Locked
CCM_PWM_TON_MF_DEF	Capacitive load charge (burst mode) PWM ton multiplying factor	CR#3→CCM_PWM_TON_MF	Fail-safe/Locked

Name	Description	Register field	Use
CCM_PWM_TON_DEF	Capacitive load charge (burst mode) PWM ton setting	CR#5→CCM_PWM_TON	Fail-safe/Locked
CCM_PWM_T_DEF	Capacitive load charge (burst mode) PWM period	CR#5→CCM_PWM_T	Fail-safe/Locked
CCM_PWM_SC_T_DEF	Capacitive load charge (burst mode) PWM period for short circuit check at start	CR#5→CCM_PWM_SC_T	Fail-safe/Locked
CCM_PWM_SC_T_NB_DEF	Capacitive load charge (burst mode) max number of PWM pulses for short circuit check at start	CR#5→CCM_PWM_SC_T_NB	Fail-safe/Locked
CCM_TIMEOUT_DEF	Capacitive load charge (burst mode) maximum time duration	CR#5→CCM_TIMEOUT	Fail-safe/Locked

3 NVM read operation

The steps for NVM read execution are the following:

1. The user optionally (1) resets the target RAM register fields by writing 0.

(1) Note: ***This step is not mandatory; however, to guarantee a successful reading of the NVM content, it is advisable to first save the contents of the NVM fields (refer to table 30 in the device datasheet), then overwrite these fields with zero values. Afterward, perform the remaining NVM read operations via the SPI sequence and compare the results with the previously saved data to verify the success of the NVM reading process.***

2. The user performs the required 2-step access sequence via SPI (see Section 2).
3. The user writes (via SPI) the sector address, access type, and start command into the unlocked dedicated register (CR#4).
4. Subsequently, the following steps are automatically executed by the device FSM (finite-state machine):
   a. The control logic unit generates control signals and the address for the NVM.
   b. The NVM manages the reading procedure.
   c. Upon completion of the reading phase, the NVM notifies the control logic unit.
   d. The control logic unit maps the sector data output to the corresponding RAM register fields.
5. The user reads (and clears) the RAM register field by reporting the NVM operation status via SPI in SR#2.

Example: let's suppose that in the NVM, there are the following fields:

- OVC = 10.4 mV (OVC_THR = 00011b in bits [15:11] of CR#2)
- HSHT_THR = 105.6 mV (HSHT_THR = 1100b in bits [10:7] of CR#2)
- NVM default configuration (NVM_DEF_CFG_EN = 1b in bit 16 of CR#1)

Environment setup:

- V_{SPI} = 3.3 V (same as µC supply)
- Shunt sense resistor = 5 mΩ
- Ambient temperature
- Device in Unlocked state
- V_{BATT} = 13 V

Frames to be sent sequentially to perform NVM reading (as previously listed):

- 2-step SPI access sequence:
  - SPI write frame (2) to set UNLOCK = 1b (bit 9) in the CR#3 register

(2) Note: ***Bit0 (P) and Bit1 (WD) must be set according to relevant microcontroller task for watchdog trigger and parity bit check***

OP		ADDRESS						Data Byte 1								Data Byte 2								Data Byte 3							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	WD	P

  - SPI write frame to set NVM_CTM_ACCESS_KEY = 0x105B96 (customer access key, bits [23:2]) in the CR#4 register

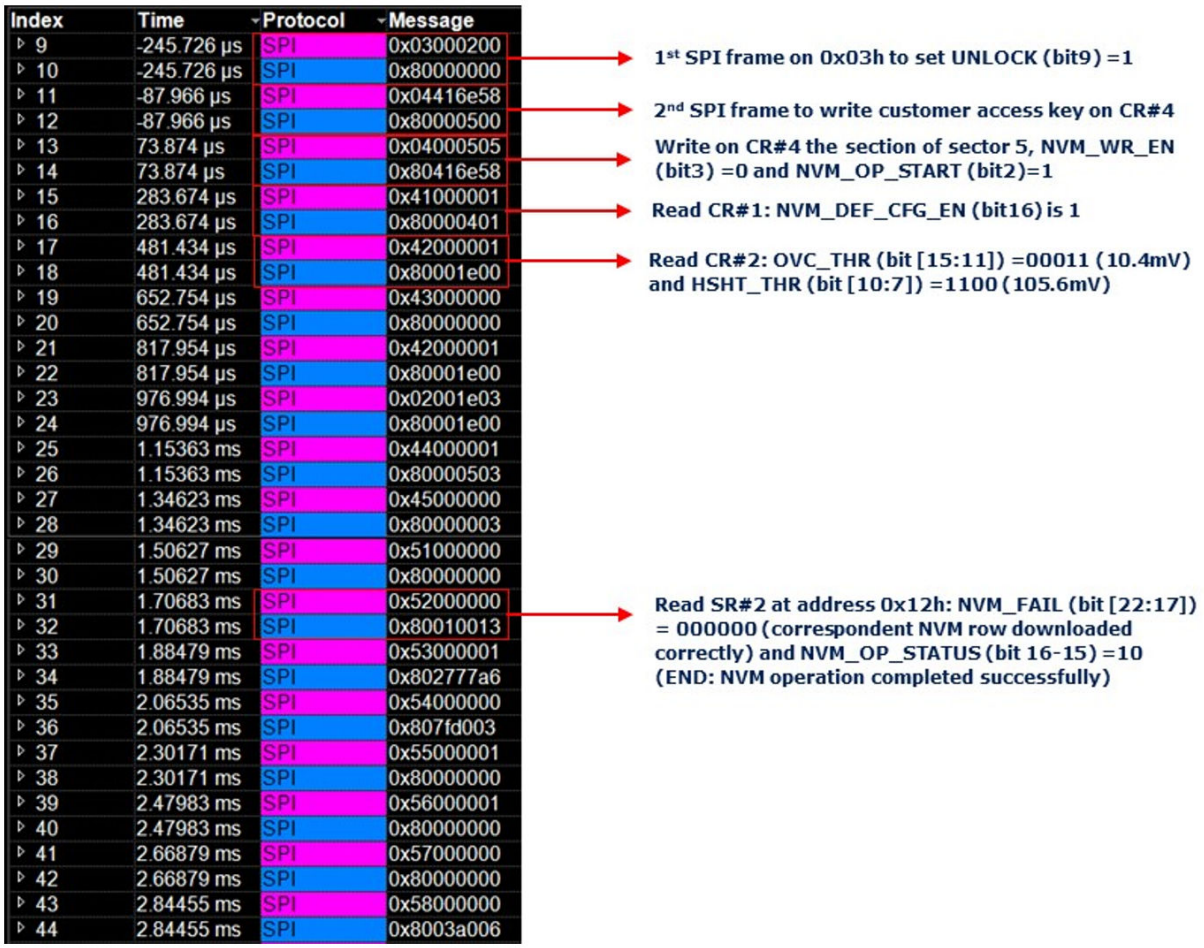
OP		ADDRESS						Data Byte 1								Data Byte 2								Data Byte 3							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	1	1	0	1	1	1	0	0	1	0	1	1	0	WD	P

- Function 2 of CR#4 is enabled. SPI write frame at CR#4 to set:
  - NVM_ADDR = 0x5 (bits [11:8]), the only available address for customer access
  - NVM_WR_EN = 0b (bit 3) for read operation
  - NVM_OP_START = 1b (bit 2) to give the NVM start command

OP		ADDRESS						Data Byte 1								Data Byte 2								Data Byte 3							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	WD	P

The NVM registers' reading procedure starts and all CRs will be checked in sequence (in pink the SDI message and in blue the SDO message):

Figure 3. **NVM read: SPI log**



Index	Time	Protocol	Message
9	-245.726 µs	SPI	0x03000200
10	-245.726 µs	SPI	0x80000000
11	-87.966 µs	SPI	0x04416e58
12	-87.966 µs	SPI	0x80000500
13	73.874 µs	SPI	0x04000505
14	73.874 µs	SPI	0x80416e58
15	283.674 µs	SPI	0x41000001
16	283.674 µs	SPI	0x80000401
17	481.434 µs	SPI	0x42000001
18	481.434 µs	SPI	0x80001e00
19	652.754 µs	SPI	0x43000000
20	652.754 µs	SPI	0x80000000
21	817.954 µs	SPI	0x42000001
22	817.954 µs	SPI	0x80001e00
23	976.994 µs	SPI	0x02001e03
24	976.994 µs	SPI	0x80001e00
25	1.15363 ms	SPI	0x44000001
26	1.15363 ms	SPI	0x80000503
27	1.34623 ms	SPI	0x45000000
28	1.34623 ms	SPI	0x80000003
29	1.50627 ms	SPI	0x51000000
30	1.50627 ms	SPI	0x80000000
31	1.70683 ms	SPI	0x52000000
32	1.70683 ms	SPI	0x80010013
33	1.88479 ms	SPI	0x53000001
34	1.88479 ms	SPI	0x802777a6
35	2.06535 ms	SPI	0x54000000
36	2.06535 ms	SPI	0x807fd003
37	2.30171 ms	SPI	0x55000001
38	2.30171 ms	SPI	0x80000000
39	2.47983 ms	SPI	0x56000001
40	2.47983 ms	SPI	0x80000000
41	2.66879 ms	SPI	0x57000000
42	2.66879 ms	SPI	0x80000000
43	2.84455 ms	SPI	0x58000000
44	2.84455 ms	SPI	0x8003a006

4 NVM write operation

The steps for NVM programming (write) execution are the following:

1. The user writes the RAM register fields related to parameters target of NVM programming through SPI
2. The user performs the required 2-step access sequence via SPI.
3. The user writes the sector address, access type, and start command into the unlocked dedicated register (CR#4) via SPI.
4. Subsequently, the following steps are automatically executed by the device FSM:
   a. The control logic unit generates control signals and the address for the NVM.
   b. The NVM IP interface manages the reading procedure.
   c. Upon completion of the reading phase, the NVM notifies the digital control logic.
   d. The control logic unit maps the sector data output to the corresponding
5. The user reads (and clears) the RAM register field by reporting the NVM operation status via SPI in SR#2.

Note: During NVM write operation, correspondent RAM register fields shall be kept constant, considering they are the direct sources of data stored into the NVM sector (no intermediate buffering).

In the case of an NVM write that involves only a subset of the allowed programmable parameters (partial write), it is mandatory to first perform an NVM read operation. This ensures that the RAM register fields corresponding to parameters not affected by the changes are properly populated, thereby preventing the overwriting of their NVM locations with unintended values. This precaution is necessary because the NVM write operation considers all RAM register fields belonging to the targeted NVM sector.

Example: let's suppose that the following parameters are written in the NVM:

- OVC = 89.3 mV (OVC_THR = 11111b in bits [15:11] of CR#2)
- HSHT_THR = 160 mV (HSHT_THR = 1111b in bits [10:7] of CR#2)
- NVM default configuration (NVM_DEF_CFG_EN = 0b in bit 16 of CR#1)

Environment setup

- V_{SPI} = 3.3 V (same µC supply)
- Shunt sense resistor = 5 mΩ
- Ambient temperature
- Device in Unlocked state
- V_{BATT} = 13 V

Frames to be sent sequentially to perform NVM writing (as previously listed):

- 2-step SPI access sequence:
  – SPI write frame to set UNLOCK = 1b (bit 9) in the CR#3 register

OP	ADDRESS							Data Byte 1								Data Byte 2								Data Byte 3							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	WD	P

  – SPI write frame to set NVM_CTM_ACCESS_KEY = 0x105B96 (customer access key, bits [23:2] in the CR#4 register

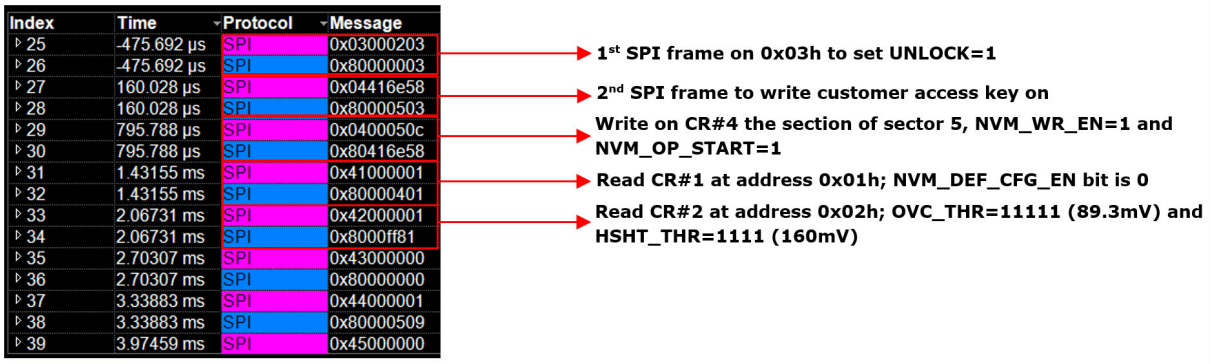
OP	ADDRESS							Data Byte 1								Data Byte 2								Data Byte 3							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	1	1	0	1	1	1	0	0	1	0	1	1	0	WD	P

- Function 2 of CR#4 is enabled. SPI write frame at CR#4 to set:
  - NVM_ADDR = 0x5 (bits [11:8]), the only available address for customer access
  - NVM_WR_EN = 1b (bit 3) for write operation
  - NVM_OP_START = 1b (bit 2) to give the NVM start command

OP		ADDRESS						Data Byte 1								Data Byte 2								Data Byte 3							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	WD	P

The NVM registers reading will start and all CRs will be checked in sequence (in pink the SDI message and in blue the SDO message):

Figure 4. NVM write: SPI log



5 Transition from Unlocked state to Locked state

If the NVM default configuration bit is enabled (NVM_DEF_CFG_EN = 1b bit 16 in CR#1), the device is configured with the fixed parameters that are stored into the NVM when the transition occurs from Unlocked state to Locked state.

Users are enabled to write into the RAM configuration register fields listed in Table 2, considering that those settings are stored as shadow registers that are not effective until the unlocked to locked transition occurs.

Other RAM control register fields, which are not part of the NVM default configuration and are mainly used for output control, feature activation, and specific device controls, which are writable by the user. These fields provide full output control while keeping the parameter settings fixed. The register fields that are not mapped into the NVM are reported in Table 3, derived from device datasheet.

Table 3. Control register fields (not NVM mapped)

Register field	Description	Use
CR#1 → OUTCTL	Output channel (external power switch) control	
CR#1 → BYPASSCTL	Internal bypass switch control	
CR#1 → S_T_START	Self-test start trigger	Effective only in the Unlocked/Self-test states
CR#1 → S_T_STOP	Self-test stop trigger	
CR#1 → S_T_CFG	Self-test type selection	
CR#1 → EN	Unlocked state transition control	
CR#1 → GOSTBY	Standby state transition control	
CR#1 → CCM_CTRL_ON	Capacitive charge mode start trigger	
CR#1 → CCM_CTRL_OFF	Capacitive charge mode stop trigger	
CR#1 → LOCKED_MODE_EN	Locked mode enable	
CR#1 → FS_CFG_UPLOAD	NVM configuration upload to RAM registers	
CR#3 → UNLOCK	Unlock access for specific control register fields	
CR#1,2,3,4,5 → WD_TRIG	Watchdog monitor trigger	

If the NVM default configuration bit is disabled (NVM_DEF_CFG_EN = 0b, bit 16 in the CR#1 register), the RAM configuration registers for the NVM (see Table 2) are locked to prevent unsafe changes to the device configuration while in the Locked or Fail-safe state: Fail-safe/locked states parameters setting depends on values stored into RAM registers.

If the NVM default configuration bit is enabled (NVM_DEF_CFG_EN = 1b, bit 16 in the CR#1 register), the RAM configuration registers for the NVM (see Table 2) are unlocked and are used by device while in the Locked or Fail-safe state: Fail-safe/Locked states parameters setting depends on values stored into NVM registers.

Example: let's suppose that the following parameters are written in the NVM and then perform the transition from Unlocked to Locked state:

- OVC = 26.5 mV (OVC_THR = 10000b in bits [15:11] of CR#2)
- HSHT_THR = 160 mV (HSHT_THR = 1111b in bits [10:7] of CR#2)
- NVM default configuration (NVM_DEF_CFG_EN = 1b in bit 16 of CR#1)

Environment setup:

- V_{SPI} = 3.3 V (same as µC supply)
- Shunt sense resistor = 5 mΩ
- Ambient temperature

- Device in Unlocked state
- V_{BATT} = 12 V
- R_{LOAD} = 2 Ω
- Nominal time = 1 s (T_NOM = 0x00, bits [23:16] in the CR#2 register)

In the Unlocked state, an OVC_THR of 41.7 mV (OVC_THR = 10111b), an HSHT_THR of 160 mV (HSHT_THR = 1111b), and a nominal time of 1 s (T_NOM = 0x00) are set in the CR#2. When the channel is turned on, the output will go high and the I^2t protection will not be triggered because the current flowing is lower than the set threshold (ΔV on R_{shunt} ~28.2 mV vs OVC = 41.7 mV), as shown in Figure 5.

Figure 5. Channel is turned on when the device is in Unlocked state and the I^2t protection is not triggered

Upon transitioning the device from Unlocked to the Locked state bit 14 of SR#1 is flagged as per Figure 7 (LOCKED_STATE = 1b), and the previously programmed NVM content is transferred into the RAM configuration registers. In this condition, when the channel is enabled, the load current exceeds the predefined OVC threshold, causing the I^2t protection triggering and the channel turning off after ~500 ms as shown in Figure 6.

Figure 6. I²t protection is triggered and the channel turning off after ~500 ms

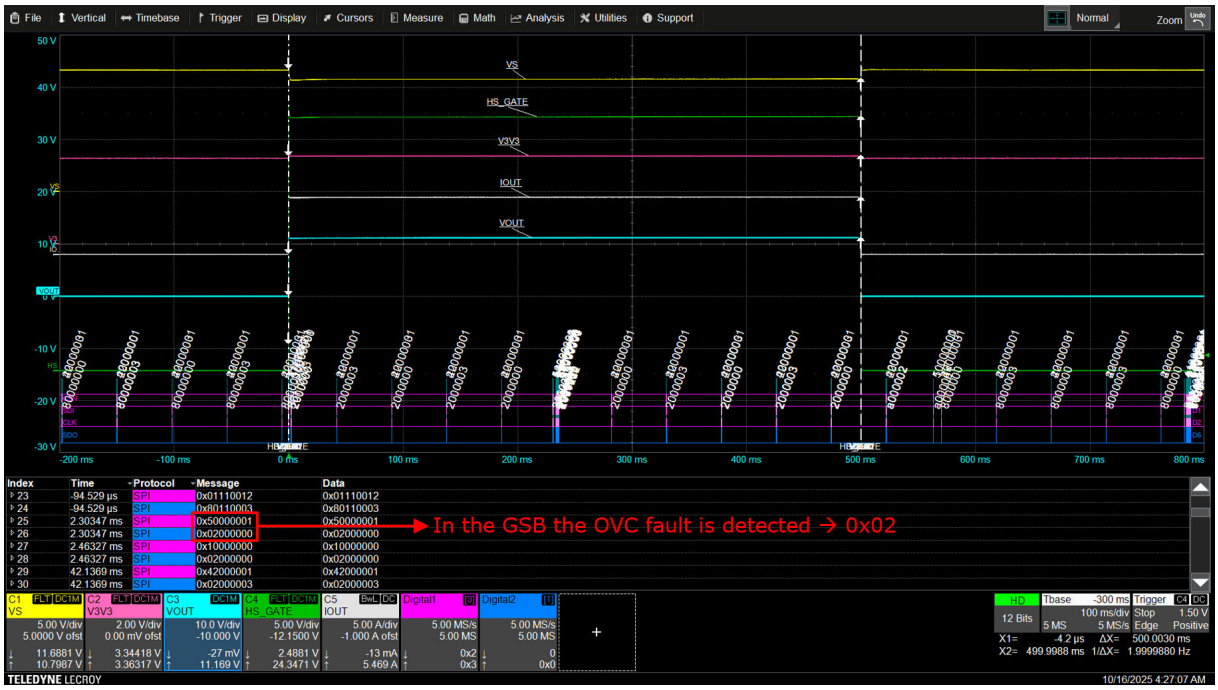
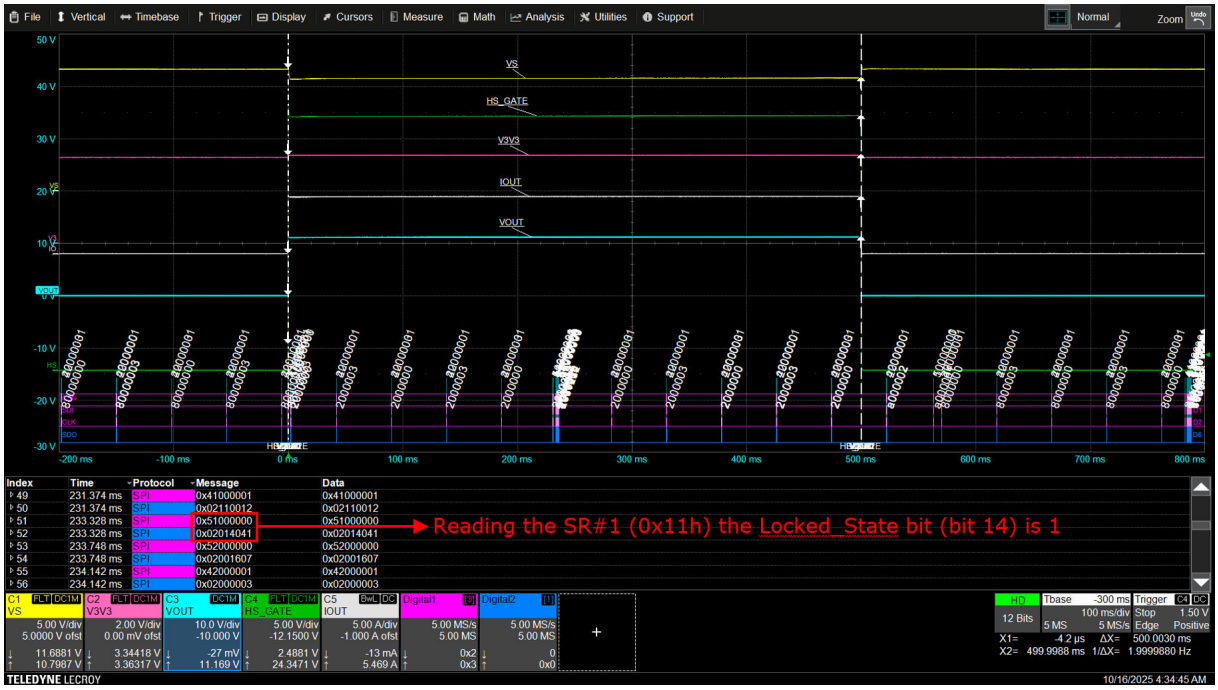


Figure 7. Device in Locked state



6 Transition from Unlocked state to Fail-safe state

Example: let's suppose that the following parameters are written in the NVM and then perform the transition from Unlocked to Fail-safe state:

- OVC = 26.5 mV (OVC_THR = 10000b in bits [15:11] of CR#2)
- HSHT_THR = 160 mV (HSHT_THR = 1111b in bits [10:7] of CR#2)
- NVM default configuration (NVM_DEF_CFG_EN = 1b in bit 16 of CR#1)

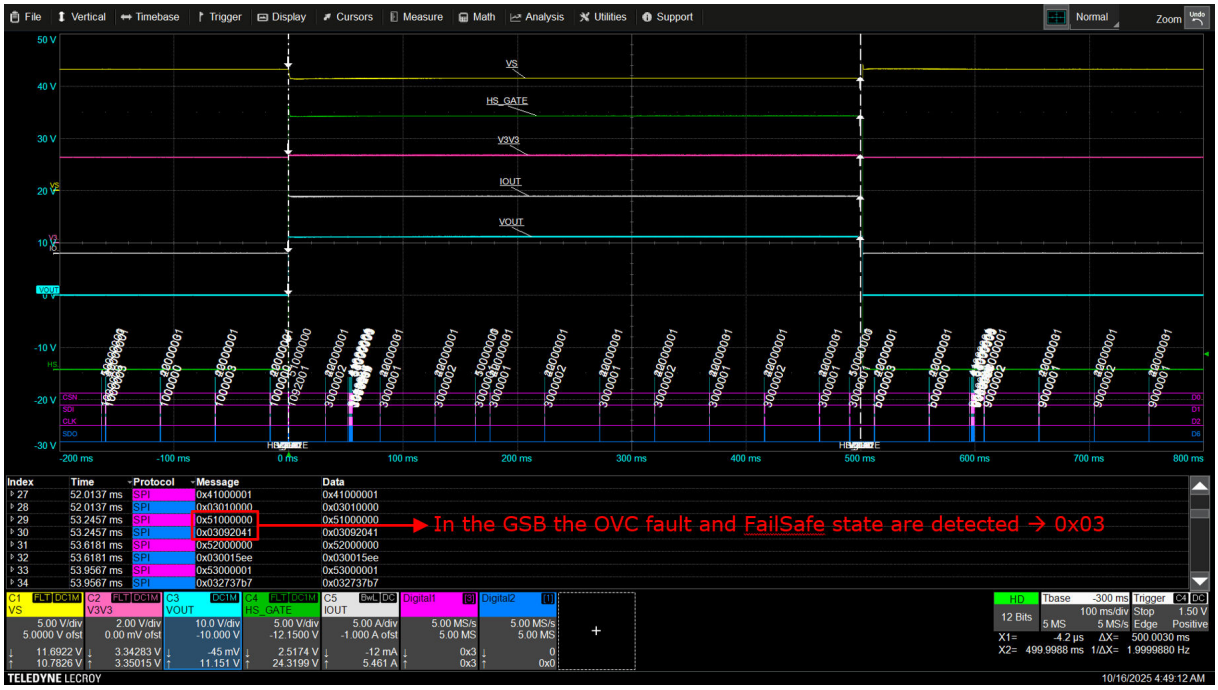
Environment setup:

- V_{SPI} = 3.3 V (same as µC supply)
- Shunt sense resistor = 5 mΩ
- Temp = Ambient temperature
- Device in Unlocked state
- V_{BATT} = 12 V
- R_{LOAD} = 2 Ω
- Nominal time = 1 s (T_NOM = 0x00, bits [23:16] in CR#2 register)

The output behavior, when the device is in the Unlocked state, is the same as the behavior described in Section 5 and Figure 5, with an OVC_THR of 41.7 mV (OVC_THR = 10111b), an HSHT_THR of 160 mV (HSHT_THR = 1111b) and a nominal time of 1 s (T_NOM = 0x00)

Upon transitioning the device from Unlocked to the Fail-safe state bit 13 on SR#1 is flagged (FAILSAFE_STATE = 1b) and the previously programmed NVM content is transferred into the RAM configuration registers. In this condition, when the channel is enabled through DIN, the load current exceeds the predefined OVC threshold, causing the I^2t protection to trigger and the channel turning off after ~500 ms as shown in Figure 8.

Figure 8. I^2t protection is triggered and the channel turning off after ~500 ms



Revision history

Table 4. **Document revision history**

Date	Revision	Changes
11-Dec-2025	1	First release.

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