Application note

Capacitive Charging Mode (CCM) for M0-9 Monolithic STi^{2}Fuse

Introduction

The purpose of this document is to demonstrate the functionality of the capacitive charging mode (CCM) feature in an application environment using the evaluation boards (EV-VNF9D5F and EV-VNF9Q20F) and the companion software package (STSW-EV-VNF9F) of M0-9 monolithic STi^{2}Fuse devices.

All the application examples refer to VNF9Q20F (quad channel STi^{2}Fuse) but they can be easily extended to VNF9D5F (dual channel STi^{2}Fuse).

All tests were conducted on a typical sample representative of the standard populations.

1 Capacitive Charging Mode (CCM) for M0-9 Monolithic STi2Fuse

The M0-9 monolithic STi^{2}Fuse HSD Family implements the CCM feature aimed to address the driving of capacitive loads for the power distribution domain.

STi^{2}Fuse HSD features an operative condition called capacitive charging mode (CCM) which is available in both Fail-safe and Normal mode device states when the channels are configured in bulb mode.

The CCM feature is selectable for each channel independently.

The capacitive charging mode charges the load capacitors with a burst of I_{CCM} pulses, provided that the total impedance is low enough to reach I_{CCM} when charging the capacitor. If I_{CCM} is not reached, the capacitor is charged with a single continuous charging pulse.

When a channel is set in capacitive charging mode and the output stage is turned on, an auto-restart procedure is started. If the ESR of the connected capacitor and the total output line impedance is low enough to let the output current reach the I_{CCM} value, then the channel will turn off after the differential thermal threshold of ΔT_{PLIM_CCM} has been reached, and autonomously turned on again after the differential thermal hysteresis goes below $\Delta T_{PLIM\_CCM\_HYST}$ = 7°C (typical value) threshold. In this operating mode, a smooth capacitor charging with low, moderate RMS current is enabled allowing the user to disable the I^2t wire harness protection. Thanks to the lower values of Δ_{TPLIM_CCM} and I_{CCM} compared to the normal operating mode, capacitor charging mode is compatible with capacitors up to C_{MAX} even in high ambient temperature conditions.

Table 1. CCM - Capacitive loads charging mode symbols

Symbol	Parameter
I_{CCM}	Charging current
t_{CCM_DIS}	Timing needed to leave CCM
t_{CCM_EN}	Timing needed to enter CCM
ΔT_{PLIM_CCM}	Junction-case temperature difference triggering power limitation
C_{MAX}	Maximum capacitive load
ESR	Equivalent series resistance of the capacitor
T_{TSD}	Shutdown temperature
MCUext	Bit #9 of RAM registers “FSITCR$_x$” (one register for each channel)

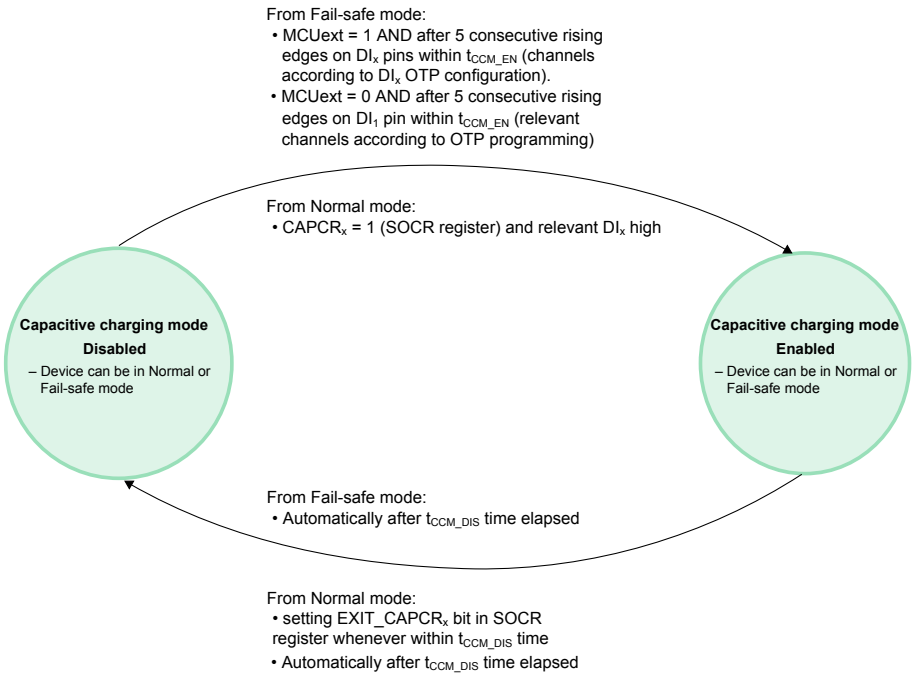
As anticipated above, the CCM function for M09 monolithic eFuses can be activated either from **Fail-safe** or from **Normal** states:

Table 2. Application operating conditions

Entering conditions	Leaving conditions	Characteristics
From Fail-safe mode: • If `MCUext = 1` AND after 5 consecutive rising edges on DI$_x$ pins within t_{CCM_EN}, the corresponding channels will enter the CCM, according to DI$_x$ OTP configuration. • If `MCUext = 0` AND after 5 consecutive rising edges on DI$_1$ pin within t_{CCM_EN}, according to the OTP programming, relevant channels will enter the CCM.	Automatically after t_{CCM_DIS} time frame in both Fail-safe mode and Normal mode states.	• Harness protections: disabled • LED mode: disabled • SPI: active • Latch-off delay time ($t_{D\_RESTART}$) after TSD event is disabled
From normal mode: • Set CAPCR$_x$ bit in the SOCR register	Automatically after t_{CCM_DIS} time frame in both fail-safe and normal states. Through a SPI frame, setting EXIT_CAPCR$_x$ bit in the SOCR register whenever within the t_{CCM_DIS} time frame	

The state of the channel of the CCM can be represented by the following diagram:

Figure 1. CCM channel states



If the device is in Fail-safe mode, then it is possible to exit from the CCM automatically after t_{CCM_DIS} time is elapsed.

If the device is in Normal mode, then it is possible to exit from the CCM by setting the EXIT_CAPCR$_x$ bit in the SOCR register whenever within t_{CCM_DIS} time or automatically after t_{CCM_DIS} time is elapsed.

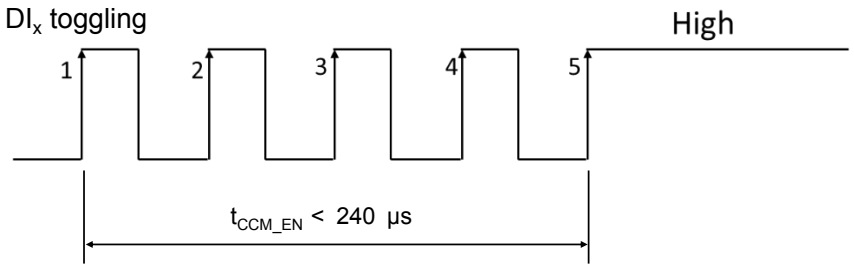
When a channel is in CCM, the I^2t protection on that specific channel is disabled, however, in CCM, the wire harness remains in any case fully protected, since the CCM mode is the latest aborted after t_{CCM_DIS}, keeping the RMS current low overall.

2 Activation Details

2.1 Procedure to enter CCM from Fail-safe mode

- If `MCUext = 1`, after 5 consecutive rising edges on DI_0 and/or DI_1 pins within 240 µs, the corresponding channels will enter CCM, according to the DI_x OTP configuration (see "**OTP memory map - MCUext = 1**" of the product datasheet).

Figure 2. CCM activating sequence



- If `MCUext = 0`, after 5 consecutive rising edges on the DI_1 pin within 240 µs as above, according to OTP mapping, relevant channels shall enter CCM.

For more information regarding the MCUext and DI_x configuration, please see the device datasheet.

2.2 Procedure to enter CCM from Normal mode

Set the $CAPCR_x$ bit in the SOCR register to enter CCM.

During CCM, the following behaviours are applied:

- Harness protection is disabled.
- Latch-off delay time after TSD ($t_{D\_RESTART}$) is disabled.

2.3 Procedure to exit CCM from Fail-safe mode

The CCM is automatically aborted after t_{CCM_DIS}.

2.4 Procedure to exit CCM from Normal mode

The CCM is automatically aborted after t_{CCM_DIS}.

In the Normal mode, the CCM can also be aborted through an SPI communication, setting the $EXIT\_CAPCR_x$ bit in the SOCR register, whenever within the t_{CCM_DIS} time frame.

3 Capacitive charging examples

The following CCM procedures are explored here.

The first two examples show good CCM setup, while the other three show some limited cases that should be avoided.

When CCM is enabled, in general, the following parameters must be considered:

- ΔT_{PLIM_CCM} threshold (30°C, or 35°C depending on the monolithic eFuse)
- I_{CCM} = 0.4 * I_{LimH} (typical value of the CCM current)
- t_{CCM_DIS} = 100 ms (typical value, timing needed to leave the capacitive charging mode)
- Harness protection disabled

Device under test: VNF9Q20F, mounted on the EV-VNF9Q20F, connected to the discovery board EV-SPC582B (flashed with the companion firmware, and driven by the GUI, both included in the software package STSW-EV-VNF9F)

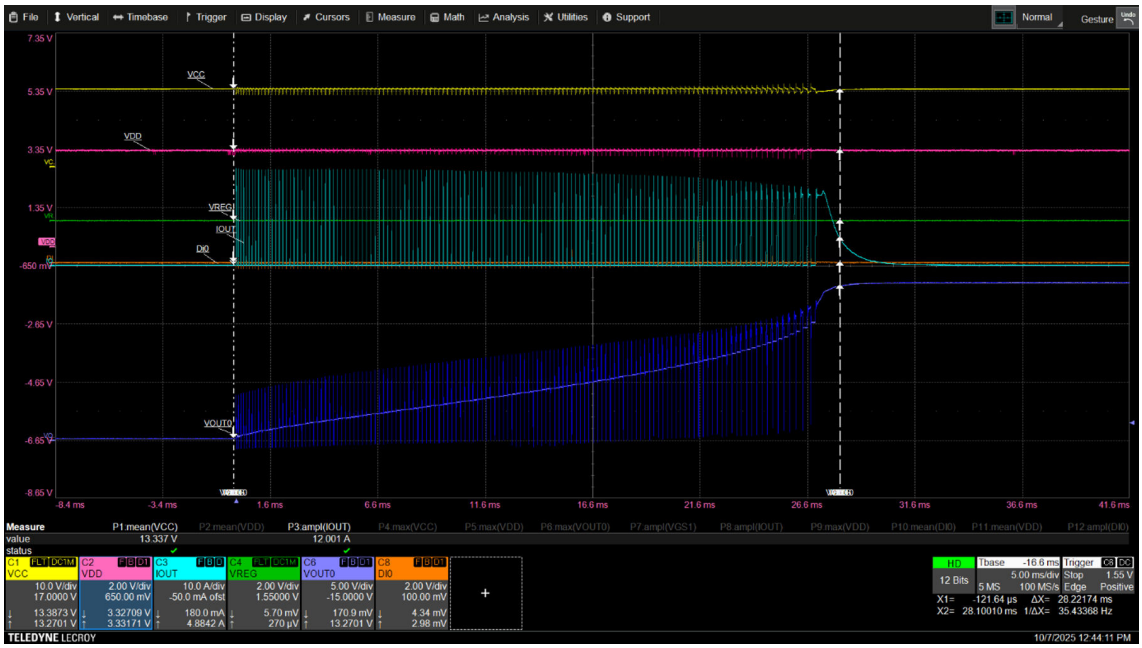
3.1 Example 1 (Normal mode operation)

Bench setup:

- Tested device channel: CH_0 in bulb mode, **CCM mode, and Normal mode**, with latch-off counter, set to max (0xF) in the GUI.
- Supply voltage: 13.5 V
- Ambient temperature: 25°C
- DI_0 = HIGH
- OUT_0 enabled by writing bits $SOCR_0$ = 1 together with $CAPCR_0$ = 1 in the SOCR register

*Note: When the VNF9Q20F and VNF9D5F devices are in the Normal mode, the outputs are activated according to the SPI register settings **or** DI_x input pins (see **direct input block diagram - valid for both 2 and 4 channels device** figure in the respective product datasheet for more details). Consequently, because the CCM timing is synchronized with $CAPCR_x$ bits in the SOCR register, to properly manage the CCM time window (t_{CCM_DIS} = 100 ms typically), it is enough to set both $SOCR_x$ and $CAPCR_x$ bits in the SOCR register (within the same SPI write).*

Figure 3. Capacity charging 13.5 V, Tj = 25°C, C = 4.7 mF, ESR = 27 mΩ, $T_{Saturation}$ = 31 ms



OUTCOME: 4.7 mF charged in 31 ms.

3.2 Example 2 (Fail-safe mode operation)

Bench setup:

- Device in **Standby mode initially and then to Fail-safe mode**
- **`MCUext = 1`** (OTP config: Bit 1 = 0, Bit 0 = 0)
- V_{CC} = 16 V
- V_{DD} = 3.3 V
- C_{LOAD} = 2.2 mF
- Channel immediately turned on as soon as the device is moved from standby to **FS**

Figure 4. CCM mode MCUext = 0, DI_0 toggled

To enable the CCM in Fail-safe mode, it is mandatory to send five rising edges on DI_1 as specified before (Figure 5).

OUTCOME: 2.2 mF charged in 19 ms.

Figure 5. **Rising edge particular of DI_0**

If DI_0 is not driven to enter the CCM mode (five consecutive pulses), the device tries to load the capacitor in High-Side mode (with the nominal ILIM value).

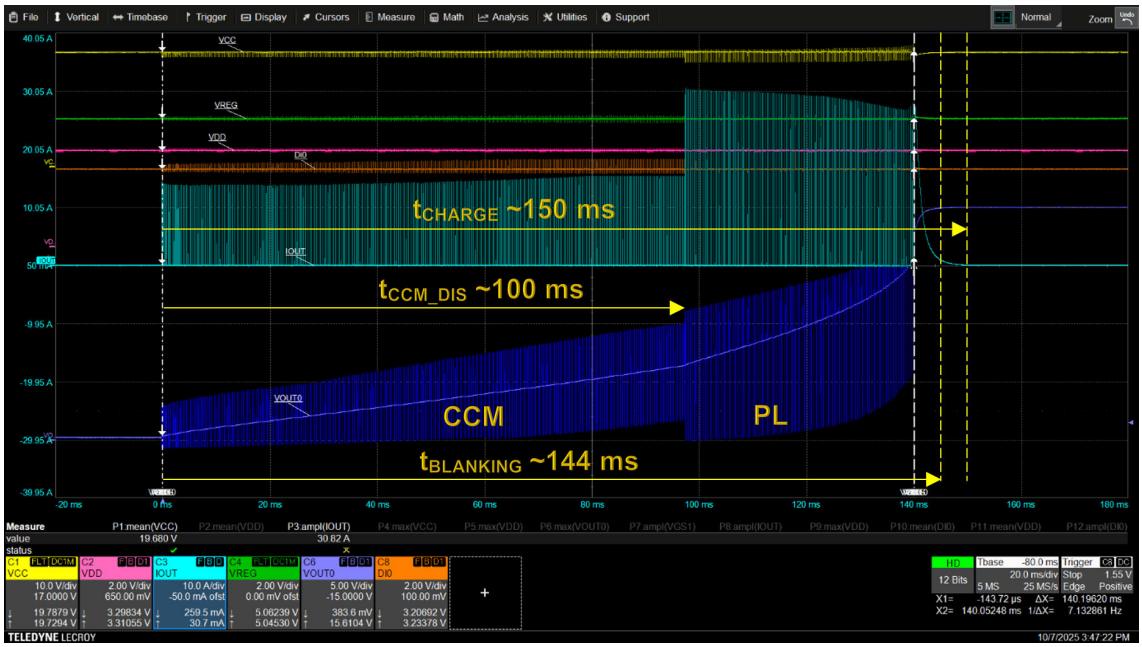
3.3 Example 3

Bench setup:

- **Normal mode**
- V_{CC} = 20 V
- V_{DD} = 3.3 V
- C_{LOAD} = 10 mF
- Ambient temperature: 25°C
- Latch-off time / $t_{BLANKING}$ = 144 ms (0x9) (CHLOFFTCR0$_x$ [x = 0, 1, 2, 3] = 0x9)

This is a case where CCM charging is followed by power limitation until the capacitor is fully charged.
Even though the capacitor is fully charged, it is recommended to avoid exceeding the t_{CCM_DIS} because using the device in power limitation mode, the thermal shutdown protection may be triggered (see Figure 6).
After t_{CCM_DIS} has elapsed (typically 100 ms with ΔT_{PLIM_CCM} = 35°C), the device exits automatically from the CCM mode and the capacitor continues to charge in power limitation (PL) condition (with ΔT_{PLIM} = 41°C typically), till it is fully charged.

Figure 6. CCM charging + power limitation till the cap is fully charged



The capacitor was successfully charged in a longer time, roughly 150 ms

OUTCOME: 10 mF charged in 150 ms.

3.4 Example 4

The following example shows one limited case where the actuation can be influenced by the intervention of the latch-off time. Here, the CCM charging period is followed by the power limitation condition until the programmed latch-off time expires. In this case, the capacitor will not be fully charged.

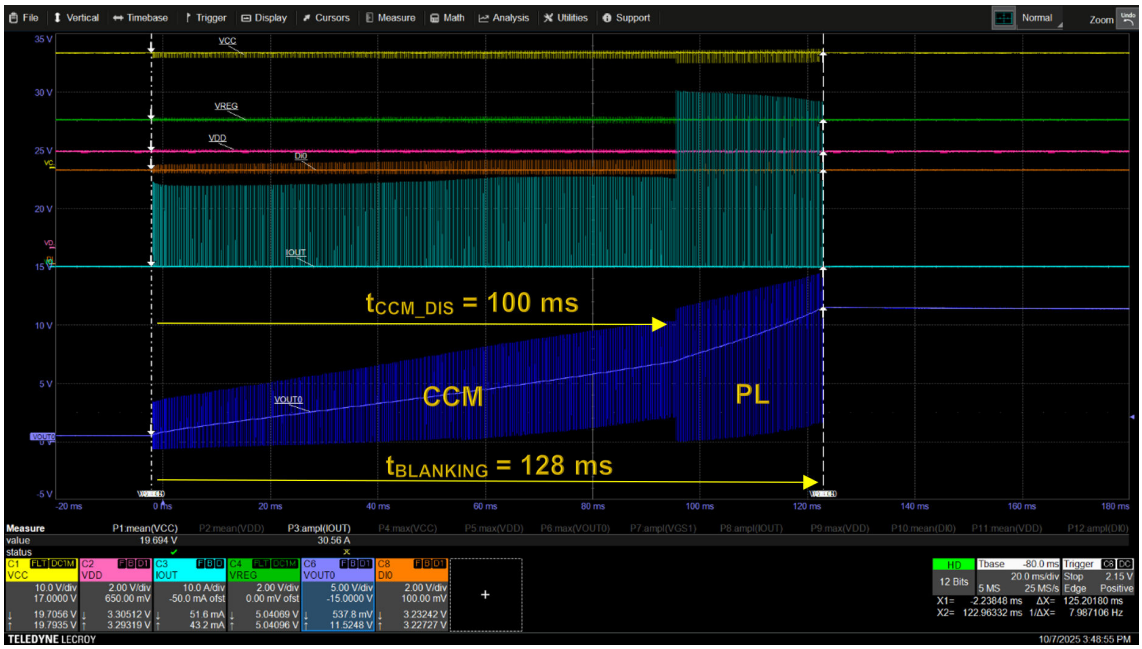
Bench setup:

- **Normal mode**
- V_{CC} = 20 V
- V_{DD} = 3.3 V
- C_{LOAD} = 10 mF
- Ambient temperature: 25°C
- Latch-off time / $t_{BLANKING}$ = 128 ms (0x8) (CHLOFFTCR0$_x$ [x = 0, 1, 2, 3] = 0x8)

In this case, the capacitor is not fully charged.

In fact, after t_{CCM_DIS} has elapsed (typically 100 ms with ΔT_{PLIM_CCM} = 35°C), the device exits the CCM mode and the capacitor continues to be charged in power limitation (PL) condition (with ΔT_{PLIM} = 41°C typically), till the programmable latch-off time of the channel has elapsed, **128 ms (0x8)**.

Figure 7. CCM charging + power limitation till the programmed latch-off time (128 ms)



The device was not able to charge the capacitor.

OUTCOME: capacitor not charged. V_{OUT} reached 11.5 V after $t_{BLANKING}$ time.

3.5 Example 5

In the following example, a limited case is shown: the actuation can be influenced by the intervention of the thermal shut-down (TSD).

The device exits from the CCM mode continuing to charge in power limitation till a TSD event (thermal shut-down) occurs.

After t_{CCM_DIS} has elapsed (typically 100 ms with ΔT_{PLIM_CCM} = 35°C), the device exits the CCM mode and the capacity continues to charge in power limitation (PL) condition (with ΔT_{PLIM} = 65°C typically) and a TSD event (with 50 ms delay of auto-restart), till it is fully charged.

Bench setup:

- **Normal mode**
- V_{CC} = 16.5 V
- V_{DD} = 3.3 V
- C_{LOAD} = 22 mF
- Ambient temperature: Hot temperature (T_a ~80°C)
- Latch-off time / $t_{BLANKING}$ = 240 ms (0xF) (CHLOFFTCR0$_x$ [x = 0, 1, 2, 3] = 0xF)

Figure 8. CCM charging with t_{CCM_DIS}, expired, and TSD event occurred during power limitation

OUTCOME: capacitor charged but in a very long time (~238 ms), but less than 240 ms (programmed latch-off).

If the same test is performed at a higher ambient temperature (T_a > 80°C), a continuous thermal shutdown may be triggered as in the following figure:

Figure 9. CCM charging with t_{CCM_DIS}, expired, and TSD event occurred during power limitation with TSD events till Latch_OFF time expiration without charging completion

OUTCOME: capacitor not charged with V_{OUT} reaching 3.3 V.

Revision history

Table 3. **Document revision history**

Date	Revision	Changes
16-Dec-2025	1	First release.

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