L9026 multi-channel driver, Off-state diagnostics overview

Introduction

The L9026 is an eight-channel IC, with two fixed HS drivers and six configurable HS/LS drivers designed for automotive applications (LEDs and relays) and compatible with resistive, inductive, and capacitive loads.

The device supports a wide set of diagnostic features such as overcurrent/overtemperature protections, open-load, short to ground and short to battery.

This document focuses on the open-load and short-circuit diagnostics.

The open-load/short-circuit diagnostics are available when the output channel is turned off and occur in two phases. The first phase determines if there is a potential fault condition with the output. A first-phase fault could be due to either an open-load or short-circuit condition. In phase one, if no fault is detected, then the second phase is not started. If the first phase detects a fault condition, the second phase of the diagnostics is used to differentiate between the open-load and short-circuit conditions.

In addition to the details of the diagnostics behavior, this document will also detail the interaction of the off-state diagnostics with ESD capacitance and its limitations.

Important note: The device characteristics listed in this document are for reference purposes only. Please refer to the current device datasheet, DS13397, for details on the operation of the device and current parametric data.

1 Off-state diagnostics overview

The L9026 supports on-demand diagnostics when the output channel is turned off and the device is in Active mode. The off-state diagnostics can be initiated by writing to the DIAG_OFF_EN register. For each of the eight channels, it is possible to either activate the off-state diagnostic (DIAG_OFF_EN[x] = ‘1’) or not activate it (DIAG_OFF_EN[x] = ‘0’).

Each time this register is written, and after any previous sequence has completed, a new diagnostics sequence is started. If a previously started diagnostic sequence is in progress and a new request is made, the device waits until the current sequence has been completed before starting the new request. The off-state diagnostics are available for both high-side and low-side configurations. The diagnostics can be activated and run on any number of off-state channels in parallel.

The off-state diagnostic sequence is essentially sourcing and sinking a small amount of diagnostic current to the load for a fixed time, and then comparing the voltage obtained on the load side after the diagnostic current application. The behavior between the high-side and low-side configuration differs and is explained in detail in the following sections.

2 Low side configuration diagnostics

2.1 Low side Off-state phase one

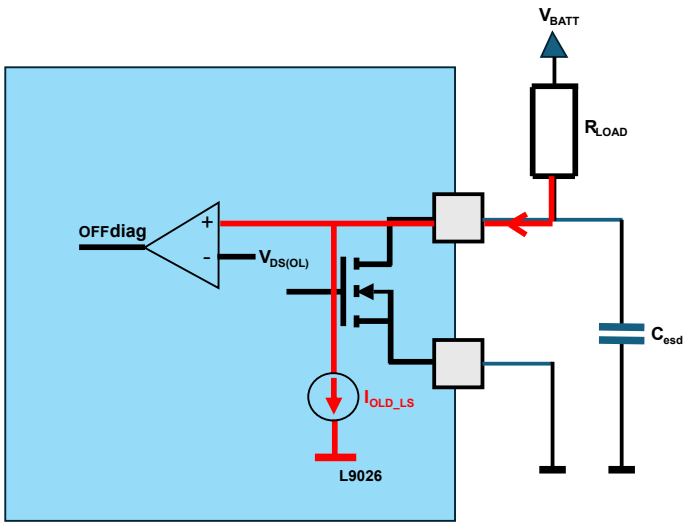
As noted previously, the low-side off-state diagnostic has two phases in the sequence. The first phase enables a pull-down current source I_{OLD_LS} for the duration of t_{OFF1LS} time (1.03 ms typical value). The voltage generated by the pull-down current flowing through the load is compared to the $V_{DS(OL)}$ threshold.

Table 1. Low-side diagnostic parameters

Symbol	Description	Test condition	Min	Typ	Max	Unit
Output status monitor						
$V_{DS(OL)}$	Output status monitor threshold voltage	V_{BATT} = 14 V; Active	1.7	1.95	2.2	V
I_{OLD_LS}	Output diagnosis pull-down current (channels used as low-side)	V_{DRAIN} = 14 V (channels used as low-side)	290	-	550	µA
I_{OLU_LS}	Output diagnosis pull-up current (channels used as low-side)	V_{DRAIN} = 0 V (channels used as low-side)	-260	-	-140	µA
I_{OLD_HS}	Output diagnosis pull-down current (channels used as high-side)	V_{SOURCE} = 14 V (channels used as high-side)	320	-	520	µA
I_{OLU_HS}	Output diagnosis pull-up current (channels used as high-side)	V_{SOURCE} = 0 V (channels used as high-side)	-310	-	-160	µA

This is graphically represented in Figure 1.

Figure 1. Low-side diagnostics phase one



The comparator output is checked after the first window time (t_{OFF1LS}). If the voltage generated by the load is greater than $V_{DS(OL)}$, the load is determined to be present, the internal OFF diagnostics signal is low, no fault is detected, and the diagnostic sequence stops.

However, the load is connected to the battery in the low-side configuration. The battery voltage creates a dependency in determining the presence of a load because the battery is the voltage source of the load. Since the battery voltage will likely not be a fixed value through the lifetime operation of the device, the variability of the battery voltage must also be considered. The $V_{DS(OL)}$ voltage measured by the device during the first diagnostic phase is found by:

$$V_{DS(OL)} = V_{BATT} - \left(R_{\mathrm{LOAD}} * I_{\mathrm{OLD\_LS}}\right)$$

Rearranging the above equation to find R_{LOAD}:

$$R_{LOAD} = \frac{(V_{BATT} - V_{DS(OL)})}{I_{OLD\_LS}}$$

The worst-case condition for detecting a fault is when $V_{DS(OL)}$ is at its maximum and I_{OLD_LS} is at its minimum. Substituting these values in the equation below leaves a dependency on the battery voltage:

$$R_{LOAD} = \frac{(V_{BATT} - 2.2V)}{290\mu A}$$

The normal battery voltage range is assumed to be 9 V to 16 V. Therefore, the load impedance spread for the given battery voltage range to always detect a fault condition from the equation above are 47.59 kΩ (at 16 V) to 23.45 kΩ (at 9 V).

There is also a window where the device may indeterminately detect a fault condition. One end of the window is at the maximum load impedance (noted above) where a fault is guaranteed to flag a fault, and the other end of the window is the point where a fault is guaranteed not to be flagged. The point where a fault will not be flagged occurs when $V_{DS(OL)}$ is at its minimum and I_{OLD_LS} is at its maximum. This results in:

$$R_{LOAD} = \frac{(V_{BATT} - 1.7V)}{550\mu A}$$

Given the same battery operating range as above and using the equation above, a load impedance less than 26 kΩ (at 16 V) to 13.27 kΩ (at 9 V) will always be detected as load present.

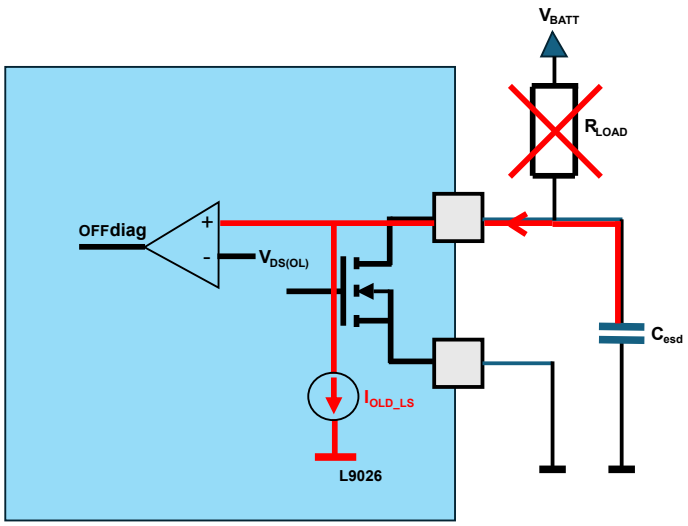
In summary, the load impedance ranges for the fault detection criteria for phase one of the low-side diagnostic sequence are:

Table 2. Impedance range versus battery

V_{BATT}	Fault condition	R_{LOAD} (kΩ)	Indeterminate range (kΩ)
9	No fault detected	< 13.27	13.27 < R_{LOAD} < 23.45
	Fault detected	> 23.45	
16	No fault detected	< 26.00	26.00 < R_{LOAD} < 47.59
	Fault detected	> 47.59	

If the load is missing, the diagnostic current pulls a charge from the ESD capacitor as shown in Figure 2.

Figure 2. Low-side diagnostics phase one, no load



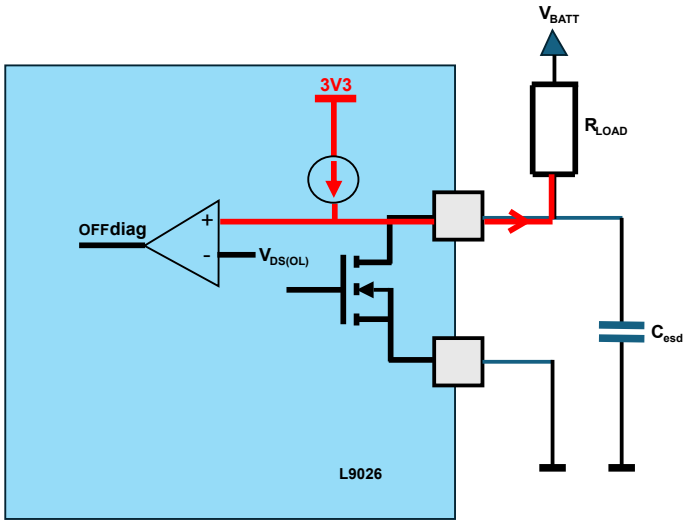
In case of a missing load, the only load seen by the device is the ESD capacitor (C_{ESD}) as shown in Figure 2. If the voltage generated with the application of the diagnostic current is less than $V_{DS(OL),}$ a fault condition is present, the internal OFF diagnostics signal is high, and the diagnostic sequence advances to phase two. The diagnostic current will typically discharge the ESD capacitor. The resulting capacitor voltage at the end of phase one is typically below the $V_{DS(OL)}$ threshold. This allows a fault to be detected with only the ESD capacitor present.

2.2 Low side Off-state phase two

The second phase of the diagnostic sequence is only entered if a fault condition is detected in phase one. The purpose of the second phase is to determine the type of fault condition, either open-load or short-to-ground. The second phase enables a pull-up current source I_{OLU_LS} for the duration of t_{OFF2LS} time (250 µs typical value). The voltage generated by the pull-up current flowing through the load is compared to the $V_{DS(OL)}$ threshold. The phase two current and duration parameters are found in Table 1.

The diagnostic pull-up current load interaction is graphically represented in Figure 3.

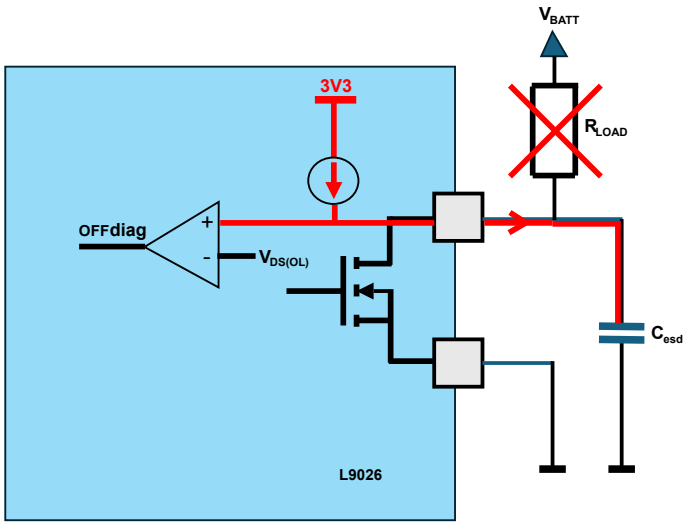
Figure 3. Low-side diagnostics phase two



The resulting voltage of the application of the diagnostic current at the comparator is used to determine if the fault condition is an open-load or a short-to-ground. If the voltage at the comparator is greater than $V_{DS(OL)}$, the internal OFF diagnostics signal is high, and an open-load fault is flagged. Conversely, if the comparator input voltage is lower than the $V_{DS(OL)}$ threshold, the OFF diagnostics signal is low, and a short to ground fault is flagged. The battery voltage again is a factor in the detection of an open-load condition. However, if the battery voltage is greater than the internally generated 3.3 V source and a load impedance is present, an open-load fault will be flagged. If the voltage at the drain of the output is less than $V_{DS(OL)}$, a short-to-ground will be flagged.

The most interesting case is when R_{LOAD} is not connected, leaving only the ESD capacitor as the load on the output as shown in Figure 4.

Figure 4. **Low-side diagnostics phase two, no load**



The same criteria are applied to this case where the diagnostic current will charge the capacitor. This will create a voltage on the capacitor, which will be compared against the $V_{DS(OL)}$ threshold. Depending on the size of the capacitor, this could create a situation where, if the capacitor is not charged above the $V_{DS(OL)}$ threshold, the diagnostic result will incorrectly determine that a short-to-ground is present instead of the correct open-load condition. This is covered in more detail in the next section.

2.3 Low side Off-state ESD capacitance interactions

The main area of interest with the ESD capacitor interactions for the diagnostics on the low-side is during the second phase. The ESD capacitor is likely to be fully discharged in the first phase, allowing the second phase to progress. If the load is missing, the diagnostic current charges the ESD capacitor in the second phase of the diagnostic sequence. The size of the capacitor, the amount of diagnostic current, and the time the diagnostic current is applied will impact the resulting capacitor voltage. The goal is to ensure that the device correctly determines that the load is missing and an open-load fault is flagged.

The analysis is based on the capacitor current – voltage relationship defined by:

$$i = c * \frac{\mathrm{dv}}{\mathrm{dt}}$$

As per Table 1, the device will supply a diagnostic current of I_{OLU_LS} for the duration of t_{OFF2LS} . The worst-case condition guarantees that the charge on the ESD capacitor will result in a capacitor voltage that is high enough to trigger an open-load condition when the diagnostic current and duration are at their minimums, and the $V_{DS(OL)}$ threshold is at its highest. Rearranging the equation above to solve for capacitor C:

$$c = i * \frac{\mathrm{dt}}{\mathrm{dv}}$$

Inserting the worst-case parameters into the above equation yields:

$$c = 140\mu\mathrm{A} * \frac{210\mu\mathrm{S}}{2.2\mathrm{V}} = 13.36\mathrm{nF}$$

An ESD capacitor greater than 13.36 nF will not guarantee that an open-load will be detected when just the ESD capacitor is connected to the output. Too large of an ESD capacitor cannot be charged above the maximum $V_{DS(OL)}$ threshold given the minimum diagnostic current and the minimum time. This results in a lower capacitor voltage, which is below the $V_{DS(OL)}$ threshold and causes the device to incorrectly flag a short-to-ground condition instead of the correct open-load condition.

Just as with the first phase and the range of impedances to cause a fault condition, the amount of capacitance also has an indeterminate range where the device may detect an open-load condition. The end of the window occurs where the amount of capacitance will guarantee that the device will always incorrectly determine a short-to-ground condition when the load is missing. The worst-case parameters to guarantee that a short-to-ground will be incorrectly flagged are when the diagnostic current and duration are at their maximums and the $V_{DS(OL)}$ threshold is at its lowest:

$$c = 260\mu A * \frac{290\mu S}{1.7V} = 44.30nF$$

In summary, the amount of ESD capacitance impacts the ability of the second phase to correctly determine the diagnostic state of the output when the load is missing:

Table 3. Low-side phase two ESD capacitance diagnostics behavior

Amount of ESD capacitance (C_{ESD})	Device behavior – missing load
< 13.36 nF	Correctly flags an open-load condition, across all device parameters
> 44.30 nF	Incorrectly flags an open-load condition as short-to-ground, across all device parameters
13.36 nF < C_{ESD} < 44.30 nF	May indeterminately flag an open-load or short-to-ground, depending on device characteristics

2.4 Low side Off-state diagnostic examples

The following oscilloscope plots show the behavior of the device when activating the off-state diagnostics and the influence the ESD capacitance has on the detected result. The first examples are using the 10 nF ESD capacitance placed on the evaluation board with no load connected.

Figure 5. Multiple low-side diagnostics activations, no load, C_{ESD} = 10 nF

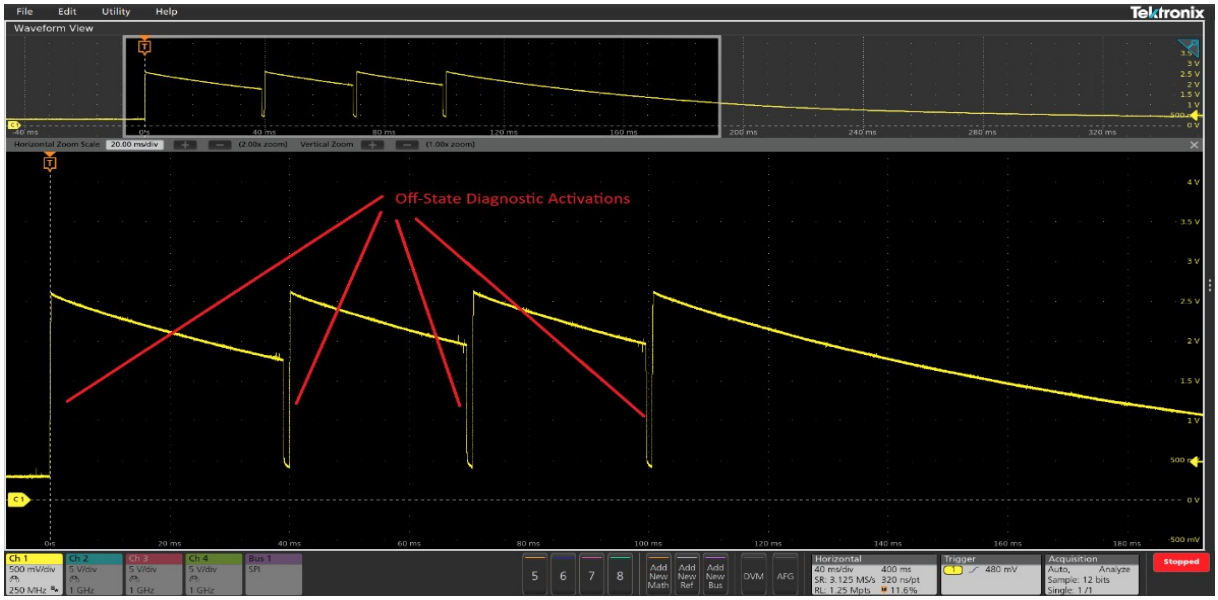


Figure 5 captures multiple sequential diagnostics requests to show the interactions of the first and second phases of the diagnostic sequence. The first phase discharges the ESD capacitance via the pull-down current. Note that the limiting low voltage during the discharge (pull-down) segment is the bias supply of the pull-down current source. The device cannot pull the output down to 0 V due to the bias voltage. The second phase enables a pull-up current source to charge the ESD capacitor. After the diagnostic sequence completes, the residual voltage on the ESD capacitor gradually dissipates due to device leakages.

Figure 6. Single low-side diagnostics activation, no load, C_{ESD} = 10 nF

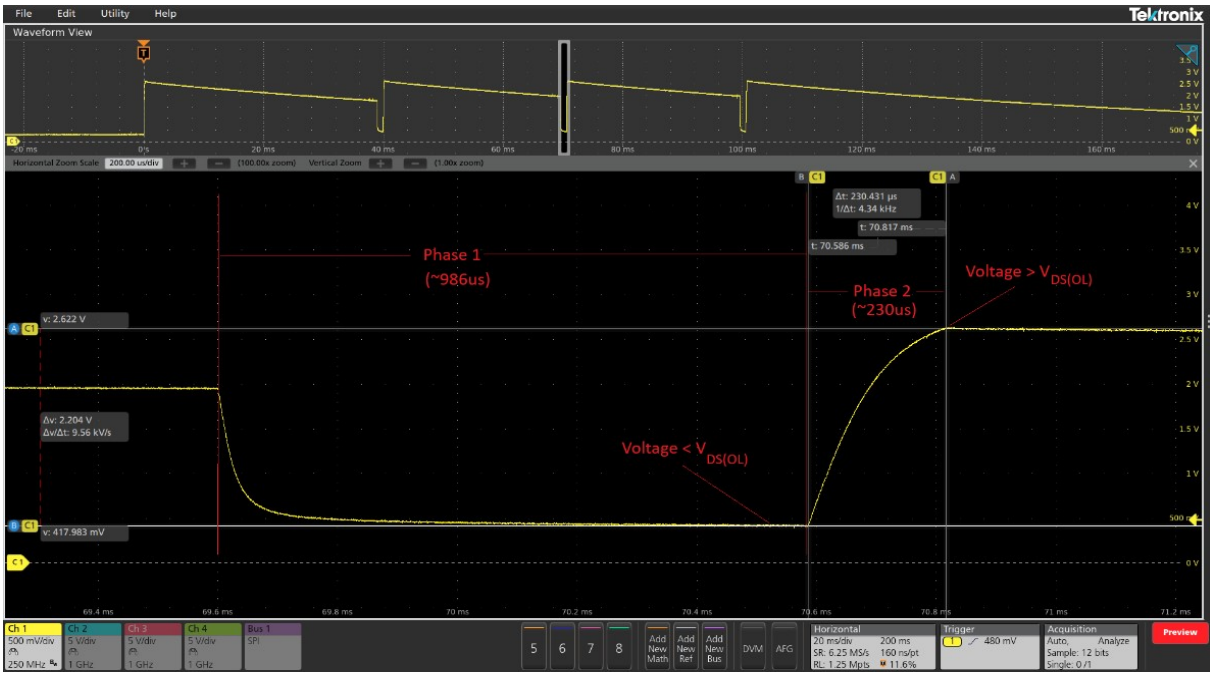


Figure 6 captures the details of a single diagnostics request. In the first phase, the residual charge on the ESD capacitor is discharged by the diagnostic pull-down current. The device enables the pull-down current source for around 986 µs and then compares the output voltage to the $V_{DS(OL)}$ threshold.

In the capture above, the output voltage (417 mV) is much lower than the minimum $V_{DS(OL)}$ threshold, which indicates a fault condition. This advances the diagnostic sequence to phase two, where a pull-up current is enabled. The device enables the pull-up current for around 230 µs for phase two and compares the output voltage at the end of the phase against the $V_{DS(OL)}$ threshold. The capture shows that the resulting output voltage (2.6 V) is greater than the maximum $V_{DS(OL)}$ threshold. Based on this, the device correctly flags an open-load result.

The second case will investigate the behavior of the device by increasing the ESD capacitance to 110 nF. This is accomplished by adding 100 nF to the output pin of the evaluation board, still with no load connected.

Figure 7. **Multiple low-side diagnostics activations, no load, C_{ESD} = 110 nF**

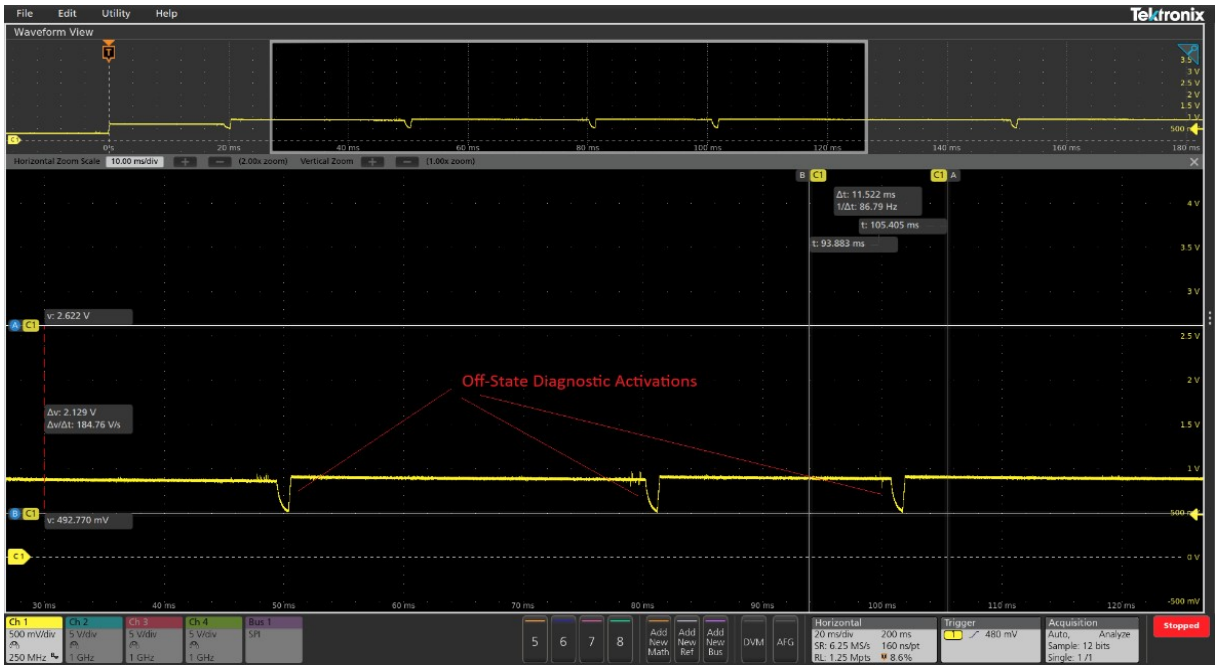


Figure 7 shows multiple sequential diagnostics requests with a total ESD capacitance of 110 nF with no load connected to the output.

Figure 8. **Single low-side diagnostics activation, no load, C_{ESD} = 110 nF**

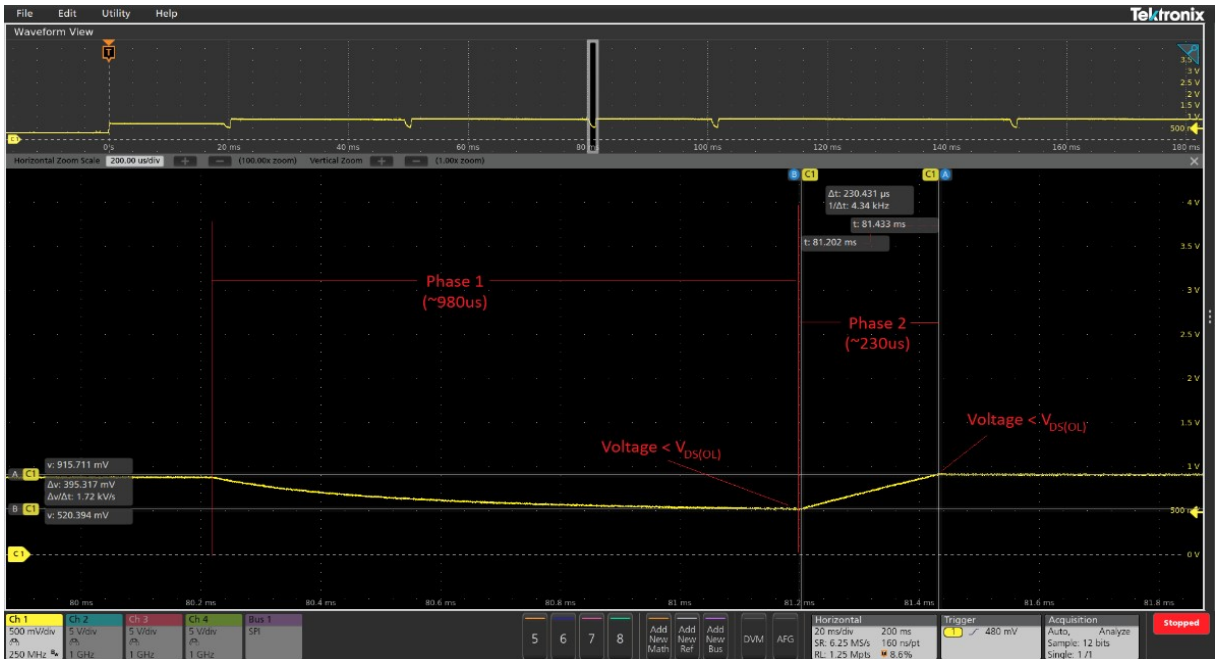


Figure 8 shows the details of a single diagnostics activation with the increased ESD capacitance. In phase one, the residual charge on the ESD capacitor is discharged by the diagnostic pull-down current. In phase one, the device enables the pull-down current source for around 980 µs and then compares the output voltage to the $V_{DS(OL)}$ threshold. In the capture above and at the end of phase one, the output voltage (520 mV) is much lower than the minimum $V_{DS(OL)}$ threshold, which indicates a fault condition. This advances the diagnostic sequence to phase two, where a pull-up current source is enabled. The device enables the pull-up current for around 230 µs and compares the output voltage at the end of phase two against the $V_{DS(OL)}$ threshold. The capture shows that the resulting output voltage (915 mV) is lower than the minimum $V_{DS(OL)}$ threshold. Based on this, the device incorrectly flags a short-to-ground result.

The combination of the diagnostic current used to charge the ESD capacitor, the length of time the diagnostic current is applied, and the amount of capacitance, all contribute to the resulting voltage on the ESD capacitor at the end of the phase. The device controls the amount of diagnostic current and the time that the diagnostic current is applied but the application controls the amount of ESD capacitance. These factors must be considered when selecting the ESD capacitance to allow diagnostics to function correctly.

3 High side configuration diagnostics

3.1 High side Off-state phase one

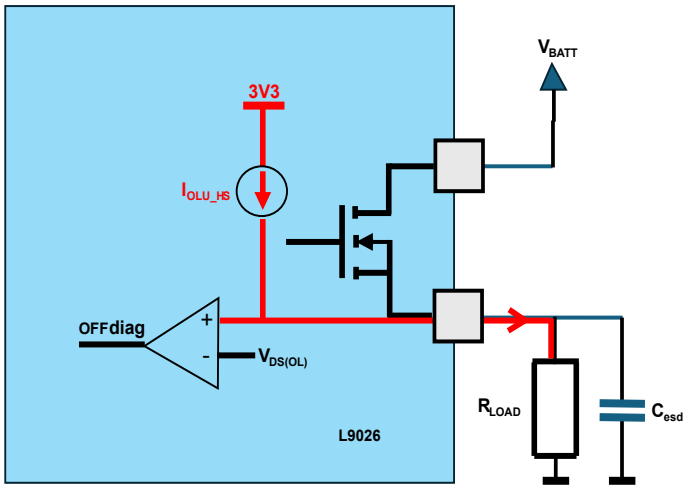
Like the low-side off-state diagnostic, the high-side off-state diagnostics has two phases in the sequence. However, the order and direction of the pulling currents are reversed, and the threshold trigger points are also reversed. The first phase enables a pull-up current source I_{OLU_HS} for the duration of t_{OFF1HS}. The voltage generated by the pull-up current flowing through the load is compared to the $V_{DS(OL)}$ threshold as listed in Table 4

Table 4. High-side diagnostic parameters

Symbol	Description	Test condition	Min	Typ	Max	Unit
Output status monitor						
$V_{DS(OL)}$	Output status monitor threshold voltage	V_{BATT} = 14 V; Active	1.7	1.95	2.2	V
I_{OLD_HS}	Output diagnosis pull-down current (channels used as high-side)	V_{SOURCE} = 14 V (channels used as high-side)	320	-	520	µA
I_{OLU_HS}	Output diagnosis pull-up current (channels used as high-side)	V_{SOURCE} = 0 V (channels used as high-side)	-310	-	-160	µA
t_{OFF1HS}	Diag OFF HS first window	Covered by SCAN	210	250	290	µs
t_{OFF2HS}	Diag OFF HS second window	Covered by SCAN	0.96	1.03	1.28	ms

This is graphically represented in Figure 9.

Figure 9. High-side diagnostics phase one



The internal OFF diagnostics signal state is also reversed from the low-side behavior. If a load is connected, the voltage generated by the diagnostic current through the load will typically be relatively small and be lower than the $V_{DS(OL)}$ threshold. Therefore, the OFF diagnostics signal will be low when a load is present, and no fault will be indicated. However, the range of load impedances will also determine the fault status. The resulting diagnostic voltage at the source pin of the device during phase one will be determined by the equation below:

$$V_{DIAG} = I_{OLU\_HS} * R_{LOAD}$$

The worst-case condition is when the $V_{DS(OL)}$ threshold is at a limit and the diagnostic current is at the opposite limit. Solving for R_{LOAD} and inserting the worst-case parameters:

$$R_{LOAD(\max)} = \frac{2.2V}{160\mu A} = 13.75\text{K}\Omega$$

$$R_{LOAD(\min)} = \frac{1.7V}{310\mu A} = 5.48\text{K}\Omega$$

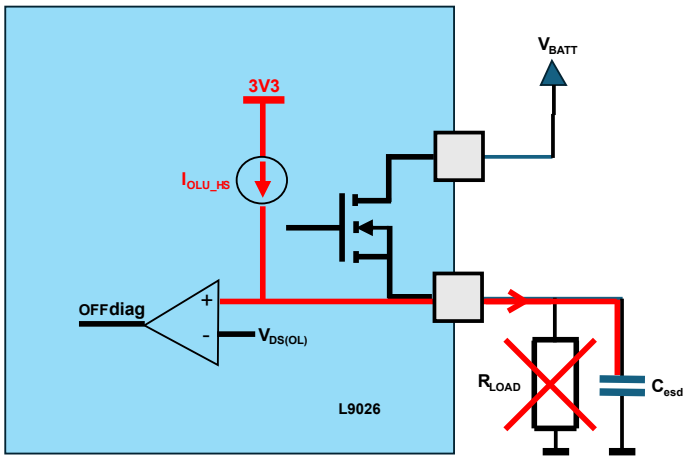
The range of load impedances and their associated behaviors are summarized in Table 5

Table 5. High-side diagnostics phase one, impedance behavior

R_{LOAD})	Device behavior
< 5.48 kΩ	Guaranteed not to flag a fault condition, across all device characteristics
> 13.75 kΩ	Guaranteed to flag a fault condition, across all device characteristics
5.48 kΩ < R_{LOAD} < 13.75 kΩ	May indeterminately flag a fault condition, depending on device characteristics

In the case of a missing load, the only load seen by the device is the ESD capacitor (C_{ESD}) as shown in Figure 10

Figure 10. High-side diagnostics phase one, no load



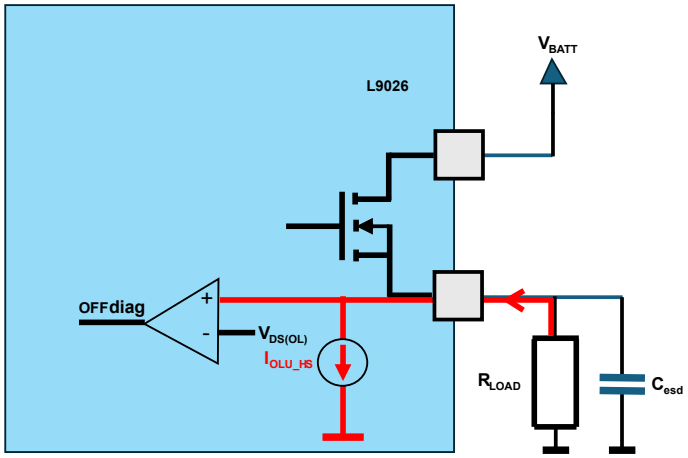
Without the ESD capacitor and no load, the source pin would be pulled up to 3.3 V, which is above the $V_{DS(OL)}$ threshold. In this case, the diagnostic phase one would detect a fault condition. With the ESD capacitor only on the output, the diagnostic current adds a charge to the ESD capacitor, which increases the capacitor voltage. This will create a voltage on the capacitor, which will be compared against the $V_{DS(OL)}$ threshold. Depending on the size of the capacitor, this could create a situation where, if the capacitor is not charged above the $V_{DS(OL)}$ threshold, the diagnostic result would not correctly flag a fault condition and stop the diagnostic sequence. The analysis of the interaction with the ESD capacitor is discussed in Section 3.3.

3.2 High side Off-state phase two

The second phase of the diagnostic sequence is only entered if a fault condition is detected in phase one. The purpose of the second phase is to determine the type of fault condition, either open-load or short-to-battery. The second phase enables a pull-down current source I_{OLD_HS} for the duration of t_{OFF2HS}. The voltage generated by the pull-down current flowing through the load is compared to the $V_{DS(OL)}$ threshold. The phase two current and duration parameters are found in Table 4.

The diagnostic pull-up current load interaction for phase two is graphically represented in Figure 11.

Figure 11. **High-side diagnostics phase two**



$$V_{DIAG} = I_{OLD\_HS} * R_{LOAD}$$

The equation above is used to determine the range of impedances for short-to-battery and open-load conditions by inserting the worst-case $V_{DS(OL)}$ thresholds and corresponding diagnostic currents:

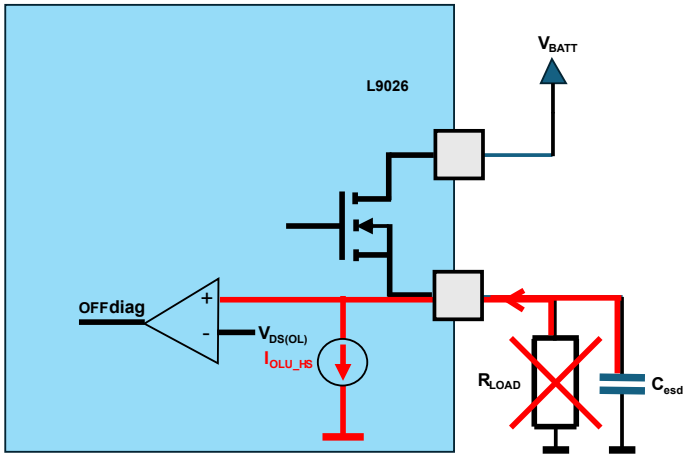
$$R_{LOAD(\max)} = \frac{2.2V}{320\mu A} = 6.88\text{K}\Omega$$

$$R_{LOAD(\min)} = \frac{1.7V}{520\mu A} = 3.27\text{K}\Omega$$

The results from the equations above show that an impedance higher than 6.88 kΩ will guarantee a short-to-battery detection, and an impedance lower than 3.27 kΩ will guarantee an open-load detection, where values in between result in an indeterminate result. However, entering phase two requires that the load impedance must be higher than the minimum (5.48 kΩ) as determined by $R_{LOAD(\min)} = \frac{1.7V}{310\mu A}$. Note that this impedance value is placed within the indeterminate range.

A missing R_{LOAD} circuit is shown in Figure 12

Figure 12. **High-side diagnostics phase two, no load**



The ESD capacitor is seen as the load when R_{LOAD} is not connected. For the high-side phase two, the diagnostic current will typically discharge the ESD capacitor. The resulting capacitor voltage at the end of phase two is typically below the $V_{DS(OL)}$ threshold. This allows an open-load fault to be detected with only the ESD capacitor present. The most interesting ESD interaction case concerns phase one, and is discussed in the next section.

3.3 High side Off-state ESD capacitance interactions

In contrast to the low-side ESD capacitance interactions, the concern with the high-side diagnostics is during the first phase. The interaction with the ESD capacitance during phase one will determine if a fault condition is detected. A short-to-battery condition will charge the ESD capacitance of any amount to the battery voltage and thus will always detect a short-to-battery fault. The potential issue is that an open-load condition may not be detected in phase one if the ESD capacitance is high enough.

If the voltage generated by the application of the diagnostic current is greater than $V_{DS(OL)}$, the OFF diagnostics signal is high, and a fault condition is present. If both the ESD capacitor and R_{LOAD} are not present, the source pin of the device would be pulled to 3.3 V and correctly detect a missing load. However, with only the ESD capacitor present, the diagnostic current will attempt to charge the ESD capacitor, increasing the voltage of the capacitor. This leads to the possibility that, with the diagnostic current and its application time, too much ESD capacitance may result in a lower capacitor voltage. This could cause the device to incorrectly determine that a load is “present” when a load is in fact not present. This is because the capacitance may not be charged above the $V_{DS(OL)}$ threshold with the diagnostic current and within the phase one timing.

Using the capacitor relationship defined in the equation $i = c * \frac{\mathrm{dv}}{\mathrm{dt}}$ and inserting the worst-case conditions to guarantee a fault condition will be flagged:

$$C_{ESD} = \frac{160\mathrm{uA} * 210\mathrm{us}}{2.2V} = 15.3\mathrm{nF}$$

To guarantee that a fault condition will be flagged in phase one under all device characteristics, C_{ESD} must be 15.3 nF or less. This calculation is assuming the capacitor voltage starts at 0 V.

However, the device leakage causes the ESD capacitor to charge to approximately 1.7 V. This reduces the required charge on the ESD capacitor to exceed the $V_{DS(OL)}$ threshold needed to detect a fault condition when R_{LOAD} is missing. This alters the delta voltage that the capacitor must charge to reach a worst-case $V_{DS(OL)}$ threshold. If the device has a $V_{DS(OL)}$ threshold close to the minimum (1.7 V), any amount of capacitance could be detected as a fault condition. However, this may cause issues with the second phase and the determination of an open-load or short condition. If the device has a high $V_{DS(OL)}$ threshold, it is possible that the device will not be able to charge the ESD capacitance above the $V_{DS(OL)}$ threshold and will not detect a fault condition. In this case, the device would not be able to detect an open-load condition if only the ESD capacitance is connected. Examples of the device behavior in this context are examined in the next section.

3.4 High side Off-state diagnostic examples

In this section the device behavior will be observed when the ESD capacitance is 10 nF and 110 nF. Starting with the 10 nF ESD capacitance, Figure 13 shows the device during multiple diagnostics activations. With each activation phase, the ESD capacitance is charged, and the result is compared to the $V_{DS(OL)}$ threshold. In the second phase, the ESD capacitance is discharged and compared against the $V_{DS(OL)}$ threshold.

Figure 13. **Multiple high-side diagnostics activations, no load, C_{ESD} = 10 nF**

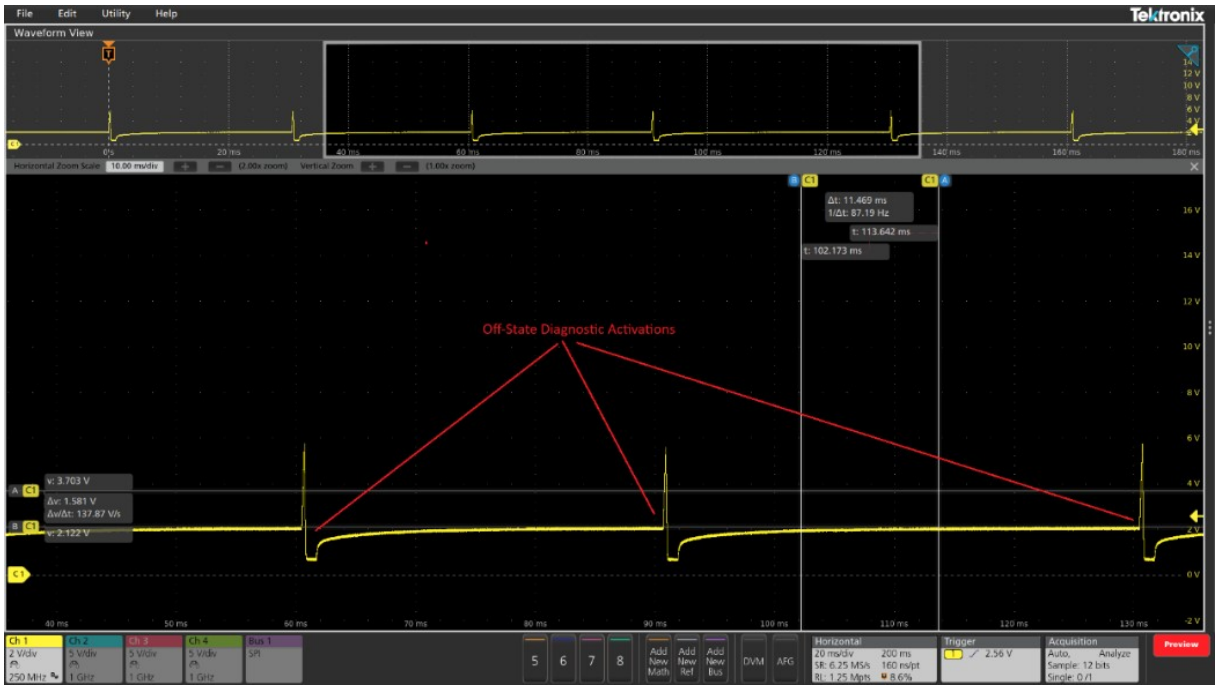


Figure 14. **Single high-side diagnostics activation, no load, C_{ESD} = 10 nF**

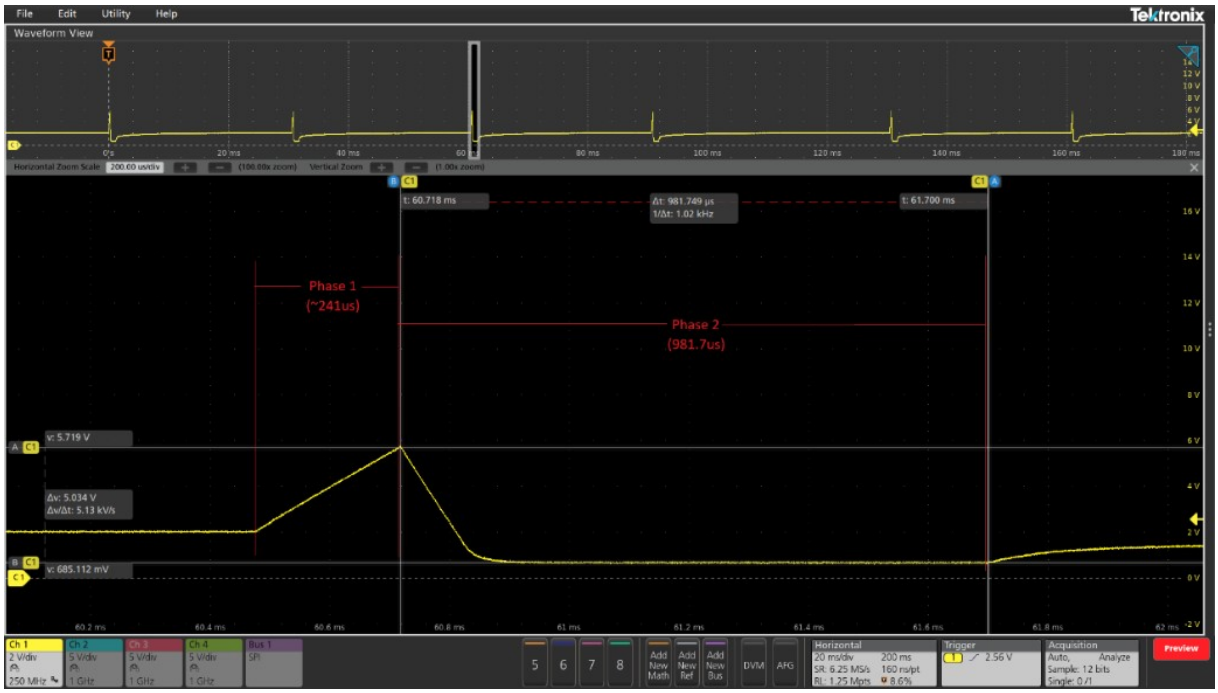


Figure 14 shows a zoomed-in view of a single diagnostics activation. The first phase lasts for around 241 µs and charges the ESD capacitor to 5.7 V, which is well above the maximum $V_{DS(OL)}$ threshold. This causes a fault condition to be detected, and progression to phase two. Phase two lasts for around 982 µs, which discharges the ESD capacitance to around 685 mV. This is much lower than the minimum $V_{DS(OL)}$ threshold, where the device would correctly flag an open-load condition.

Moving to the 110 nF test case, Figure 15 shows multiple diagnostics activations. The first item that stands out is the reduced spikes that occur during phase one.

Figure 15. **Multiple high-side diagnostics activations, no load, C_{ESD} = 110 nF**

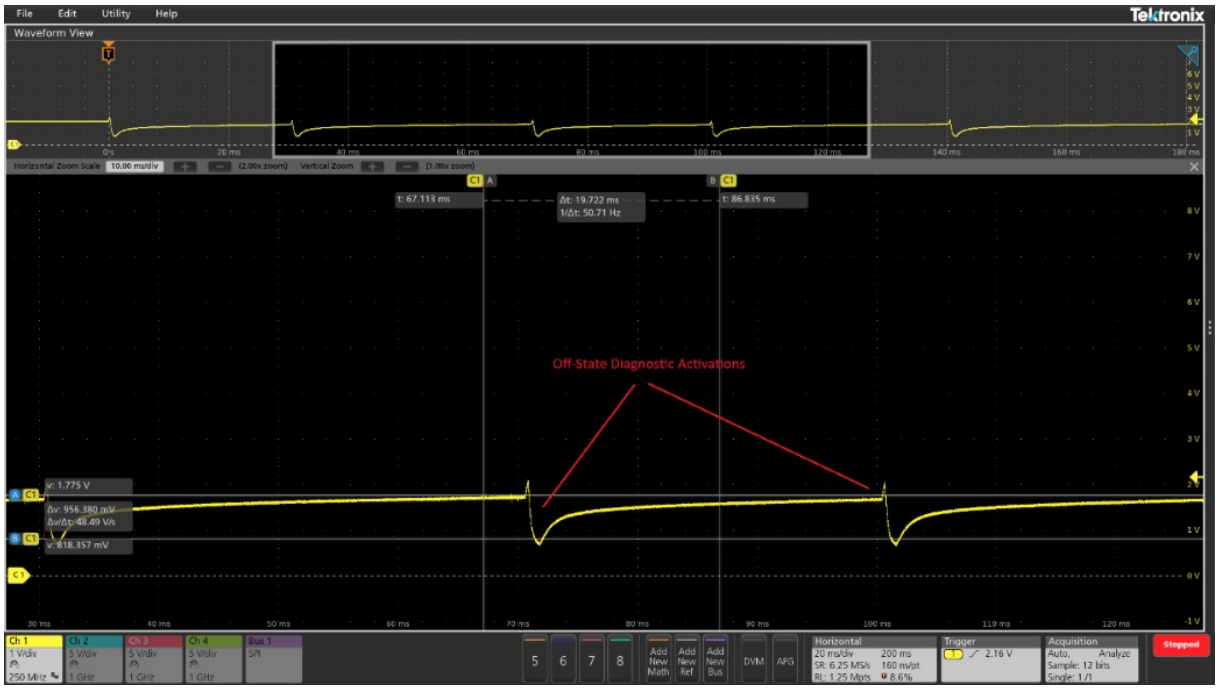


Figure 16. **Single high-side diagnostics activation, no load, C_{ESD} = 110 nF**

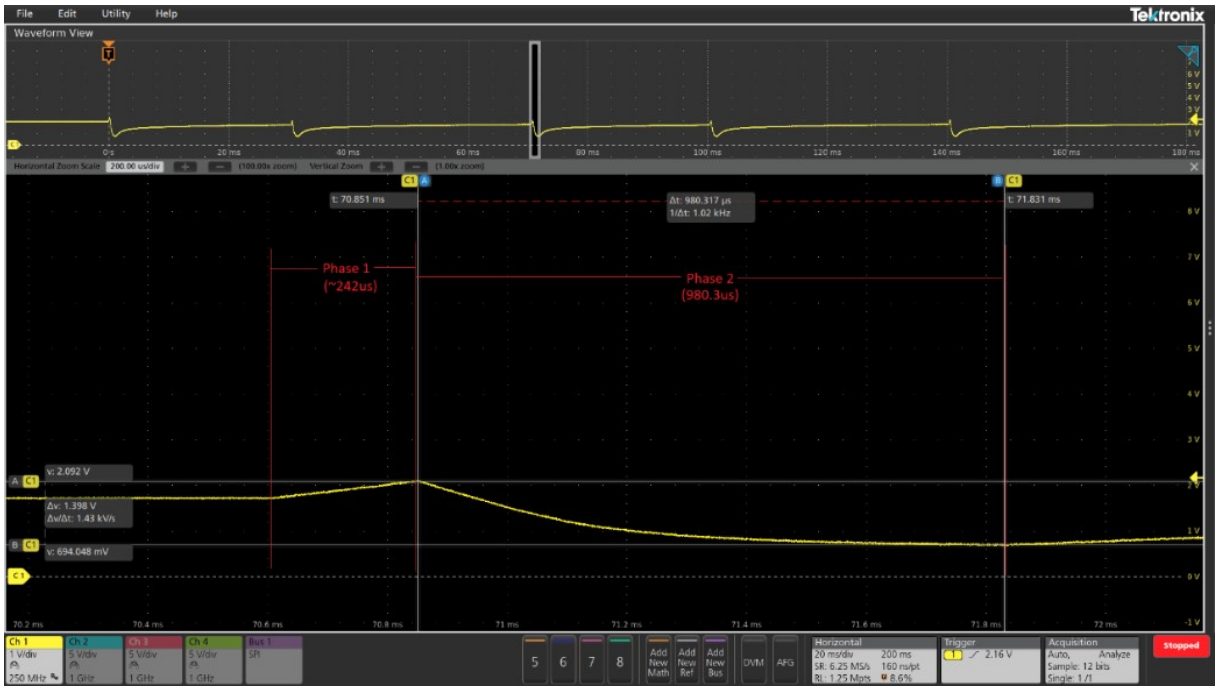


Figure 16 shows the zoomed-in view of a single high-side diagnostic activation. The first phase lasts for around 242 µs and in contrast with the 10 nF case, only charges to 2.09 V. This voltage is within the minimum and maximum range of $V_{DS(OL)}$. This is a marginal case. The device measured in Figure 16 detects the fault condition because its $V_{DS(OL)}$ threshold must be 2.09 V or lower. If the device had a $V_{DS(OL)}$ threshold greater than 2.09 V, then the device would not flag a fault condition, resulting in the missing detection of the fault condition. If the ESD capacitance is increased further, it is possible to have a high enough capacitance for the fault detection to not be possible in phase one. This is assuming the device's $V_{DS(OL)}$ threshold is greater than the leakage voltage of the device.

However, since the device did flag a fault condition in phase one of Figure 16, the second phase is started. The second phase lasts for around 980 µs, discharging the ESD capacitance to a resulting voltage of 694 mV. Again, this voltage is much lower than the minimum $V_{DS(OL)}$ threshold, which results in the device correctly detecting an open-load condition.

Appendix A Acronyms, abbreviations and reference documents

Table 6. Acronyms and abbreviations

Terms	Terms
STB	Short to battery
STG	Short to ground

Table 7. Referenced documents

Document name	Document title
DS13397	L9026 Datasheet, Revision 8, January 2023

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
18-Mar-2026	1	Initial release.

Contents

List of figures

List of tables