SLLIMM 2nd series Super-Junction MOSFET based small low-loss intelligent molded module

Introduction

The SLLIMM (small low-loss intelligent molded module) 2nd series SJ MOSFET is ST's new family of compact, high efficiency, dual-in-line intelligent power modules, with optional extra features. This family is designed with a new internal configuration with only two drivers: one high-side driver and one low-side driver.

This new approach allows a more compact package and, thanks to the new features provided by the low-side driver, advanced protection functions. In addition, this new product offers the best compromise between conduction and switching energy with outstanding robustness and EMI behavior, rendering it ideal for improving efficiency for compressors, pumps, fans and low-power motors working up to 20 kHz in hard-switching circuitries.

The SLLIMM 2nd series SJ MOSFET features:

- DBC package technology for improved thermal behavior
- Superjunction MDmesh MOSFET technology for efficiency improvement
- Higher max. junction temperature of power chips (150 °C)
- Newly developed high-side and low-side driver pinout arrangement for easier PCB routing
- Expanded line-up to 20 A
- Two different temperature monitoring options: NTC thermistor and thermal sensor
- Two fault events with signal output: overcurrent and undervoltage lockout

The SLLIMM 2nd series SJ MOSFET product family combines optimized silicon chips, integrated into three main inverter blocks:

- Power stage
  - Six SJ MOSFETs with fast body diode
- Driving network
  - Two different low and high-voltage gate drivers
  - Three bootstrap diodes
- Protection and optional features
  - Comparators for fault protection against overcurrent and short-circuit
  - Two temperature monitoring options: output thermal sensor (TSO) embedded on the low-side gate driver and NTC thermistor (optional)
  - Two fault event types with fault signal output: overcurrent and undervoltage
  - Smart shutdown function and undervoltage lockout on V_{CC} and V_{boot} voltages

The aim of this application note is to provide a detailed description of the new products family, providing the guidelines to the motor drive designers for an efficient, reliable, and fast design when using the 2nd series SJ MOSFET of ST SLLIMM family.

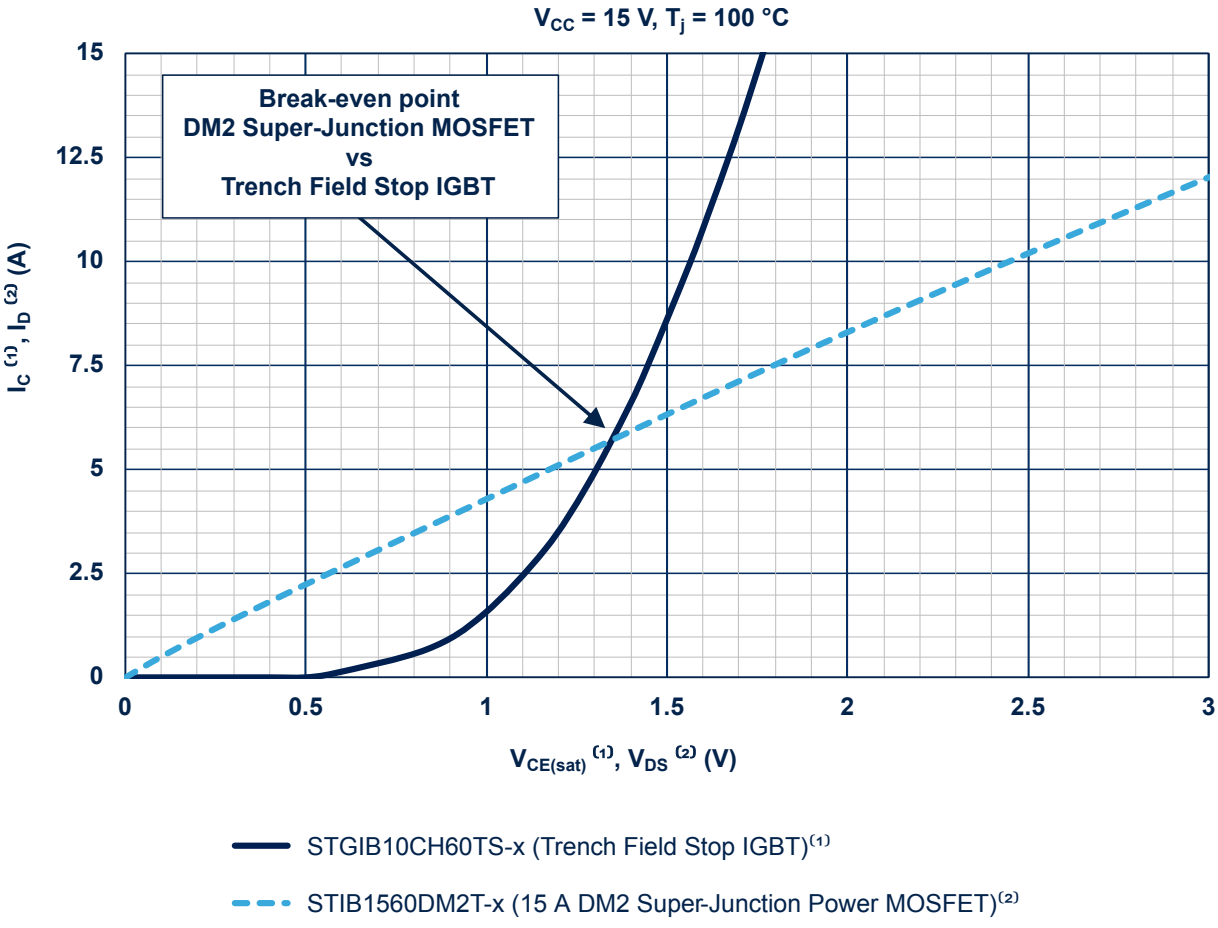
1 Major advantages of the MOSFET technology

The emergence of MOSFET-based intelligent power modules is the result of continuous improvements in the development of more efficient, low-loss MOSFET switching transistors.

The main household appliances target the best energy class to increase energy saving. One of the most important requirements in these applications is the power loss reduction during the steady state operation. This leads designers to select power switches which offer low loss mainly at low-load conditions, but are still capable of providing the necessary current under high-load conditions.

The MOSFET technology benefits of a forward voltage ($V_{DS(on)}$) which decreases linearly with the drain current, whilst in the IGBT the voltage drop ($V_{CE(sat)}$) is not linear with the collector current. It shows a threshold voltage (knee) before getting the on-state, and saturates with an almost constant forward drop above a certain collector current. Thanks to their static characteristics, Power MOSFETs offer lower conduction loss than IGBTs at a low-current level, as shown in the following figure.

Figure 1. MOSFETs and IGBTs static characteristics comparison

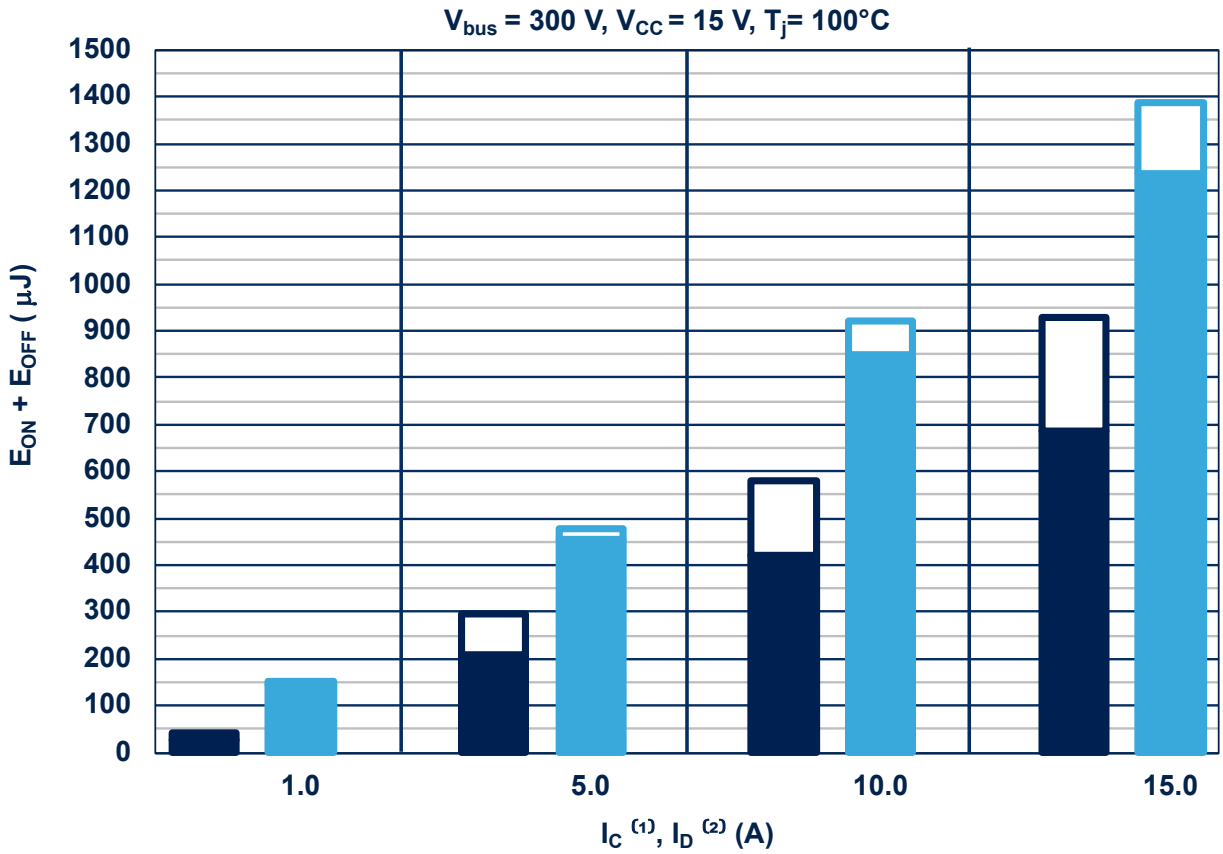


Furthermore, MOSFETs offer very fast turn-off commutation since they are unipolar devices without minority carriers and their intrinsic body diode has been optimized to significantly reduce the reverse recovery energy, which is one of the main sources of power loss impacting also the MOSFET turn-on energy.

The intrinsic body diode of the MOSFETs replaces the need for a separate freewheeling diode, as required for IGBT-based modules. This reduces the complexity of the module assembly and improves overall reliability.

Finally, MOSFETs can offer lower conduction loss, mainly at low-current level, very low turn-off energy and minimal turn-on energy depending on the technology process used to make the body diode fast.

Figure 2. **MOSFETs and IGBTs turn-on and turn-off energies comparison**



1.1 Product synopsis

The SLLIMM 2nd series SJ MOSFET family has been designed to satisfy the requirements of a wide variety of final applications up to 2.5 kW, including:

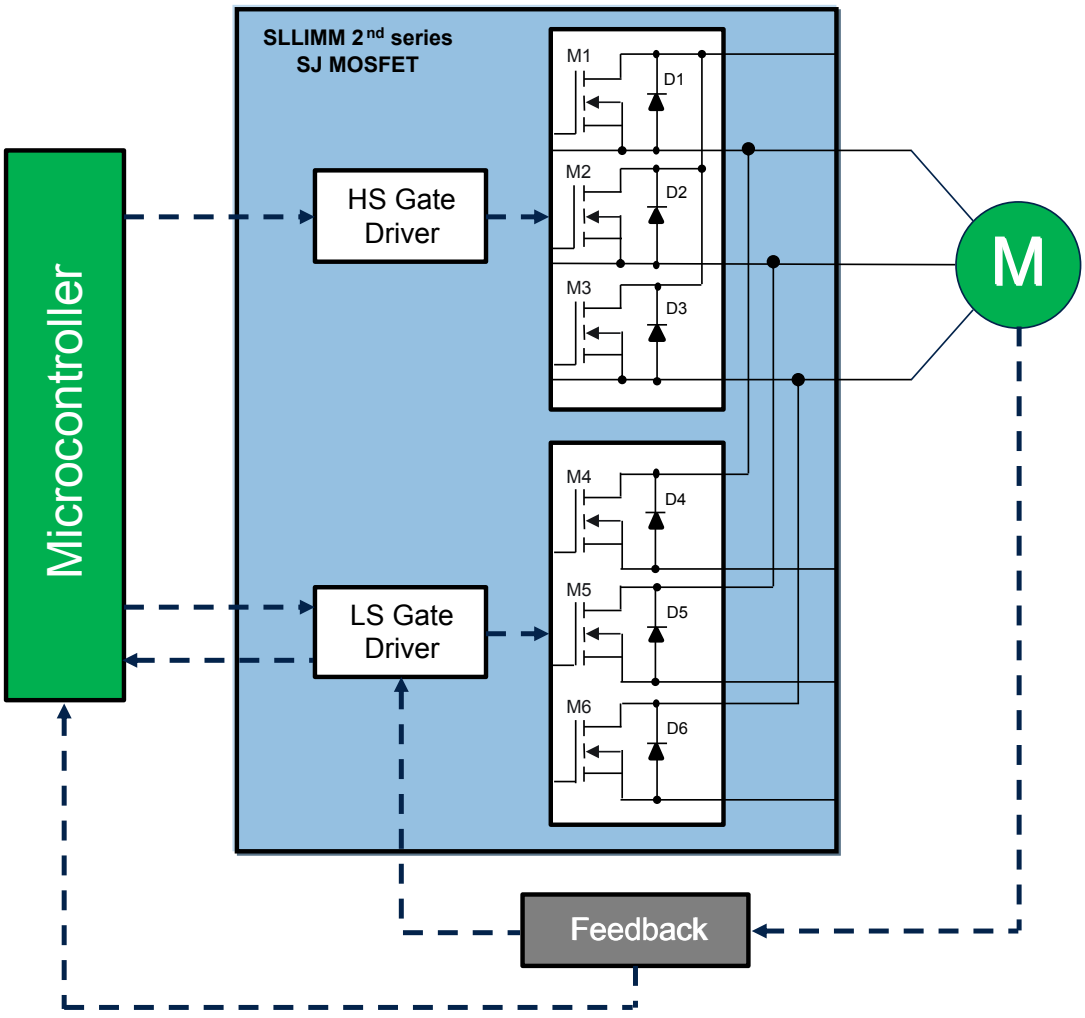
- Washing machines
- Dish washers
- Refrigerators
- Air conditioning compressor drives
- Sewing machines
- Pumps
- Tools
- Low-power industrial applications

The main features and integrated functions can be summarized as follows:

- 600 V, 10 - 20 A ratings
- 3-phase MOSFETs inverter bridge including:
  - Six SJ MOSFETs with fast body diode
- Two control ICs for gate driving and protection including:
  - Three integrated bootstrap diodes
  - Smart shutdown function
  - Comparator for fault protection against overcurrent and short-circuit (on low-side gate driver IC)
  - Undervoltage lock out on V_{CC} (on high and low-side gate driver ICs) and V_{boot} (on high-side gate driver ICs)
  - Two fault signal outputs (on low-side gate driver IC): overcurrent protection and V_{CC} undervoltage (on low-side gate driver IC only)
- Output thermal sensor (TSO) embedded on the low-side gate driver IC
- NTC thermistor for temperature monitor on the power stage (optional)
- Open source configuration for individual phase current sensing
- DBC fully isolated package for enhanced thermal behavior
- Isolation voltage rating of 1600 V_{RMS}/min

The figure below shows the block diagram of an inverter solution including a SLLIMM.

Figure 3. SLLIMM block diagram



1.2 Product line-up and nomenclature

The table below shows the products in production. Additional modules are being developed to extend the current range.

Table 1. Product line-up

Package	Part number	I_C (A) T_C at 25 °C	Voltage (V)	V_{ISO} (Vrms)	Max T_j (°C)	Typical power (W)
SDIP2B-26L	STIB1060DM2x-y	10	600	1600	150	1500
	STIB1560DM2x-y	15	600	1600	150	2000

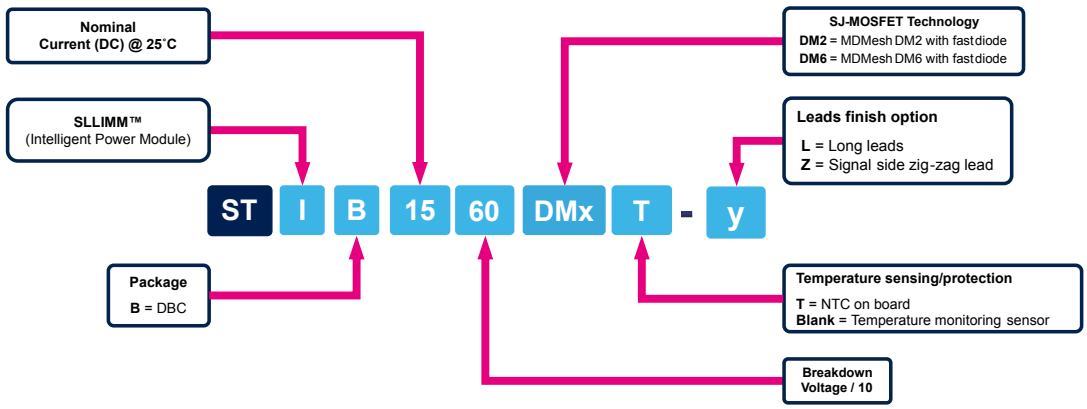
Table 2. Synoptic table

Feature	STIB1060DM2x-y	STIB1560DM2x-y
Voltage (V)	600	600
Continuous collector current each MOSFET (A) (T_C = 25 °C)	12.5	17
$R_{th(j-c)}$ max single MOSFET (°C/W)	1.59	1.1
Package type	SDIP2B-26L	SDIP2B-26L
Number of pins	26 (NTC on board)	26 (NTC on board)
	25	25
Package size (mm) X, Y, Z	38.0 x 24.0 x 3.5	38.0 x 24.0 x 3.5
Integrated bootstrap diode	Yes	Yes
SD function	Yes	Yes
Comparator for fault protection	Yes (1 pin)	Yes (1 pin)
Smart shutdown function	Yes	Yes
Undervoltage lockout	Yes	Yes
Open-source configuration	Yes (3 pins)	Yes (3 pins)
3.3/5 V input interface compatibility	Yes	Yes
High and low-side MOSFET input signal	Active high	Active high

Please refer to the STMicroelectronics website for the complete product portfolio.

The figure below describes the 2nd series SJ MOSFET product family nomenclature.

Figure 4. SLLIMM 2nd series SJ MOSFET nomenclature



1.3 Internal circuit

SLLIMM 2nd series SJ MOSFET offers two internal circuit and number of leads options, based on the presence of the NTC thermistor (STIB1560DM2-Z with no NTC on board).

Figure 5. Internal circuit for SDIP2B-26L (without NTC)

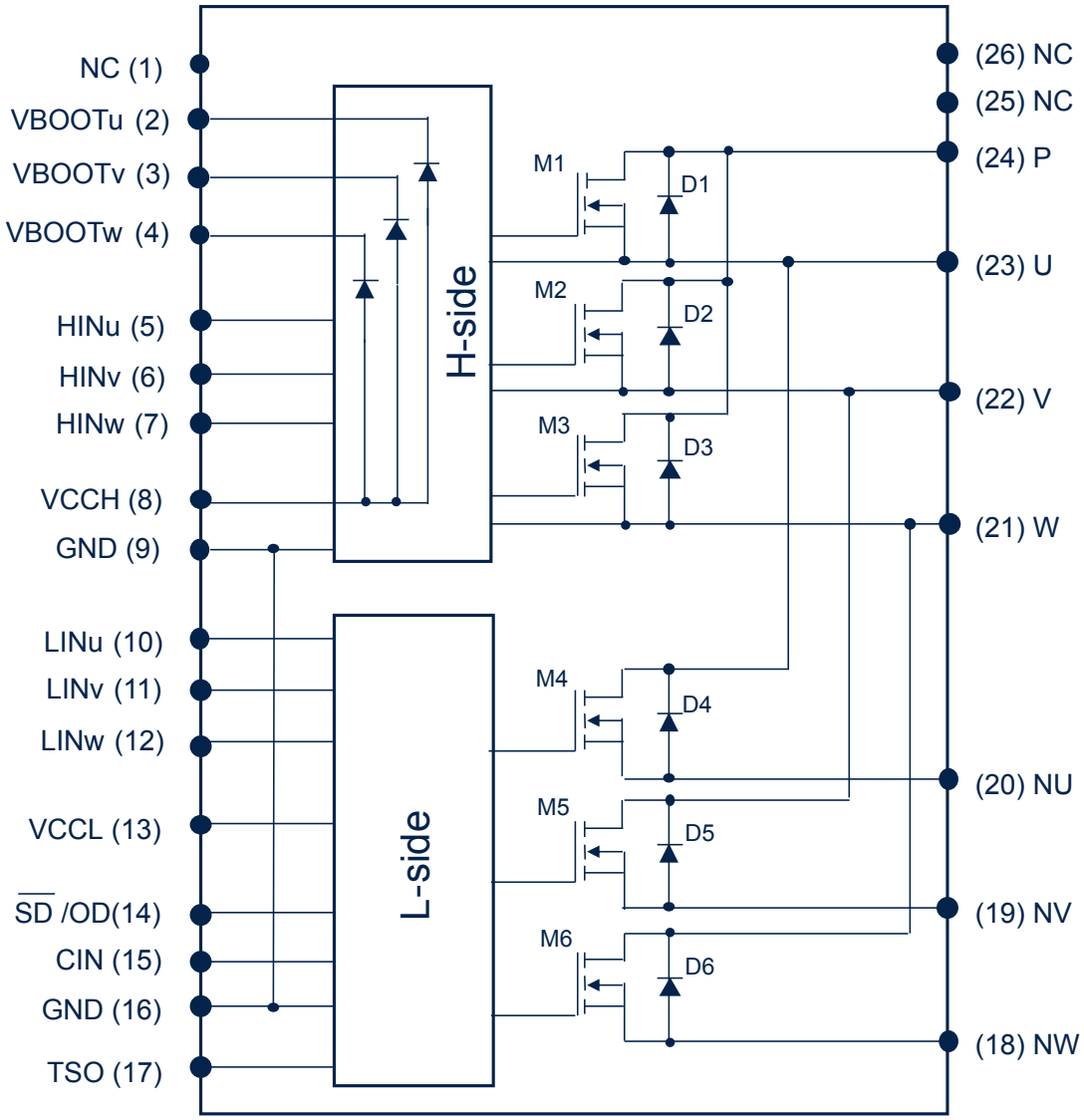
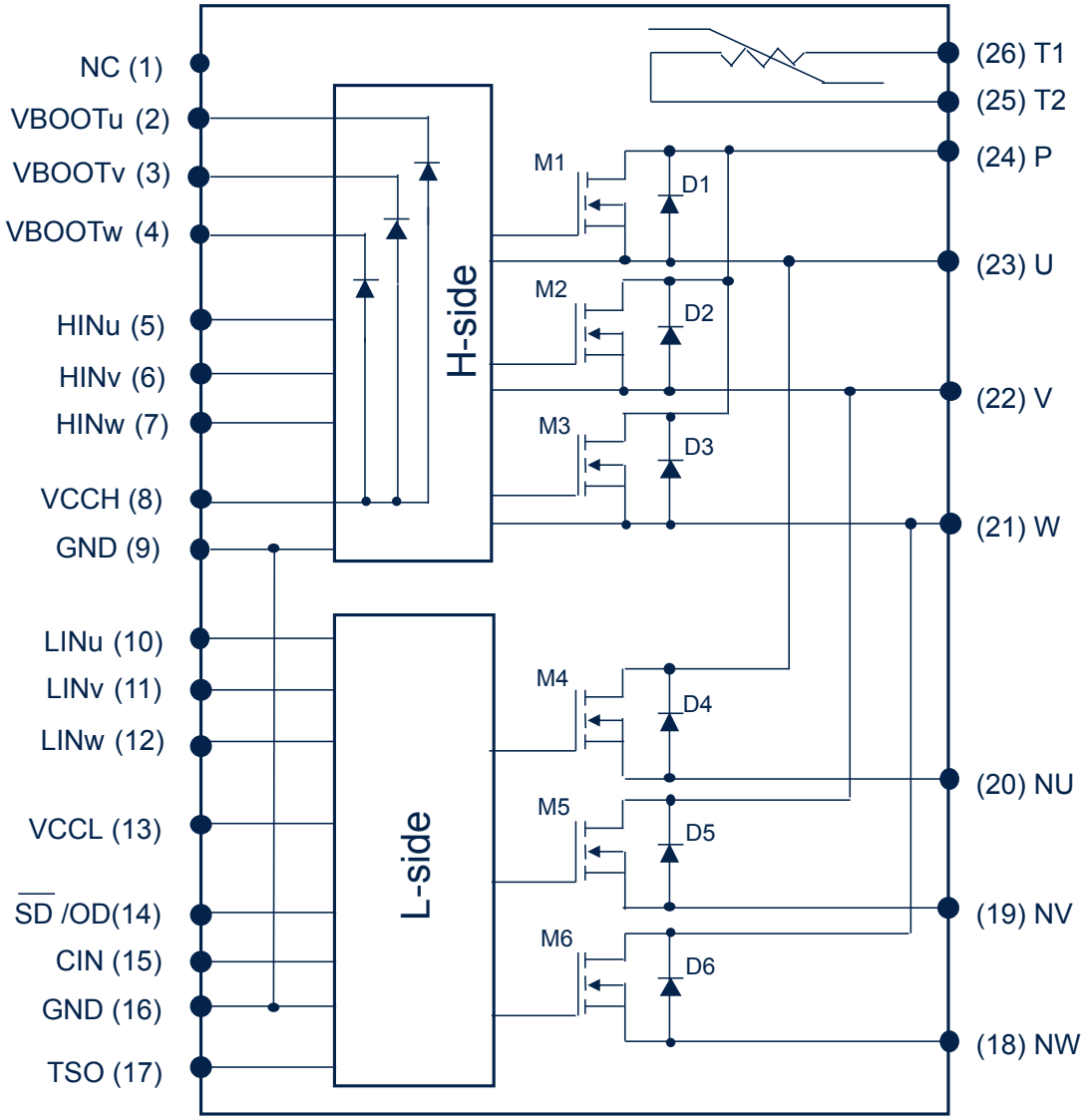


Figure 6. **Internal circuit for SDIP2B-26L (with NTC)**



1.4 Absolute maximum ratings

The absolute maximum ratings represent the extreme capabilities of the device and can be normally used to set the worst-case design limit conditions.

Absolute maximum values are based on specific test parameters such as temperature, frequency and voltage. Device performance can change according to the applied condition.

The SLLIMM specifications are described below with the STIB1060DM2x-y datasheet example. Please refer to the relevant product datasheets for detailed information regarding the other device types.

Table 3. **Inverter part of STIB1060DM2x-y**

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage applied between P - N_U, N_V, N_W	450	V
$V_{PN(surge)}$	Supply voltage surge between P - N_U, N_V, N_W	500	V
V_{DSS}	Drain-source voltage each MOSFET	600	V
$\pm I_D$	Each MOSFET continuous drain current at T_j = 25 °C	12.5	A
$\pm I_{DP}$	Peak drain current of each MOSFET (less than 1 ms)	50	A

Symbol	Parameter	Value	Unit
P_{TOT}	Each MOSFET total dissipation at T_C = 25 °C	78	W
t_{SCW}	Short circuit withstand time, V_{DS}= 300 V, T_J= 125 °C, V_{CC}= V_{boot} = 15 V, V_{IN}= 0 to 5 V	12.5	µs

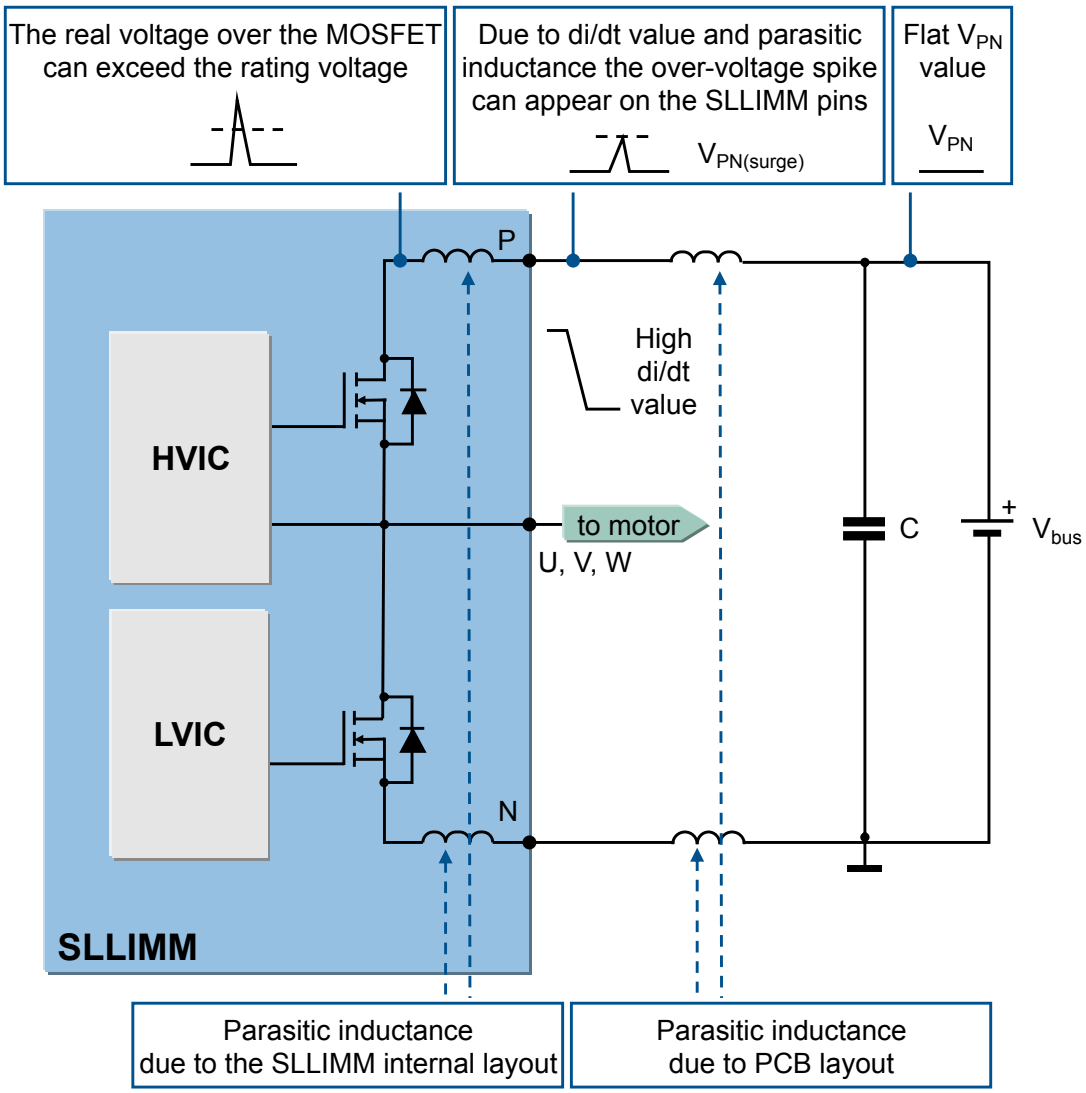
The power stage of SLLIMM is based on MOSFETs (and body diodes) with a 600 V V_{DSS} rating. Considering the SLLIMM internal stray inductance during the commutations, which can generate up to 100 V of surge voltage, the maximum surge voltage between P-N ($V_{PN(surge)}$) allowed is 500 V. At the same time, the maximum supply voltage (in steady-state) applied between P-N (V_{PN}) is limited to 450 V because of an additional 50 V surge voltage generated by the stray inductance between the SLLIMM and the DC-link capacitor.

$\pm I_D$ is the allowable DC current continuously flowing at the drain electrode of each MOSFET (T_J = 25 °C).

t_{SCW} is the short-circuit, nonrepetitive withstand time.

The internal SLLIMM layout and board layout shown below are the two major components of parasitic inductance.

Figure 7. Stray inductance components of output stage



The MOSFETs incorporated in the SLLIMM are tailored for motor control applications where short-circuit self-protection is one of the main module features. If the short-circuit conditions exceed the above specifications, the lifetime of the device is drastically shortened. We therefore strongly recommended not operating the SLLIMM under these conditions.

Table 4. Control part of STIB1060DM2x-y

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage between V_{CCH} - GND, V_{CCL} - GND	-0.3	20	V
V_{BOOT}	Bootstrap voltage	-0.3	619	V
V_{OUT}	Output voltage between U, V, W and GND	V_{BOOT}- 21	V_{BOOT}+ 0.3	V
V_{CIN}	Comparator input voltage	-0.3	20	V
V_{IN}	Logic input voltage applied between HINx, LINx and GND	-0.3	15	V
$V_{\overline{SD/OD}}$	Open-drain voltage	-0.3	7	V
$I_{\overline{SD/OD}}$	Open-drain sink current	-	10	mA
V_{TSO}	Temperature sensor output voltage	-0.3	5.5	V
I_{TSO}	Temperature sensor output current	-	7	mA

V_{CC} represents the supply voltage of the control part for both high-side and low-side gate drivers. Local filtering is recommended to enhance the SLLIMM noise immunity. Generally, we suggest using one electrolytic capacitor (with a higher value and not negligible ESR) and a faster and smaller ceramic capacitor (in the order of hundreds of nF) to provide current.

Refer to the details in the table below to drive the SLLIMM properly.

Table 5. Supply voltage and operation behavior

V_{CC} voltage (typ. value)	Operating behavior
< 12 V	As the voltage is lower than the UVLO threshold, the control circuit is not fully turned on. Perfect functionality cannot be guaranteed.
12 V - 13.5 V	MOSFETs can function, however conduction and switching losses increase due to low voltage gate signal.
13.5 V - 18 V	Recommended value (see the relevant datasheets).
18 V - 20 V	MOSFETs can function. Switching speed is faster and saturation current higher, increasing short-circuit broken risk and EMI issues.
> 20 V	The control circuit is destroyed. The absolute max. rating is 20 V.

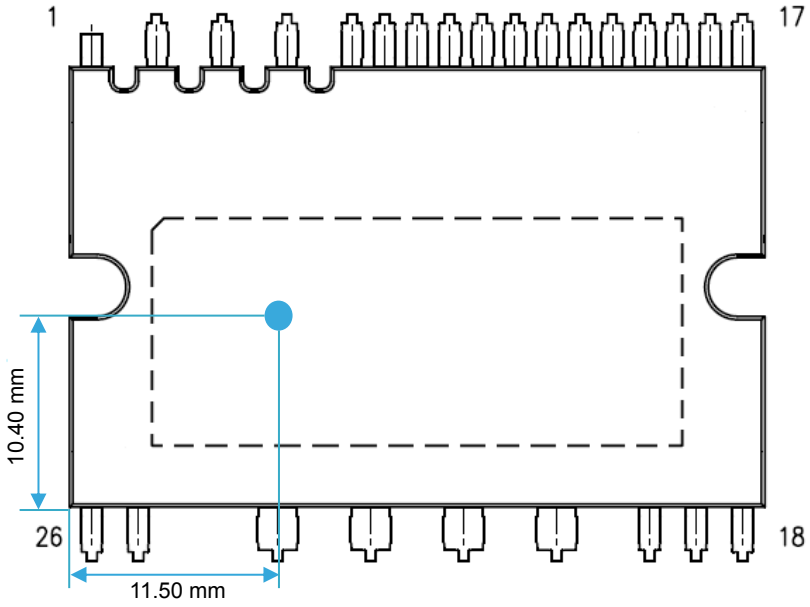
For further information, please refer to the relevant datasheet.

Table 6. Total STIB1060DM2x-y system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 s)	1600	Vrms
T_j	Power chip operating junction temperature	-40 to 150	°C
T_C	Module case operation temperature	-40 to 125	°C

The figure below shows the case temperature measurement point for all package options, right above the power chip. To obtain accurate temperature information, mount a thermocouple on the heat sink surface at this specific location. For noncomplementary switching schemes, the highest T_C point occurs in a different position. In this case, the measurement location is over the point where the highest power chip temperature is generated.

Figure 8. T_C measurement point



1.5 SCSOA

The Figure 9. SCSOA test circuit and Figure 10. SCSOA main data show the circuits for obtaining the SCSOA of SLLIMM 2nd series SJ MOSFET devices and the SCSOA main data, respectively.

Figure 9. SCSOA test circuit

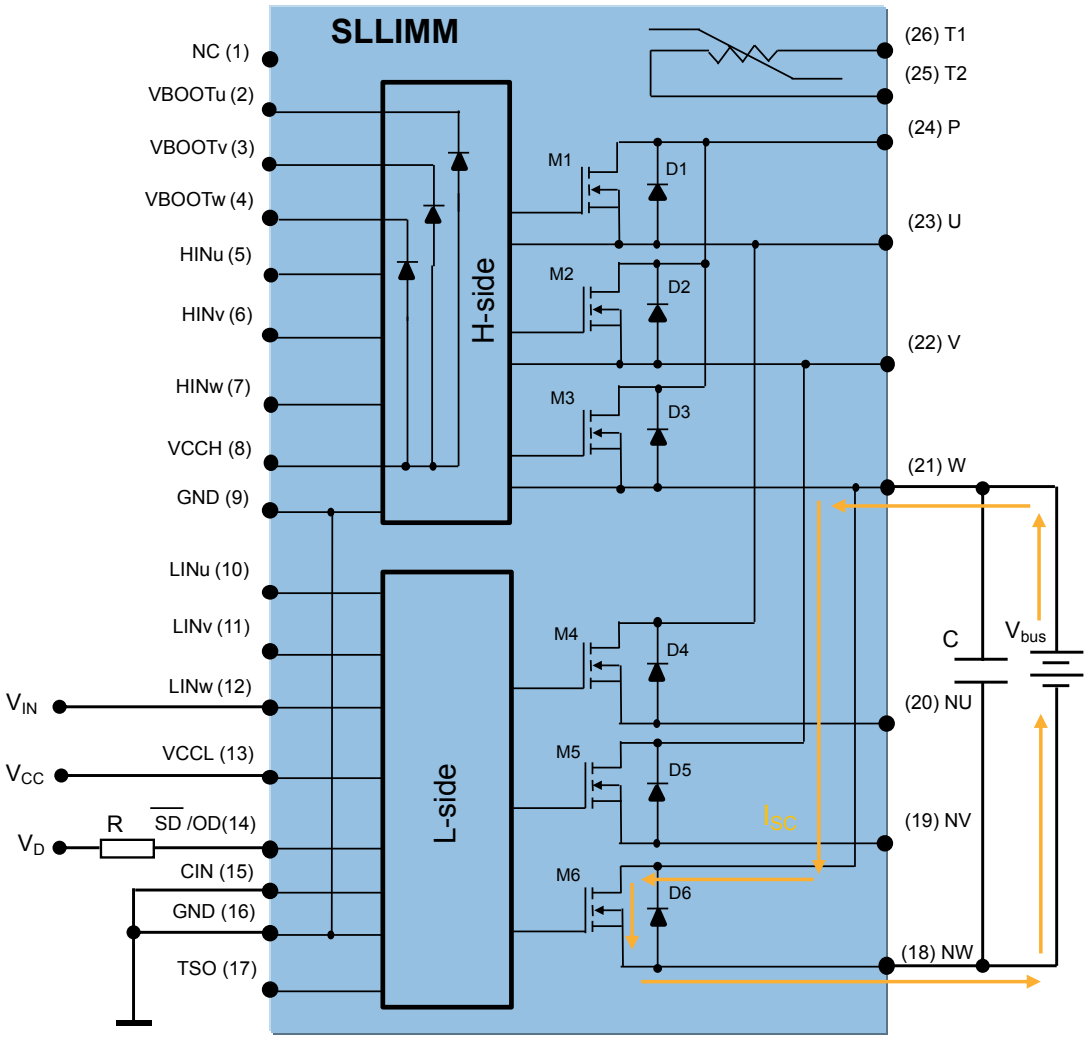
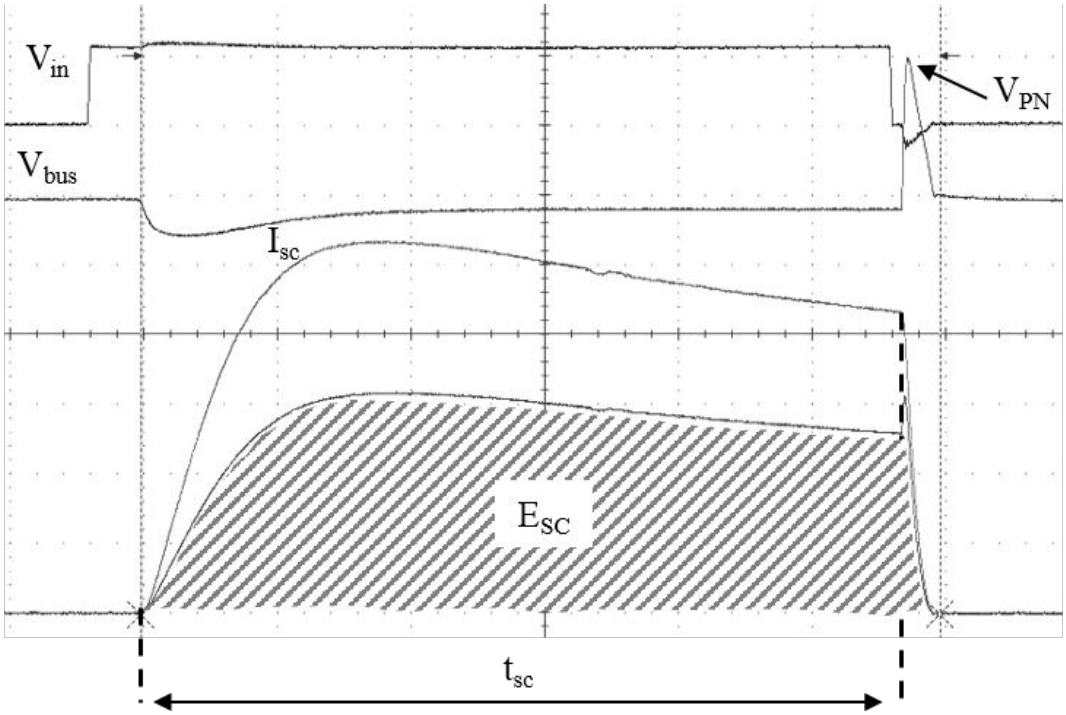


Figure 10. SCSOA main data



V_{PN} is the surge voltage generated at the end of the switching by the inductor wiring between the IPM and DC-Link capacitor.

E_{sc} is the total energy during the switch.

t_{sc} is the impulse width.

The following figures show the typical SCSOA performance curves of STIB1060DM2x-y and STIB1560DM2x-y devices.

The testing conditions for all the devices are: V_{bus} = 400 V, T_{case} = 125 °C, V_{IN} = 5 V, nonrepetitive.

Figure 11. Typical STIB1060DM2x-y SCSOA curve

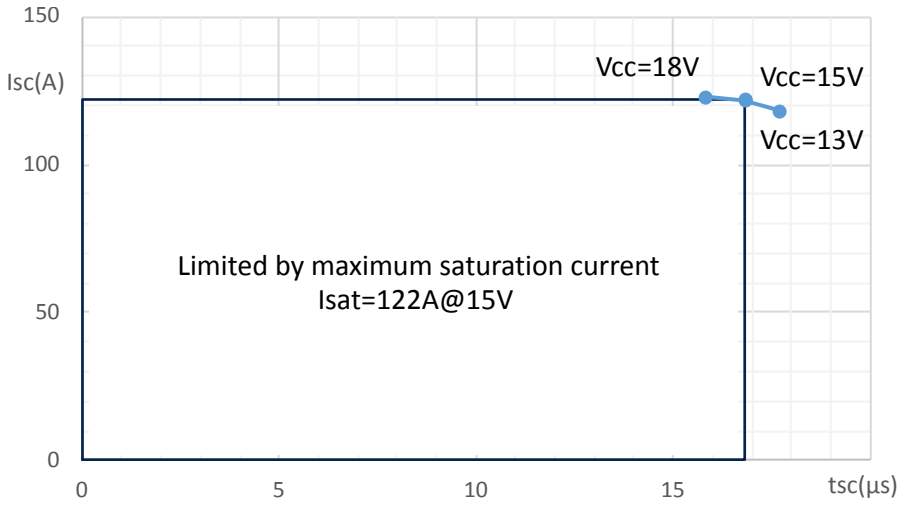
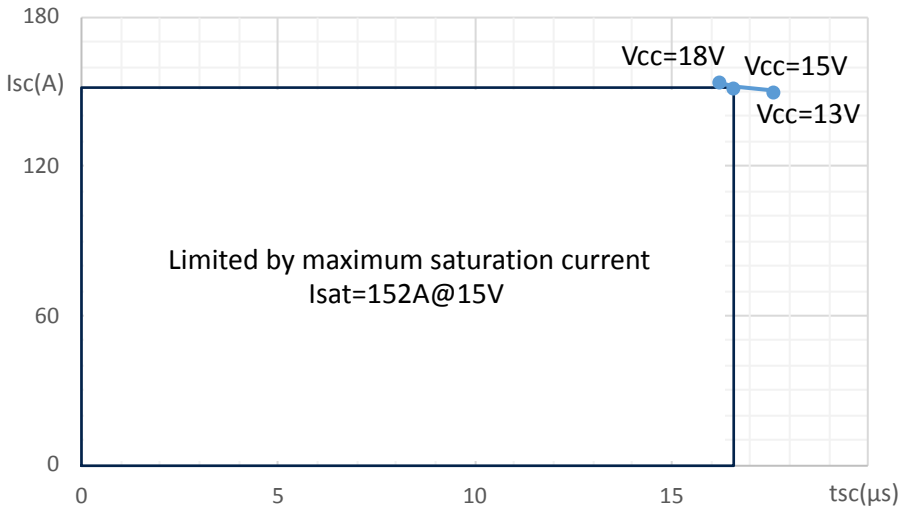


Figure 12. **Typical STIB1560DM2x-y SCSOA curve**



2 Electrical characteristics and functions

In this section, the main electrical characteristics of the power stage are discussed, together with a detailed description of the SLLIMM functions.

2.1 SJ MOSFETs with fast body diode

The SLLIMM 2nd series SJ MOSFET leverages advanced superjunction MOSFETs based on proprietary MDmesh technology, delivering exceptional power efficiency and reliability for demanding applications. These MOSFETs are manufactured using proprietary advanced processes that optimize performance at typical motor control switching frequencies, providing an excellent trade-off between voltage drop (V_{DS}) and switching energy (E_{on} and E_{off}). This balance minimizes the two primary sources of energy loss (conduction and switching) resulting in significant power savings in the inverter stage and reducing the environmental impact of daily use equipment.

The MDmesh technology ensures ultra-low on-resistance and high voltage blocking capability, while the improved lifetime killing process enhances the intrinsic body diode, making it faster, softer, and more robust. Additionally, the devices offer very low recovery charge (Q_{rr}) and recovery time (t_{rr}) combined with very low $R_{DS(on)}$, making them highly suitable for high-efficiency bridge topology converters. Compared to previous IPM generations and standard MOSFET solutions, this series stands out by delivering higher efficiency positioning it as a leading solution for modern power conversion and motor control challenges. A full analysis of the power loss for the complete system is reported in the Section 4: Power loss and dissipation.

2.2 IC gate drivers

The new SLLIMM family is equipped with two different IC gate drivers: a triple low voltage gate driver for LS MOSFETs and a triple high-voltage gate driver for HS MOSFETs. They are designed using BCD and BCD offline (bipolar, CMOS, and DMOS) technologies respectively and are particularly suited to field oriented control (FOC) motor driving applications, able to provide all the functions and the proper current capabilities necessary for MOSFET driving. The HS driver includes a patented internal circuitry which replaces the external bootstrap diode.

Figure 13. High-side gate driver block diagram

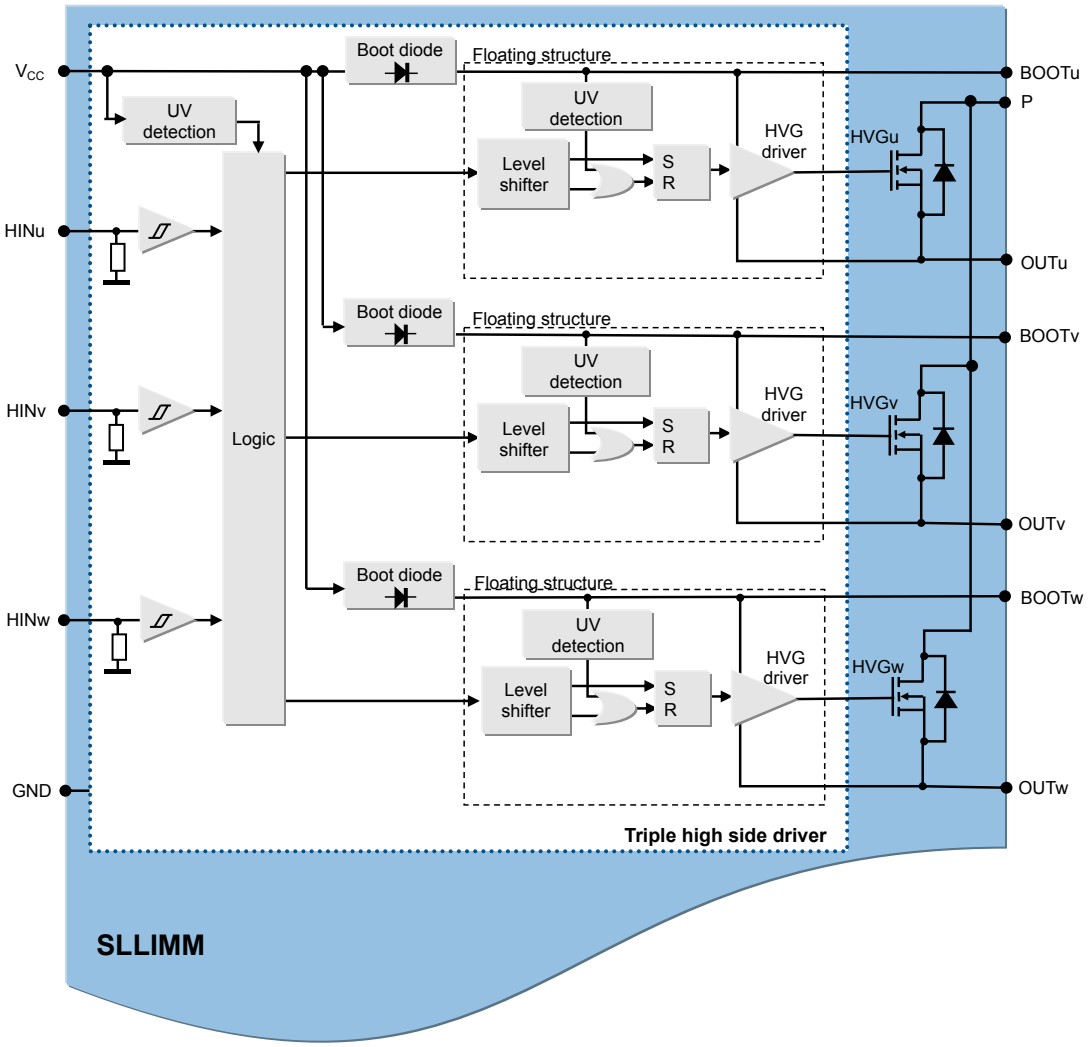
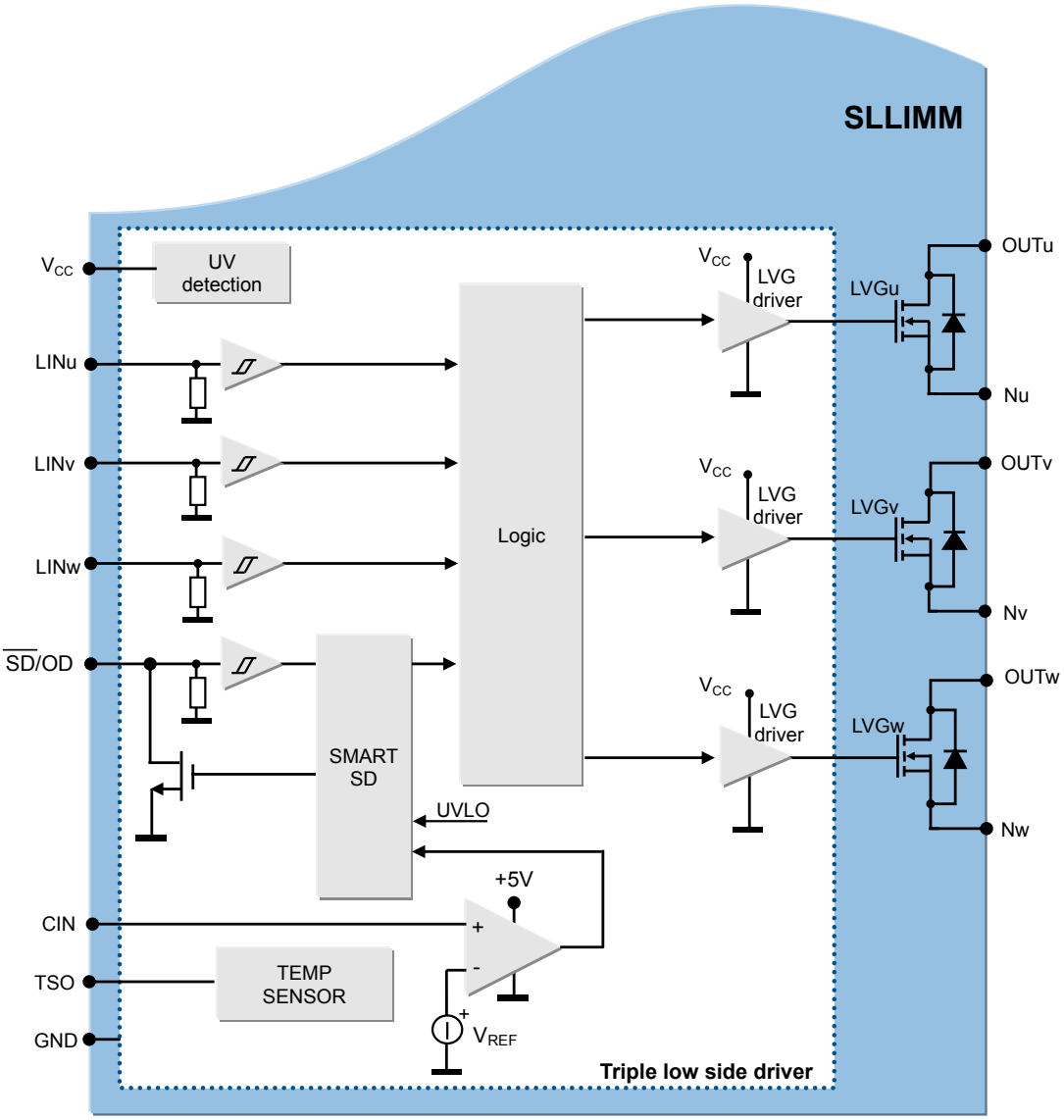


Figure 14. **Low-side gate driver block diagram**



For pin descriptions, refer to the Section 3.3: Input and output pin descriptions.

2.2.1 Logic inputs

All the logic inputs include hysteresis (~ 1 V) for low noise sensitivity and are TTL/CMOS-3.3-V compatible. Thanks to this low voltage interface logic compatibility, the SLLIMM can be used with any kind of high-performance controller like microcontrollers, DSPs or FPGAs.

As shown in the Figure 13. High-side gate driver block diagram and Figure 14. Low-side gate driver block diagram, the logic inputs have internal pull-down resistors to set the proper logic level in case of interruption in the logic lines. If logic inputs are left floating, the gate driver outputs LVG and HVG are set to low level. This simplifies the interface circuit by eliminating the six external resistors, therefore saving on cost, board space and number of components.

Table 7. **Integrated pull-down resistor values**

Input pin	Input pin logic	Internal pull-down
High-side gate driving HINu, HINv, HINw	Active high	100 kΩ
Low-side gate driving LINu, LINv, LINw	Active high	100 kΩ
$\overline{SD}$/OD shutdown	Active low	100 kΩ

2.2.2 High voltage level shift

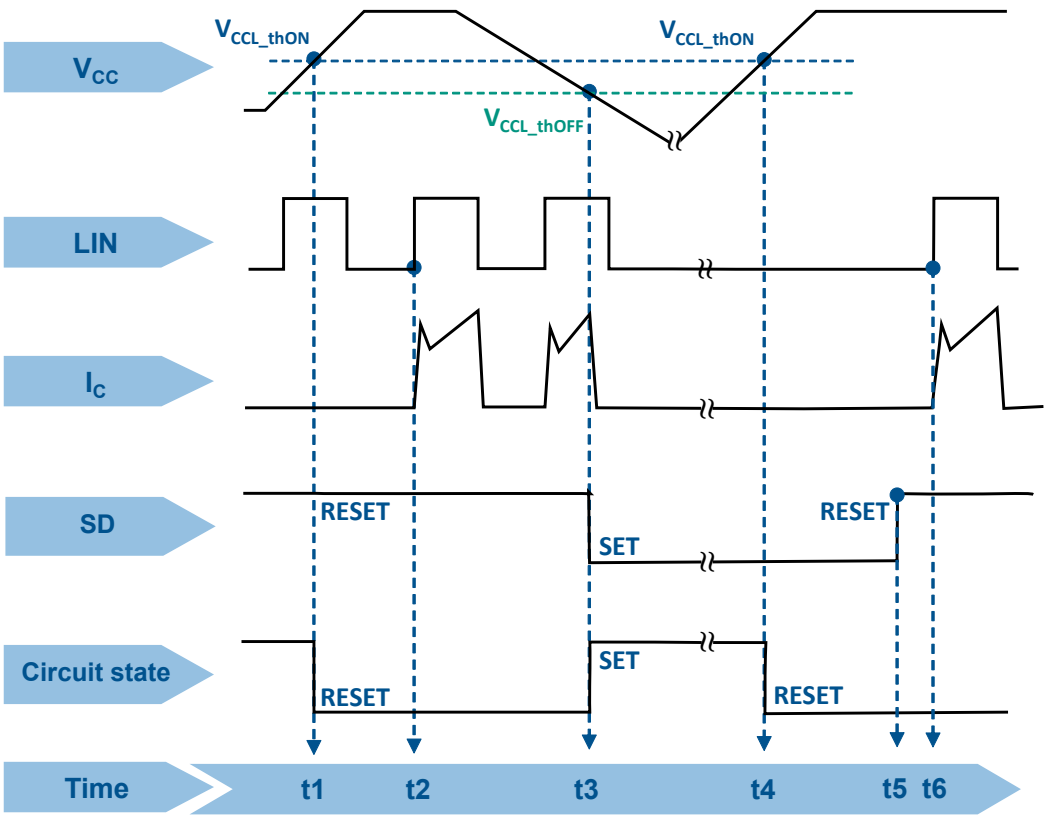
In the HS gate driver IC, the built-in high voltage level shift allows direct connection between the low voltage control inputs and the high voltage power half bridge in any power application up to 600 V. It is obtained thanks to the BCD offline technology which integrates, in the same die, low and medium voltage CMOS bipolar devices for analog and logic circuitry and high voltage DMOS transistors with a breakdown voltage in excess of 600 V. This key feature eliminates the need for external optocouplers, resulting in significant savings, component count and power losses. Other advantages are high-frequency operation and short input-to-output delays.

2.2.3 Undervoltage lockout

Both HS and LS gate driver IC supply voltages, V_{CCH} and V_{CCL} respectively, are continuously monitored by an undervoltage lockout (UVLO) circuit able to turn the low-side and high-side gate driver outputs off when the supply voltage falls below the V_{CCx_thOFF} threshold specified on the datasheet, and turns the IC on when the supply voltage rises above the V_{CCx_thON} voltage. A hysteresis of about 1.4 V is provided for noise rejection purposes. In addition, a fault signal on the $\overline{SD}$ pin is activated if an undervoltage is detected by the LS gate driver IC only (see the Section 2.2.9: Fault management for further details).

Furthermore, in the HS gate driver IC, the high voltage floating supply V_{boot} is also provided with similar undervoltage lockout circuitry. In case of an UVLO condition on V_{boot}, the HVG outputs are set to low level.

Figure 15. **Timing chart of undervoltage lockout function on low-side section**



The timing chart is based on the following steps:

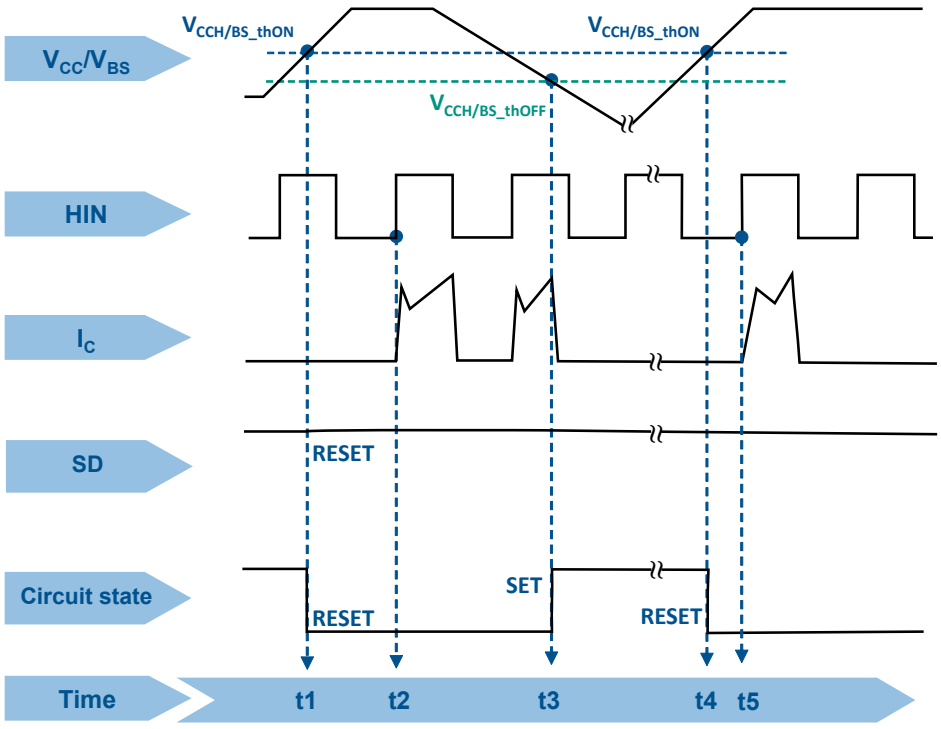
- t1: when the V_{CC} supply voltage rises above the V_{CCL_thON} threshold, the low-side gate driver starts operating after the next input signal LIN is on. The SD signal is in the pull-up condition (RESET) from the external network and the circuit state is RESET.
- t2: the input signal LIN is on and the related MOSFET is turned on.
- t3: when the V_{CC} supply voltage falls below the V_{CCL_thOFF} threshold, an UVLO event is detected. The LS MOSFETs are turned off even if the input signals LIN from the MCU are switching. The SD signal jumps to the SET condition and the circuit is now in the SET state.
- t4: at this time, the V_{CC} supply voltage rises above the V_{CCL_thON} threshold again, but the driver is waiting for the SD reset. During this time, despite the V_{CC} having the right voltage, the LIN signals coming from the MCU are filtered. The SD is in the SET condition and fault information is sent to the MCU. The circuit state changes to RESET.
- t5: the LS gate driver restarts when the SD jumps to the RESET condition.
- t6: the first useful input signal LIN now is able to turn on the LS MOSFETs.

The undervoltage event on the LS gate driver enables a fault signal on the $\overline{SD}$ pin with a specific interval (t4 - t3):

- SD is SET for t_{UVLO} (70 µs) in case of short UVLO event (≤ 70 µs)
- SD is SET for t_{UVLO} (> 70 µs) in case of long UVLO event (> 70 µs)

Further details regarding SD timing can be found in the Section 2.2.9: Fault management.

Figure 16. Timing chart of undervoltage lockout function on high-side section



The timing chart applies to the high-side gate driver for an undervoltage on V_{CC} or V_{boot}. It is based on the following steps:

- t1: when the V_{CC} (or V_{boot}) supply voltage rises above the V_{CCH_thON} (or V_{BS_thON}) threshold(s), the HS gate driver starts operating after the next input signal HIN is on. The SD signal is in the pull-up condition (RESET) from the external network and the circuit state changes to RESET.
- t2: the input signal HIN is on and the MOSFETs are turned on.
- t3: when the V_{CC} (or V_{boot}) supply voltage falls below the V_{CCH_thOFF} (or V_{BS_thOFF}) threshold(s), an UVLO event is detected. The HS MOSFETs are turned off even if the HIN input signals from the MCU are switching. The circuit changes to the SET state. During UVLO on the HS section, there is no fault signal so the SD remains in the RESET condition.
- t4: at this time, the V_{CC} (or V_{boot}) supply voltage again rises above the V_{CCH_thON} (or V_{BS_thON}) threshold and the gate driver restarts.
- t5: the first useful input signal HIN now is able to turn on the MOSFET.

The Table 8. SD duration time per event summarizes the possible UVLO events and their effect on the MOSFETs and the SD pin.

2.2.4 Comparators for fault sensing

The SLLIMM family integrates one comparator intended for advanced fault protection such as overcurrent, over temperature or any other type of fault measurable via a voltage signal. The comparator has an internal reference voltage V_{REF}, specified in the datasheet, on its inverting input (see the Figure 14. Low-side gate driver block diagram), while the noninverting input is available on the CIN pin. The comparator input can be connected to an external shunt resistor to implement a simple overcurrent or short-circuit detection function, as discussed in the following section.

2.2.5 Short-circuit protection and smart shutdown function

The SLLIMM is able to monitor the output current and provide protection against overcurrent and short-circuit conditions in a very short time (comparator triggering to high/low-side driver turn-off propagation delay t_{isd} = 300 ns), thanks to the smart shutdown function.

This feature is based on patented circuitry which provides intelligent fault management and greatly reduces the protection intervention delay, regardless of the protection time duration which can be set by the user.

The comparator input can be connected to an external shunt resistor, R_{SHUNT}, to implement a simple overcurrent detection function.

An RC filter network (R_{SF} and C_{SF}) is necessary to prevent erroneous operation of the protection.

The output signal of the comparators is fed into an integrated MOSFET with the open drain available on the $\overline{SD}$/OD pin, shared with the input.

When the comparator triggers, the device is set to the shutdown state and all LS MOSFETs are turned off. In common overcurrent protection architectures, the comparator output is connected to the $\overline{SD}$/OD input and an external RC network (R_{SD} and C_{SD}) is connected to this $\overline{SD}$/OD line to provide a mono-stable circuit which implements a protection time when a fault condition occurs.

Contrary to common fault detection systems, the smart shutdown structure allows immediate turn-off of the LS gate driver output in the event of a fault, without having to wait for the external capacitor to discharge.

This strategy minimizes the propagation delay between the fault detection event and the actual switching off of the outputs. In fact, the time delay between the fault and output disabling is not dependent on the RC value of the external SD circuitry but, thanks to the internal architecture, it has a preferential internal path in the LS driver.

As shown in the Figure 18. Timing chart of smart shutdown function, the device immediately turns off the LS driver outputs (with a propagation delay of 300 ns) and simultaneously latches the turn-on of the open drain switch (with propagation delay t_{CIN_SD}). The SD signal decreases to its unlatch threshold V_{SSD} and holds the open drain on until t_{OC} (24 µs) has elapsed. This time interval (taken from the V_{il} threshold) distinguishes the overcurrent fault event from other fault events like UVLO. The driver outputs restart following the input pins as soon as the voltage at the $\overline{SD}$ pin reaches the higher threshold of the SD logic input V_{ih}.

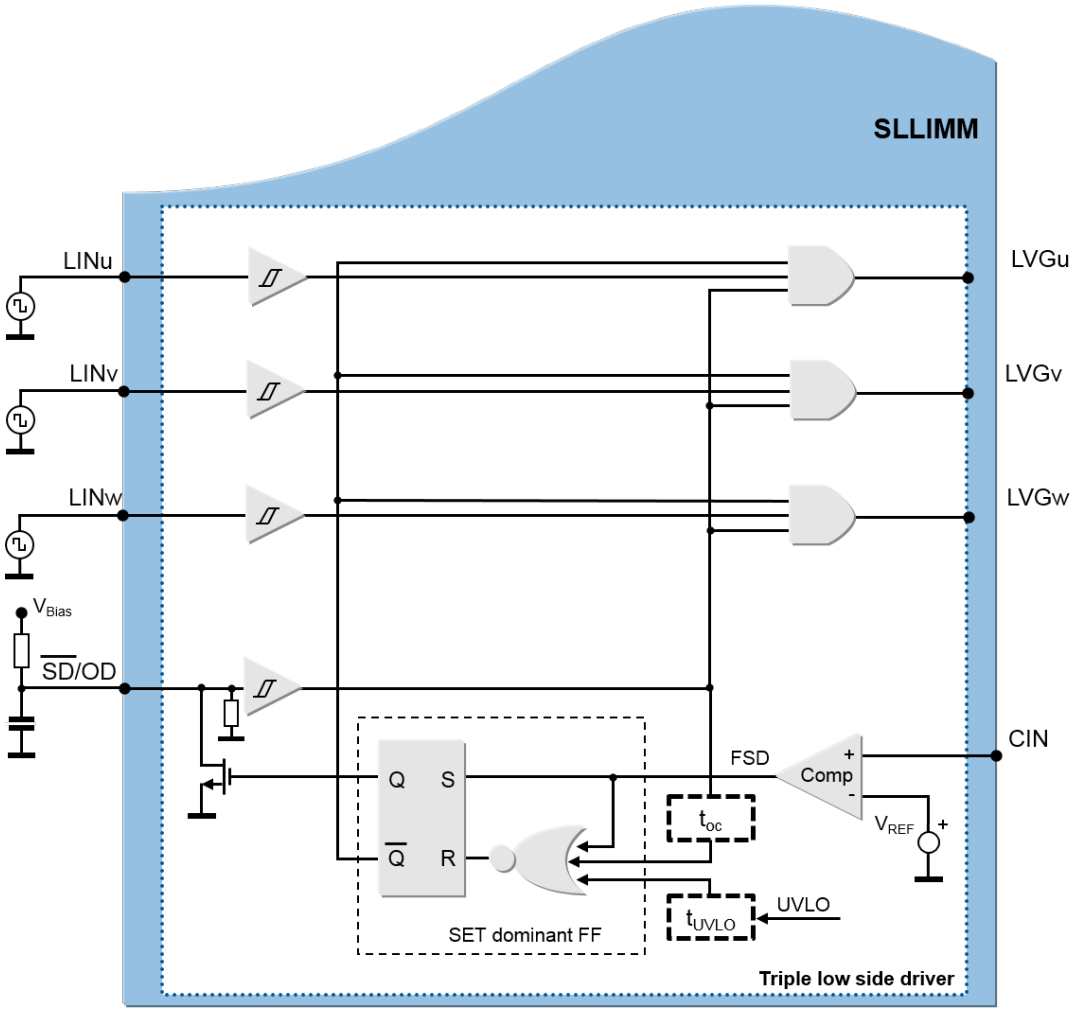
If the short-circuit is present during restart, the IPM enters a smart shutdown phase again.

Important: *Repeated short-circuit operations stress the device.*

The smart shutdown system allows increasing the value of the external RC network across the $\overline{SD}$ pin over the time t_{OC} (sized to fix the disable time generated after the fault event) as much as desired by the user without compromising the intervention time delay of the SLLIMM protection.

The figure below shows a block diagram of the smart shutdown architecture inside the low-side driver.

Figure 17. **Smart shutdown equivalent circuitry**



In normal operation, the outputs follow the commands received from the respective input signals.

When a fault detection event occurs, the fault signal (FSD) is set to high by the fault detection circuit output and the FF receives a SET input signal. Consequently, the FF outputs set the low-side output signals to low level and simultaneously turn on the open drain MOSFET which works as an active pull-down for the SD signal.

Note that the low-side gate driver outputs remain at the low level until the $\overline{SD}$ pin has experienced both a falling edge and a rising edge, although the fault signal could be returned to low level immediately following fault sensing. In fact, even if the FF is reset by the falling edge of the $\overline{SD}$ input, the SD signal also acts as the enable for the outputs, thanks to the AND ports.

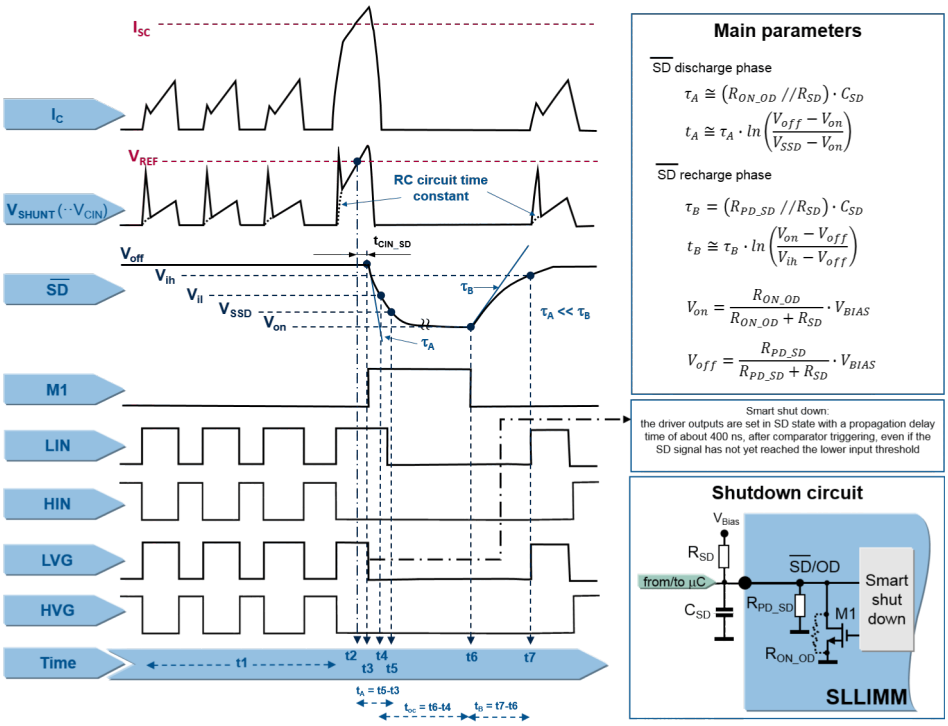
Moreover, once the internal open drain transistor has been activated, due to the latch, it cannot be turned off until the $\overline{SD}$ pin voltage reaches V_{SSD} and t_{OC} has elapsed.

Note: As the FF is SET dominant, oscillations of the $\overline{SD}$ pin are disregarded if the fault signal remains steady at the high level.

2.2.6 Timing chart of short-circuit protection and smart shutdown function

The figure below shows the timing chart during an overcurrent or short circuit event.

Figure 18. Timing chart of smart shutdown function



The timing chart is based on the following steps:

- t1: when the output current is lower than the max. allowed level, the SLLIMM functions normally.
- t2: when the output current reaches the max. allowed level (I_{SC}), the overcurrent/short-circuit event is detected and the protection is activated. The voltage across the shunt resistor, and then on the CIN pin (V_{CIN}), reaches the V_{REF} value; the comparator triggers and the shutdown phase begins.
- t3: after t_{cin_SD} time, the M1 internal open-drain MOSFET is switched on, the SD starts the discharge phase (with a time constant according to the Eq. (1)) and the smart shutdown switches off the low-side MOSFETs gate (LVG) through a preferential path (400 ns as typical internal delay time).

$$\tau_A \cong \left(R_{ON_{OD}} // R_{SD}\right) \cdot C_{SD} \quad (1)$$

- t4: at this time, the SD signal reaches the low voltage logic level (V_{il}) and, starting from this point, an internal timer fixes the t_{OC} time (20 µs for an overcurrent or short-circuit event).
- t5: the SD signal reaches the Smart SD unlatch threshold (V_{SSD}). In the meantime, the MCU detects the fault and it switches the input signals LIN and HIN off. The open drain MOSFET M1 remains on.
- t6: when the t_{OC} has elapsed, the SD can rise with a time constant given by the following equation:

$$\tau_B \cong \left(R_{PD\_SD} // R_{SD}\right) \cdot C_{SD} \quad (2)$$

- t7: the SD signal reaches the upper threshold V_{ih} (in the worst case) and the system is ready to be re-enabled.

The discharging time t_A and the charging time t_B are the time intervals between t5-t3 and t7-t6, respectively.

2.2.7 Current sensing shunt resistor selection

As previously discussed, the shunt resistors R_{SHUNT} externally connected between the N pins and ground are used in the overcurrent detection circuitry.

When the output current exceeds the short-circuit reference level (I_{SC}), the CIN signal overtakes the V_{REF} value and the short-circuit protection is activated. For reliable and stable operation, the current sensing resistor should be a high quality, low tolerance noninductive type. In fact, stray inductance in the circuit due to the layout, the RC filter, and even the shunt resistor, must be minimized to avoid undesired short-circuit detection.

For these reasons, the shunt resistor and the filtering components must be placed as close as possible to the SLLIMM pins. Refer to layout suggestions

The value of the current sense resistor can be calculated according to different guidelines, functions of the design specifications, or requirements. A common criterion is presented here based on the following steps:

- Definition of the overcurrent threshold value (I_{OC_th}). This value can, for example, be set by considering the MOSFET typical working current in the application and adding 20-30% as overcurrent.
- Calculation of the shunt resistor value according to the conditioning network.
- Selection of the closest shunt resistor commercial value.
- Calculation of the power rating of the shunt resistor, considering that this parameter is strongly temperature dependent. Therefore, the power derating ratio of the shunt resistor, ΔP(T)%, shown in the manufacturer's datasheet, must be considered, as shown in the formula below:

$$P_{SHUNT}(T) = \frac{R_{SHUNT} \cdot I_{RMS}^2}{\Delta P(T)\%} \quad (3)$$

Where I_{RMS} is the MOSFET RMS working current.

For proper selection of the shunt resistor, a safety margin of at least 30% is recommended on the calculated power rating.

Below is an example for the STIB1060DM2x-y IPM.

The value of the shunt resistor is calculated by the following equation:

$$R_{SH} = \frac{V_{ref}}{I_{OC}} \quad (4)$$

Where V_{ref} is the internal comparator (CIN) (0.51 V typ.) and I_{OC} is the OC trigger level.

The maximum OC protection level should be set less than the pulsed collector current in the datasheet. In this design, the overcurrent threshold level is fixed at 30% more than the nominal current (10 A). Therefore the shunt resistor value is:

$$R_{SH} = \frac{V_{\text{ref}}}{I_{OC}} = \frac{0.51}{1.3\text{x}10} = 0.039\ \Omega \quad (5)$$

For the power rating of the shunt resistor, these parameters must be considered:

- Maximum load current of inverter (85% of I_{nom} (A_{rms})): I_{load}(max)
- Shunt resistor value at T_C = 25 °C
- Power derating ratio of shunt resistor at T_{SH} = 100 °C
- Safety margin

The power rating is calculated with the following equation:

$$P_{SH} = \frac{1}{2} \cdot \frac{I_{load(\max)}^2 \cdot R_{SH} \cdot margin}{Derating\ ratio} \quad (6)$$

For STIB1060DM2x-y and R_{SH} = 0.04 Ω (commercial value):

$$I_{nom} = 10\ \text{A} \rightarrow I_{nom[rms]} = \frac{I_{nom}}{\sqrt{2}} \rightarrow I_{load(\max)} = 85\%\left(I_{nom[rms]}\right) = 6\ A_{rms} \quad (7)$$

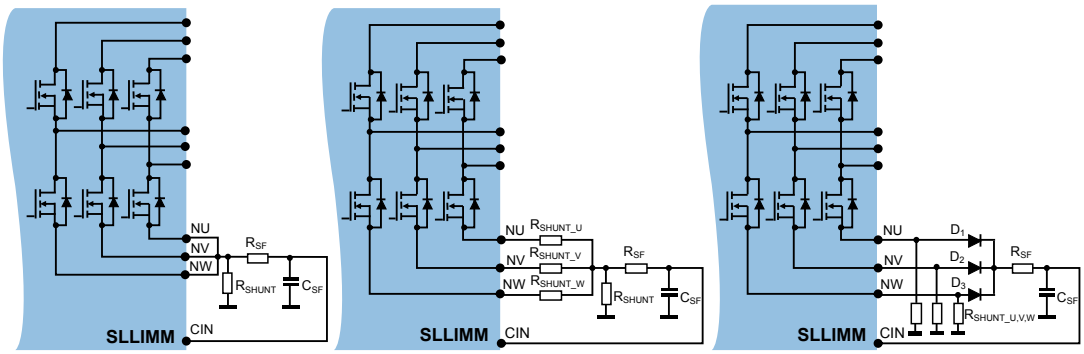
- Power derating ratio of shunt resistor at T_{SH} =100 °C: 80% (from datasheet manufacturer)
- Safety margin: 30%

$$P_{SH} = \frac{1}{2} \cdot \frac{6^2 \cdot 0.04 \cdot 1.3}{0.8} = 1.17\,W \quad (8)$$

2.2.8 RC filter network selection

Two options of shunt (1- or 3-shunt) resistor circuits can be adopted for different control and short-circuit protection techniques. For 3-shunt resistor configurations, the following figure shows two simple overcurrent protection variants: type A, using an additional shunt resistor (R_{SHUNT}) and type B, using a diode OR gate circuit.

Figure 19. Examples of SC protection circuits



An RC filter network is required to prevent undesired short-circuit operation due to noise on the shunt resistor.

All the solutions allow detection of the total current in all the three phases of the inverter. The filter is based on the R_{SF} and C_{SF} network and its time constant is given by:

$$t_{SF} = R_{SF} \cdot C_{SF} \quad (9)$$

In addition to the RC time constant, the turn-off propagation delay of the gate driver, t_{CIN_LVG} (specified in the datasheet) and the MOSFET turn-off time (in the order of hundreds of ns), must be considered in the total delay time (t_{Total}), which is the time necessary to completely switch the MOSFET off once the short-circuit event is detected. Therefore, t_{Total} is calculated as follows:

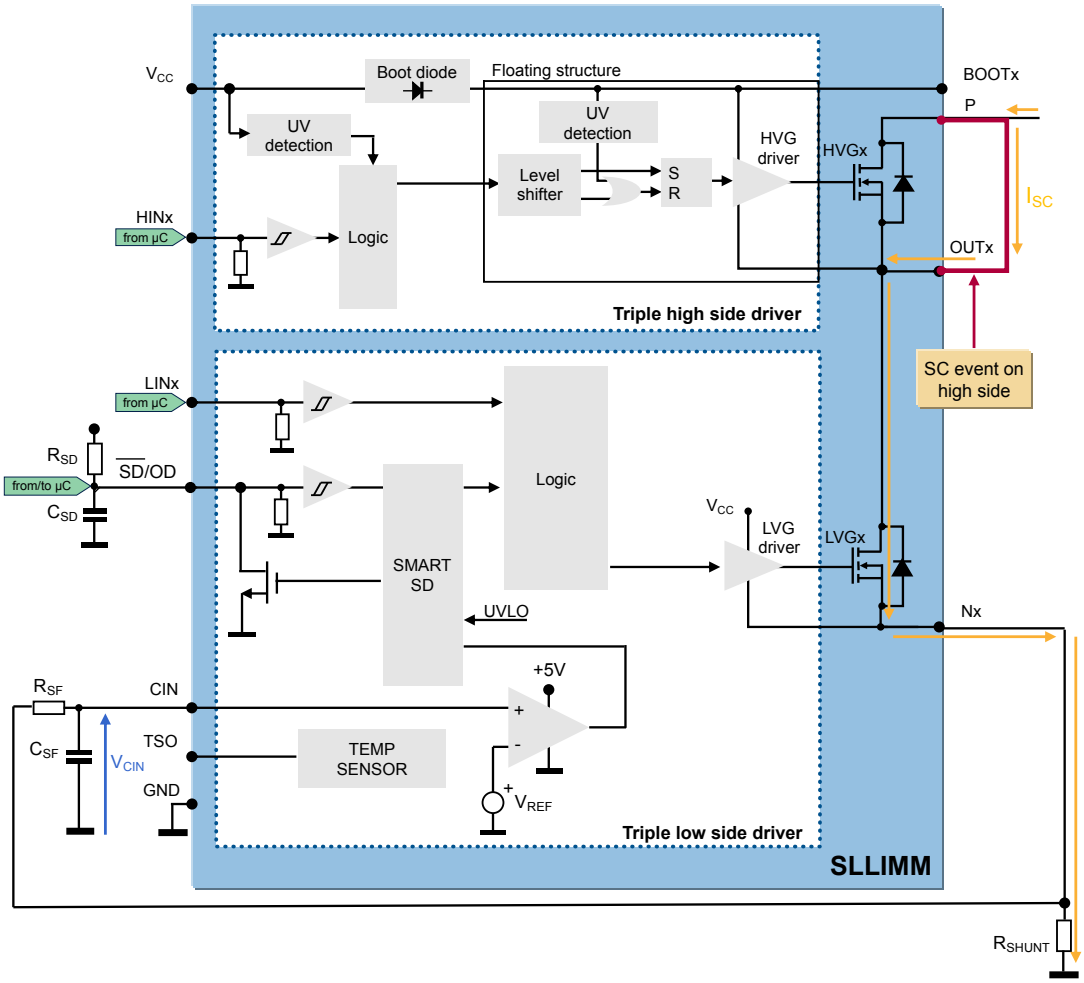
$$t_{Total} = t_{SF} + t_{CIN\_LVG} + t_{off} \quad (10)$$

Considering that the MOSFET short-circuit withstand time (t_{SC}) is 12 µs, t_{SF} should be set in the order of a few microseconds.

In a 3-shunt resistor circuit, a specific control technique can be implemented by using the three shunt resistors (R_{SHUNT_U}, R_{SHUNT_V} and R_{SHUNT_W}) to monitor each phase current.

An example short-circuit event during normal operation, between P and OUTx when LINx is high, is shown in the figure below.

Figure 20. **Example of a short-circuit event**



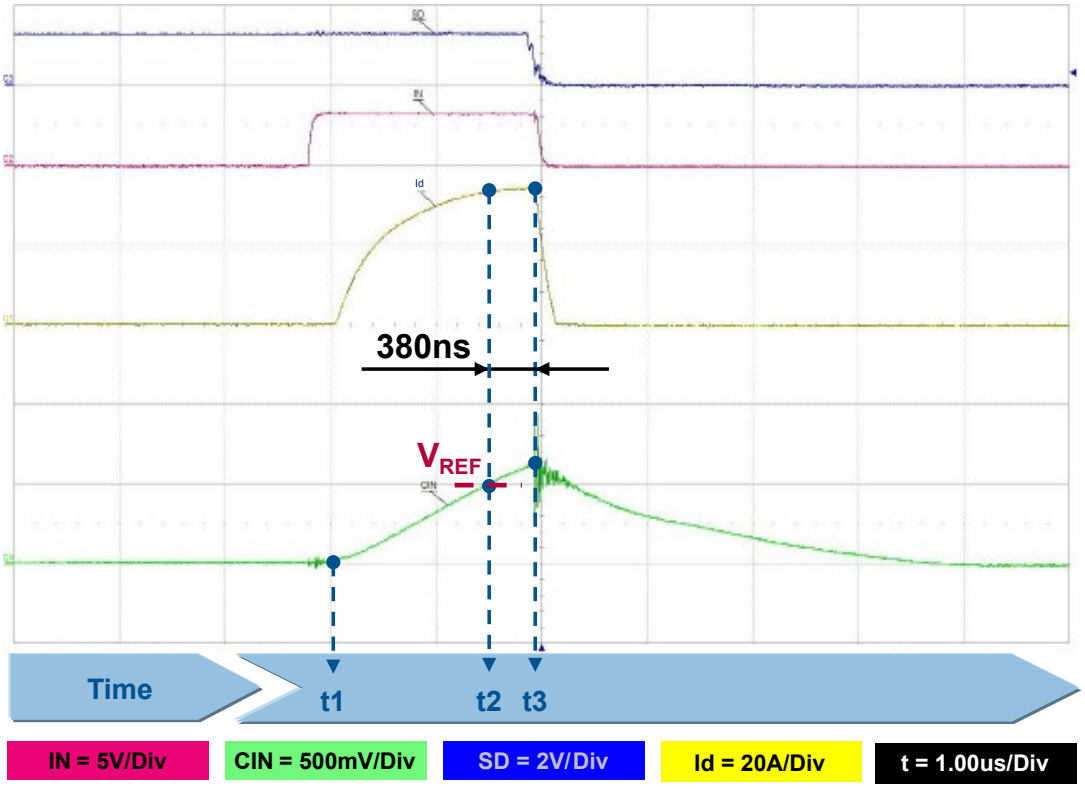
Smart shutdown operation clearly demonstrates the highly rapid protection offered by the smart shutdown function for an overcurrent fault event occurring on an HS MOSFET.

The main steps, shown in the figure below, are:

- t1: drain current I_D starts to rise. An SC event is not detected yet due to the RC network on the CIN pin
- t2: voltage on V_{CIN} reaches V_{REF}. An SC event is detected and the smart shutdown starts turning off the LS MOSFETs. The SD signal is enabled (for 24 µs) so the MCU can stop the PWM signals and as a consequence of this, even the HS MOSFETs are turned off.
- t3: the SLLIMM is definitively turned off in less than 400 ns (including the $t_{d(off)}$ time of MOSFET) from SC detection.

In summary, the total disable time is t3-t2 and the total SC action time is t3-t1.

Figure 21. **Smart shutdown operation**



2.2.9 Fault management

The SLLIMM 2nd series SJ MOSFET integrates a specific kind of fault management, useful when the $\overline{SD}$ pin acts as output and is able to identify the type of fault event.

As previously described, as soon as a fault occurs, the open-drain (DMOS) is activated and LVG outputs are forced low and consequently the LS MOSFETs.

Two types of fault can be identified:

- Overcurrent (OC) sensed by the internal comparator (C_{IN})
- Undervoltage (UVLO) on LS gate driver supply voltage (V_{CCL})

During an UVLO event, the supply voltage must in any case be higher than 4 V to ensure the full functionality of fault management logic.

Each fault event enables the $\overline{SD}$ open drain for a different time interval to allow the type of failure event to be identified. Actually, the device remains in a fault condition for a total duration time also depending on the RC network connected to the $\overline{SD}$ pin. The network generates a time contribution that is added to the internal value shown in the table below.

Table 8. SD duration time per event

Symbol	Parameter	Event time	SD open-drain enable time result
OC	Overcurrent event	≤ 24 µs(1)	24 µs(1)(2)
		> 24 µs(1)	OC time
UVLO	Undervoltage lock out even	≤ 70 µs(1)	70 µs(1)(2)
		> 70 µs(1) until the V_{CC_LS} exceeds the $V_{CC\_LS\ UV\ turn\ ON\ threshold}$	UVLO time

1. *Typical value (T_J = - 40 °C to 125 °C).*
2. *Without the contribution of RC network on SD.*

The table below summarizes the fault events and the effect on the MOSFETs and $\overline{SD}$ pin.

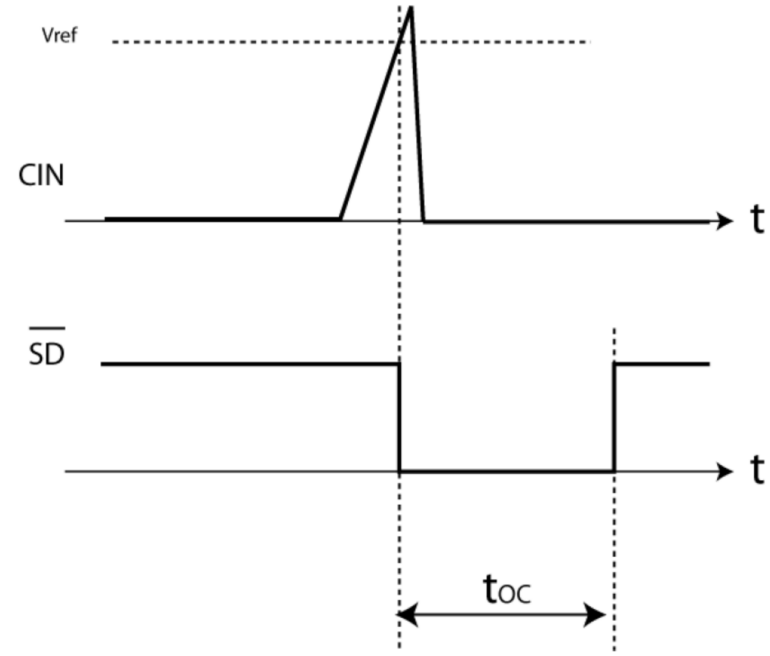
Table 9. Fault event summary effect on MOSFET and SD

Fault event	HS MOSFETs	LS MOSFETs	$\overline{SD}$/OD
OC	ON	OFF	Low (SET) (for t_{OC})(1)
UVLO V_{CCH}	OFF	Operative	High (RESET)
UVLO V_{CCL}	Operative	OFF	Low (SET) (for t_{UVLO})(1)
UVLO V_{boot}	OFF	Operative	High (RESET)

1. *Without the contribution of RC network on SD.*

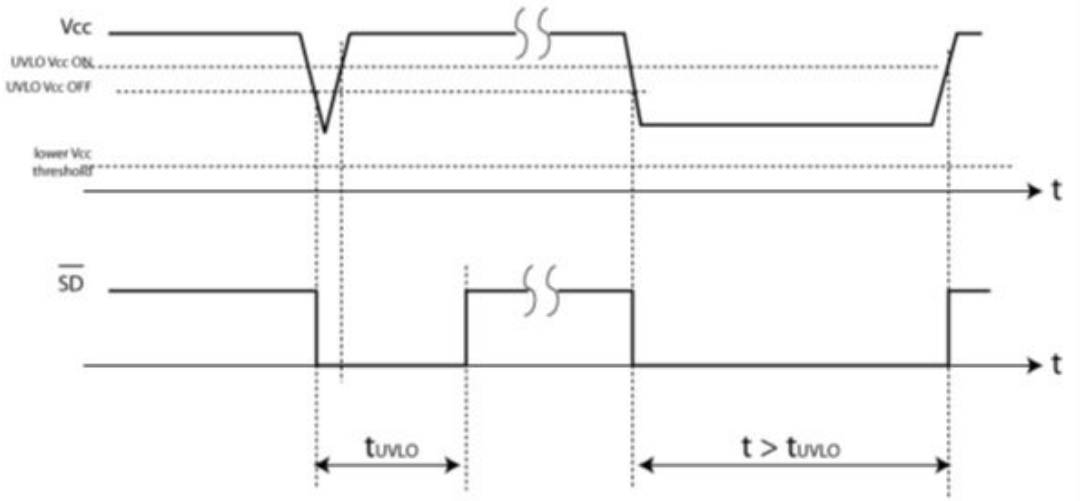
The following figures demonstrate device behavior during OC and UVLO events.

Figure 22. **OC event**



*without contribution of RC network on SD

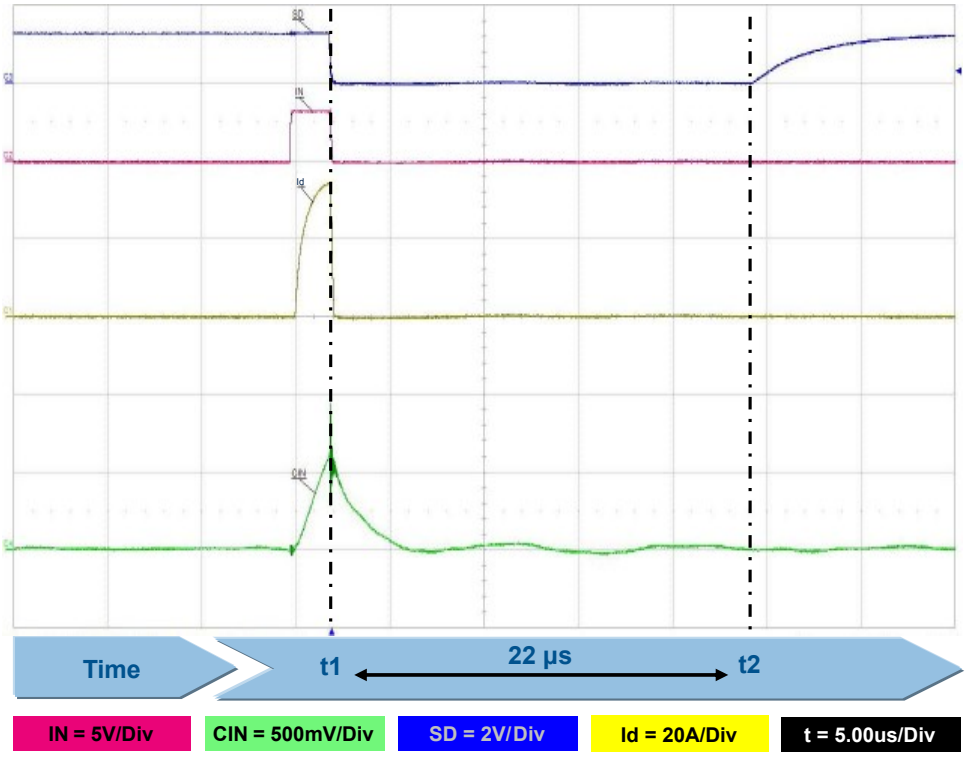
Figure 23. **UVLO event**



*without contribution of RC network on SD

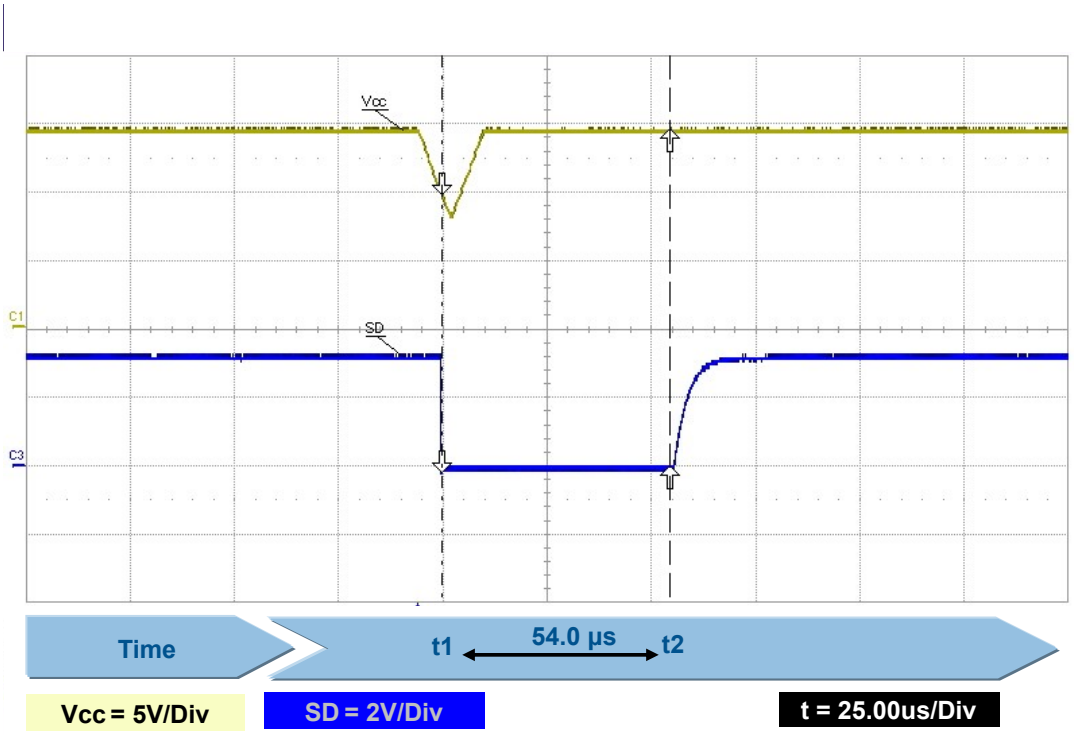
The figure below shows a shutdown as the result of an overcurrent event. During the overcurrent, the voltage on the comparator (CIN) exceeds the threshold (0.51 V typ.) and the shutdown is able to stop the application. In this case, the SD event time is about 24 µs (for OC event less than 24 µs).

Figure 24. **SD duration for OC event**



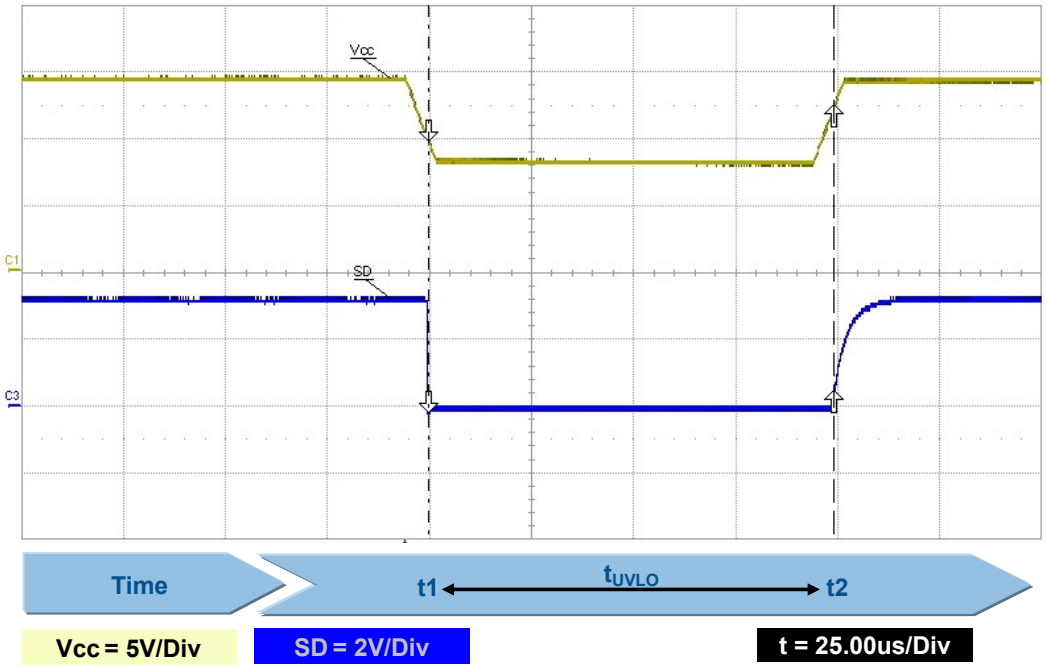
The following figure shows real acquisition data for a short UVLO event (≤ 70 µs) on the V_{CCL} (yellow waveform) supply voltage (V_{CCL} > 4 V). When this voltage drops to the undervoltage threshold ($V_{CC\_th(off)}$), the SD (blue waveform) is SET. The figure clearly shows an SD duration of about 70 µs (for a UVLO event less than 70 µs).

Figure 25. **SD duration for short UVLO event (≤ 70 µs)**



The following figure shows real acquisition data for a long UVLO event (> 70 µs) on the V_{CCL} (yellow waveform) supply voltage (V_{CCL} > 4 V). In this case, V_{CCL} remains in the UVLO condition for more than 70 µs and the SD duration is the same as the UVLO duration.

Figure 26. **SD duration for long UVLO event (> 70 µs)**



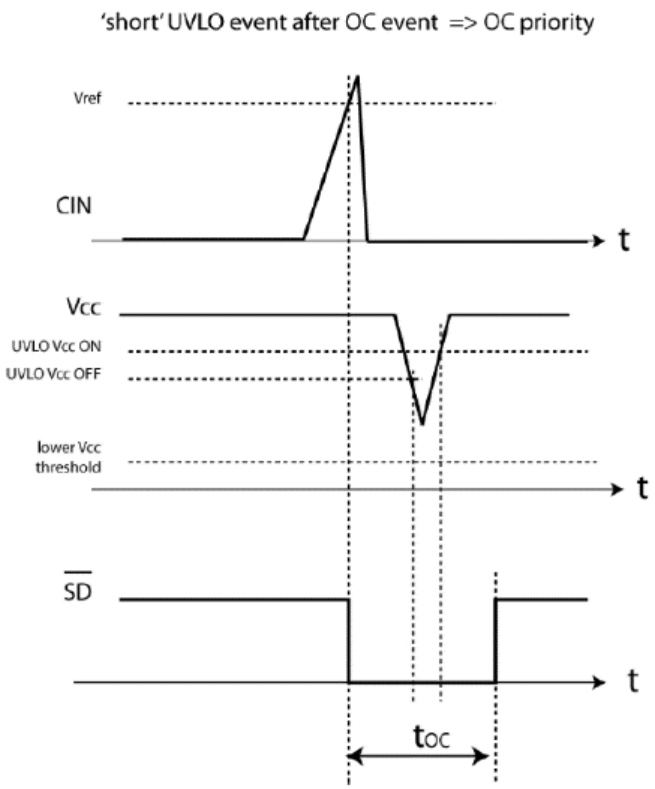
The following simultaneous fault events are in any case highly unlikely:

The Figure 27. Short UVLO event after OC event shows a short (≤ 24 µs) UVLO event within an OC event. In this case, the fault duration is t_{OC} (24 µs).

The Figure 28. Long UVLO event after OC event shows a long (> 24 µs) UVLO event while the IPM is an OC event. In this case, the fault signal only elapses when UVLO terminates (> 70 µs).

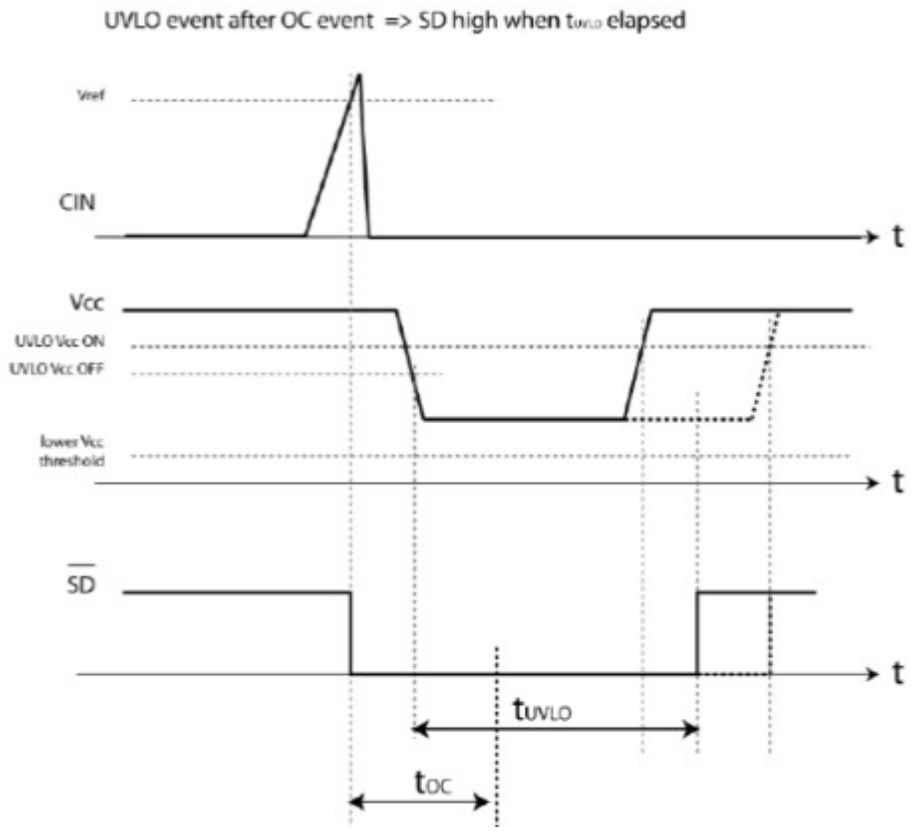
If the internal comparator is not used for overcurrent protection, comparator triggering may occur when the device is in a UVLO state, as shown in the Figure 29. Comparator triggering in UVLO condition. In this case the fault duration is given by the overlap between t_{OC} and t_{UVLO}.

Figure 27. **Short UVLO event after OC event**



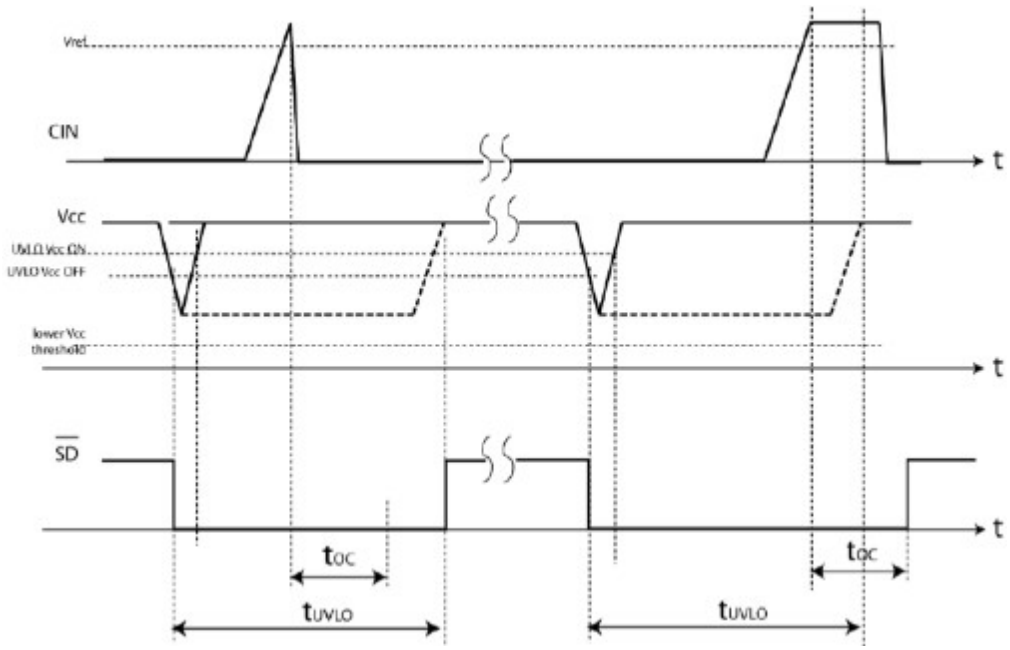
*without contribution of RC network on SD

Figure 28. **Long UVLO event after OC event**



*without contribution of RC network on SD

Figure 29. **Comparator triggering in UVLO condition**

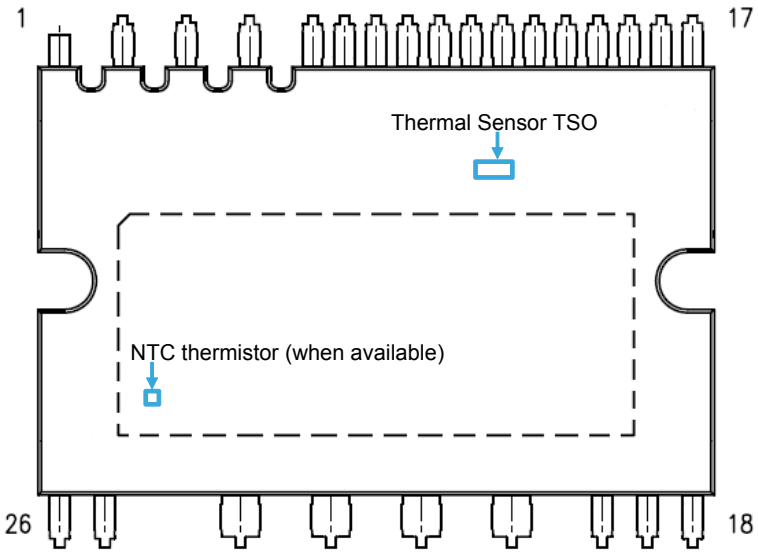


*without contribution of RC network on SD

2.2.10 Temperature monitoring

The SLLIMM 2nd series SJ MOSFET family integrates a thermal sensor (TSO) on the low-side gate driver and an NTC thermistor (optional) placed near the power stage for internal IPM temperature monitoring.

Figure 30. Temperature detection points (top view)



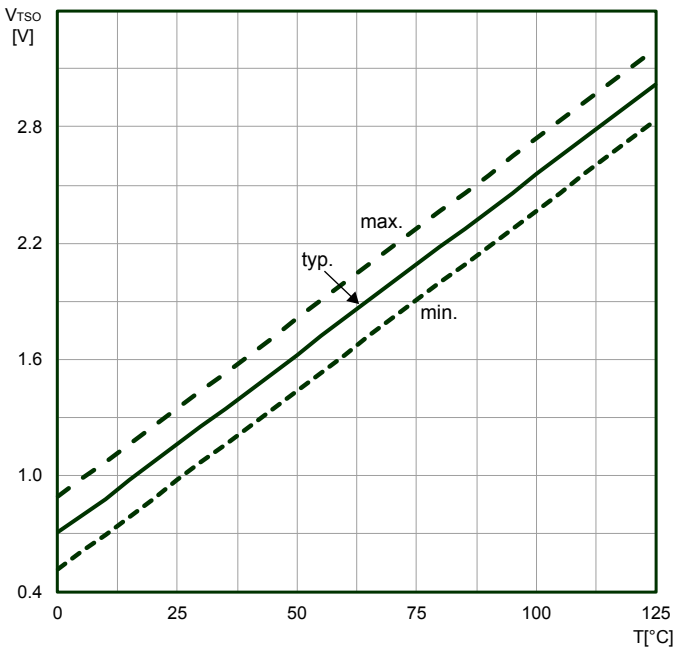
2.2.10.1 Thermal sensor (TSO)

The SLLIMM 2nd series SJ MOSFET family includes a temperature sensor integrated on the LS gate driver. The internal heat generated during normal operation is transferred to the sensor through the internal resin and heatsink. Temperature and consequent voltage variation is therefore not immediate. For this reason, we recommend using this function for monitoring and eventual protection when slow temperature increases are detected in cases such as during continuous overload. A voltage proportional to the temperature is available on TSO pin (17) and the sensor does not need any pull-down resistor. To increase the noise immunity, a capacitor filter of 1 to 10 nF must be placed on this pin.

This function cannot shut the SLLIMM down directly if the temperature rises above safe temperatures, but the output voltage can be sent to a circuit (such as a comparator) to provide feedback to the MCU which can in turn halt the IPM.

The figure below shows a typical voltage variation with a temperature graph. For specific device information, please refer to the relevant datasheet.

Figure 31. **Thermal sensor voltage vs temperature**



The output voltage is a linear characteristic compatible with the 3.3 V MCU supply voltage. If a safety margin is required, a 3.3 V clamp circuit at can be used. The following figures show typical circuits that can be used to monitor internal temperature and provide relevant information to the MCU, which can halt the IPM if necessary.

Figure 32. **Normal voltage controller (MCU)**

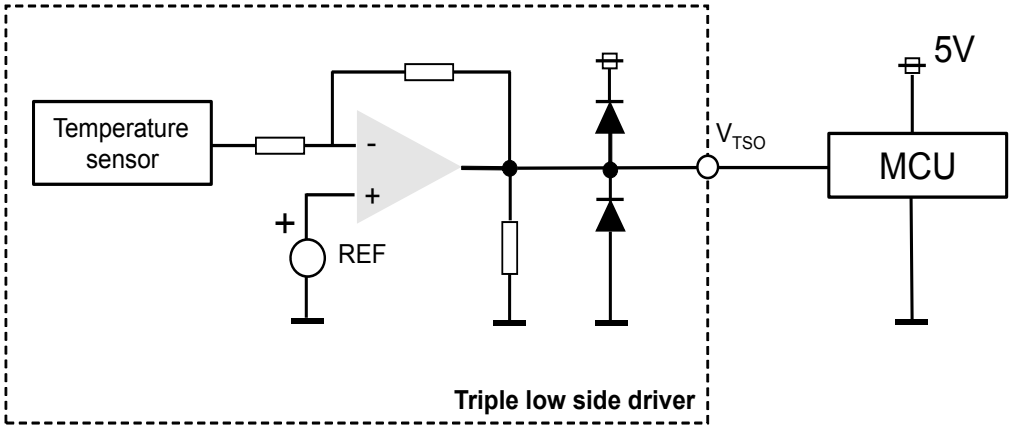
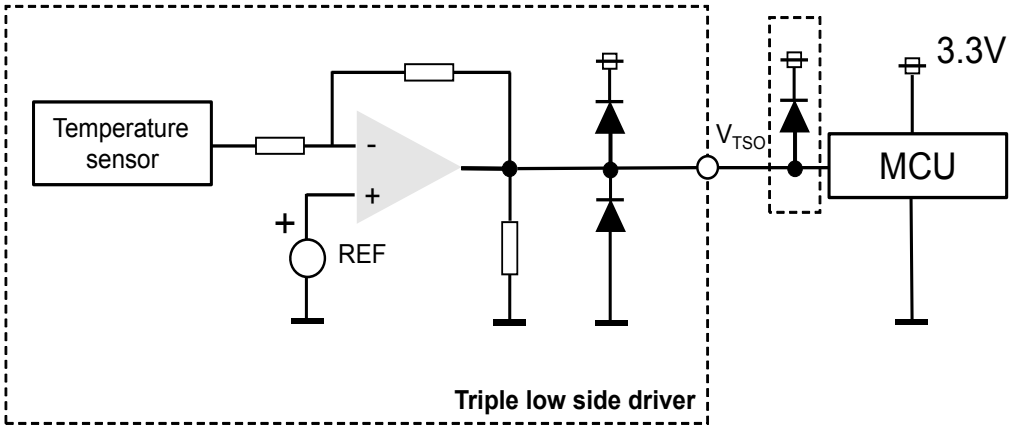


Figure 33. **Low voltage controller (MCU): optional clamping**



The internal circuit consists of a temperature sensor, an amplification network to amplify the signal and ESD protection. Its current capability is 4 mA min. source (I_{TSO_SRC}) and 0.1 mA typ. (I_{TSO_SNK}).

When this function is not used, the TSO pin can be left floating.

2.2.10.2 *NTC thermistor*

The SLLIMM 2nd series SJ MOSFET can be optionally equipped with a negative temperature coefficient (NTC) thermistor for easy over temperature protection, by sending the microcontroller real-time temperature data.

Due to the thermal impedance of SLLIMM and its own time constant, the NTC thermistor is not suited to detecting rapid junction temperature rises directly in the power devices. Therefore, it cannot be used for short-circuit or overcurrent protection, but only to monitor gradual changes in temperature.

The NTC thermistor is placed very close to the power stage for accurate junction temperature monitoring of power chips.

The resistance versus temperature characteristic of NTC thermistor is nonlinear and it is described by the following expression:

$$R\left(T\right) = R_{25} \cdot e^{B\left(\frac{1}{T} - \frac{1}{298}\right)} \quad (11)$$

Where T is the temperature in Kelvin, B is a constant in the SLLIMM operating range and R25 is the resistance at 25 °C; these last two parameters are shown in the datasheet.

The built-in thermistor (85 kΩ at 25 °C) is inside the IPM and connected between T1 and T2 pins (26, 25).

Figure 34. **NTC resistance vs temperature**

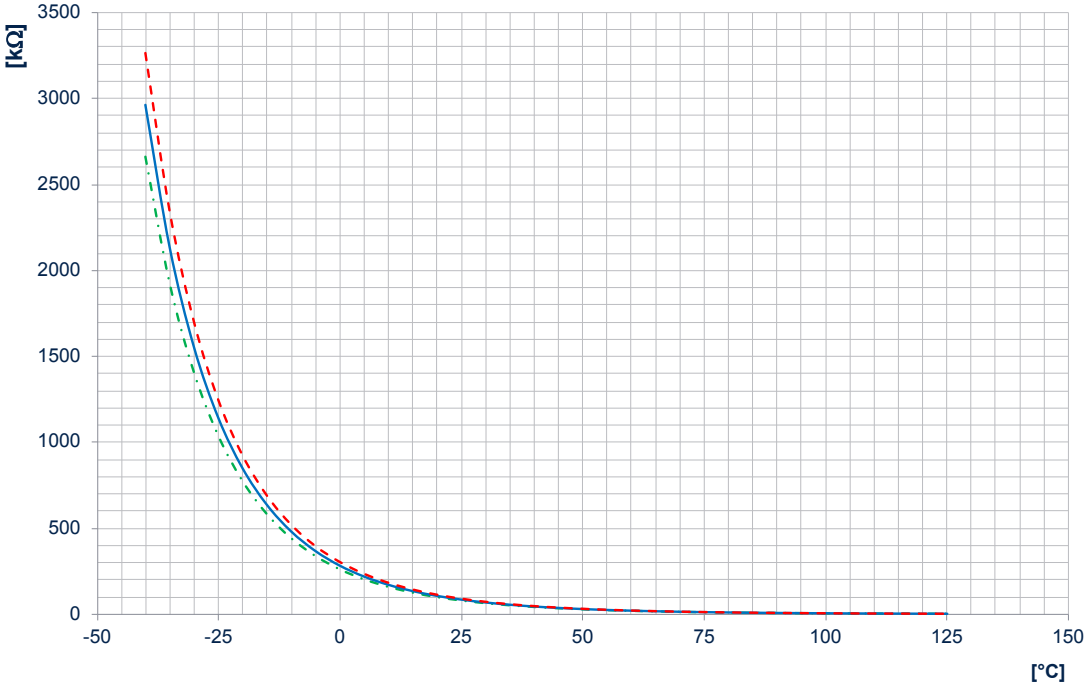
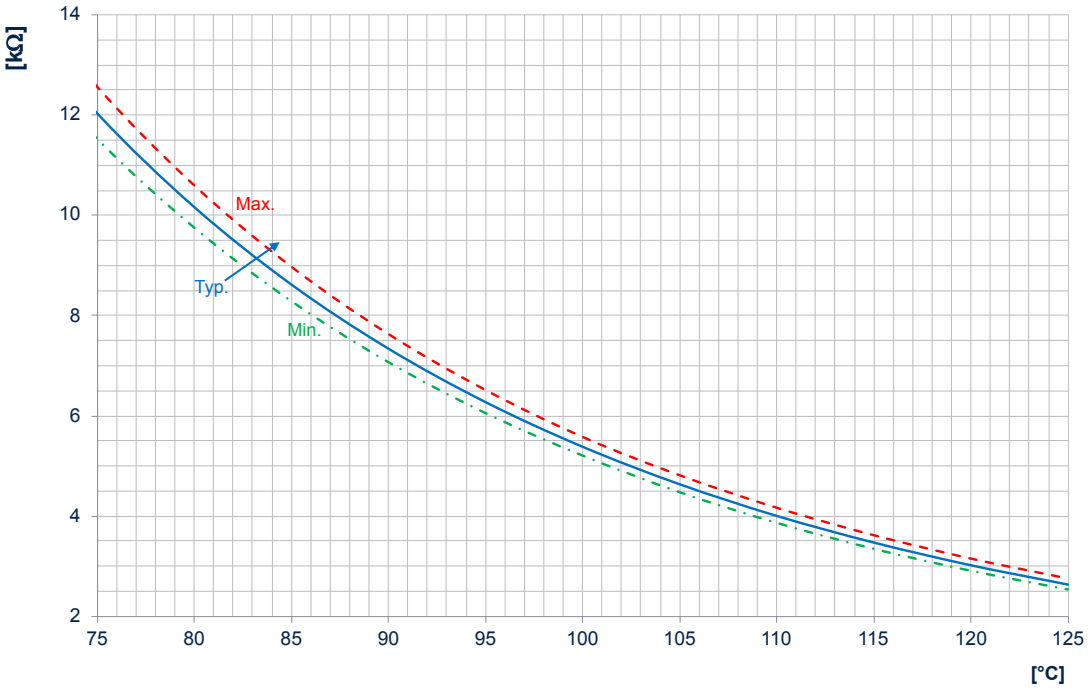
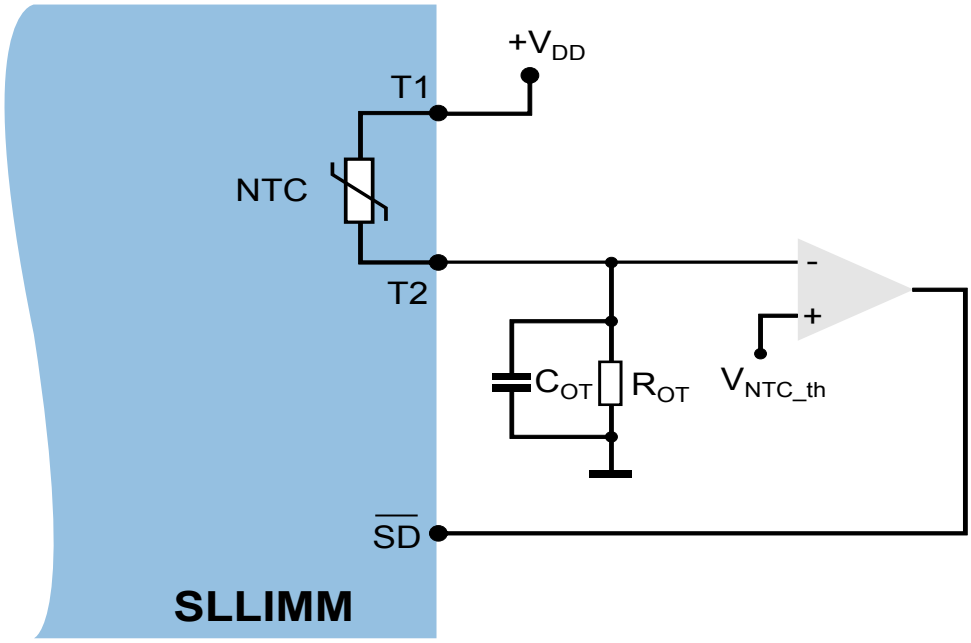


Figure 35. **NTC resistance vs temperature – zoom**



The following figure shows a simple circuit using a voltage divider for both overtemperature protection and temperature monitoring.

Figure 36. **Sample overtemperature protection circuit**



The external comparator is used to send a shutdown signal to the SLLIMM in case of over temperature. V_{NTC_th} is a threshold voltage, fixed by design, and connected to the noninverting input, while the inverting input is connected to a voltage divider based on the NTC and R_{OT} resistors. When the voltage on the inverting input exceeds the V_{NTC_th} value, the comparator triggers, pulling down the $\overline{SD}$ pin and consequently switching off the LS MOSFETs.

For a proper sizing of the voltage divider, the maximum allowed temperature level (T_{OT_Max}) must first be set and the thermistor resistance derived from the Eq. (11), as well as from the Figure 34. NTC resistance vs temperature and Figure 35. NTC resistance vs temperature – zoom. The value of resistance R_{OT} can be calculated with the voltage divider formula:

$$V^{-}(T) = \frac{R_{OT}}{R_{NTC}(T) + R_{OT}} \cdot V_{DD} \quad (12)$$

Considering that, if $T = T_{OT\_Max}$ then $V\text{-}(T_{OT\_Max}) = V_{NTC\_th}$.

The maximum allowed power on the thermistor should not exceed 5 mW across the entire operating range to guarantee safe operation and avoid power consumption affecting the temperature measurement through self-heating.

Therefore, for $T = T_{OT\_Max}$:

$$R_{NTC} \cdot I^2 = R_{NTC} \cdot \left(\frac{V_{DD}}{R_{NTC}+R_{OT}}\right)^2 \leq 5mW \quad (13)$$

Finally, to increase the noise immunity of the NTC thermistor, we recommend placing a decoupling capacitor (C_{OT}) in parallel, whose value must be between 10 and 100 nF.

The following figures show two samples pull-up and pull down resistor configurations and corresponding voltage output graphs as function of temperature. Both curves include the maximum spread according to the tolerance of the NTC and RPU/RPD resistances.

Figure 37. V_{NTC} vs temperature (pull up configuration)

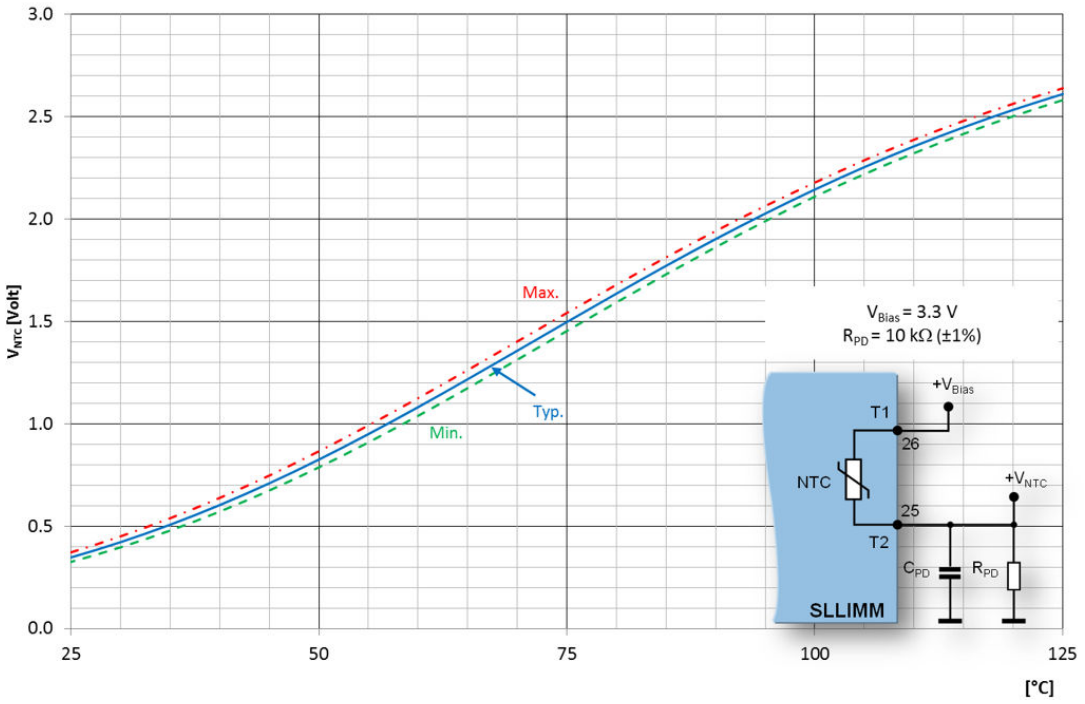
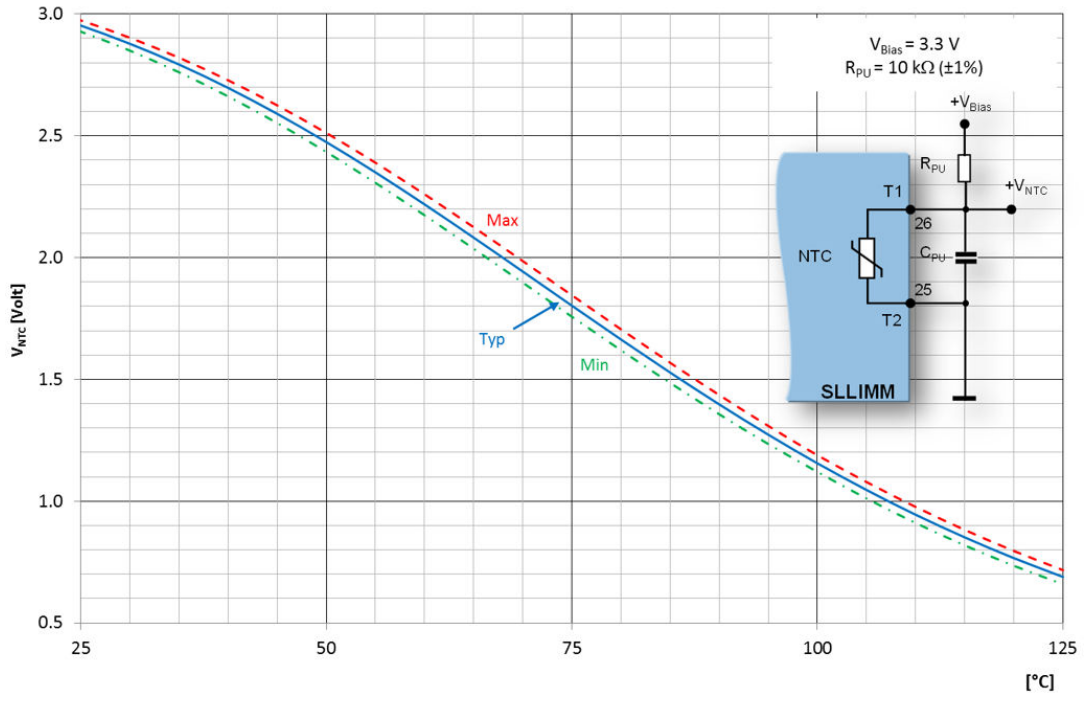


Figure 38. V_{NTC} vs temperature (pull down configuration)



2.2.11 Bootstrap circuit

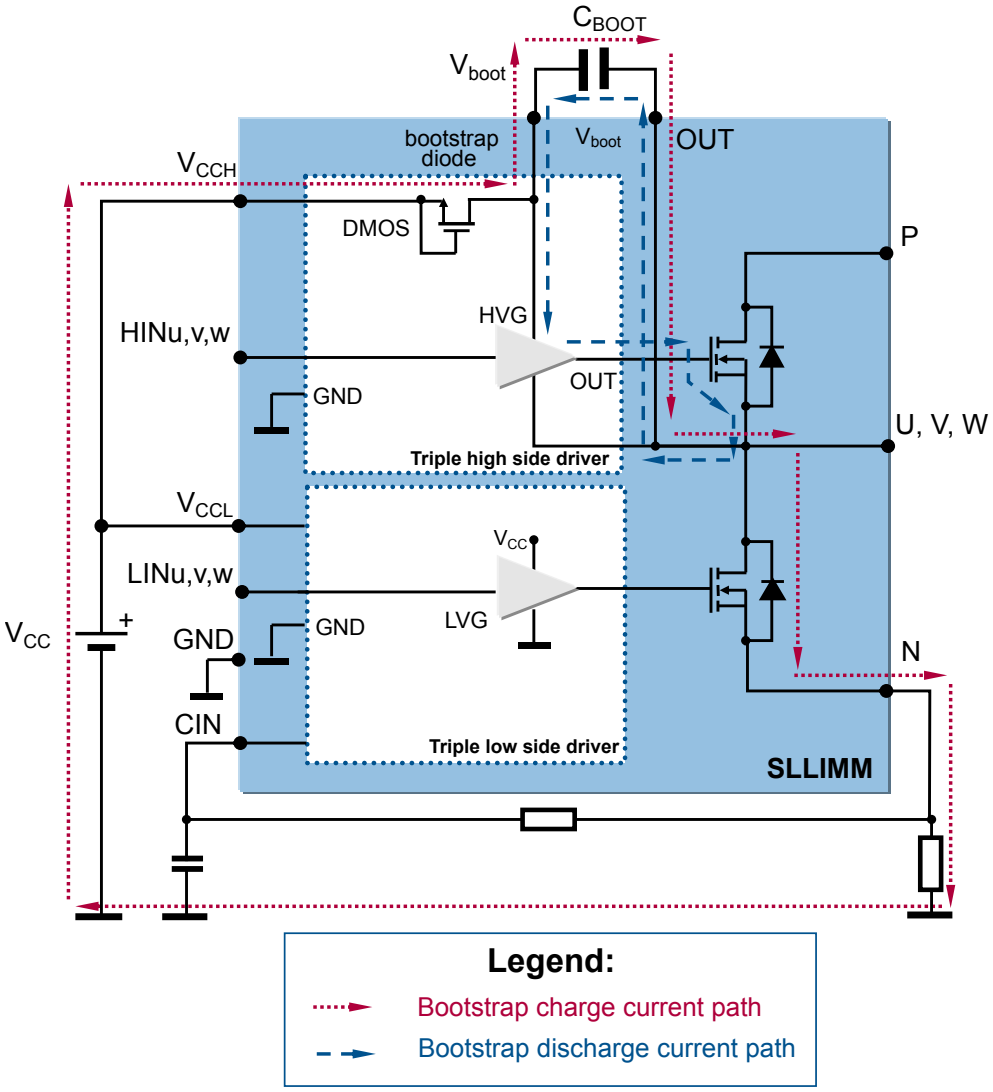
In the 3-phase inverter, the sources of the low-side MOSFETs are connected to the negative DC bus (VDC-) as the common reference ground, which allows all low-side gate drivers to share the same power supply, while the source of the high-side MOSFETs is alternately connected to the positive (VDC+) and negative (VDC-) DC bus during operation.

A bootstrap method is a simple and cheap solution to supply the high-voltage section. This function is normally accomplished by a high-voltage fast recovery diode.

The SLLIMM family includes a patented integrated structure that replaces the external diode. It is realized with a high-voltage DMOS working as a diode with a series resistor.

The operation of the bootstrap circuit is shown in the figure below. The floating supply capacitor C_{BOOT} is charged by the V_{CC} supply when V_{OUT} is lower than V_{CC} through the bootstrap diode and the DMOS path with reference to the “bootstrap charge current path”. During the high-side MOSFET on phase, the bootstrap circuit provides the right gate voltage to properly drive the MOSFET (see the “bootstrap discharge current path” in the figure below). This circuit is iterated for all the three half-bridges.

Figure 39. Bootstrap circuit



The value of the C_{BOOT} capacitor should be calculated according to the application condition and must consider the following:

- The voltage across C_{BOOT} must be maintained at a value higher than the undervoltage lockout level (V_{BS_th}). This enables the high-side MOSFET to work with the correct gate voltage (lower dissipation and better overall performances).
- The voltage across C_{BOOT} is affected by different components such as drops across the integrated bootstrap structure, drops across the low-side MOSFET, and others.
- When the high-side MOSFET is on, the C_{BOOT} capacitor discharges mainly to provide the right MOSFET gate charge, but other phenomena must be considered such as leakage currents, quiescent current, etc.
- Bear in mind that if a voltage below the UVLO threshold is applied on the bootstrap channel, the HS gate driver disables its output without a fault signal.

2.2.11.1 *Bootstrap capacitor selection*

A simple method to properly size the bootstrap capacitor considers only the amount of charge that is needed when the high-voltage side of the driver is floating and the MOSFET gate is driven once. This approach does not consider either the duty cycle of the PWM or the fundamental frequency of the current. Observations on PWM duty cycle, type of modulation (6-step, 12-step and sine-wave) must be considered with their own peculiarities to achieve optimal bootstrap circuit sizing.

During the bootstrap capacitor charging phase, the low-side MOSFET is on and the voltage across C_{BOOT} (V_{CBOOT}) can be calculated as follows:

$$V_{CBOOT} = V_{CC} - V_F - V_{RDS(on)} - V_{DS(on)max} \quad (14)$$

Where:

V_{CC}: supply voltage of gate driver

V_F: bootstrap diode forward voltage drop

$V_{DS(on)max}$: maximum drain source voltage drop of the low-side MOSFET

$V_{RDS(on)}$: DMOS voltage drop

The dimension of the bootstrap capacitance C_{BOOT} value is based on the minimum voltage drop (ΔV_{CBOOT}) to guarantee when the high-side MOSFET is on, and it must be:

$$\Delta V_{CBOOT} = V_{CC} - V_F - V_{RDS(on)} - V_{GS(min)} - V_{DS(on)max} \quad (15)$$

Under the condition:

$$V_{CBOOT(\min)} > V_{BS\_th(on)} \quad (16)$$

Where:

$V_{GS(min)}$: minimum gate-source voltage of high side MOSFET

$V_{BS\_th(on)}$: bootstrap turn-on undervoltage threshold (maximum value, refer to the related datasheet)

Considering the factors contributing to a decrease in V_{CBOOT}, the total charge supplied by the bootstrap capacitor (during the high-side on phase) is:

$$Q_{TOT} = Q_{GATE} + \left(I_{LKGS} + I_{QBO} + I_{LK} + I_{LKDiode} + I_{LKCap}\right) \cdot t_{Hon} + Q_{LS} \quad (17)$$

Where:

Q_{GATE}: total MOSFET gate charge

I_{LKGS}: MOSFET gate source leakage current

I_{QBO}: bootstrap circuit quiescent

I_{LK}: bootstrap circuit leakage current

$I_{LKDiode}$: bootstrap diode leakage current

I_{LKCap}: bootstrap capacitor leakage current (relevant when using an electrolytic capacitor, but can be ignored if other types of capacitors are used)

t_{Hon}: high-side on time

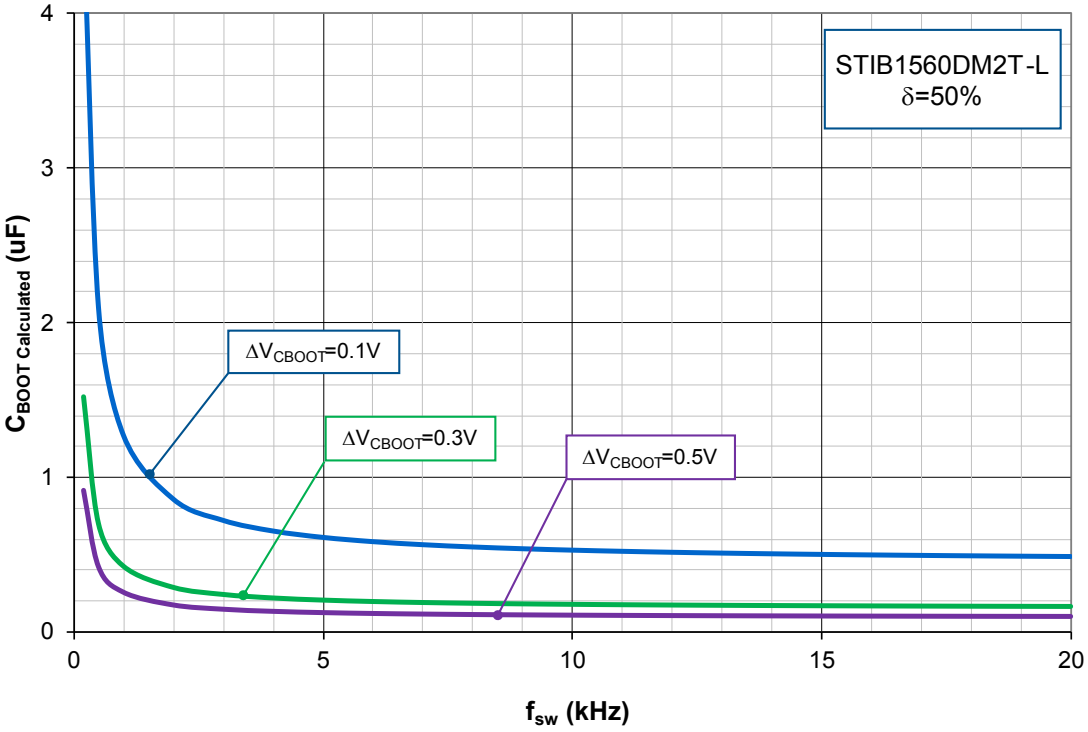
Q_{LS}: charge required by the internal level shifters

Finally, the minimum size of the bootstrap capacitor is:

$$C_{BOOT} = \frac{Q_{TOT}}{\Delta V_{CBOOT}} \quad (18)$$

For an easier selection of the bootstrap capacitor, the following figure shows the behavior of C_{BOOT} (calculated) versus the switching frequency (f_{sw}), with different values of ΔV_{CBOOT}, corresponding to Eq. (18) for continuous sinusoidal modulation and for STIB1560DM2T-L (worst case) and a duty cycle of δ = 50 %. For all the other devices, the bootstrap capacitor can be calculated using the same curve.

Figure 40. **Bootstrap capacitor vs switching frequency**



Considering the limit cases during the PWM control and further leakages and dispersions in the board layout, the capacitance value for the bootstrap circuit should be two or three times higher than C_{BOOT} derived from the Figure 40. Bootstrap capacitor vs switching frequency . The bootstrap capacitor should have a low ESR value for good local decoupling, therefore, if an electrolytic capacitor is used, one parallel ceramic capacitor placed directly on the SLLIMM pins is highly recommended.

Related links

STEVAL-IPMM15B: 1500 W motor control power board based on STIB1560DM2T-L SLLIMM 2nd series IPM

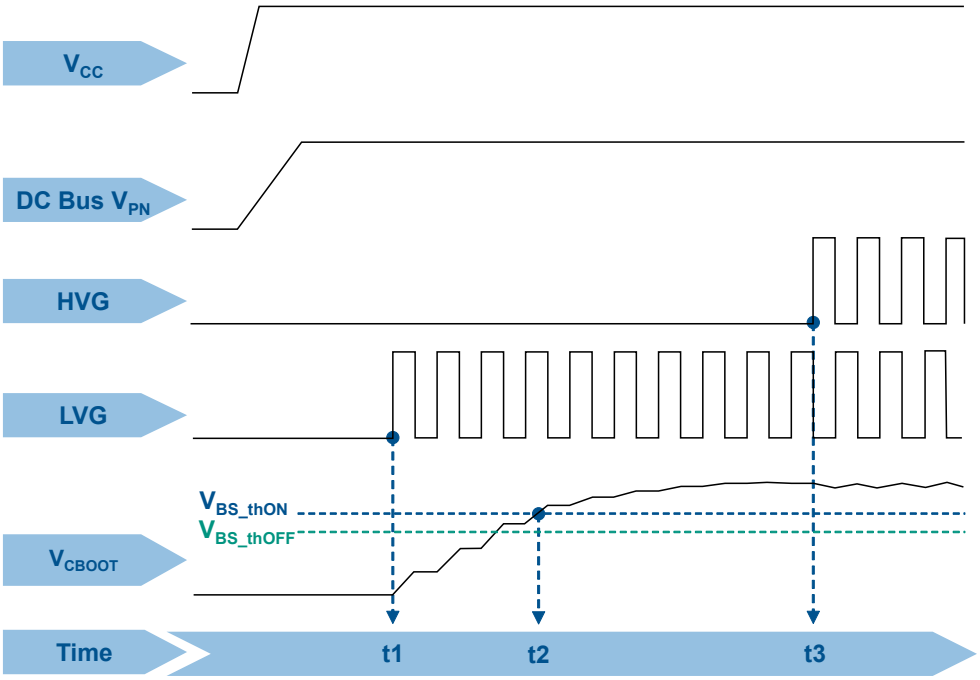
2.2.11.2 *Initial bootstrap capacitor charging*

During the startup phase, the bootstrap capacitor must be charged long enough to complete the initial charging time (t_{CHARGE}), which is at least the time V_{CBOOT} needs to exceed the turn-on undervoltage threshold V_{BS_thON}, as already stated in the Eq. (14).

For normal operation, the voltage across the bootstrap capacitor must never drop down to the turn-off undervoltage threshold V_{BS_thOFF}.

During startup, only the low-side MOSFET is switched on and the PWM is run immediately after this phase, as shown by the sequence in the following figure.

Figure 41. **Initial bootstrap charging time**



The timing chart is based on the following steps:

- t1: the bootstrap capacitor starts to charge through the low-side MOSFET (LVG)
- t2: the voltage across the bootstrap capacitor (V_{CBOOT}) reaches its turn-on undervoltage threshold V_{BS_thON}
- t3: the bootstrap capacitor is fully charged, this enables the high-side MOSFET and the C_{BOOT} capacitor starts discharging to provide the right MOSFET gate charge. The bootstrap capacitor recharges during the on state of the low-side MOSFET (LVG).

The initial charging time is given by the Eq. (19) and must, for safety reasons, be at least three times longer than the calculated value.

$$t_{CHARGE} \geq \frac{C_{BOOT} \cdot R_{DS(on)}}{\delta} \cdot ln\left(\frac{V_{CC}}{\Delta V_{CBOOT}}\right) \quad (19)$$

Where δ is the duty cycle of the PWM signal and $R_{DS(on)}$ is 150 Ω typical value, as per the datasheet.

A practical example can be analyzed by considering a motor drive application where the PWM switching frequency is 6 kHz, with a duty cycle of 50%, and ΔV_{CBOOT} = 0.1 V (considering V_{CC} = 15 V). From the graph in the Figure 40. Bootstrap capacitor vs switching frequency , the bootstrap capacitance is 0.6 µF so C_{BOOT} can be chosen between 1.2 and 1.8 µF. We shall adopt the commercially available 1.5 µF capacitor.

From the Eq. (19), the initial charging time is:

$$t_{CHARGE} \geq \frac{1.5 \cdot 10^{-6} \cdot 150}{0.5} \cdot ln\left(\frac{15}{0.1}\right) = 2.25\ ms \quad (20)$$

For safety reasons, the initial charging time must be at least 6.75 ms.

2.2.12 Output safe clamp

Both HS and LS gate driver ICs are designed with an output safe clamp to guarantee the low impedance of the MOSFET driving network (V_{LVG}, V_{HVG} = 1 V at I_{sink} = 10 mA, V_{CC} > 3 V) even in the shutdown condition. This feature guarantees the off state of the MOSFET and avoids any undesired turning on due to the Miller effect, for example.

3 Package

The SLLIMM 2nd series SJ MOSFET benefits from a more compact package while providing high-power density, the best thermal performance, and good electrical isolation (> 1600 V_{RMS}).

The SDIP2B-26L is a dual-in-line transfer mold package featuring DBC (direct bonded copper) technology for best performance in terms of thermal behavior.

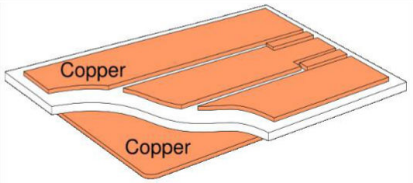
This package technology is available in 26-lead version (SDIP2B-26L) with or without an additional on-board NTC thermistor. A vacuum soldering process is used to avoid the inclusion of any gas (voids) during the soldering process that could cause potential hot spots. This results in a further increase in the reliability of the SLLIMM family due to the improved thermal and electrical conductivity.

The DBC technology allows extremely low thermal resistance values, high stability in thermal cycling and high quality.

3.1 DBC structure

DBC stands for direct bonded copper, a process in which copper and a ceramic material are directly bonded, as shown in the figure below. Direct bonded copper substrates are a proven, high-performance solution for the electrical isolation and thermal management of high-power semiconductor modules.

Figure 42. DBC structure



The advantages of DBC substrates are:

- High current-carrying capability, due to thick copper metallization
- A thermal expansion coefficient close to the silicon value at the copper surface.

DBC has two layers of copper that are directly bonded onto an aluminum-oxide (Al_2O_3) ceramic base. The DBC process yields a superthin base and eliminates the need for the thick, heavy copper bases used prior to this process.

Because SLLIMM with DBC bases has fewer layers, it has much lower thermal resistance values than those one based on different materials.

The main properties of DBC include:

- High mechanical strength
- Mechanically stable dimensions
- Good adhesion
- Corrosion resistance
- Excellent electrical isolation
- High thermal conductivity
- A thermal expansion coefficient is similar to that of the silicon, so no interface layers are required
- Good heat diffusion
- Can be structured just like printed circuit boards or "IMS substrates"
- Environmentally friendly

The DBC package consists of a DBC substrate for the power stage and a lead frame structure for the control stage, both housed using the transfer molding process.

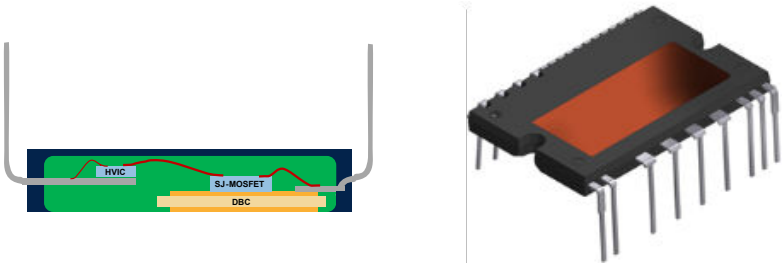
Table 10. $R_{th(j-c)}$ comparison

Part number	I_D	$R_{TH(J-C)}$ MOSFET
STIB1060DM2x-y	10 A	1.59 °C/W
STIB1560DM2x-y	15 A	1.1 °C/W

3.2 Package structure

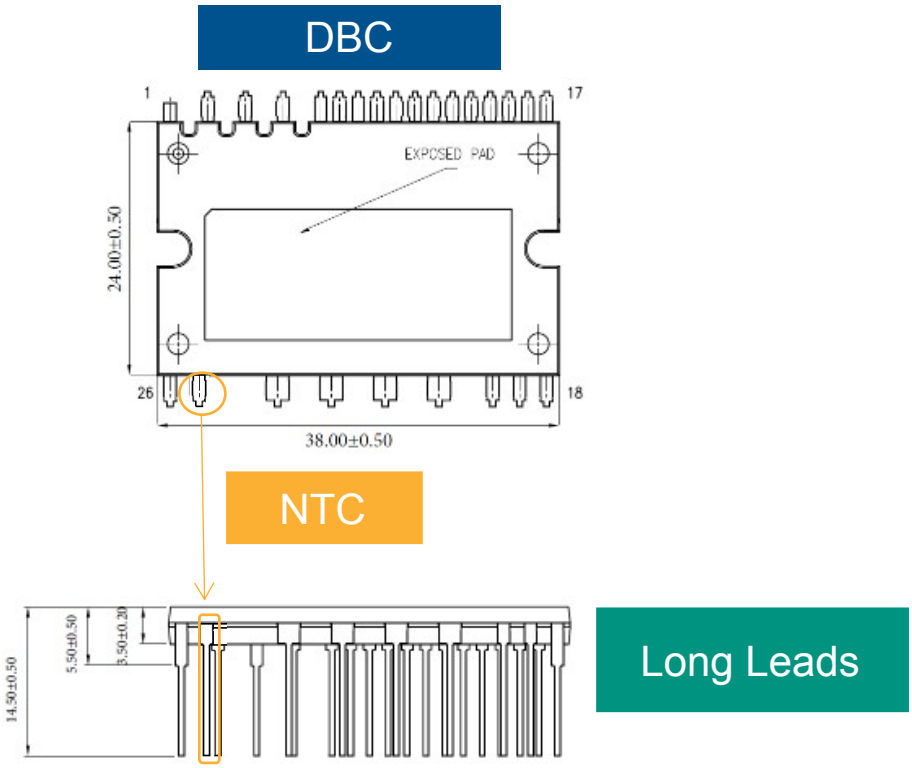
The following figure shows both the external and internal structures of the SDIP2B-26L package.

Figure 43. SDIP2B-26L external and internal representation



The following figure shows the long leads version of the SDIP2B-26L package.

Figure 44. SDIP2B-26L - Long leads package



All dimensions are expressed in millimeters

For further package outline details and dimensions, refer to the relevant datasheet.

3.3 Input and output pin descriptions

This section defines the SLLIMM 2nd series SJ MOSFET input and output pins. For a more accurate description and layout suggestions, please consult the relevant sections.

Table 11. SDIP2B-25/26L input and output pins

Pin	Name	Description
1	-	NC
2	VBOOTu	Bootstrap voltage for U phase
3	VBOOTv	Bootstrap voltage for V phase
4	VBOOTw	Bootstrap voltage for W phase
5	HINu	High-side logic input for U phase
6	HINv	High-side logic input for V phase
7	HINw	High-side logic input for W phase
8	VCCH	High-side low voltage power supply
9	GND	Ground
10	LINu	Low-side logic input for U phase
11	LINv	Low-side logic input for V phase
12	LINw	Low-side logic input for W phase
13	VCCL	Low-side low voltage power supply
14	SD	Shutdown logic input (active low) / open-drain (comparator output)
15	CIN	Comparator input
16	GND	Ground
17	TSO	Temperature sensor output
18	NW	Negative DC input for W phase
19	NV	Negative DC input for V phase
20	NU	Negative DC input for U phase
21	W	Phase output
22	V	Phase output
23	U	Phase output
24	P	Positive DC input
25	T2	NTC thermistor terminal 2 (only if NTC is present)
	NC	NC only
26	T1	NTC thermistor terminal 1 (only if NTC is present)
	NC	NC only

3.3.1 High-side bias voltage pins / high-side bias voltage reference

Pins: VBOOTu, VBOOTv, VBOOTw

- The bootstrap section is designed to facilitate a simple and efficient floating power supply, to provide the gate voltage signal to the high-side MOSFETs.
- The SLLIMM family integrates the bootstrap diodes to save on cost, board space and number of components.
- The advantage of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side MOSFETs.
- Each bootstrap capacitor is charged from the V_{CC} supply.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins.
- The size of the bootstrap capacitor is strictly related to the application conditions (see the Section 2.2.11: Bootstrap circuit for more information).

3.3.2 Gate driver bias voltage

Pins: VCCH, VCCL

- Control supply pin for the built-in ICs.
- Separate supply.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to this pin.

3.3.3 Gate driver supply ground

Pin: GND

- Ground reference pin for the built-in ICs.
- Two pins are internally connected.
- To avoid being affected by noise, the main power circuit current should not be allowed to flow through this pin (see the Section 5.2: Layout suggestions).

3.3.4 Signal input

Pins: HINU, HINV, HINW; LINU, LINV, LINW

- These pins control the operation of the built-in MOSFETs.
- The signal logic of the HINU, HINV, HINW, LINU, LINV, and LINW pins is active high. The MOSFET associated with each of these pins is turned on when a sufficient logic (higher than a specific threshold) voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the SLLIMM against noise.

3.3.5 Internal comparator non-inverting

Pin: CIN

- The current sensing shunt resistor connected on each phase leg may be used by the internal comparator (pin CIN) to detect short-circuit current.
- The shunt resistor should be selected to meet the detection level requirements for the specific application.
- An RC filter (typically ~1 µs) should be connected to the CIN pin to eliminate noise.
- The connection length between the shunt resistor and CIN pin should be minimized.
- If a voltage signal higher than the specified V_{REF} (see datasheet) is applied to this pin, the SLLIMM automatically shuts down and the $\overline{SD}$/OD pin is pulled down (to inform the microcontroller).

3.3.6 Shutdown/open-drain

Pin: $\overline{SD}$/OD

- The $\overline{SD}$/OD pin acts as an enable/disable pin.
- The signal logic of the $\overline{SD}$/OD pin is active low. The SLLIMM shuts down if a voltage lower than a specific threshold is applied to this pin, leading each half bridge in tri-state.
- The $\overline{SD}$/OD status is also connected to the internal comparator status (see the Section 2.2.5: Short-circuit protection and smart shutdown function). When the comparator triggers, the $\overline{SD}$/OD pin is pulled down and acts as a FAULT pin.
- When pulled down by the comparator, the $\overline{SD}$/OD pin is open drain configured. The $\overline{SD}$/OD voltage should be pulled up to the 3.3 V or 5 V logic power supply through a pull-up resistor.

3.3.7 Thermistor

Pins: T1, T2

- A copackaged NTC (optional) is available for temperature monitoring purposes.
- A simple voltage divider can be made with an external resistor to create a temperature-dependent voltage signal.
- The NTC is not able to sense rapid variations in MOSFET junction temperature (due to the slow thermal dynamics).

3.3.8 Thermal sensor

Pin: TSO

- A voltage proportional to the temperature inside the package is available on the TSO pin. It does not need any pull-down resistor. To improve noise immunity, a capacitor filter between 1 and 10 nF should be placed on this pin. When this function is not used, the TSO pin can be left floating.

3.3.9 Positive DC-link

Pin: P

- This is the DC-link positive power supply pin of the inverter and is internally connected to the drains of the high-side MOSFETs.
- To suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a snubber capacitor close to this pin (typically, high voltage, metal film capacitors of about 0.1 µF or 0.22 µF).

3.3.10 Negative DC-link

Pins: NU, NV, NW

- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side MOSFET sources of each phase.
- The power ground of the application should be separated from the logic ground of the system and reconnected at one specific point (star connection).

3.3.11 Inverter power output

Pins: U, V, W

- Inverter output pins for connection to the inverter load (for example, motors).

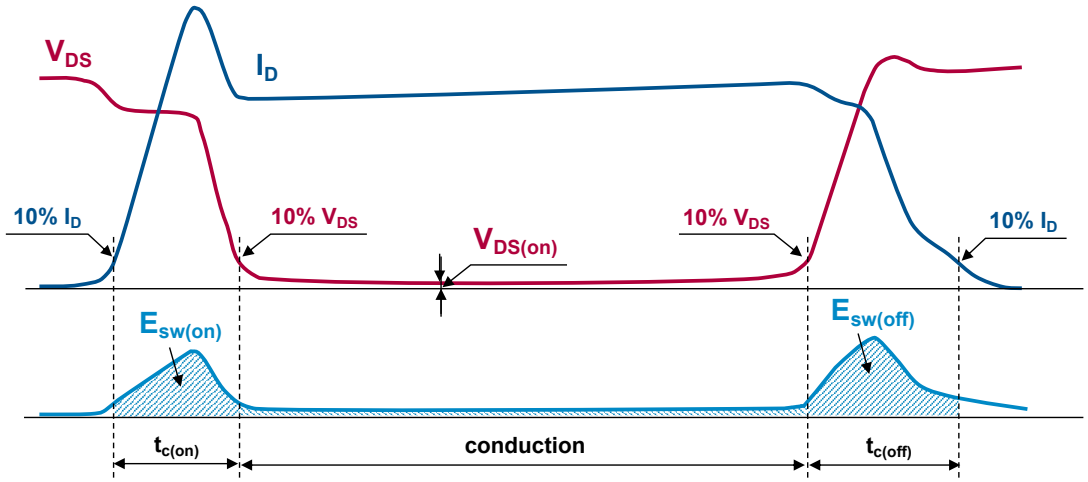
4 Power loss and dissipation

The total power loss in an inverter is comprised of conduction loss, switching loss and off-state loss, and it is essentially generated by the power devices of the inverter stage, such as the MOSFETs. The conduction loss (P_{cond}) is the on-state loss during the conduction phase. The switching loss (P_{sw}) is the dynamic loss encountered during the turn-on and the turn-off. The off-state loss, due to the blocking voltage and leakage current, can be neglected. Finally, the total power loss is given by:

$$P_{tot} \approx P_{cond} + P_{sw} \quad (21)$$

The following figure shows a typical waveform of an inductive hard switching application such as a motor drive, where the major sources of power loss are specified.

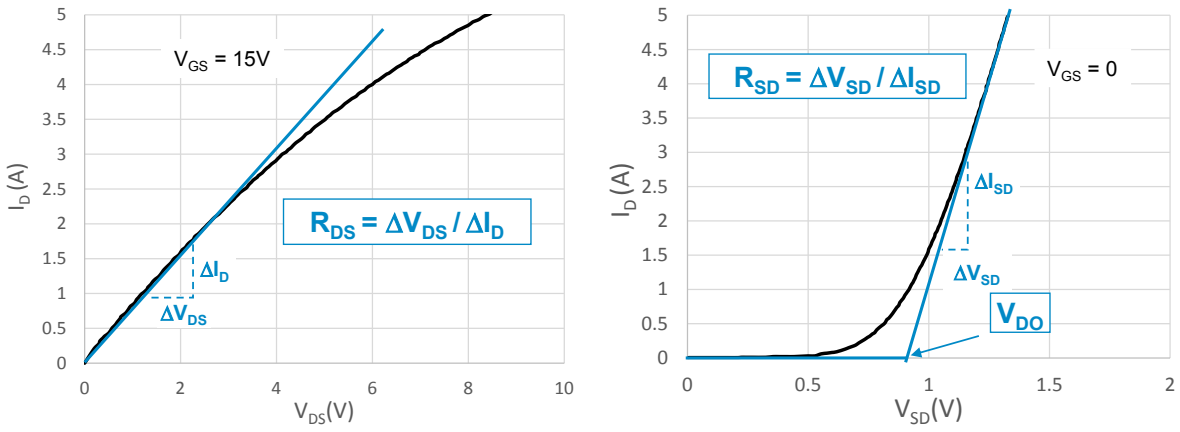
Figure 45. Typical MOSFET power loss



4.1 Conduction power loss

The conduction loss is caused by the MOSFET's and the body diode's voltage drop at rated current. It can be calculated using a linear approximation of the output characteristics for both the MOSFET and the body diode, having a drain-source on-state resistance (R_{DS}) for the first and a series connection of DC voltage source, representing the threshold voltage (V_{DO}) plus a source-drain resistance (R_{SD}) for the latter, as shown in the following figure as a reference.

Figure 46. Examples of MOSFET and body diode approximation of the output



Both forward characteristics are temperature-dependent, and thus they must be considered under a specified temperature. The linear approximations can be translated for the MOSFET in the following equation:

$$v_{ds}(i_d) = R_{DS} \cdot i_d \quad (22)$$

While for the drain-source body diode:

$$v_{sd}(i_d) = V_{DO} + R_{SD} \cdot i_d \tag{23}$$

The conduction loss of the MOSFET and the body diode can be derived as the time integral of the product of conduction current and voltage across the devices, as follows:

$$P_{cond\_MOSFET} = \frac{1}{T}\int_0^T v_{ds} \cdot i_d(t)dt = \frac{1}{T}\int_0^T R_{DS} \cdot {i_d}^2(t)dt \tag{24}$$

$$P_{cond\_Diode} = \frac{1}{T}\int_0^T v_{sd} \cdot i_d(t)dt = \frac{1}{T}\int_0^T \left(V_{DO} \cdot i_d(t) + R_{SD} \cdot {i_d}^2(t)\right)dt \ (@V_{GS} = 0) \tag{25}$$

Where T is the fundamental period. The different utilization modes of the SLLIMM-nano, modulation technique, and working conditions make the power loss very difficult to estimate; it is therefore necessary to establish some starting points.

Assuming that:

- The application is a variable voltage variable frequency (VVVF) inverter based on the sinusoidal PWM technique.
- The switching frequency is high and therefore the output currents are sinusoidal.
- The load is ideal inductive.

Under these conditions, the output inverter current is given by:

$$i = \hat{I} \cos(\theta - \emptyset) \tag{26}$$

Where Î is the current peak, θ stands for ωt and ϕ is the phase angle between output voltage and current.

The conduction power loss can be obtained as:

$$P_{cond\_MOSFET} = \frac{R_{DS} \cdot \hat{I}^2}{2\pi}\int_{-\frac{\pi}{2}+\emptyset}^{\frac{\pi}{2}+\emptyset} \xi cos^2(\theta - \emptyset)d\theta \tag{27}$$

$$P_{cond\_Diode} = \frac{V_{DO} \cdot \hat{I}^2}{2\pi}\int_{-\frac{\pi}{2}+\emptyset}^{\frac{\pi}{2}+\emptyset} \xi \cos^2(\theta - \emptyset)d\theta + \frac{R_{SD} \cdot \hat{I}^2}{2\pi}\int_{-\frac{\pi}{2}+\emptyset}^{\frac{\pi}{2}+\emptyset} \xi \cos^2(\theta - \emptyset)d\theta \tag{28}$$

Where ξ is the duty cycle for this PWM technique and is given by:

$$\xi = \frac{1 + m_a \cdot cos\theta}{2} \tag{29}$$

and m_a is the PWM amplitude modulation index. Finally, solving the Eq. (27) and Eq. (28), we have:

$$P_{cond\_MOSFET} = R_{DS} \cdot \hat{I}^2\left(\frac{1}{8} + \frac{ma \cdot \cos\emptyset}{3\pi}\right) \tag{30}$$

$$P_{cond\_Diode} = V_{DO} \cdot \hat{I}\left(\frac{1}{2\pi} - \frac{ma \cdot \cos\emptyset}{8}\right) + R_{SD} \cdot \hat{I}^2\left(\frac{1}{8} - \frac{ma \cdot \cos\emptyset}{3\pi}\right) \ (@V_{GS} = 0) \tag{31}$$

and therefore, the conduction power loss of one device (MOSFET and body diode) is:

$$P_{cond} = P_{cond\_MOSFET} + P_{cond\_Diode} \tag{32}$$

Of course, the total conduction loss per inverter is six times this value.

4.2 Switching power loss

The switching loss is the power consumption during the turn-on and turn-off transients. As shown in the Figure 45. Typical MOSFET power loss, it is given by the pulse of the power dissipated during the turn-on (t_{on}) and turn-off (t_{off}). Experimentally, it can be calculated by the time integral of the product of the drain current and drain source voltage for the switching period. In any case, the dynamic performances are strictly related to many parameters such as voltage, current and temperature, so it is necessary to use the same conduction power loss assumptions (see the Section 4.1: Conduction power loss) to simplify the calculations.

Under these conditions, the switching energy loss is given by:

$$E_{on}(\theta) = \widehat{E}_{on}\cos(\theta - \emptyset) \tag{33}$$

$$E_{off}(\theta) = \widehat{E}_{off}\cos(\theta - \emptyset) \tag{34}$$

Where $\hat{E}_{on}$ and $\hat{E}_{off}$ are the maximum values taken at T_{jmax} and $\hat{I}_c$, θ stands for ωt and ϕ is the phase angle between output voltage and current.

Finally, the switching power loss per device depends on the switching frequency (f_{sw}) and is calculated as follows:

$$P_{sw} = \frac{1}{2\pi}\int_{-\frac{\pi}{2}+\emptyset}^{\frac{\pi}{2}+\emptyset}(E_{MOSFET} + E_{Diode})\cdot f_{sw}d\theta = \frac{(E_{MOSFET} + E_{Diode})\cdot f_{sw}}{\pi} \tag{35}$$

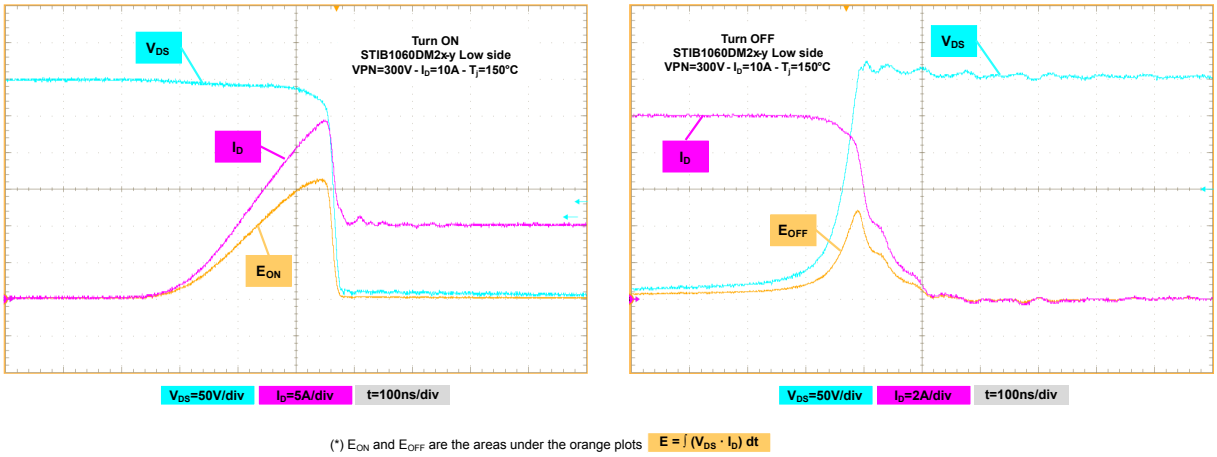
Where E_{MOSFET} and E_{Diode} is the total switching energy for the MOSFET and the body diode, respectively. Also in this case, the total switching loss per inverter is six times this value.

The Figure 47. STIB1060DM2x-y typical switching waveforms shows the real turn-on and turn-off waveforms of STIB1060DM2x-y under the following conditions:

- V_{PN} = 300 V, I_D = 10 A, T_j = 150 °C with inductive load on full-bridge topology, taken on the low-side MOSFET.

The yellow plots represent instantaneous power as a result of I_D (in purple) and V_{DS} (in light blue) waveform multiplication, during the switching transitions. The areas under these plots are the switching energies computed by graphic integration, thanks to the digital oscilloscope.

Figure 47. STIB1060DM2x-y typical switching waveforms



(*) E_{ON} and E_{OFF} are the areas under the orange plots $E = \int (V_{DS} \cdot I_D)\, dt$

4.3 Thermal impedance overview

During operation, power losses generate heat which elevates the temperature in the internal SLLIMM semiconductor junctions, limiting its performance and lifetime. To ensure safe and reliable operation, the junction temperature of power devices must be kept below the limits defined in the datasheet, therefore, the generated heat must be conducted away from the power chips and into the environment using an adequate cooling system.

The most common schemes are based on one heatsink designed for free conventional air flow or, in some cases, for forced air circulation. Free conventional air flow systems require larger heatsinks (about 50% bigger) than a forced air-based heatsink, for a given thermal resistance. Therefore, the choice of the cooling system becomes the starting point for the application designer and the thermal aspect of the system is one of the key factors in designing high efficiency and high reliability equipment. In this respect, the package and its thermal resistance play a fundamental role.

Thermal resistance quantifies the ability of a given thermal path to transfer heat in the steady-state and is generally expressed as the ratio between the temperature increase above the reference and the relevant power flow:

$$R_{th} = \frac{\Delta T}{\Delta P} \tag{36}$$

The thermal resistance specified in the datasheet is the junction-case $R_{th(j-c)}$, defined as the temperature difference between the junction and case reference divided by the power dissipation per device:

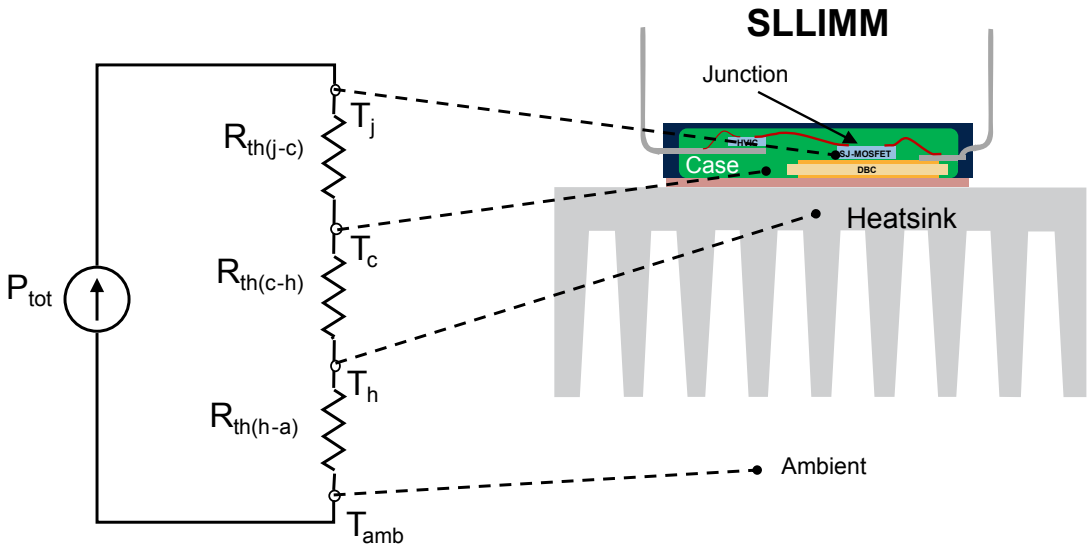
$$R_{th(j-c)} = \frac{T_j - T_c}{P_D} \tag{37}$$

The SLLIMM 2nd series SJ MOSFET with DBC package, benefits from a state of the art DBC substrate offering a very low $R_{th(j-c)}$ value. The backside of the DBC substrate is used as the cooling interface to the heatsink.

Thermal grease or some other thermal interface material between the backside and the heatsink is used to reduce the thermal resistance of the interface ($R_{th(c-h)}$) and, of course, depends on the material and its thickness.

Basically, the sum of the three thermal resistance components above gives the thermal resistance between junction and ambient $R_{th(j-a)}$, as shown in the figure below.

Figure 48. Equivalent thermal circuit with heatsink single MOSFET

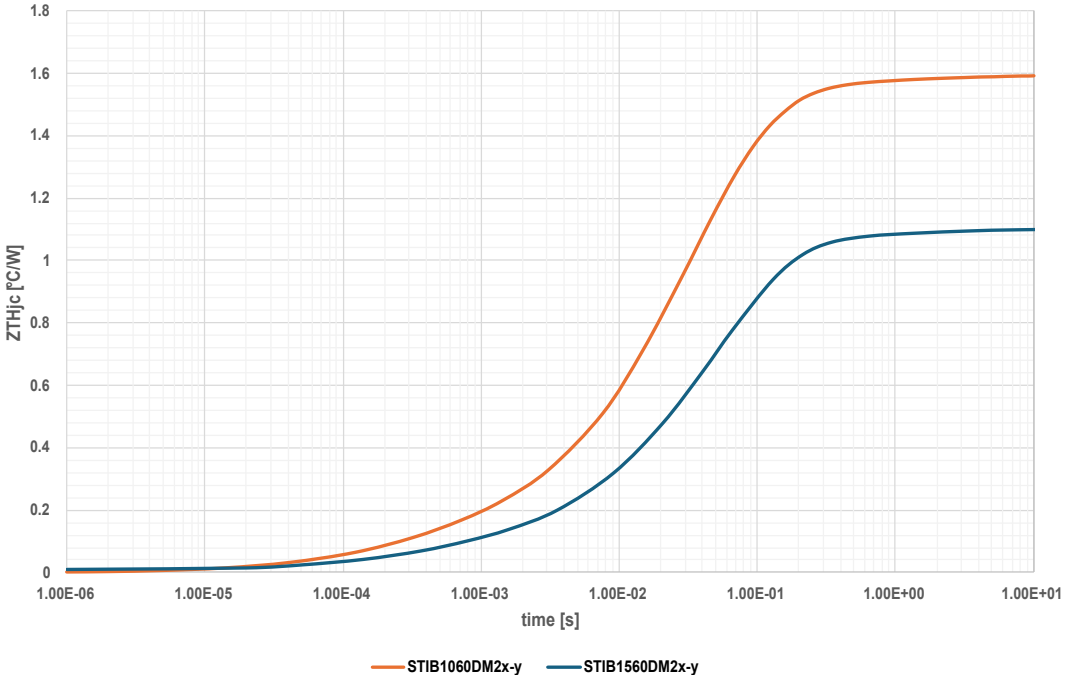


As the power loss P_{tot} is cyclic, the transient thermal impedance must also be considered. It is defined as the ratio of the time dependent temperature increase ΔT(t) above the reference and the relevant heat flow:

$$Z_{th}\left(t\right) = \frac{\Delta T(t)}{\Delta P} \tag{38}$$

Contrary to what we have already seen regarding thermal resistance, thermal impedance is typically represented by an RC equivalent circuit. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature and therefore the advantage of this behavior is the short-term overload capability of the SLLIMM.

Figure 49. **Thermal impedance curves**



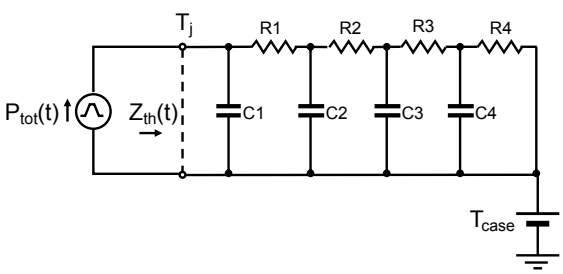
More generally, in the case of the device, power is time dependent too. The device temperature can be calculated via the convolution integral method applied to the following equation thus:

$$\Delta T(t) = \int_0^t Z_{th}(t-\tau) \cdot P(\tau) d\tau \quad (39)$$

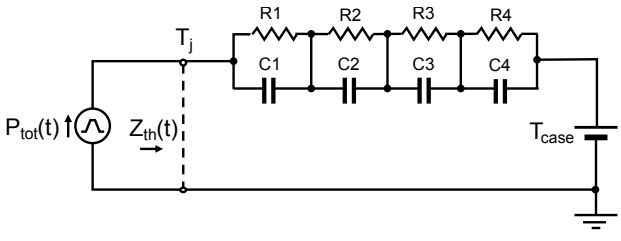
An alternative and very useful method for simulator tools, is the transient thermal impedance model, which provides a simple method for estimating the junction temperature rise under a transient condition.

By using the thermo-electrical analogy, the transient thermal impedance Zth(t) can be transformed into an electrical equivalent RC network. The number of RC sections increases the model detail, therefore fourth order models based on the Cauer and Foster networks has been adopted to improve the accuracy of the model, as shown in the following figure.

Figure 50. **Thermal impedance RC Cauer and Foster thermal networks**



RC Cauer thermal network



RC Foster thermal network

Temperatures inside the electrical RC network represent voltages, power flows represent currents, electrical resistances and capacitances represent thermal resistances and capacitances respectively. The case temperature is represented with a DC voltage source and can be interpreted as the initial junction temperature.

Transient thermal impedance models are derived by curve fitting an equation to the measured data. Values for the individual resistors and capacitors are the variables from this equation and are defined for each device in the table below.

Table 12. RC Cauer and Foster thermal network elements by device

Element	STIB1060DM2x-y		STIB1560DM2x-y	
	Cauer	Foster	Cauer	Foster
R1 (°C/W)	1.76E-01	1.38E-01	8.99E-02	1.12E-01
R2 (°C/W)	6.77E-01	9.44E-01	3.74E-01	7.39E-02
R3 (°C/W)	6.33E-01	1.61E-01	5.57E-01	1.94E-01
R4 (°C/W)	9.90E-02	3.43E-01	7.55E-02	7.17E-01
C1 (W·s/°C)	1.71E-03	1.94E-03	2.29E-03	3.23E+00
C2 (W·s/°C)	1.37E-02	4.58E-02	2.30E-02	2.53E-03
C3 (W·s/°C)	5.06E-02	1.44E+00	7.66E-02	3.50E-02
C4 (W·s/°C)	2.26E+00	2.19E-02	4.67E+00	8.07E-02

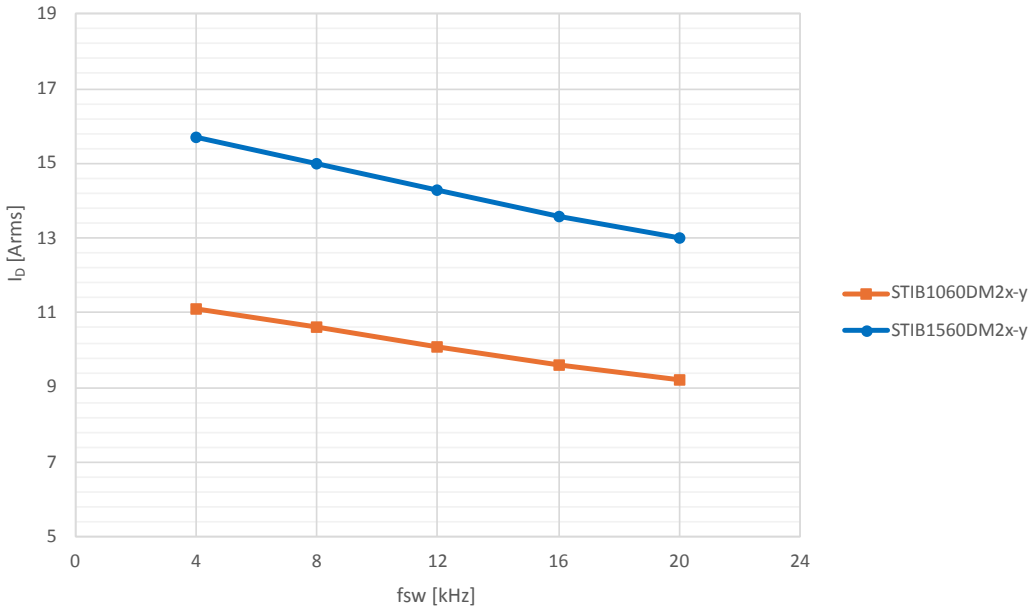
4.4 Power loss calculation example

From the power loss calculation and thermal aspects detailed in the previous sections, we can simulate the maximum $I_{D(RMS)}$ current versus switching frequency curves for an inverter using a 3-phase continuous PWM modulation to synthesize sinusoidal output currents.

The curves in Figure 51. Maximum $I_{D(RMS)}$ current vs. f_{sw} simulated curves represent the maximum current managed by the SLLIMM under safe conditions, when the junction temperature rises to 150 °C and the case temperature is 100 °C, which is a typical operating condition to guarantee the reliability of the system.

These curves, functions of the motor drive typology and control scheme, are simulated under the conditions reported in the figure below, with typical power loss.

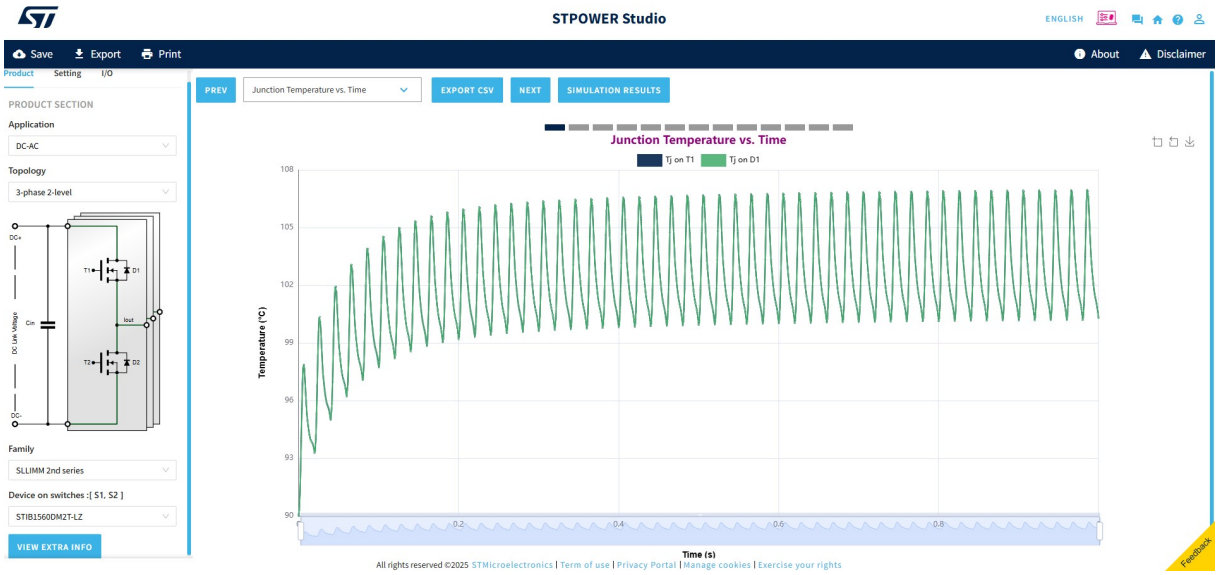
Figure 51. Maximum $I_{D(RMS)}$ current vs. f_{sw} simulated curves



4.5 STPOWER Studio simulation software

STPOWER Studio is a dynamic electrothermal simulation tool dedicated to STPOWER devices. This tool is part of eDesignSuite, the STMicroelectronics official platform for the simulators, and it provides a comprehensive power and thermal analysis which allows the user to predict the device performance, shorten the solution design and save time and resources. Furthermore, the tool helps to select the proper device that fits the application mission profile. The figure below shows the GUI.

Figure 52. STPOWER Studio graphical user interface



Note: Use this link www.st.com for eDesignSuite platform.

Based on a very precise built-in electrical and thermal model and on an iterative calculation, considering self-heating effects, STPOWER Studio provides a highly accurate estimation of the power loss as well as the junction and case temperatures.

The tool can simulate a mission profile by setting the input conditions and performing a very long simulation time.

STPOWER Studio allows the simulation of several thermal setup input conditions, such as:

- Devices without heat sink, by estimating the case and junction temperatures.
- Fixed case temperature (with heat sink), by estimating the junction temperature and the heat sink Rth.
- Fixed heat sink thermal resistance, by estimating the case and junction temperatures.
- Fixed heat sink thermal impedance, by estimating the case and junction temperatures and considering the thermal inertia of the system.

Simulation results are displayed in tables and dedicated scope views, in function of the time, the current load and the switching frequency. An output report can be generated, which summarizes all information and results to allow easy archiving.

STPOWER Studio currently enables different topologies (including 3-phase 2-level) with several PWM techniques and supports a large selection of power devices (SLLIMM and ACEPACK) and facilitates the connectivity with st.com for dedicated documentations and resources. An online forum provides additional support to STPOWER Studio users.

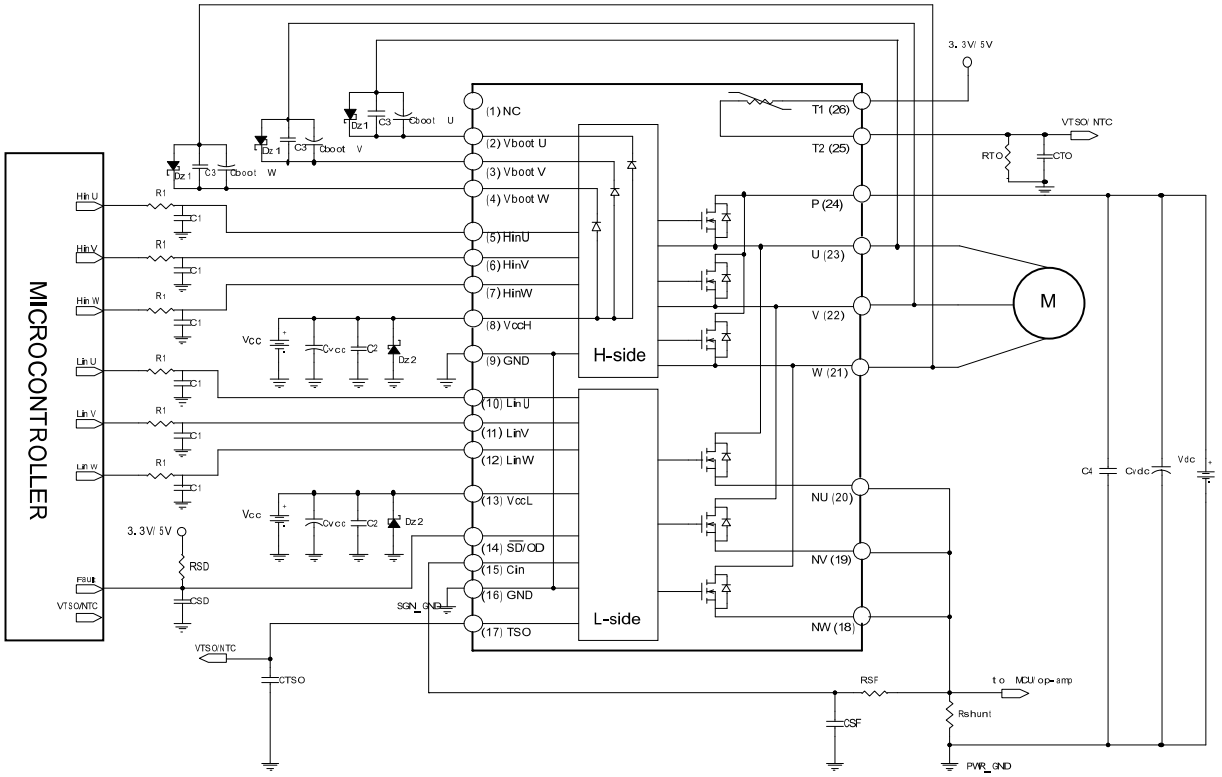
5 Design and mounting guidelines

This section provides suggestions regarding typical circuits, optimized design layouts and important mounting recommendations to aid in the appropriate handling and assembly of the SLLIMM 2nd series SJ MOSFET family.

5.1 Typical circuit and recommendations

The figure below shows a typical application circuit using SLLIMM 2nd series SJ MOSFET with signal interfaces with the MCU.

Figure 53. Typical application circuit



Below are some hardware and PCB layout recommendations:

- Input signals HIN, LIN are active-high logic. A 100 kΩ (typ.) pull-down resistor is built-in for each input pin. To prevent input signal oscillation, the wiring of each input should be as short as possible and the use of RC filters (R_1, C_1) on each input signal is suggested. The filters should be done with a time constant of about 100 ns and placed as close as possible to the IPM input pins.
- The use of a bypass capacitor C_{VCC} (aluminum or tantalum) can help reduce the transient circuit demand on the power supply. Also, to reduce high frequency switching noise distributed on the power lines, placing a decoupling capacitor C_2 (100 nF to 220 nF, with low ESR and low ESL) as close as possible to each Vcc pin and in parallel with the bypass capacitor is suggested.
- The use of RC filter (R_{SF}, C_{SF}) for preventing protection circuit malfunction is recommended. The time constant (R_{SF} x C_{SF}) should be set to 1 µs and the filter must be placed as close as possible to the CIN pin.
- The $\overline{SD}$ is an input/output pin (open-drain type if used as output). It is recommended that it be pulled up to a power supply (that is, MCU bias at 3.3/5 V) by a resistor value able to keep the I_{od} no higher than 5 mA (V_{OD} ≤ 500 mV when open-drain MOSFET is ON). The filter on $\overline{SD}$ should be sized to get a desired restarting time after a fault event and placed as close as possible to the $\overline{SD}$ pin.
- A decoupling capacitor C_{TSO} between 1 nF and 10 nF can be used to increase the noise immunity of the TSO thermal sensor; a similar decoupling capacitor C_{OT} (between 10 nF and 100 nF) can be implemented if the NTC thermistor is available and used. In both cases, their effectiveness is improved if the capacitors are placed close to the MCU.
- The decoupling capacitor C_3 (100 nF to 220 nF with low ESR and low ESL) in parallel with each C_{boot} is useful to filter high frequency disturbances. Both C_{boot} and C_3 (if present) should be placed as close as possible to the U,V,W and V_{boot} pins. Bootstrap negative electrodes should be connected to U,V,W terminals directly and separated from the main output wires.
- To prevent overvoltage on the V_{CC} pin, a zener diode (D_{z1}) can be used. Similarly on the V boot pin, a zener diode (D_{z2}) can be placed in parallel with each C_{boot}.
- The use of the decoupling capacitor C_4 (100 nF to 220 nF, with low ESR and low ESL) in parallel with the electrolytic capacitor C_{vdc} is useful to prevent surge destruction. Both capacitors C_4 and C_{vdc} should be placed as close as possible to the IPM (C_4 has priority over C_{vdc}).
- By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an opto-coupler is possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- To avoid malfunction, the wiring between N pins, the shunt resistor and PWR_GND should be as short as possible.
- The connection of SGN_GND to PWR_GND at only one point (close to the shunt resistor terminal) can help to reduce the impact of power ground fluctuation.

5.2 Layout suggestions

PCB layout optimization for high voltage, high current and high switching frequency applications is a critical factor. PCB layout is a complex matter involving several aspects such as track length and width and circuit areas, but also the proper routing of the traces and the optimized reciprocal arrangement of the various system elements in the PCB area.

A good layout can help the application function properly and achieve expected performance. On the other hand, PCBs without careful layout can generate EMI issues (both induced and perceived by the application), can provide overvoltage spikes due to parasitic inductances along the PCB traces, and can produce higher power loss and even malfunction in the control and sensing stages.

The compactness of the SLLIMM solution, which offers an optimized gate driving network and reduced parasitic elements, allows designers to concentrate on other issues such as the ground or noise filter. In any case, to avoid the aforementioned conditions, the following general PCB layout guidelines and suggestions should be followed for 3-phase applications.

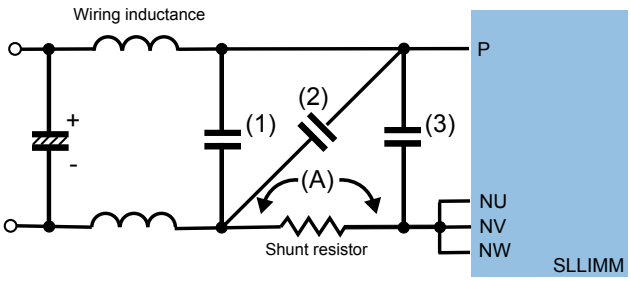
Related links

AN4694: EMC design guides for motor control applications

5.3 General suggestions

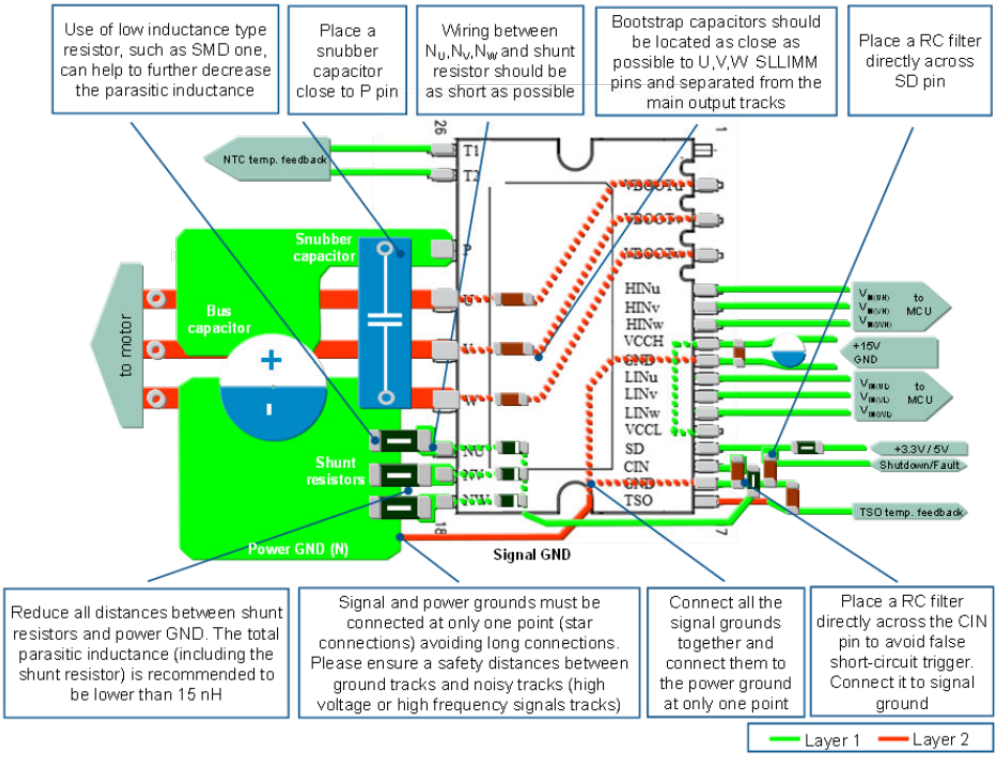
- PCB traces should be designed as short as possible and the area of the circuit (power or signal) minimized to reduce the sensitivity of such structures to surrounding noise.
- Ensure a good distance between switching lines with high-voltage transitions and the signal lines sensitive to electrical noise. Specifically, the tracks of each OUT phase carrying significant currents and voltages should be separated from logic lines and analog op amp and comparator sensing circuits.
- Place the R_{SENSE} resistors as close as possible to the low-side pins of the SLLIMM (NU, NV and NW). Parasitic inductance can be minimized by connecting the ground line (also called driver ground) of the SLLIMM directly to the cold terminal of sense resistors. Use a low inductance type resistor, such as an SMD resistor instead of long-lead type resistors, to help further decrease parasitic inductance. The total parasitic inductance (including the shunt resistor) should be lower than 15 nH.
- Avoid any ground loop. Only a single path must connect two different ground nodes.
- Place each RC filter as close as possible to the SLLIMM pins to increase their efficiency.
- Fixed voltage tracks such as GND or HV lines can be used to shield the logic and analog lines from electrical noise produced by the switching lines (for example, OUTu, OUTv and OUTw).
- Generally, it is recommended to connect each half bridge ground in a star configuration and the three R_{SENSE} very close to each other and to the power ground.
- To prevent surge destruction, the wiring between the snubber capacitor and the P - N pins should be as short as possible. The use of a high frequency, high-voltage noninductive capacitor of about 0.1 µF or 0.22 µF is recommended. To effectively suppress the surge voltage, the snubber capacitor has to be placed in position (2) in the Figure 54. Recommended snubber capacitor position. The position (1) is incorrect for effective surge voltage suppression. If the capacitor is placed on the position (3), the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor with possible undesired protection activation, even if the surge suppression effect is the greatest. Finally, position (2) is the right compromise. The parasitic inductance on the "A" tracks (including that of the shunt resistor) should be as small as possible to suppress the surge voltage.

Figure 54. Recommended snubber capacitor position



The general suggestions for all SLLIMM products are summarized in the following figure.

Figure 55. **PCB layout general suggestions**



6 Mounting and handling instructions

Some basic assembly rules must be followed to limit thermal and mechanical stress and optimize the thermal conduction and electrical isolation for SDIP2B-26L package when mounting a heatsink.

Moreover, semiconductors are normally electrostatic discharge sensitive devices (ESDS) requiring specific precautionary measures regarding handling and processing. Static discharges caused by human touch or by processing tools may cause high-current and/or high-voltage pulses which may damage or even destroy sensitive semiconductor structures. Integrated circuits (ICs) may also be charged by static during processing. If discharging takes place too quickly (“hard” discharge), it may cause peak loads and consequent damage.

Make careful choices regarding workspaces, personal equipment and processing and assembly equipment.

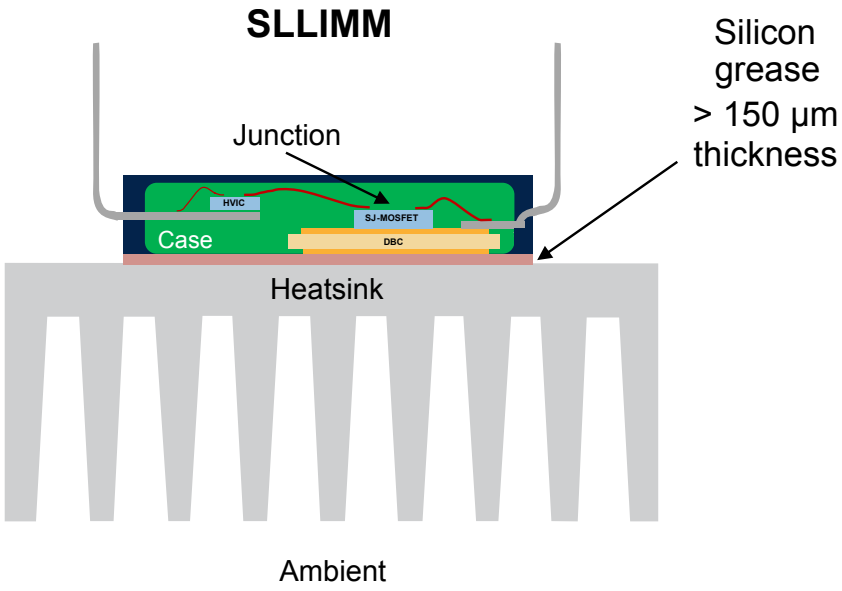
6.1 Heatsink mounting

When attaching a heatsink to a SLLIMM, do not apply excessive force to the device for assembly. Drill holes for screws in the heatsink exactly as specified. Smooth the surface by removing burrs and protrusions. Do not touch the heat-sink when the SLLIMM is operational to avoid burn injury.

To get the most effective heat dissipation, enlarge the contact area as much as possible to minimize the contact thermal resistance. Properly apply thermal-conductive grease over the contact surface between modules and heatsinks, which is also useful for preventing contact surfaces from corrosion. Apply a minimum 150 µm layer of thermal grease to the module base plate or to the heatsink, as shown in the Figure 56. Recommended silicon grease thickness and positioning. Use a torque screwdriver to fasten up to the max specified torque rating. Exceeding the maximum torque may lead to module damage or degradation. Remove any dirt from the contact surface.

Ensure the grease quality remains constant over time and is able to perform long term over a wide operating temperature range.

Figure 56. Recommended silicon grease thickness and positioning



6.1.1 Mounting torque

Mounting torque and heatsink flatness specifies the correct fastening torque. Inappropriate mounting can damage the device and over tightening the screws may cause DBC substrate or molding compound cracks. Avoid mechanical stress due to tightening on one side only. It is recommended to first lightly fasten both screws fastening them permanently to the specified torque value with a torque wrench.

Table 13. Mounting torque and heatsink flatness

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw: M3	Recommended 0.55 N•m	0.40	0.55	0.70	N•m
Device flatness	See the Figure 57. Device flatness specification		0	-	150	µm
Heatsink flatness	See the Figure 58. Heatsink flatness specification		-50	-	100	µm

The following two figures provide device and heatsink flatness details, respectively.

Figure 57. Device flatness specification

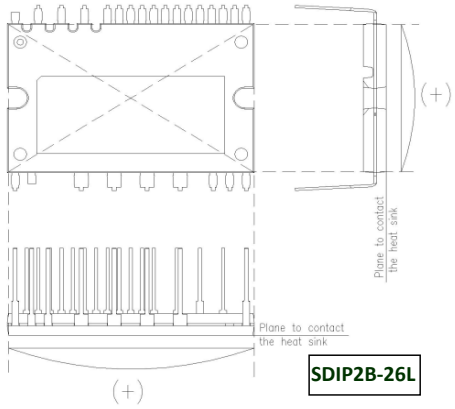
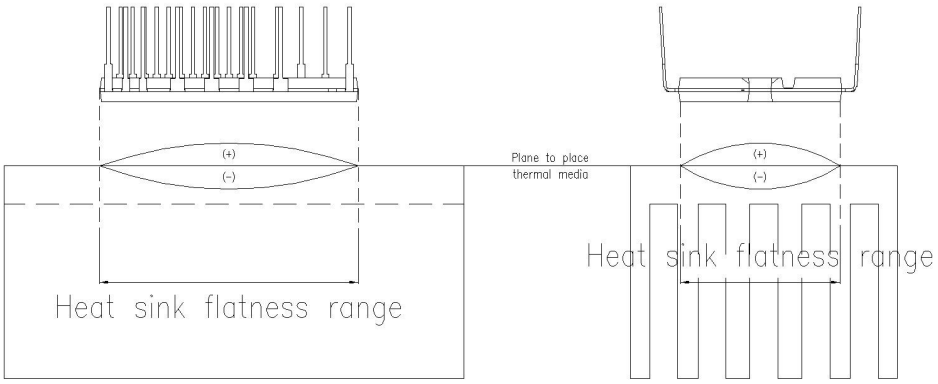


Figure 58. Heatsink flatness specification



Do not exceed the specified fastening torque. Over tightening the screws may cause ceramic or molding compound cracks and heat-fin threaded hole destruction.

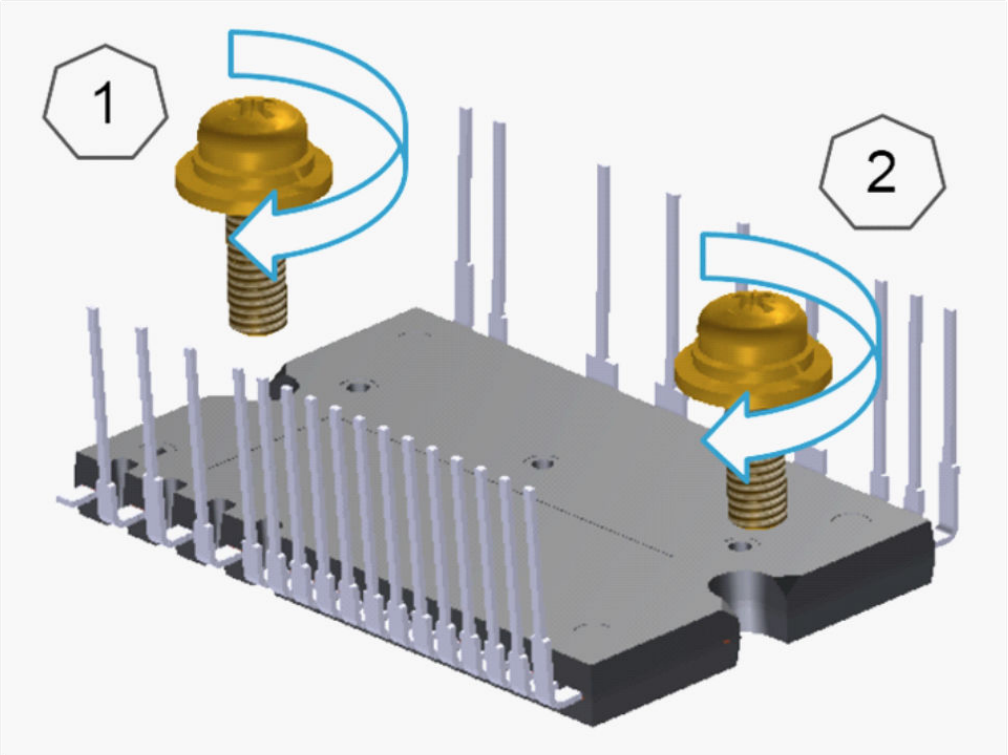
Tightening the screws beyond a certain torque can cause saturation of the contact thermal resistance.

The Figure 59. Recommended mounting screw fastening sequence shows the recommended fastening sequence for mounting screws. ST recommends temporarily tightening mounting screws with the fixing torque set at 0.1/0.2 Nm and then permanently screwing them with a torque 0.55 Nm (0.70 Nm max.) crosswise:

1. Fasten temporarily in the sequence 1 → 2
2. Screw down permanently in the sequence 1 → 2

When using electrical or pneumatic screwdrivers, ST suggests limiting the revolution to 200 rpm as the rapid impact of the screw may damage the module plastic body.

Figure 59. **Recommended mounting screw fastening sequence**



Many other precautions regarding handling and contamination, ESD, storage, transportation and soldering should be considered, and further details are available in technical note TN1220.

Related links

TN1220: Mounting instruction for SLLIMM 2nd series (SDIP2F-26L full molded and SDIP2B-26L DBC based)

7 Motor control power board based on the ST SLLIMM 2nd series SJ MOSFET

The STEVAL-IPMnmx interface demo board is a reference design compact motor drive power board based on the SLLIMM 2nd series SJ MOSFET product portfolio.

It provides an easy-to-use solution for driving high-power motors for a wide range of applications such as domestic appliances, air conditioning, compressors, power fans, high-end power tools and generally, 3-phase inverters for motor drives.

The main characteristics of this evaluation board are small size, minimal BOM list and easily testable and scalable. It consists of an interface circuit (BUS and VCC connectors), bootstrap capacitors, snubber capacitor, hardware short-circuit protection, fault event signal and temperature monitoring. To increase flexibility, it is designed to work in single or three shunt configurations and with double current sensing options such as three dedicated op-amps onboard or op-amps embedded on the MCU. The Hall/encoder part completes the circuit.

Thanks to these advanced characteristics, the system has been specially designed to achieve accurate and fast conditioning of the current feedback, matching the typical requirements for field oriented control (FOC).

The STEVAL-IPMnmx is compatible with ST's control board based on STM32, so as to provide a complete platform for motor control.

Features:

- Input voltage: 125 to 400 V DC
- Nominal power: up to 3000 W
- Input auxiliary voltage: up to 20 V DC
- Single- or three-shunt resistors for current sensing (with sensing network)
- Two options for current sensing: dedicated op-amps or through MCU
- Overcurrent hardware protection
- IPM temperature monitoring and protection
- Hall sensor or encoder input
- Scalable for the SLLIMM 2nd series SJ MOSFET product portfolio
- Motor control connector (32pins) interfacing with ST MCU boards
- Universal conception for further evaluation with breadboard and testing pins
- Very compact size

The following table shows the order code for the power board based on the equipped IPMs.

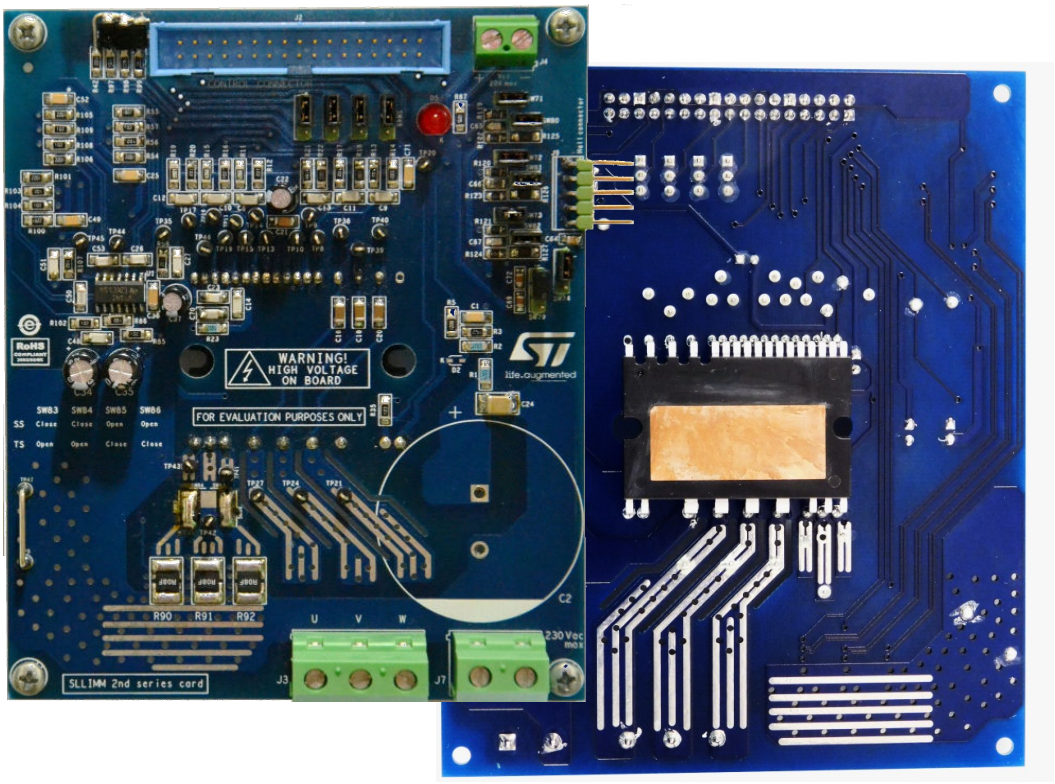
Table 14. SLLIMM 2nd series SJ MOSFET power board order code

Reference	STEVAL-IPMMnmx(1)		
SLLIMM mounted	n	m	x
STIB1060DM2x-y	1	0	B
STIB1560DM2x-y	1	5	B

1. *Board extension on going.*

The following figure shows a top and bottom view of STEVAL-IPMM15B mounting the DBC package STIB1560DM6x-y, for 2000 W power level applications.

Figure 60. **Top and bottom view of STEVAL-IPMM15B**



Related links

STEVAL-IPMM15B: 1500 W motor control power board based on STIB1560DM2T-L SLLIMM 2nd series IPM

Appendix A Other information

A.1 Reference documents

[1] Application note *EMC design guides for motor control applications* (AN4694)

[2] Application note *SLLIMM™ 2nd series small low-loss intelligent molded module* (AN4768)

[3] Application note *SLLIMM™-nano MOSFET small low-loss intelligent molded modules* (AN5244)

[4] Databrief *1200 W motor control power board based on STIB1060DM2T-L SLLIMM™ 2nd series MOSFET IPM* (DB4140)

[5] Databrief *1500 W motor control power board based on STIB1560DM2T-L SLLIMM™ 2nd series IPM* (DB4141)

[6] Datasheet *SLLIMM - 2nd series IPM, 3-phase inverter, 180 mΩ typ., 10 A, 600 V Power MOSFET* (DS13941)

[7] Datasheet *SLLIMM 2nd series IPM, 3-phase inverter, 0.15 Ω typ., 15 A, 600 V Power MOSFET* (DS14670)

[8] Technical note *Mounting instruction for SLLIMM™ 2nd series (SDIP2F-26L full molded and SDIP2B-26L DBC based)* (TN1220)

Revision history

Table 15. **Document revision history**

Date	Revision	Changes
24-Jul-2026	1	First release.

Contents

1 **Major advantages of the MOSFET technology 2**
1.1 Product synopsis 3
1.2 Product line-up and nomenclature 5
1.3 Internal circuit 6
1.4 Absolute maximum ratings 7
1.5 SCSOA 11
2 **Electrical characteristics and functions 14**
2.1 SJ MOSFETs with fast body diode 14
2.2 IC gate drivers 15
2.2.1 Logic inputs 16
2.2.2 High voltage level shift 17
2.2.3 Undervoltage lockout 17
2.2.4 Comparators for fault sensing 19
2.2.5 Short-circuit protection and smart shutdown function 19
2.2.6 Timing chart of short-circuit protection and smart shutdown function 21
2.2.7 Current sensing shunt resistor selection 22
2.2.8 RC filter network selection 23
2.2.9 Fault management 26
2.2.10 Temperature monitoring 33
2.2.11 Bootstrap circuit 38
2.2.12 Output safe clamp 42
3 **Package 43**
3.1 DBC structure 43
3.2 Package structure 44
3.3 Input and output pin descriptions 45
3.3.1 High-side bias voltage pins / high-side bias voltage reference 46
3.3.2 Gate driver bias voltage 46
3.3.3 Gate driver supply ground 46
3.3.4 Signal input 46
3.3.5 Internal comparator non-inverting 46
3.3.6 Shutdown/open-drain 47
3.3.7 Thermistor 47
3.3.8 Thermal sensor 47
3.3.9 Positive DC-link 47
3.3.10 Negative DC-link 47

3.3.11 Inverter power output . . . 47
4 Power loss and dissipation . . . 48
4.1 Conduction power loss . . . 48
4.2 Switching power loss . . . 50
4.3 Thermal impedance overview . . . 50
4.4 Power loss calculation example . . . 53
4.5 STPOWER Studio simulation software . . . 54
5 Design and mounting guidelines . . . 55
5.1 Typical circuit and recommendations . . . 55
5.2 Layout suggestions . . . 56
5.3 General suggestions . . . 57
6 Mounting and handling instructions . . . 59
6.1 Heatsink mounting . . . 59
6.1.1 Mounting torque . . . 59
7 Motor control power board based on the ST SLLIMM 2nd series SJ MOSFET . . . 62
Appendix A Other information . . . 64
A.1 Reference documents . . . 64
Revision history . . . 65

List of tables

Table 1. Product line-up . . . 5
Table 2. Synoptic table . . . 5
Table 3. Inverter part of STIB1060DM2x-y . . . 7
Table 4. Control part of STIB1060DM2x-y . . . 9
Table 5. Supply voltage and operation behavior . . . 9
Table 6. Total STIB1060DM2x-y system . . . 9
Table 7. Integrated pull-down resistor values . . . 17
Table 8. SD duration time per event . . . 26
Table 9. Fault event summary effect on MOSFET and SD . . . 26
Table 10. $R_{th(j-c)}$ comparison . . . 44
Table 11. SDIP2B-25/26L input and output pins . . . 45
Table 12. RC Cauer and Foster thermal network elements by device . . . 53
Table 13. Mounting torque and heatsink flatness . . . 60
Table 14. SLLIMM 2nd series SJ MOSFET power board order code . . . 62
Table 15. Document revision history . . . 65

List of figures

Figure 1. MOSFETs and IGBTs static characteristics comparison . . . 2
Figure 2. MOSFETs and IGBTs turn-on and turn-off energies comparison . . . 3
Figure 3. SLLIMM block diagram . . . 4
Figure 4. SLLIMM 2nd series SJ MOSFET nomenclature . . . 5
Figure 5. Internal circuit for SDIP2B-26L (without NTC) . . . 6
Figure 6. Internal circuit for SDIP2B-26L (with NTC) . . . 7
Figure 7. Stray inductance components of output stage . . . 8
Figure 8. T_C measurement point . . . 10
Figure 9. SCSOA test circuit . . . 11
Figure 10. SCSOA main data . . . 12
Figure 11. Typical STIB1060DM2x-y SCSOA curve . . . 12
Figure 12. Typical STIB1560DM2x-y SCSOA curve . . . 13
Figure 13. High-side gate driver block diagram . . . 15
Figure 14. Low-side gate driver block diagram . . . 16
Figure 15. Timing chart of undervoltage lockout function on low-side section . . . 17
Figure 16. Timing chart of undervoltage lockout function on high-side section . . . 18
Figure 17. Smart shutdown equivalent circuitry . . . 20
Figure 18. Timing chart of smart shutdown function . . . 21
Figure 19. Examples of SC protection circuits . . . 23
Figure 20. Example of a short-circuit event . . . 24
Figure 21. Smart shutdown operation . . . 25
Figure 22. OC event . . . 27
Figure 23. UVLO event . . . 27
Figure 24. SD duration for OC event . . . 28
Figure 25. SD duration for short UVLO event (≤ 70 µs) . . . 29
Figure 26. SD duration for long UVLO event (> 70 µs) . . . 30
Figure 27. Short UVLO event after OC event . . . 31
Figure 28. Long UVLO event after OC event . . . 32
Figure 29. Comparator triggering in UVLO condition . . . 32
Figure 30. Temperature detection points (top view) . . . 33
Figure 31. Thermal sensor voltage vs temperature . . . 34
Figure 32. Normal voltage controller (MCU) . . . 34
Figure 33. Low voltage controller (MCU): optional clamping . . . 35
Figure 34. NTC resistance vs temperature . . . 36
Figure 35. NTC resistance vs temperature – zoom . . . 36
Figure 36. Sample overtemperature protection circuit . . . 37
Figure 37. V_{NTC} vs temperature (pull up configuration) . . . 38
Figure 38. V_{NTC} vs temperature (pull down configuration) . . . 38
Figure 39. Bootstrap circuit . . . 39
Figure 40. Bootstrap capacitor vs switching frequency . . . 41
Figure 41. Initial bootstrap charging time . . . 42
Figure 42. DBC structure . . . 43
Figure 43. SDIP2B-26L external and internal representation . . . 44
Figure 44. SDIP2B-26L - Long leads package . . . 44
Figure 45. Typical MOSFET power loss . . . 48
Figure 46. Examples of MOSFET and body diode approximation of the output . . . 48
Figure 47. STIB1060DM2x-y typical switching waveforms . . . 50
Figure 48. Equivalent thermal circuit with heatsink single MOSFET . . . 51
Figure 49. Thermal impedance curves . . . 52
Figure 50. Thermal impedance RC Cauer and Foster thermal networks . . . 52
Figure 51. Maximum $I_{D(RMS)}$ current vs. f_{sw} simulated curves . . . 53
Figure 52. STPOWER Studio graphical user interface . . . 54

Figure 53. Typical application circuit 55
Figure 54. Recommended snubber capacitor position 57
Figure 55. PCB layout general suggestions 58
Figure 56. Recommended silicon grease thickness and positioning 59
Figure 57. Device flatness specification 60
Figure 58. Heatsink flatness specification 60
Figure 59. Recommended mounting screw fastening sequence 61
Figure 60. Top and bottom view of STEVAL-IPMM15B 63

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