AN6419

Application note

Migrating microcontroller applications from STM32F405 and STM32F407, to STM32H543/553 MCUs

Introduction

The designers of STM32 microcontroller applications must have the possibility to easily replace one microcontroller type with another one from the same product family or products from a different family. The reasons for migrating an application to a different microcontroller can be for example:

- To fulfill higher product requirements, extra demands on memory size, or an increased number of I/Os
- To meet cost reduction constraints that require to switch to smaller components and shrink the PCB area.

This application note details the steps required to migrate from an existing design based on the STM32F405 and STM32F407 MCUs, to one based on the STM32H543/553 MCUs.

Note: The STM32F405 and STM32F407 is referred to as STM32F405/407 unless otherwise stated.

This document provides the full set of features available for the STM32F405/407 devices, and the equivalent features on the STM32H543/553 product lines. This document also provides guidelines on both hardware and peripheral migration.

To better understand the information inside this application note, the user must be familiar with the STM32 microcontroller family.

This application note is a complement to the STM32F405/407 and STM32H543/553 datasheets and reference manuals. For additional information, refer to the product datasheets and reference manuals.

1 General information

STM32F405/407 and STM32H543/553 MCUs are 32-bit microcontrollers based on the Arm® Cortex® processor.

Note: Arm, Cortex, and the Arm logo are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1 Reference documents

Table 1. Reference documents

Document number	Title
[1]	*STM32F405/415, STM32F407/417, STM32F427/437 and STM32F429/439 advanced Arm®-based 32-bit MCUs* reference manual (RM0099)
[2]	*STM32H523/33xx, STM32H543/553, STM32H562/63xx, and STM32H573xx Arm®-based 32-bit MCUs* reference manual (RM0481)
[3]	*STM32F405xx STM32F407xx datasheet* (DS8626)
[4]	*STM32H543xx Datasheet (Non-crypto)* datasheet (DS15168)
[5]	*STM32H553xx Datasheet(crypto)* datasheet (DS15167)
[6]	*Introduction to system memory boot mode on STM32 MCUs* (AN2606)

2 STM32H543/553 MCUs overview

2.1 Main features

The STM32H543/553 MCUs include a larger set of peripherals and with more advanced features, compared to the STM32F405/407 MCUs.

Some of the new peripherals for STM32H543/553 are:

- Security
  - TrustZone®-aware and securable peripherals
  - Active tamper, secure firmware installation, secure firmware upgrade support, secure data storage with hardware unique key
  - Preconfigured immutable root of trust (ST-iROT)
  - Flexible life cycle scheme with secure debug authentication
  - Up to eight configurable SAU regions
  - Additional encryption accelerator engine
    - Advanced encryption hardware accelerator (AES)
    - Public key accelerator (PKA)
    - Secure AES coprocessor (SAES)
    - On-the-fly decryption engine on OCTOSPI (OTFDEC)
  - Coupling and chaining bridge (CCB)
- Performance
  - Frequency up to 250 MHz
  - Direct access to flash interface through the instruction cache (ICACHE)
  - ICACHE for internal and external memories
  - Data cache (DCACHE) for external memories
- Power supply
  - Embedded regulator (LDO)
- New peripherals
  - CORDIC coprocessor
  - New communication interface: I3C, FDCAN, LPUART, USB Type-C® connector/USB power delivery interface (UCPD)
  - Programmable logic array (PLAY)
  - OCTOSPI
  - Comparator (COMP)

Note: This document only manages the differences between STM32F405/407, and STM32H543/553 for the common features. The new features of STM32H543/553, mainly linked to the TrustZone® support, are not covered. The detailed list of available features and packages for each product is available in the respective product datasheet.

The table below summarizes the memory availability of the STM32F405/407, STM32H543/553 MCUs.

Table 2. Memory availability

Products	Flash memory		RAM size (Kbytes)				Feature level
	Size	Bank	SRAM1	SRAM2	SRAM3	BKPSRAM	
STM32H553	Up to 1 Mbytes	Dual	128	80	96	2	With hardware crypto: AES, PKA, SAES, and OTFDEC
STM32H543	Up to 1 Mbytes	Dual	128	80	96	2	NA(1)
STM32F405/407	Up to 1 Mbytes	Single	112	16	-	4	NA

1. NA stands for Not applicable

2.2 System architecture

The STM32H543/553 MCUs embed:

- High-speed memories (Up to 1 Mbytes of dual-bank flash memory and 304 Kbytes of SRAM)
- A flexible external memory controller (FMC) for devices with packages of 100 pins and more
- One Octo-SPI memory interface
- An extensive range of enhanced I/Os and peripherals connected to three APB buses.
- Three AHB buses and a 32-bit multi-AHB bus matrix.

The following table illustrates the bus matrix differences between STM32F405/407, and STM32H543/553.

Table 3. Bus matrix

Bus type	STM32F405/407	STM32H543/553
AHB bus matrix masters	**Up to 8 masters**: • CPU I-bus, D-bus, and S-bus • DMA1 memory bus • DMA2 memory bus • DMA2 peripheral bus • Ethernet DMA bus • USB OTG HS, DMA bus	**Up to 12 masters**: • Fast C-bus • Slow C-bus • CPU core S-bus (three masters connected to three internal SRAMs without latency) • CPU core S-bus connected to the external memories through the data cache • GPDMA1 and GPDMA2 (general-purpose DMAs, both featuring two master ports) • SDMMC1 • Ethernet MAC
AHB bus matrix slaves	**Up to 7 slaves**: • Internal flash memory ICode bus • Internal flash memory DCode bus • Main internal SRAM1 • Auxiliary internal SRAM2 • AHB1 peripherals (including AHB to APB bridges and APB peripherals) • AHB2 peripherals • FSMC (flexible static memory controller)	**Up to 10 slaves**: • Internal flash memory • SRAM1 • SRAM2 • SRAM3 • AHB1 peripherals (including APB1 and APB2) and backup RAM (BKPSRAM) • AHB2 peripherals • FMC (flexible memory controller) • OCTOSPI • AHB3 peripherals • AHB4 peripherals

The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously.

The figures below show the system architectures of STM32F405/407, and STM32H543/553.

Figure 1. STM32F405/407 devices system architecture

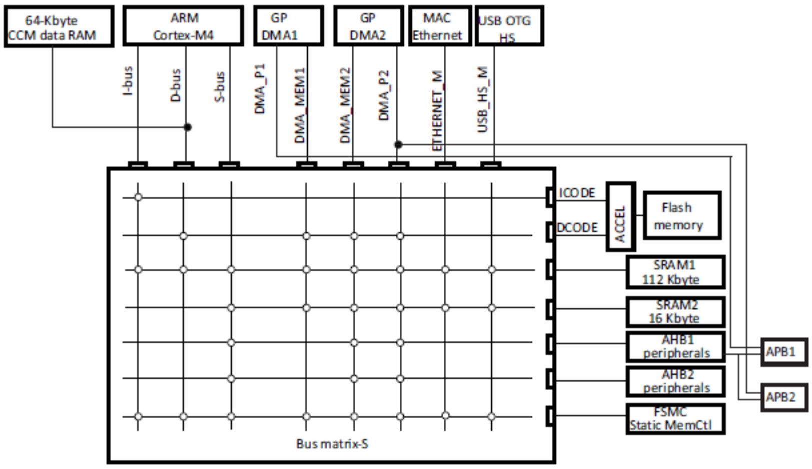

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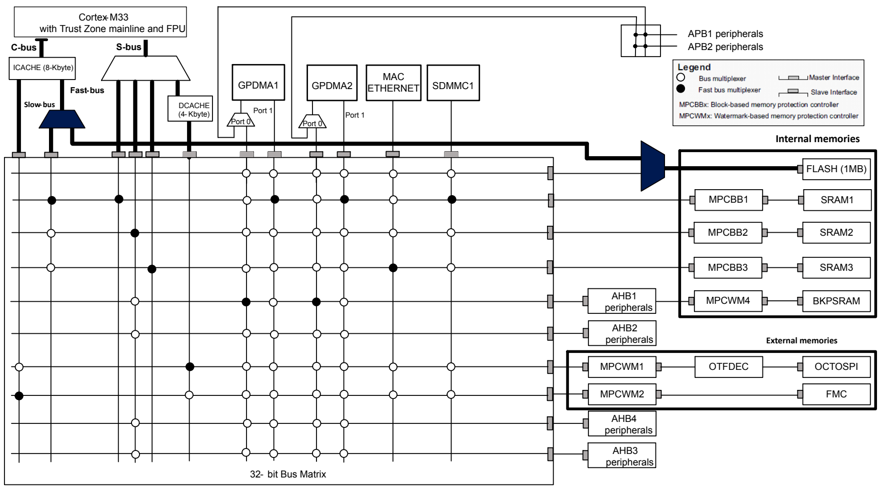
Figure 2. STM32H543/553 devices system architecture



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3 Hardware migration

This section presents the package and pinout compatibility details for the hardware migration.

3.1 Package availability

The STM32H543/553 devices offer ten packages from 48 to 144 pins. The LDO pinout option is partially compatible with STM32F405/407.

For more details on the pinout, refer to the product datasheets.

The table below lists the available packages on the STM32H543/553 compared to STM32F405/407.

Table 4. Packages available

Package (Size in mm x mm)	STM32F405/407	STM32H543/553
UFQFPN48 (7 x 7 mm)	NA	X
LQFP48 (7 x 7 mm)	NA	X
LQFP64 (10 × 10 mm)	X	X
LQFP100 (14 × 14 mm)	X	X
LQFP100-EP (14 x 14 mm)	NA	X
LQFP144 (20 × 20 mm)	X	X
LQFP144-EP (20 x 20 mm)	NA	X
LQFP176 (24 × 24 mm)	X	NA
UFBGA100 (7 x 7 mm)	NA	X
UFBGA144 (10 × 10 mm)	NA	X
UFBGA176 (10 × 10 mm)	X	NA
WLCSP	WLCSP90	WLCSP63

Note: X = available, NA = not available

3.2 Pinout compatibility

The STM32F405/407 devices are not identical with the STM32H543/553 devices in term of MCU port assignment to package terminals, that is, in term of pinout or ballout. This holds for all common package types of the package listed in Table 4. Packages available .

In the STM32H543/553, for the LQFP64 packages, the VCAP_1 and VCAP_2 pins are replaced by VSS pins and, the VREF+ and VREF- functions have been added to the VDDA and VSSA pins, respectively. For the LQFP100 and LQFP144 packages, the VCAP_1 pin is replaced by a VSS pin, and the VCAP_2 pin is replaced by a VDDUSB pin.

The following sections show the packages pinout figures and the packages pinout differences tables.

3.2.1 LQFP64 package

Figure 3. STM32H543/553 LQFP64 pinout

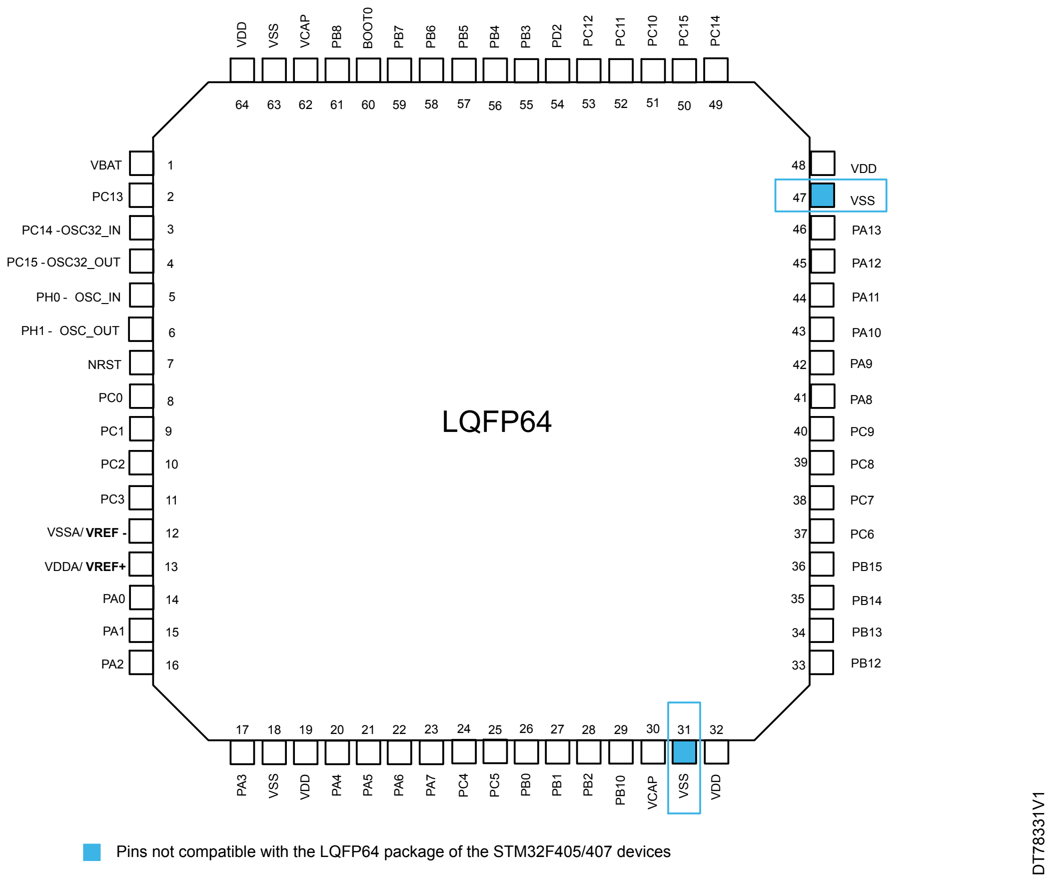


Table 5. LQFP64 pinout differences

LQFP64 pin number	STM32F405/407 pinout	STM32H543/553 pinout
31	VCAP_1	VSS
20	VCAP_2	VSS

3.2.2 LQFP100 package

Figure 4. STM32H543/553 LQFP100 pinout

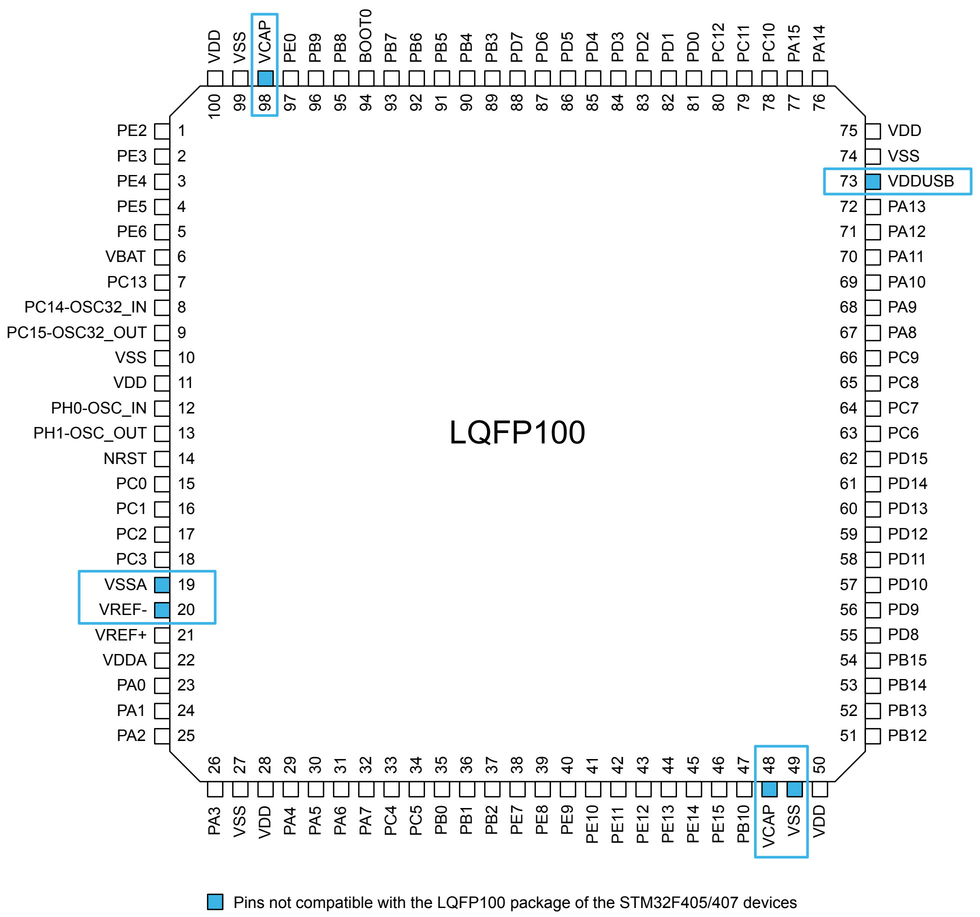


Table 6. LQFP100 pinout differences

LQFP100 pin number	STM32F405/407 pinout	STM32H543/553 pinout
19	VDD	VSSA
20	VSSA	VREF-
48	PB11	VCAP
49	VCAP_1	VSS
73	VCAP_2	VDDUSB
98	PE1	VCAP

3.2.3 LQFP144 package

Figure 5. STM32H543/553 LQFP144 pinout

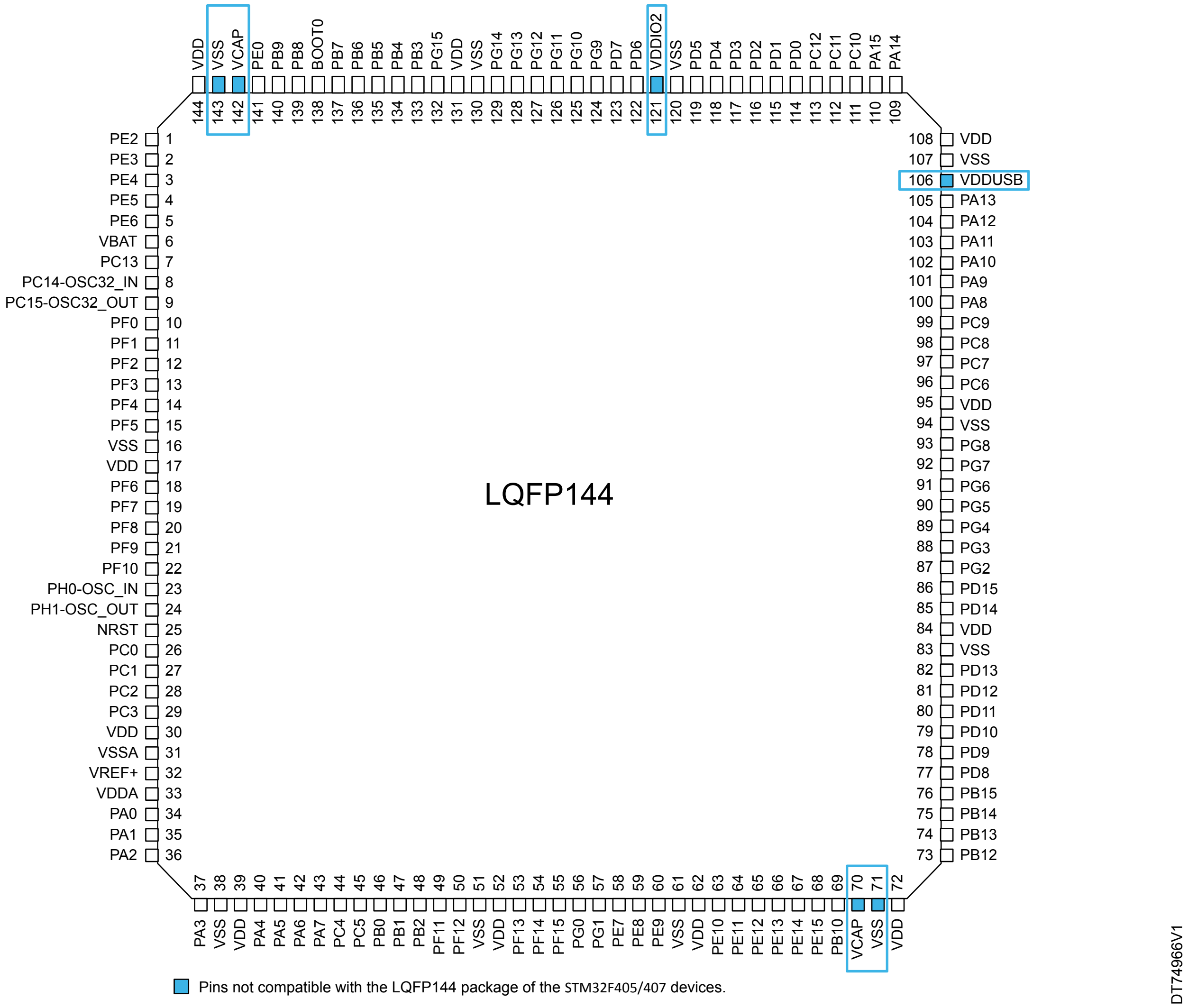


Table 7. LQFP144 pinout differences

LQFP144 pin number	STM32F405/407 pinout	STM32H543/553 pinout
70	PB11	VCAP
71	VCAP_1	VSS
106	VCAP_2	VDDUSB
121	VDD	VDDIO2
142	PE1	VCAP
143	PDR_ON	VSS

4 Boot mode compatibility

4.1 Boot mode selection

In STM32F405/407, three different boot modes can be selected through the BOOT[1:0] pins as shown in the table below.

Table 8. **Boot modes for STM32F405/407**

Boot mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
X	0	Main flash memory	Main flash memory is selected as the boot space
0	1	System memory	System memory is selected as the boot space
1	1	Embedded SRAM	Embedded SRAM is selected as the boot space

STM32H543/553 embed an SBS peripheral that controls boot and security features. For these devices, the main boot control actions are listed below:

- Run the product with or without TrustZone® enabled.
- Select between ST-iROT or OEM-iROT (refer to [2] for more details).
- Boot when launching a debug authentication sequence.
- Select boot between the bootloader or the user flash memory boot.
- Initialize the HDPL boot value.

For STM32H543/553 devices, the boot configurations are selected considering the product settings:

- **BOOT0**: to select booting on user flash memory or RSS (root secure services).
- **BOOT_UBE**: option byte to select the iROT between ST-iROT and OEM-iROT.
- **TZEN**: option byte to activate/deactivate the TrustZone®.
- **sbs_boot_addresses**: list of addresses defined by the flash memory:
  - NSBOOTADD: nonsecure boot address
  - SECBOOTADD: secure boot address
- **PRODUCT_STATE**: option byte to activate the different security mechanisms depending on the product use.
- **sbs_dbg_req:** used to launch the debug authentication protocol when booting.

The tables below present the STM32H553 boot modes, when TrustZone® is disabled or enabled.

Table 9. **STM32H553 Boot modes when TrustZone® is disabled (TZEN=0xC3)**

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	NA	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000
	1	NA	NA	Bootloader	Bootloader
Provisioning	x	NA	NA	RSS	RSS
Provisioned, Closed, Locked	x	NA	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000

Table 10. **STM32H553 Boot modes when TrustZone® is enabled (TZEN=0xB4)**

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	x	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000
	1	0xB4	NA	Bootloader	Bootloader
	1	0xC3	NA	ST-iROT	ST-iROT
Provisioning	x	NA	NA	RSS	RSS
Provisioned, TZ_Closed, Closed, Locked	x	0xC3	ST-iROT	ST-iROT	ST-iROT
	x	0xB4	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000

The tables below illustrate the STM32H543 boot modes, when TrustZone® is disabled or enabled.

Table 11. **STM32H543 Boot mode when TrustZone® is disabled (TZEN=0xC3)**

PRODUCT_STATE	BOOT0 pin	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000
	1	NA	Bootloader	Bootloader
Provisioning	x	NA	RSS	RSS
Provisioned, Closed, Locked	x	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000

Table 12. **STM32H543 Boot mode when TrustZone® is enabled (TZEN=0xB4)**

PRODUCT_STATE	BOOT0 pin	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000
	1	NA	Bootloader	Bootloader
Provisioning	x	NA	RSS	RSS
Provisioned, TZ_Closed, Closed, Locked	x	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000

4.2 System bootloader

The system bootloader is in the system memory, programmed by STMicroelectronics during the production.

It is used to reprogram the flash memory using one of the following serial interfaces.

The following table shows the supported communication peripherals by the system bootloader. For more details, refer to the application note *STM32 microcontroller system memory boot mode* (AN2606).

Table 13. Bootloader communication peripherals

System bootloader peripherals	STM32F405/407	STM32H543/553 I/O pin
DFU(1)	PA11/PA12	
USART1	PA10/PA9	
USART2	NA	PA3/PA2
USART3	PB10 / PB11 and PC10 / PC11	PD9/PD8(2)
CAN	CAN2 (PB5/PB13)	FDCAN2(PB5/PB13)
I2C1	NA	PB8/PB9(2)
I2C3	NA	PA8/PC9 (3)
I3C1	NA	PB6/PB7
SPI1	NA	PA7/PA6/PA5/PA4
SPI2	NA	PC1(4)/PB14/PB10/PB12
SPI3	NA	PC12/PC11/PC10/PA15(5)

1. *On STM32H5, USB DFU bootloader does not need an external quartz. It uses internal HSI48.*
2. *Not available for LQFP48, UFQFN48, LQFP64, and WLCSP63.*
3. *PC9 is replaced by PB4 on LQFP48 and UFQFN48*
4. *PC1 is replaced by PB15 on LQFP48 and UFQFN48.*
5. *Not available for LQFP48 and UFQFN48.*

5 Peripheral migration

5.1 Cross-compatibility between STM32 products

STM32 microcontrollers embed a set of peripherals that can be classified in the following groups:

- Group1: peripherals by definition common to all products
  Those peripherals are identical, so they have the same structure, registers, and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- Group2: peripherals shared by all products but with only minor differences (in general to support new features)
  The migration from one product to another is very easy and does not need any significant new development effort.
- Group3: peripherals that have considerable changes from one product to another (new architecture or new features for example)
  For this group of peripherals, the migration requires a new development at application level.

For STM32H543/553, all of the following can be configured as trusted or untrusted: each GPIO or peripheral, DMA channel, clock configuration register, ICACHE, DCACHE, and every small part of flash memory or SRAM. The following table summarizes the available peripherals in STM32F405/407 compared to STM32H543/553.

Table 14. STM32 peripheral compatibility between products

Peripherals		STM32F405/407	STM32H543/553
Core		Cortex®-M4	Cortex®-M33
Maximum CPU frequency		Up to 168 MHz	Up to 250 MHz
Flash memory		Up to 1 Mbyte	Up to 1 Mbyte
SRAMs	System	192 Kbytes (112+16+64[(1)])	304 Kbytes (128+80+96)
	Backup	4 Kbytes	2 Kbytes
Timers	General purpose	2 (32 bits) and 8 (16 bits)	2 (32 bits) and 4 (16 bits)
	Advanced control	2(16 bits)	2 (16 bits)
	Basic	2 (16 bits)	2 (16 bits)
	Low power	No	2 (16 bits)
	SysTick timer	1	2
	Watchdog timers (independent, window)	2	2
Communication interfaces	**SPI/I2S**	Up to 3 SPIs, 2 with muxed full-duplex I2S	Up to 4 SPIs, including three multiplexed in full-duplex I2S audio class accuracy via internal audio PLL or external clock, and up to four additional SPIs from four USARTs when configured in Synchronous mode (one additional SPI with OctoSPI)
	I2C	3 (Sm and Fm interfaces (SMBus/PMBus)	Up to 3 I2Cs Fm+ (SMBus/ PMBus®)
	I3C	No	2
	USART/UART	4 / 2	4 / 4
	LPUART	No	1
	USB	USB OTG FS and USB OTG HS	USB FS
	UCPD	No	Yes

Peripherals		STM32F405/407	STM32H543/553
Communication interfaces	CAN	2	2 FDCAN
	SDIO/SDMMC	1	1
	DCMI	Yes	No
	Ethernet	Yes	Yes (1x Ethernet 10/100)
Flexible memory controller (FMC)		FSMC	Yes (8,16-bit data bus width)
OCTOSPI		No	1
HDMI-CEC		No	Yes
CRC		Yes	Yes
DMA		2	2 GPDMA (featuring two master ports) TrustZone® support/linked-list
Programmable Logic Array (PLAY)		No	Yes
CORDIC coprocessor (CORDIC)		No	Yes
Real-time clock (RTC)		Yes	Yes
Random number generator (RNG)		Yes	Yes
SAES, AES		No	Yes
Public key accelerator (PKA)		No	Yes
Coupling and chaining bridge (CCB)		No	Yes
HASH (SHA-512)		No	Yes (SHA-1, SHA-2, SHA-3)
Comparator (COMP)		No	Yes
On-the-fly decryption engine (OTFDEC)		No	Yes
GPIOs		Up to 140	Up to 112
ADC (12 bits)	count	3 (12-bit ADC 2.4 MSPS and 7.2 MSPS in triple interleaved mode)	3 (12-bit ADC with up to 5 MSPS)
	Number of channels	Up to 24	Up to 30
DAC (12 bits)	Count	1	1
	Number of channels	2	2
Digital temperature sensor (DTS)		No	Yes
RCC		Yes	Yes
Operating temperatures		Ambient temperature: : –40 to +85°C /–40 to +105°C Junction temperature: –40 to + 125°C	Ambient operating temperature: • -40 °C to 85 °C • -40 °C to 105 °C • -40 °C to 125 °C Junction temperature: -40 °C to 140 °C
Operating voltage		1.8 to 3.6 V	1.71 to 3.6 V
Internal voltage reference buffer		No	Yes

1. *CCM (core coupled memory)*

5.2 Migration of system peripherals

5.2.1 Embedded flash memory (FLASH)

The following table compares the flash memory interface on the STM32F405/407, and STM32H543/553 devices.

Table 15. FLASH features

Flash memory	STM32F405/407	STM32H543/553
Main / program memory	• Up to 1 Mbytes • 4 sectors of 16 Kbytes • 1 sector of 64 Kbytes • 7 sectors of 128 Kbytes	• Up to 1 Mbytes of nonvolatile memory (dual bank) • Flash memory read operations supporting multiple lengths: 128 bits, 64 bits, 32 bits, 16 bits, or one byte • 8 Kbyte sector erase, bank erase and dual-bank mass erase
Features	Read while write (RWW)	
Error code correction (ECC)	No	One error detection/correction or two error detections per 128-bit flash word using 9 ECC bits, on 16-bit words with 6 bits within configurable Flash high-cycle data area
Wait states	Up to 8 (depending on the supply voltage and frequency)	Up to 6 (depending on the supply voltage and frequency)
One time programmable (OTP) memory	512 bytes (OTP) for user data	2 Kbytes (OTP) area
FLASH security and protections	• Read protection (RDP) • Write protections	• TrustZone® backed watermark and block security protection • HDP protection providing temporal isolation • Configuration protection • Write protection • Device nonvolatile security life cycle and application boot state management
User option bytes (1)	nRST_STDBY nRST_STOP WDG_SW BOR_LEV OPTSTRT OPTLOCK nWRP RDP	NRST_STBY NRST_STOP IWDG_SW WWDG_SW IWDG_STBY, IWDG_STOP BOR_LEV BORH_EN BOOT_UBE OPTSTRT OPTLOCK WRPSG PRODUCT_STATE IO_VDDIO2_HSLV SWAP_BANK

1. *Refer to the “Option-bytes organization” table in [2] that provides all user option bytes.*

5.2.2 SRAMs

The RAMCFG controller, a new peripheral available on STM32H543/553, is dedicated to control SRAM1, SRAM2, SRAM3, and BKPSRAM. Refer to section *RAMs configuration controller* section in the corresponding reference manual for more details.

Table 16. SRAM features

Features	STM32F405/407	STM32H543/553
Size	• Up to 128 Kbytes of system SRAM • Main internal SRAM1 (112 KB) – Auxiliary internal SRAM2 (16 KB) • 4 Kbytes of backup SRAM	Up to 304 Kbytes: • 128-Kbyte SRAM1 • 80-Kbyte SRAM2 • 96-Kbyte SRAM3 • 2-Kbyte BKPSRAM
Access by DMA and CPU	Possible access types: • Bytes • Half-words (16 bits) • Full words (32 bits) .	
CPU access bus	• System bus or I-Code/D-ode buses • BKPSRAM (system bus)	• System bus or C-bus • BKPSRAM (only system bus)
Retention	BKPSRAM: • Optional retention in Standby mode • Optional retention in VBAT mode	
Security	NA	• When the TrustZone® security is enabled, all SRAMs are secure after reset • The SRAMs can be programmed as nonsecure, using the MPCBB with a block granularity of 512 bytes
Hardware and software erase conditions	The backup SRAM is not mass erased by a tamper event Backup SRAM is only erased when the RDP changes from level 1 to 0	SRAM1 and SRAM2 erase can be requested by executing a specific software sequence, detailed in section *RAMCFG* of the product reference manual SRAM2 and optionally backup SRAM are protected by the tamper detection circuit, and is erased by hardware in case of tamper detection SRAM2 is deleted in case of regression
System reset erase	NA	SRAM2 can be erased with a system reset using the option bit SRAM2_RST option bit in the Flash memory user option bytes SRAM1 and SRAM3 are erased when a system reset occurs if the SRAM13_RST option bit is selected in the Flash memory user option bytes
Error detection and correction	NA	• Single error detection and correction with interrupt generation • Double error detection with interrupt or NMI generation • The ECC is supported by SRAM2, SRAM3, and BKPSRAM when enabled with the SRAM2_ECC, SRAM3_ECC, and BKPRAM_ECC user option bits • ECC: 7 bits are added per 32 bits • Interrupts are generated when single- and/or double-ECC errors are detected: – Two ECC RAMCFG interrupts – One ECC NMI interrupt
Write protection	NA	SRAM2 can be write-protected with a page granularity of 1 Kbyte Each 1-Kbyte page can be write-protected by setting its corresponding PxWP (x = 0 to 79) bit in RAMCFG registers
Read access latency	NA	3-bit programmable wait-states depending on AHB clock frequency (HCLK) and voltage scaling range

5.2.3 System configuration controller

The table below illustrates the system configuration controller (SYSCFG) main differences between STM32F405/407, and STM32H543/553 devices.

Note: For STM32H5 series, the SYSCFG (system configuration controller) is integrated in the SBS (system configuration, boot, and security).

Table 17. System configuration features

STM32F405/407	STM32H543/553
• Manage the I/O compensation cell • Select the Ethernet PHY interface	
• Remap the memory accessible in the code area • Manage the external interrupt line connection to the GPIOs	NA
NA	• Enable/disable the FMP high-drive mode of some I/Os and voltage booster for I/O analog switches • Configuring TrustZone® security register access • Tracking the PVT conditions to control the current slew-rate and output impedance in I/O buffer through compensations cells • Two compensation cells are embedded, one for the I/Os supplied by VDDIO power rail and one for the I/Os supplied by VDDIO2 power rail

5.2.4 Instruction and data caches (ICACHE/DCACHE)

The STM32H543/553 embed an ICACHE (8 Kbytes) and a DCACHE (4 Kbytes) that allows more efficient use of the external memory through OCTOSPI and FMC ports.

The STM32F405/407 devices do not embed these caches.

5.2.5 Direct memory access controller (DMA)

The STM32F405/407, and STM32H543/553 have different DMA architecture and features.

All devices embed two DMA controllers:

- DMA1 (8 channels) and DMA2 (8 channels) for STM32F405/407
  Each channel is dedicated to manage the memory access requests from one or more peripherals. The devices embed also an arbiter for handling the priorities among the DMA requests
- GPDMA1 (8 channels) and GPDMA2 (8 channels) for STM32H543/553
  Each GPDMA instance has the same channel-based implementation and is connected to the same requests and triggers

The following table illustrates the main differences between DMA requests in STM32F405/407, and STM32H543/553.

Table 18. DMA features

Peripherals	STM32F405/407		STM32H543/553	
	DMA1	DMA2	GDMA1	GDMA2
Architecture	Each instance of DMA controllers can access memory and peripherals			
Number of instances	1	1	1	1
Number of masters	Dual AHB master bus	Dual AHB master bus	Dual bidirectional AHB master	
Number of channels	8	8	8	8
TrustZone® security	NA		Yes	
Privileged/unprivileged DMA				
Linked-List				

5.2.6 Reset and clock control (RCC)

The table below presents the main differences related to the RCC (reset and clock controller) between the STM32F405/407, STM32H543/553 devices.

Table 19. RCC features

RCC	STM32F405/407	STM32H543/553
HSI	16 MHz RC oscillator	64 MHz RC oscillator
CSI	NA	CSI is a low-power RC oscillator that can be used directly as system clock, peripheral clock, or PLL input: • Low-cost clock source since no external crystal is required. • Faster startup time than HSI (a few microseconds) • Very low-power consumption. The CSI provides a clock frequency of about 4 MHz.
HSI48	NA	48 MHz RC oscillator HSI48 can drive USB and RNG.
LSI	Clock frequency around 32 kHz Lower consumption, higher accuracy	
HSE	From 4 to 26 MHz	From 4 to 50 MHz
LSE	32.768 kHz	32.768 kHz Provide a low-power, highly accurate clock source to the real-time clock (RTC) for clock/calendar or other timing functions.
PLL	Two PLLs: • PLLI2S used to generate an accurate clock on the I2S interface. • A main PLL (PLL) clocked by the HSE or HSI oscillator and featuring two different output clocks: – One output generates the high-speed system clock (up to 180 MHz) – One output for USB OTG FS, RNG, and SDIO	Two PLLs: • Main PLL (PLL1) provides clocks for CPU and some peripherals • PLL2 generates the kernel clock for peripherals Each PLL offers three outputs with post-dividers. Input frequency range: • 2 to 16 MHz for the VCO in wide-range mode • 1 to 2 MHz for the VCO in low-range mode
AHB frequency	Up to 168 MHz	Up to 250 MHz
APB1 frequency	Up to 42 MHz	Up to 250 MHz
APB2 frequency	Up to 84 MHz	Up to 250 MHz
RTC clock source	LSE, LSI, or HSE/ 32	
Kernel clock	NA	Independent kernel clock for each IP, allowing frequency scaling without impact on communication interfaces
System clock source	HSI, HSE, or PLL	HSI, CSI, HSE, or PLL1
Clock security system	CSS on HSE	CSS on HSE CSS on LSE
MCO clock source	• MCO1 pin (PA8): HSI, LSE, HSE, or PLL • MCO2 pin (PC9): HSE, PLL, SYSCLK, or PLLI2S	• MCO1 pin (PA8): HSI,LSE,HSE, PLL1 or HSI48 • MCO2 pin (PC9): SYSCLK, PLL2, HSE, PLL1,CSI, or LSI

Peripheral clock configuration

The peripherals presented below have a dedicated clock source, that is used to generate the clock required for their operation. This section presents the difference between STM32F405/407, and STM32H543/553 devices, for peripherals with different clock sources.

Table 20. Peripherals with different clock sources

Peripherals	STM32F405/407	STM32H543/553
U(S)ART	APB1 or APB2 clock (PCLK1 or PCLK2)	rcc_pclk2[(1)] rcc_pclk1[(2)] pll2_q_ck hsi_ker_ck csi_ker_ck lse_ck
I2Cs	APB1 clock (PCLK1)	csi_ker_ck pll2_r_ck hsi_ker_ck rcc_pclk1[(3)] rcc_pclk3[(4)]
SPI	APB2 clock (PCLK2)	rcc_pclk2[(5)] pll2_q_ck[(5)] hsi_ker_ck[(5)] hse_ck[(5)] csi_ker_ck[(5)] pll1_q_ck[(6)] pll2_p_ck[(6)] AUDIOCLK[(6)] per_ck[(6)]
I2S	PLLI2S External clock mapped on I2S_CKIN pin	pll2_p_ck AUDIOCLK per_ck pll1_q_ck
CAN	APB1 clock (PCLK1)	hse_ck pll1_q_ck pll2_q_ck
ADC	APB2 clock (PCLK2)	sys_ck pll2_r_ck hse_ck hsi_ker_ck csi_ker_ck rcc_hclk
USB FS	PLL 48 MHz derived from main PLL VCO (PLLQ clock)	hsi48_ker_ck pll1_q_ck pll2_q_ck
RNG		hsi48_ker_ck

Peripherals	STM32F405/407	STM32H543/553
	PLL 48 MHz derived from main PLL VCO (PLLQ clock)	pll1_q_ck lse_ck lsi_ker_ck
SDMMC	SDIO/SDMMC1: PLL48CLK	pll1_q_ck pll2_r_ck
PLAY	NA	rcc_pclk3 lse_ker_ck lsi_ker_ck pll2_p_ck per_ck
IWDG	LSI	

1. *Only for USART1*
2. *Only for USARTx (x=2, 3, 6) and UARTx (x=4,5,7,8)*
3. *Only for I2Cx (x=1,2)*
4. *Only for I2C3*
5. *Only for SPI4*
6. *Only for SPIx (x=1,2,3)*

5.2.7 Power (PWR)

The table below presents the PWR controller differences between STM32F405/407 devices, and STM32H543/553 devices. Both dynamic and static power-consumption were optimized for the STM32H543/553 devices.

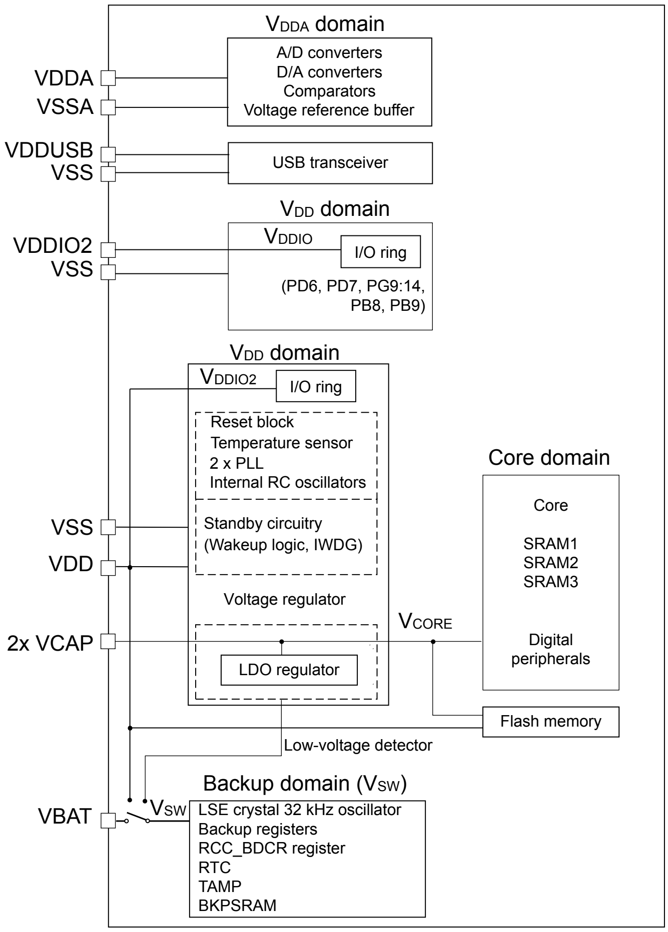
Table 21. PWR features

PWR	STM32F405/407	STM32H543/553
Power supplies	**VDD = 1.8 to 3.6 V:** external power supply for I/Os and the internal regulator (when enabled), provided externally through VDD pins	**VDD = 1.71 V to 3.6 V:** external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.
	VSSA, VDDA = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, reset blocks, RCs, and PLL. VDDA and VSSA must be connected to VDD and VSS, respectively.	**VDDA = 1.62 V (ADCs, COMP) or 1.8 V (DAC) / 2.1 (VREFBUF) to 3.6 V:** VDDA is the external analog power supply for A/D converters, D/A converters, and voltage reference buffer. The VDDA voltage level is independent from the VDD voltage, and must preferably be connected to VDD when these peripherals are not used.
	V12: voltage source through VCAP_1 and VCAP_2 pins/ around **1.2 V**	**VCAP = 1.0 V to 1.35 V:** power supply for digital peripherals, SRAMs (except BKPSRAM), and embedded flash memory
	VBAT = 1.65 to 3.6 V: when VDD is not present, VBAT is power supply for RTC, external clock 32 kHz oscillator, and backup registers	**VBAT = 1.2 V to 3.6 V:** when VDD is not present, VBAT is the power supply for RTC, external clock 32 kHz oscillator, backup registers, and optionally backup SRAM
	NA	**VDDUSB = 3.0 V to 3.6 V**: external independent power supply for USB transceivers The VDDUSB voltage level is independent from the VDD voltage.
	NA	**VDDIO2 = 1.08 V to 3.6 V:** external power supply for 10 I/Os (PD6, PD7, PG9:14, PB8, PB9). This voltage is independent from the VDD voltage.

PWR	STM32F405/407	STM32H543/553
Battery backup domain	RTC with backup registers LSE Backup SRAM when the low-power backup regulator is enabled. PC13 to PC15 I/Os, plus PI8 I/O (when available)	RTC with backup registers (128 bytes) LSE PC13 to PC15 I/Os
Power supply supervisor	POR, PDR, BOR, PVD	
	NA	AVD Backup domain voltage and temperature monitoring
Sleep mode wake-up sources	Any peripheral interrupt/wakeup event	
Standby mode, wake-up sources	WKUP pin PA0 on rising edge RTC event (RTC ALARM, Tamper event, Time stamp event) IWDG reset External reset in NRST pin	WKUPx pin edge, RTC event, external reset in NRST pin, IWDG reset, BOR reset
Stop mode, wake-up sources	Any EXTI line (configured in the EXTI registers, internal and external lines)	Any EXTI line (configured in the EXTI registers) Specific peripherals events
Wakeup system clock	Stop: HSI RC oscillator	Stop: CSI when STOPWUCK = 1 in RCC_CFGR HSI with the frequency before entering the Stop mode, up to 64 MHz, when STOPWUCK Standby: HSI clock at 64 MHz
Low-power modes	Sleep mode	Sleep mode
	Stop mode	Stop mode: To further optimize the power consumption, the unused RAMs can be totally or partially Shut-off.
	Standby mode	Standby mode

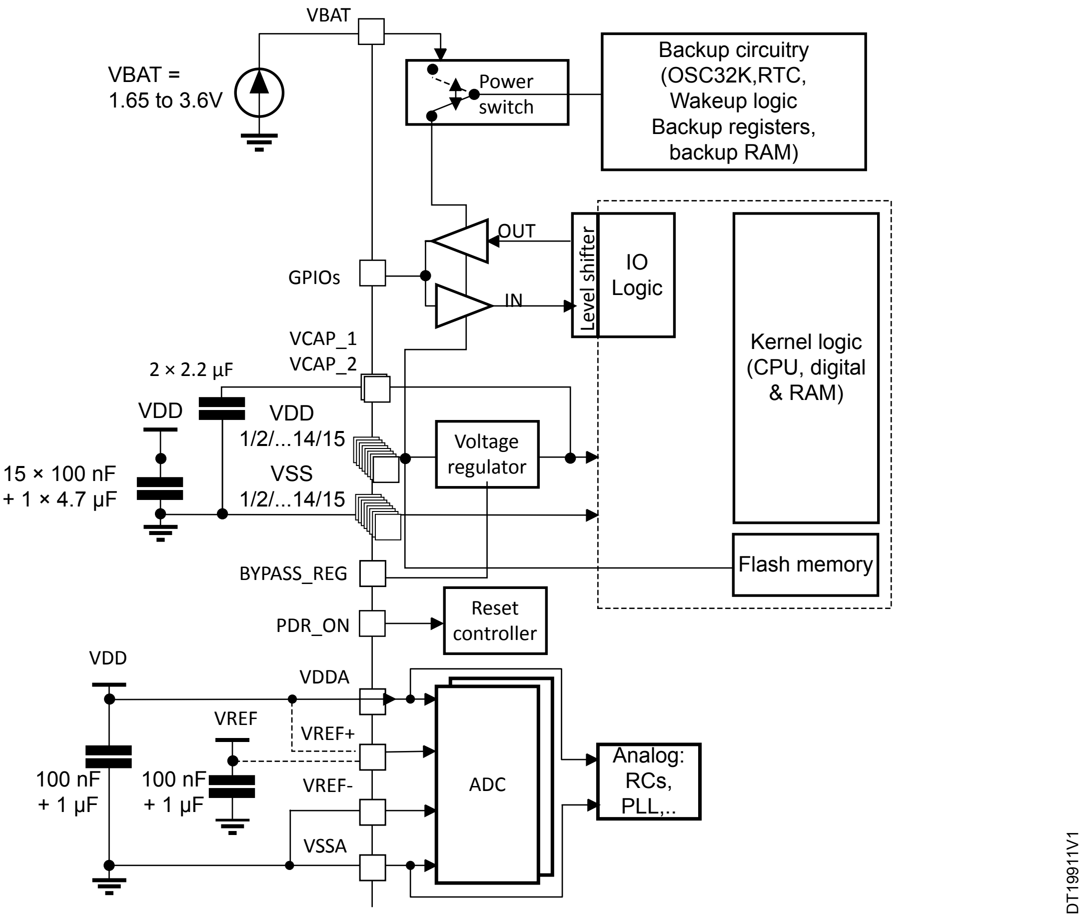
The following figures present the power supply for the STM32F405/407, and STM32H543/553 devices. The differences are summarized in the previous table.

Figure 6. STM32H543/553 power supply overview



DT78002V1

Figure 7. **Power supply overview for STM32F405/407**



5.2.8 General-purpose I/Os (GPIO)

STM32H543/553 implement the same GPIO features as STM32F405/407, but with main differences.

For STM32H543/553, each GPIO port has four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR and GPIOx_PUPDR), two 32-bit data registers (GPIOx_IDR and GPIOx_ODR), a 16 bits reset register (GPIOx_BRR) and a 32-bit set/reset register (GPIOx_BSRR).

In addition, all GPIOs have a 32-bit locking register (GPIOx_LCKR), two 32-bit alternate function selection registers (GPIOx_AFRH and GPIOx_AFRL), a secure configuration register (GPIOx_SECCFGR) and a high-speed low-voltage register (GPIOx_HSLVR).

Each general-purpose I/O pin of GPIO port in STM32H543/553 can be individually configured as secure through the GPIOx_SECCFGR register. After reset, all GPIO ports are secure.

All GPIO registers can be read and written by privileged and unprivileged accesses, whatever the security state secure or nonsecure.

- Additional TrustZone® security support.
  The TrustZone® security is activated by the TZEN option byte in the Flash Option Byte register. When the TrustZone® is active (TZEN = 0xB4), each I/O pin of GPIO port can be individually configured as secure through the GPIOx_SECCFGR register.
- I/Os state retention during Standby mode.
  In the Standby mode, the I/Os in STM32H543/553 are by default in floating state. If the IORETEN bit in the PWR_IORETR register is set, the I/Os state is sampled during standby entry. The state of I/Os is applied to the pin via pull-up and pull-down resistors. The pull-up and pull-down resistors remains applied after Standby wake-up until software clears the IORETEN bit in the PWR_IORETR register.
- High-speed low-voltage mode (HSLV)
  Some I/Os have the capability to increase their maximum speed at low voltage by configuring them in HSLV mode. The I/O HSLV bit controls whether the I/O output speed is optimized to operate at 3.3 V (default setting) or at 1.8 V (HSLV = 1).

For more information about the STM32H543/553 GPIO and TrustZone® security, refer to the *General-purpose I/Os (GPIO)* section of the reference manual and to the product datasheet for detailed description of the pinout and alternate function mapping.

5.2.9 Extended interrupt and event controller (EXTI)

5.2.9.1 EXTI main features in STM32H543/553

The extended interrupts and event controller (EXTI) manages the individual CPU and system wakeup through configurable event inputs. It provides wakeup requests to the power control and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU, an additional event generation block (EVG) is needed to generate the CPU event signal.

The STM32H543/553 feature TrustZone® security support and privileged/unprivileged mode selection and do not feature direct event inputs.

EXTI security protection

When security is enabled for an input event, the associated input event configuration and control bits can only be modified and read by a secure access. A nonsecure write access is discarded and a read returns 0.

EXTI privilege protection

When privilege is enabled for an input event, the associated input event configuration and control bits can only be modified and read by a privileged access. An unprivileged write access is discarded and a read returns 0.

The table below describes the difference of EXTI features between STM32F405/407 devices, and STM32H543/553 devices.

Table 22. EXTI features

EXTI	STM32F405/407	STM32H543/553
Features	Generation of up to 23 software event/interrupt requests	• 67 input events supported • TrustZone® support • Privileged/unprivileged mode

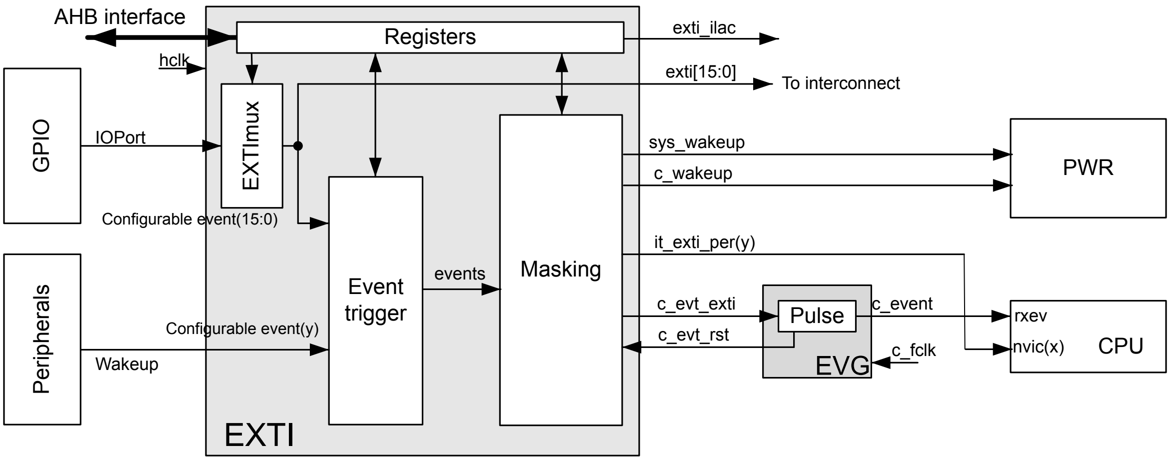
5.2.9.2 EXTI block diagram in STM32H543/553

As shown in the figure below, the EXTI consists of

- a register block accessed via an AHB interface
- an event input trigger block
- a masking block, and EXTI mux as shown in the figure below.

The register block contains all the EXTI registers. The event input trigger block provides event input edge trigger logic.

Figure 8. EXTI block diagram on STM32H543/553



The table below presents the EXTI line differences between STM32F405/407, and STM32H543/553 devices.

Table 23. EXTI line differences

EXTI line	STM32F405/407	STM32H543/553
0-15	16 external interrupt lines	GPIO
16	PVD output	PVD/AVD output
17	RTC alarm event	RTC nonsecure
18	USB OTG FS wakeup event	RTC secure
19	Ethernet wakeup event	TAMP nonsecure
20	USB OTG HS (configured in FS) wakeup event	TAMP secure
21	RTC tamper and TimeStamp events.	I2C1 wakeup
22	RTC wakeup event	I2C2 wakeup
23	NA	I2C3 wakeup
24		I3C1 wakeup
25		USART1 wakeup
26		USART2 wakeup
27		USART3 wakeup
28		UART4 wakeup
29		UART5 wakeup
30		USART6 wakeup
31		UART7 wakeup
32		UART8 wakeup
33		Reserved
34		Reserved
35		Reserved
36		Reserved
37		LPUART1 wakeup
38		LPTIM1
39		LPTIM2

EXTI line	STM32F405/407	STM32H543/553
40	NA	SPI1 wakeup
41		SPI2 wakeup
42		SPI3 wakeup
43		SPI4 wakeup
44		Reserved
45		Reserved
46	NA	ETH wakeup
47		USB FS wakeup
48		UCPD1 wakeup
49		LPTIM2 CH1
50		DTS wakeup
51		HDMI-CEC wake-up
52		Reserved
53		UVM output
54		Reserved
55		Reserved
56		Reserved
57		Reserved
58	NA	COMP1 output
59		COMP2 output
60		Reserved
61		I3C2 wake-up
62		Reserved
63		Reserved
64		play_out14
65		IWDG
66		VDDIO2 Voltage monitor

5.2.10 CRC calculation unit

The table below presents the CRC differences between the STM32F405/407 and STM32H543/553 devices.

Table 24. CRC features

<table>
<tr><th>CRC</th><th>STM32F405/407</th><th>STM32H543/553</th></tr>
<tr><td rowspan="2">Features</td><td colspan="2">• Uses CRC-32 (Ethernet) polynomial
• Single input/output 32-bit data register
• CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size
• General-purpose 8-bit register (can be used for temporary storage)</td></tr>
<tr><td>Handles 32-bit data size</td><td>• Handles 8-,16-, 32-bit data size fully programmable polynomial with programmable size (7, 8, 16, 32 bits)
• Programmable CRC initial value
• Input buffer to avoid bus stall during calculation
• Reversibility option on I/O data
• Accessed through AHB slave peripheral by 32-bit words only, with the exception of CRC_DR register that can be accessed by words, right-aligned half-words and right-aligned bytes</td></tr>
<tr><td rowspan="2">CRC registers</td><td colspan="2">• CRC data register (CRC_DR)
• CRC independent data register (CRC_IDR)
• CRC control register (CRC_CR)</td></tr>
<tr><td>-</td><td>• CRC initial value (CRC_INIT)
• CRC polynomial (CRC_POL)</td></tr>
</table>

5.3 Migration of security peripherals

5.3.1 Random number generator (RNG)

The STM32H543/553, and STM32F405/407 embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit. The table below presents the RNG features of STM32H543/553, and STM32F405/407.

Table 25. RNG features

<table>
<tr><th>RNG</th><th>STM32F405/407</th><th>STM32H543/553</th></tr>
<tr><td rowspan="2">Features</td><td>• RNG delivers 32-bit random numbers
• 40 periods of the RNG_CLK clock signal between two consecutive random numbers
• RNG passed the FIPS PUB 140-2 tests with a success ratio of 99%
• Monitoring of the RNG entropy to flag abnormal behavior</td><td>• RNG delivers 32-bit true random numbers
• Can be used as entropy source to construct a non-deterministic random bit generator (NDRBG)
• Tested using German BSI statistical tests of AIS-31 (T0 to T8)
• Embeds start-up and NIST SP800-90B approved continuous health tests
• AMBA AHB slave peripheral, accessible through 32-bit word single accesses only
• RNG internal tamper event signal to TAMP
• Can be enabled with an automatic low-power mode (default configuration)</td></tr>
<tr><td colspan="2">Can be disabled to reduce power consumption</td></tr>
</table>

In STM32H543/553, the RNG is transparently used by SAES and PKA.

When an unexpected error is found by the RNG an internal tamper event is triggered in TAMP peripheral, and the RNG stops delivering random data. When this event occurs, secure application needs to reset the RNG peripheral either using the central reset management or the global SoC reset. Then a proper initialization of the RNG is required, again.

5.3.2 HASH processor (HASH)

The STM32H543/553 devices embed one HASH processor peripheral. While in STM32F405/407, this peripheral is not supported. The following table illustrates the STM32H543/553 HASH features.

Table 26. HASH features

HASH	STM32H543/553
Features	• Secure HASH algorithm (SHA-1, SHA-2 family, SHA-3 family) • HMAC (keyed-hash message authentication code) algorithm
	• FIPS PUB 180-4 • Secure HASH standard (SHA-1 and SHA-2 family) • FIPS PUB 186-4, digital signature standard (DSS) • Internet engineering task force (IETF) request for comments RFC 2104, • Federal information processing standards publication FIPS PUB 202, secure hash standard (SHA-3 family)
	Fast computation of SHA-1, SHA2-224, SHA2-256, SHA2-384, and SHA2-512
	50 × 32-bit words (HR0 to HR41) for output message digest and general purpose SHA-3 outputs
	Single 32-bit, write-only, input register associated to an internal input FIFO, that can receive a single data block with a size that depends on the selected algorithm.
	• Automatic data flow control supporting direct memory access (DMA) • Support for both single and fixed DMA burst transfers of four words
	• AMBA AHB target peripheral • Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message • Automatic padding to complete the input bit string

5.3.3 On-the-fly decryption engine (OTFDEC)

The OTFDEC decrypts in real-time the encrypted content stored in the external OCTOSPI memories used in Memory-mapped mode. The OTFDEC uses the AES-128 algorithm in counter mode (CTR).

The STM32H543/553 embed one OTFDEC peripheral. While in STM32F405/407, this peripheral is not supported.

5.3.4 Public key accelerator (PKA)

The STM32H543/553 devices embed one PKA peripheral intended for the computation of cryptographic public key primitives within the Montgomery domain.

The STM32H543 devices use the PKA in limited mode (only ECDSA signature verification is available).

All needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

The STM32F405/407 devices do not support a PKA peripheral.

5.3.5 AES and SAES hardware accelerators

The STM32H543/553 embed two AES accelerators: one secure AES (SAES) and a faster AES. The SAES is a new feature in STM32H543/553.

In STM32H543/553, the SAES with hardware-unique key embeds protection against differential power analysis (DPA) and related side channel attacks.

When an unexpected hardware fault occurs, an output tamper event is triggered, and the AES automatically clears key registers. A reset is required for the AES to be usable again.

The AES peripheral can use the SAES peripheral as security coprocessor. In this case, the secure application performs two actions:

- prepares the key in the robust SAES peripheral
- when they key is ready, the AES can load this prepared key through a dedicated hardware key bus.

5.3.6 Coupling and chaining bridge (CCB)

The STM32H543/553 devices embed the CCB that can be programmed to implement special coupling and chaining operations, required to the protect private keys used in PKA protected operations.

These coupling and chaining operations involve the PKA, the SAES, and sometimes the RNG peripherals.

5.3.7 Global TrustZone controller (GTZC)

The security architecture of STM32H543/553 is based on Arm® TrustZone® with the Armv8-M mainline extension.

The following components can be configured as trusted or untrusted:

- Each GPIO
- Each peripheral
- Each DMA channel
- Each clock configuration register
- Each DCACHE/ICACHE
- A small part of the flash memory or SRAM

The GTZC embedded in the STM32H543/553 is used to configure secure TrustZone® and privileged attributes within the full system. Refer to [2] for a detailed description of the GTZC.

This controller is a new feature of STM32H543/553 and is not embedded in STM32F405/407.

5.4 Migration of communication peripherals

5.4.1 Serial peripheral interface (SPI)

This section highlights the SPI features(1) implemented on STM32F405/407, and STM32H543/553 devices.

Table 27. SPI features

SPI	STM32F405/407	STM32H543/553
Instances	3x SPIs	4x SPIs
Speed	Up to 42 Mbit/s	Up to 50 Mbps
Features	SPI + I2S	
	2 SPIs muxed with full-duplex I2S	3 SPIs muxed with full-duplex I2S
Full-duplex synchronous transfer on three lines	X	X
Half-duplex	X	X
Simplex synchronous transfer on two lines	With or without a bidirectional data line	With unidirectional data line
Data size	8- or 16-bit transfer frame format selection	Data size selection: • From 4 bits up to 32 bits • Fixed to a multiple of 8 bits
Multimaster mode capability	X	X
Baudrate prescalers	8 master mode baud rate prescalers (fPCLK/2 max.)	Baud rate prescaler up to kernel frequency/2 or bypass from RCC in master mode
Protection of configuration and settings	NA	X
Slave select (SS) management	NSS management by hardware or software for both master and slave: dynamic change of master/slave operations	Hardware or software management of SS for both master and slave
Configurable SS signal polarity and timing	NA	Configurable SS signal polarity and timing, MISO x MOSI swap capability

SPI	STM32F405/407	STM32H543/553
Programmable transaction data	NA	Programmable number of data within a transaction to control SS and CRC
Programmable data order with MSB-first or LSB-first shifting	X	X
Programmable clock polarity and phase	X	X
Data sampling delay on master input	NA	X
Dedicated transmission and reception flags with interrupt capability	X	X
SPI Motorola and TI formats support	X	X
Hardware CRC feature for reliable communication: • CRC value can be transmitted as last byte in Tx mode • Automatic CRC error checking for last-received byte	X	X
Interrupt events and error detection with interrupt capability	Interrupts: • Transmit buffer-empty flag • Receive buffer not empty flag • Master mode fault event • Overrun error • CRC error flag • TI frame format error	Interrupts: • TxFIFO ready to be loaded • Data received in RxFIFO • Both TXP and RXP active • Transmission transfer filled • Overrun error • Underrun error • TI frame format error • CRC error • Mode fault • End of transfer • Master mode suspended • TxFIFO transmission complete All the interrupt events are capable to wakeup system from Sleep mode at each instance
Configurable behavior at slave-underrun condition	NA	X (support of cascaded circular buffers)
FIFOs	NA	• Two multiply of 8-bit embedded Rx and Tx FIFOs (FIFO size depends on instance) • Configurable FIFO thresholds (data packing)
RDY status pin	NA	Optional status pin RDY signalizing the slave device ready to handle the data flow

1. *X = available, NA = not available.*

5.4.2 Inter-integrated circuit (I2C)

The STM32H543/553 devices implement the same I2C features than the STM32F405/407 devices but with some enhancements. The main differences are stated in the table below.

Table 28. **I2C differences**

I2C	STM32F405/407	STM32H543/553
Instances	x3 (I2C1, I2C2, I2C3)	x3 (I2C1, I2C2, and I2C3)
Features	• 7-bit and 10-bit addressing mode • SMBus/PMBus • Standard mode (up to 100 kbit/s) • Fast mode (up to 400 kbit/s)	
	Single clock source	• Fast-mode plus (up to 1 MHz) I2C bus • Wakeup from stop mode only (no autonomous mode) • Independent clock

5.4.3 Improved inter-integrated circuit (I3C)

The STM32H543/553 devices implement a new feature compared to the STM32F405/407 devices, which is the I3C peripherals.

5.4.4 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32H543/553 devices implement several new features on the U(S)ART compared to the STM32F405/407 devices. The following table shows the U(S)ART differences.

Table 29. **U(S)ART features**

USART	STM32F405/407	STM32H543/553
Instances	• 4 USARTs • 2 UARTs	• 4 USARTs • 4 UARTs • LPUART
Baud rate	Up to 10.5 Mbit/s	Depends on the frequency (oversampling by 16 or by 8)(1)
Clock	Single clock domain	Dual clock domain and Wakeup from low-power mode
Data	Word length: programmable (8 or 9 bits)	• Word length: programmable (7, 8 or 9 bits) • Programmable data order with MSB-first or LSB-first shifting
Interrupt	10 interrupt sources with flags	23 interrupt sources with flags
Others features	Hardware flow control (CTS/RTS)	• RS232 hardware flow control • RS485 hardware control mode
	• LIN mode • IrDA SIR encoder block • Continuous communication using DMA • Multiprocessor communications • Single-wire half-duplex communication	
	NA	• Modbus communication: Timeout feature, CR/LF character recognition • Two internal FIFOs for transmit and receive data • Receiver timeout interrupt (except LPUART) • Auto baud rate detection (except LPUART) • Driver enable • Swappable Tx/Rx pin configuration • Wakeup from Stop mode
	• Smartcard mode: has to be implemented by software • Number of stop bits: 0.5, 1, 1.5, 2	• Smartcard mode : Support the T=0 and T=1 asynchronous protocols • Number of stop bits: 0.5, 1, 1.5, 2

1. *Refer to the USART section in [2].*

5.4.5 Controller area network (CAN)

The main differences related to CAN between STM32F405/407 and STM32H543/553 are presented in the table below.

Table 30. CAN features

CAN	STM32F405/407	STM32H543/553
Instances	x2	x2 FDCAN
Features	• Supports CAN protocol version 2.0 A, B Active • Bit rates up to 1 Mbit/s • Supports the time triggered communication option • Tx :3 transmit mailboxes, configurable transmit priority, time stamp on SOF transmission • Rx:2 receive FIFOs with three stages, scalable filter banks, identifier list feature, configurable FIFO overrun, time stamp on SOF reception • Time-triggered communication option: disable automatic retransmission mode,16-bit free running timer, time stamp sent in last two data bytes • Management: – Maskable interrupts – Software-efficient mailbox mapping at a unique address space • Dual CAN: • – CAN1: master bxCAN for managing the communication between a slave bxCAN and the 512-byte SRAM memory – CAN2: slave bxCAN, with no direct access to the SRAM memory	• Conform with CAN protocol version 2.0-part A, B and ISO 11898-1: 2015, -4 • CAN FD with maximum 64 data bytes supported • CAN error logging • AUTOSAR and J1939 support • Improved acceptance filtering • Two receive FIFOs of three payloads each (up to 64 bytes per payload) • Separate signaling on reception of high priority messages • Configurable transmit FIFO / queue of three payload (up to 64 bytes per payload) • Transmit event FIFO • Programmable loop-back test mode • Maskable module interrupts • Two clock domains: APB bus interface and CAN core kernel clock • Power down support

5.4.6 Universal serial-bus interface (USB)

The STM32F405/407 and STM32H543/553 devices have different USB peripherals:

- The STM32F405/407 devices implement a USB OTG FS
- The STM32H543/553 devices implement an USB FS and USB Type-C® connector/USB power delivery interface (UCPD)

Most features supported by the STM32F405/407 devices are also supported by the STM32H543/553 devices. The main USB differences between the STM32F405/407 and STM32H543/553 devices are listed in the table below.

Table 31. USB differences

USB	STM32F405/407	STM32H543/553
General	Full support for the USB on-the-go (USB OTG FS)	USB FS with clock recovery
	FS mode: • One bidirectional control endpoint • Three IN endpoints (bulk, interrupt, isochronous) • Three OUT endpoints (bulk, interrupt, isochronous) **HS mode:** • 6 bidirectional endpoints (including EP0) • 12 host mode channels	Up to 8 bidirectional endpoints
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D + (USB_DP) line	USB connect / disconnect capability (controllable embedded pull-up resistor on USB_DP line)
	NA	Battery charging detection (BCD) support for device
		Independent VDDUSB power supply
Buffer memory	**FS mode:** • 1.25-Kbyte data FIFOs • Management of up to 4 Tx FIFOs (one for each IN end point) + one Rx FIFO **HS mode:** • 4 Kbytes of total RAM	2048 bytes of dedicated packet buffer memory SRAM
Low-power modes	**FS mode:** • USB suspend and resume **HS mode:** • No LPM supported	USB revision 2.4 including link power management (LPM) support

5.5 Migration of analog peripherals

5.5.1 Analog-to-digital converter (ADC)

The STM32H543/553 devices embed three ADCs::

- ADC1 and ADC2: both consist of a 12-bit successive approximation ADC that are tightly coupled and can operate in dual mode (ADC1 is master).
- ADC3 is controlled independently.

The STM32F405/407 devices embed three ADCs:

- ADC1
- ADC2
- ADC3 (12-bit resolution.) .

Table 32. ADC differences between devices

ADC	STM32F405/407	STM32H543/553
Instances	x3	x3
Resolution	12-bit	
Number of channels	Up to 24	Up to 30
Configurable resolution	12-bit, 10-bit, 8-bit or 6-bit	
Maximum sampling speed	2.4 MSPS 7.2 MSPS in triple interleaved mode	5 MSPS
Conversion modes	• Single • Continuous • Scan • Discontinuous • Dual mode	
DMA support	Yes	
Data register	16-bit data register	
Analog watchdog feature	This feature allows the application to detect if the input voltage goes outside the user-defined high or low threshold	
ADC input range:	VREF– ≤ VIN ≤ VREF+	VSSA ≤ VIN ≤ VREF+
New features	NA	• ADC conversion time independent from the AHB bus clock frequency • Manage single-ended or differential inputs • Low-power features • Three analog watchdogs per ADC • Self-calibration • Oversampling ratio adjustable from 2 to 256 • Programmable data shift up to 8 bits

5.5.2 Digital-to-analog converter (DAC)

The STM32H543/553 devices implement some enhanced DAC compared to the STM32F405/407 Series devices. Refer to the table below for the main DAC differences between them.

Table 33. DAC differences

DAC	STM32F405/407	STM32H543/553
Instances	x2 with one output channel each	x1 with maximum two output channels
Resolution	12 bits	
Output buffer	Yes	
Dual DAC channel	For independent or simultaneous conversions	
New features	NA	• Double-data DMA • Buffer offset calibration • Sample and hold mode for low-power operation in Stop mode

5.6 Migration of timer peripherals

The STM32H543/553, STM32F405/407 devices include two advanced-control timers, six general-purpose timers for the STM32H543/553, and up to ten for the STM32F405/407, two basic timers, two watchdog timers and two SysTick timers (one for STM32F405/407).

Furthermore, the STM32H543/553 devices include two low-power timers.

This section compares the features of the above listed timers and RTC in STM32H543/553,STM32F405/407 devices.

5.6.1 Advanced-control timers (TIM1/TIM8)

The STM32H543/553, and STM32F405/407 include two advanced-control timers, TIM1 and TIM8, with almost identical features detailed in the table below.

Table 34. Advanced-control timer (TIM1/8) features

Feature	STM32F405/407	STM32H543/553
Counter resolution and type	16-bit up, down, up/down auto-reload counter	
Prescaler factor	16-bit programmable prescaler allowing dividing (also “on the fly”) the counter clock frequency either by any factor between 1 and 65536	
Channels	Up to four independent channels for: • Input capture • Output compare • PWM generation (Edge and Center-aligned mode) • One-pulse mode output	Up to four independent channels for: • Input capture • Output compare • PWM generation (Edge and Center-aligned mode) • One-pulse mode output
Complementary outputs	Complementary outputs with programmable dead-time	
Synchronization with external signals and general-purpose timers	• Synchronization circuit to control the timer with external signals and to interconnect several timers together • The advanced-control (TIM1/TIM8) and general-purpose (TIMy) timers are completely independent, and do not share any resources	
Repetition counter	Repetition counter to update the timer registers only after a given number of cycles of the counter	
Break inputs	One break input to put the timer’s output signals in reset state or in a known state	Two break inputs to put the timer’s output signals in reset state or in a known state
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization or count by internal/external trigger) • Input capture • Output compare	
Encoders and sensors	Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes	
Trigger input	Trigger input for external clock or cycle-by-cycle current management	
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion)	

5.6.2 GP timers with up, down, up-down auto-reload counter (TIM2/3/4/5)

The GP (general-purpose) timers consist of a 16-bit or 32-bit auto-reload counter driven by a programmable prescaler.

The STM32H543/553, STM32F405/407 devices include GP timers with up, down or up/down auto-reload counter (TIM2, TIM3, TIM4 and TIM5), with identical features.

Table 35. **GP timer (TIM2/3/4/5) features**

Feature	STM32F405/407 and STM32H543/553
32-bit resolution	TIM2 and TIM5
16-bit resolution	TIM3 and TIM4
Counter resolution and type	16-bit or 32-bit up, down, up/down auto-reload counter
Prescaler factor	16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
Channels	Up to four independent channels for: • Input capture • Output compare • PWM generation (Edge- and Center-aligned modes) • One-pulse mode output
Synchronization with external signals and other timers	Synchronization circuit to control the timer with external signals and to interconnect several timers
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/ external trigger) • Trigger event (counter start, stop, initialization or count by internal/external trigger) • Input capture • Output compare
Encoders and sensors	Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes
Trigger input	Trigger input for external clock or cycle-by-cycle current management
Application examples	• Measuring the pulse lengths of input signals (*input capture*) • Generating output waveforms (*output compare and PWM*)

5.6.3 GP timers with auto-reload up-counter

The STM32H543/553, STM32F405/407 devices include 16-bit resolution GP timers with a 16-bit auto-reload up-counter:

- TIM12/TIM15 for STM32H543/553 devices
- TIM9 to TIM14 for STM32F405/407 devices

Table 36. GP timer (with auto-reload up-counter) features

Feature	STM32F405/407		STM32H543/553	
16-bit resolution	TIM10/TIM11 and TIM13/TIM14	TIM9/TIM12	TIM15	TIM12
Counter resolution and type	16-bit auto-reload up-counter			
Prescaler factor	16-bit programmable prescaler used to divide the counter clock frequency by any factor between 1 and 65535			
Channels	Independent channel for:	Up to two independent channels for:		
	• Input capture • Output compare • PWM generation (Edge-aligned mode) • One-pulse mode output			
Complementary outputs	NA		Complementary outputs with programmable dead-time (for channel 1 only)	NA
Break input	NA		Break input to put the timer output signals in the reset state or a known state	NA
Synchronization with external circuits and other timers	NA	Synchronization circuit to control the timer with external signals and to interconnect several timers together		
Repetition counter	NA		Repetition counter to update the timer registers only after a given number of cycles of the counter	NA
Interrupt generation	Interrupt generation on the following events:		Interrupt/DMA generation on the following events:	
	• Update: counter overflow, counter initialization (by software) • Input capture • Output compare	• Update: counter overflow, counter initialization (by software or internal trigger) • Trigger event (counter start, stop, initialization or count by internal trigger) • Input capture • Output compare	• Update: counter overflow, counter initialization (by software or internal/ external trigger) • Trigger event (counter start, stop, initialization or count by internal/external trigger) • Input capture • Output compare • Break input (interrupt request)	• Update: counter overflow/counter initialization (by software or internal/external trigger) • Input capture • Output compare • Trigger event (counter start, stop, initialization, or count by internal trigger)
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM).			

5.6.4 Basic timers (TIM6/7)

The basic timers TIM6 and TIM7 consist in a 16-bit auto-reload counter driven by a programmable prescaler.

These timers are completely independent, and do not share any resources.

The STM32H543/553, STM32F405/407 devices have the same basic timers features.

Table 37. Basic timers

Feature	STM32H543/553 and STM32F405/407
Counter resolution and type	16-bit auto-reload up-counter
Prescaler factor	16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
Synchronization signals	Synchronization circuit to trigger the DAC
Interrupt/DMA generation	Interrupt/DMA generation on the update event: counter overflow

5.6.5 Low-power timers (LPTIM1/2)

The LPTIM is a 16-bit timer that benefits from the ultimate developments in power-consumption reduction. This is a new feature in STM32H543/553, that is not available in STM32F405/407. The next table describes LPTIM features on STM32H543/553 devices.

Table 38. LPTIM features

Feature	STM32H543/553
LPTIMx	LPTIM1, and LPTIM2
Counter resolution and type	16 bit up-counter
Prescaler factor	3-bit prescaler with 8 possible dividing factors (1,2,4,8,16,32,64,128)
Selectable clock	• Internal clock sources: configurable internal clock source (see RCC section) • External clock source over LPTIM input (working with no LP oscillator running, used by pulse counter application)
Auto-reload	16 bit ARR auto reload register
Capture/compare	16 bit capture/compare register
Continuous mode	Continuous/one-shot mode
Trigger mode	Selectable software/hardware input trigger
Glitch filter	Programmable digital glitch filter
Configurable output	Configurable output: pulse, PWM
Polarity	Configurable I/O polarity
Encoder mode	Yes
Repetition counter	Yes
Input capture, PWM and one-pulse channels	Up to two independent channels for: • Input capture • PWM generation (Edge-aligned mode) • One-pulse mode output
DMA requests	DMA request generation on the following events: • Update event • Input capture

5.6.6 Watchdogs (WWDG/IWDG)

The STM32H543/553, and STM32F405/407 devices embed two watchdogs:

- A system window watchdog (WWDG) with same features
- An independent watchdog (IWDG) with same differences

Table 39. IDWG features

Feature	STM32F405/407	STM32H543/553
Clock	Clocked from an independent RC oscillator	• Independent clock • LSI used as IWDG kernel clock (iwdg_ker_ck)
Window option[(1)]	-	X
Early wakeup interrupt generation[(1)]	-	X
Reset generation[(1)]	X	

1. *"X" = supported, "-" = not supported.*

5.6.7 Real-time clock (RTC)

The following table describes the difference of RTC features between STM32F405/407 devices and STM32H543/553 devices. For more information about RTC, refer to the RTC section of the product reference manual.

Table 40. RTC features

RTC	STM32F405/407	STM32H543/553
Feature	Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year	
	Two programmable alarms	
	Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision	
	Timestamp function	
	Daylight saving time	
	Automatic wakeup	
	Digital calibration circuit with 0.95 ppm resolution	
	Alarm A, Alarm B, wakeup interrupt, timestamp, tamper detection	Alarm A, alarm B, wakeup Timer and timestamp individual privilege protection
	NA	• Binary mode with 32-bit free-running counter • On-the-fly correction from 1 to 32767 RTC clock pulses • RTC TrustZone® support
Tamper and backup registers	• 20x 32-bit backup registers • 2x tamper pins/ 2 events • Edge or level detection with configurable filtering	• 32x 32-bit backup registers • Up to 8 tamper pins • 13 internal tamper events • TrustZone® support

5.6.8 SysTick timer

The SysTick timer is dedicated to real-time operating systems but can also be used as a standard down-counter.

The STM32H543/553 Cortex®-M33 with TrustZone® embeds two SysTick timers. When TrustZone® is activated, the two SysTick timers are available:

- SysTick, secure instance
- SysTick, nonsecure instance

When TrustZone® is disabled, only one SysTick timer is available.

STM32F405/407 embeds a Cortex®-M4 with just one SysTick timer.

5.7 Migration of external memory interface peripherals

5.7.1 Flexible memory controller (FMC)

The following table presents the FMC interface for the STM32H543/553 devices.

Note: FSMC feature is supported by STM32F405/407 devices.

Table 41. FMC features

FMC	STM32H543/553
External memory interfaces	• SRAM • NOR Flash memory/one NAND Flash memory • PSRAM • Ferroelectric RAM (FRAM) • NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
Data bus width	8 or 16-bit

For STM32H543/553, FMC registers can be configured as secure through the TZSC controller (refer to [2] for more details).

5.7.2 Octo-SPI interface (OCTOSPI)

The OCTOSPI peripheral provides a serial interface that enables communication with external serial memories such as Flash memory, PSRAM, HyperRAM™, HyperFlash.

The Octo-SPI specialized communication interface targets single-, dual-, quad- or octal-SPI memories, and can be configured in three modes: Indirect, Status-polling and Memory-mapped.

The OCTOSPI peripheral is available on STM32H543/553, with the following features:

- Functional modes: Indirect, Automatic status-polling, and Memory-mapped
- Read and write support in Memory-mapped mode
- Dual-quad configuration
- SDR (single-data rate) and DTR (double-transfer rate)
- Data strobe (DS, DQS)
- GPDMA interface
- Dual chip select
- Prefetch disable
- Refresh counter

Note: OCTOSPI is not supported by STM32F405/407.

Revision history

Table 42. Document revision history

Date	Version	Changes
23-Jun-2026	1	Initial release.

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