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## STPMIC1L NVM configuration

### Introduction

The **STPMIC1L** is a fully integrated power management IC designed for the STM32MP1x MPU family applications requiring low power and high efficiency.

The device integrates advanced low-power features controlled by a host processor via I<sup>2</sup>C and I/O interfaces.

The **STPMIC1L** features a large input voltage range from 2.8 V to 5.5 V to supply:

- 5 V DC wall-adaptor applications
- 1-cell 3.6 V Li-ion / Li-Po battery applications

The **STPMIC1L** provides:

- 2 step-down (buck) converters with 2 MHz switching frequency in PWM mode
- 2 adjustable general-purpose LDOs
- 1 LDO for DDR3L/DDR4 termination (sink-source) or as a general-purpose LDO
- 1 LDO with a fixed output voltage of 3.3 V
- 2 GPO output controls for external command

The **STPMIC1L** regulators are designed to supply power to the application processor as well as to the external system peripherals, such as DDR, flash memories, and other system devices.

# 1 STPMIC1L NVM configuration

The STPMIC1L has a non-volatile memory (NVM) that can be (re)programmed via I<sup>2</sup>C directly in target applications to facilitate mass production, enabling scalability to support a wide range of applications. The main settings of the STPMIC1L are stored in the NVM memory:

- V<sub>IN</sub> voltage threshold
- Auto turn-on feature
- Default I<sup>2</sup>C slave device address
- Regulator default output voltages at startup
- Regulator power-up sequence at startup (rank)
- Safety management (behavior in case of failure), overcurrent protection, overtemperature protection, VIN\_low, watchdog and PONKEY fault counters
- Possibility to lock the NVM content to prevent further re-programming by writing the LOCK\_NVM bit
- Other features (see the [STPMIC1L](#) datasheet for further details)

The STPMIC1LA, STPMIC1LB and STPMIC1LD are the three standard NVM configurations that support the STM32MP13/15 family of MPU application versions with a minimum set of regulators enabled by default:

- STPMIC1LA:
  - Typical use case: 5 V continuous input voltage (wall adapter) applications
  - VDDIO at 3.3 V (LDO2 output)
- STPMIC1LB:
  - Typical use case: Li-ion/Li-Po single-cell battery applications
  - VDDIO at 1.8 V (LDO2 output)
- STPMIC1LD:
  - Typical use case: 5 V continuous input voltage (wall adapter) applications
  - VDDIO at 3.3 V (LDO2 output)
  - Additional note: This NVM version ensures compatibility with the STM32MP13 in an overdrive CPU setup. A dedicated GPO powers on an external buck converter (the [ST1S31](#)) with the proper rank to supply the DDR3L memory.

The main settings of the STPMIC1LA, STPMIC1LB and STPMIC1LD versions are listed in the table below:

**Table 1. Main settings of STPMIC1LA, STPMIC1LB and STPMIC1LD**

IP	STPMIC1LA				STPMIC1LB				STPMIC1LD			
	Voltage	Mode	Pull-down	Rank	Voltage	Mode	Pull-down	Rank	Voltage	Mode	Pull-down	Rank
BUCK1	1.22 V	HP	SLOW	2	1.22 V	HP	SLOW	2	1.25 V	HP	SLOW	2
BUCK2	OFF	OFF	FAST	0	OFF	OFF	FAST	0	1.25 V	HP	SLOW	3
LDO2	3.3 V	-	YES	1	1.8 V	-	YES	1	3.3 V	-	YES	1
LDO3	OFF	-	YES	0	OFF	-	YES	0	OFF	-	YES	0
LDO4	3.3 V	-	YES	5	3.3 V	-	YES	5	3.3 V	-	YES	5
LDO5	3.3 V	-	YES	4	2.9 V	-	YES	4	3.3 V	-	YES	4
GPO1	VIN	Active High	-	3	VIN	Active High	-	3	VIN	Active High	-	5
GPO2	OFF	Active High	-	0	OFF	Active High	-	0	OFF	Active High	-	0

The startup sequence of STPMIC1L is divided into four steps (Rank0 to Rank5).

Each buck converter, LDO regulator and GPO can be programmed to be turned ON automatically in one of these ranks. Each rank phase is separated by a delay, which is 1.5 ms by default. This rank delay can be programmed in the NVM (Reg0x91[7:6]) at 1.5 ms, 3 ms, 4.5 ms or 6 ms (RANK\_DLY[1:0]).

- Rank = 0: rail not turned ON automatically, no output voltage appears after POWER-UP sequence
- Rank = 1: rail automatically turned ON after 7 ms (which is the fixed delay from VIN > VINOK\_rise to the start of IPs with rank1), following a Turn\_ON condition
- Rank = 2: rail automatically turned ON after a further 1.5 ms compared to Rank1 output rails
- Rank = 3: rail automatically turned ON after a further 1.5 ms compared to Rank2 output rails
- Rank = 4: rail automatically turned ON after a further 1.5 ms compared to Rank3 output rails
- Rank = 5: rail automatically turned ON after a further 1.5 ms compared to Rank4 output rails

Regardless of the STPMIC1L version:

- AUTO\_TURN\_ON option is set

Table 2 shows the miscellaneous settings at startup of STPMIC1LA, STPMIC1LB and STPMIC1LD:

**Table 2. Miscellaneous settings of STPMIC1LA, STPMIC1LB and STPMIC1LD at startup**

Parameter	STPMIC1LA	STPMIC1LB	STPMIC1LD	Comments
VINOK_Rise	4.0 V	3.3 V	4.0 V	Default value of VIN_OK rising threshold
VINOK_HYST	0.5 V	0.5 V	0.5 V	Default VIN_OK hysteresis
AUTO_TURN_ON	ON	ON	ON	Auto turn-ON functionality enabled by default
RANK_DLY	1.5 ms	1.5 ms	1.5 ms	Power-up/power-down step (RANK) duration time
RST_DLY	0	0	0	RESET release delay after POWER_UP sequence
I <sup>2</sup> C ADDR	0x33	0x33	0x33	I <sup>2</sup> C device address
NVM_USER	0	0	0	2 free NVM bytes for the user

Table 3 shows the safety management and miscellaneous settings at startup of STPMIC1LA, STPMIC1LB and STPMIC1LD:

**Table 3. Safety management and miscellaneous settings of STPMIC1LA, STPMIC1LB and STPMIC1LD at startup**

Parameter	STPMIC1LA	STPMIC1LB	STPMIC1LD	Comments
NVM_WDG_EN	OFF	OFF	OFF	Watchdog is disabled by default and it can be enabled at runtime
PKEY_LKP_OFF	ON	ON	ON	A long PONKEY press produces a restart cycle of STPMIC25
PKEY_LKP_EN_FSLs	OFF	OFF	OFF	A long PONKEY press allows the STPMIC1L to skip the fail-safe lock State
PKEY_LKP_TMR	10 s	10 s	10 s	Long PONKEY press timer duration settings
HICCUP_DLY	100 ms	100 ms	100 ms	Hiccup mode OFF delay programmed by default
VIN_FLT_CNT_MAX	∞ restart	∞ restart	∞ restart	VINOK fault counter
TSHDN_FLT_CNT_MAX	∞ restart	∞ restart	∞ restart	Thermal shutdown protection fault counter
OCP_FLT_CNT_MAX	∞ restart	∞ restart	∞ restart	Overcurrent protection fault counter
WDG_FLT_CNT_MAX	∞ restart	∞ restart	∞ restart	Watchdog fault counter
PKEY_FLT_CNT_MAX	∞ restart	∞ restart	∞ restart	PONKEY fault counter
RST_FLT_CNT_TMR	60 m	60 m	60 m	Fault counter time reset
FAIL_SAFE_LOCK_DIS	Disabled	Disabled	Disabled	Fail-safe lock state is disabled by default
VIN_DLY	10 ms	10 ms	10 ms	Additional VIN delay

Parameter	STPMIC1LA	STPMIC1LB	STPMIC1LD	Comments
PKEY_EN_CFG	PONKEY	PONKEY	PONKEY	PONKEYn/EN feature configuration
NVM_PKEY_EN_PULL	pull-up active	pull-up active	pull-up active	PONKEYn/EN pad pull resistor selection

Table 4 shows the fail-safe OCP management at startup settings of STPMIC1LA, STPMIC1LB and STPMIC1LD:

**Table 4. Fail-safe OCP management settings of STPMIC1LA, STPMIC1LB and STPMIC1LD at startup**

Parameter	STPMIC1LA OCP mgt / OCP lim	STPMIC1LB OCP mgt / OCP lim	STPMIC1LD OCP mgt / OCP lim	Comments
BUCK1 (VDDCORE/ VDDCPU)	FS / 1.5 A	FS / 1.5 A	FS / 1.0 A	STPMIC1L switch-off in case OCP is triggered
BUCK2 (VDD_DDR)	FS / 1.0 A	FS / 1.0 A	FS / 1.0 A	STPMIC1L switch-off in case OCP is triggered
LDO2 (VDDIO)	FS / 400 mA	FS / 400 mA	FS / 400 mA	STPMIC1L switch-off in case OCP is triggered
LDO3 (VTT/VDD1_DDR)	FS	FS	Hiccup	
LDO4 (VDD33USB)	Hiccup	Hiccup	Hiccup	
LDO5 (VDD_FLASH)	Hiccup / 400 mA	Hiccup / 400 mA	Hiccup / 400 mA	
GPO1	-	-		
GPO2	-	-		

Table 5 shows the complete NVM shadow register map of the STPMIC1LA, STPMIC1LB and STPMIC1LD versions:

**Table 5. STPMIC1LA/B/D NVM shadow register map**

			STPMIC1LA/B/D default NVM shadow register map											
Reg (Hex)	Register Name	R/W	(1)Hex	BITS[7:0]										
				7	6	5	4	3	2	1	0			
0x90	NVM_MAIN_CTRL_SHR1	R/W		VINOK_HYST[1:0]		VINOK_RISE[1:0]		NVM_WDG_TMR_SET[1:0]		NVM_WD G_EN	AUTO_TU RNON			
			A: 0xF1	1	1	1	1	0	0	0	1			
			B: 0xD1	1	1	0	1	0	0	0	1			
			D: 0xF1	1	1	1	1	0	0	0	1			
0x91	NVM_MAIN_CTRL_SHR2	R/W		RANK_DLY[1:0]		RST_DLY[1:0]		NVM_PKEY_LKP_CON FIG	NVM_PKEY_LKP_FLSLS		NVM_PKEY_LKP_TM R[1:0]			
			A: 0x0A	0	0	0	0	1	0	1	0			
			B: 0x0A	0	0	0	0	1	0	1	0			
			D: 0x0A	0	0	0	0	1	0	1	0			
0x92	NVM_RAN K_SHR1	R/W		-	-	BUCK2_RANK[2:0]			BUCK1_RANK[2:0]					
			A: 0x02	0	0	0	0	0	0	1	0			
			B: 0x02	0	0	0	0	0	0	1	0			
			D: 0x1A	0	0	0	1	1	0	1	0			
0x96	NVM_RAN K_SHR5	R/W		-	-	LDO2_RANK[2:0]			-	-	-	-		
			A: 0x08	0	0	0	0	1	0	0	0			
			B: 0x08	0	0	0	0	1	0	0	0			
			D: 0x08	0	0	0	0	1	0	0	0			
0x97	NVM_RAN K_SHR6	R/W		-	-	LDO4_RANK[2:0]			LDO3_RANK[2:0]					
			A: 0x28	0	0	1	0	1	0	0	0			
			B: 0x28	0	0	1	0	1	0	0	0			
			D: 0x28	0	0	1	0	1	0	0	0			
0x98	NVM_RAN K_SHR7	R/W		-	-	-	-	-	LDO5_RANK[2:0]					
			A: 0x04	0	0	0	0	0	1	0	0			
			B: 0x04	0	0	0	0	0	1	0	0			
			D: 0x04	0	0	0	0	0	1	0	0			
0x9A	NVM_BUC K_MODE_SHR1	R/W		-	-	-	-	BUCK2_PREG_MODE[1:0]		BUCK1_PREG_MODE[1:0]				
			A: 0x00	0	0	0	0	0	0	0	0			
			B: 0x00	0	0	0	0	0	0	0	0			
			D: 0x00	0	0	0	0	0	0	0	0			
0x9C	NVM_BUC K1_VOUT_SHR	R/W		BUCK1_V RANGE_C FG	NVM_VOUT[6:0]									
			A: 0x48	0	1	0	0	1	0	0	0			
			B: 0x48	0	1	0	0	1	0	0	0			
			D: 0x4B	0	1	0	0	1	0	1	1			
0x9D	NVM_BUC K2_VOUT_SHR	R/W		BUCK2_IR RANGE_C FG	NVM_VOUT[6:0]									
			A: 0x00	0	0	0	0	0	0	0	0			
			B: 0x00	0	0	0	0	0	0	0	0			
			D: 0x4B	0	1	0	0	1	0	1	1			
0x9F	NVM_MAIN_CTRL_SH R3	R/W		-	-	-	-	-	-	GPO2_POL_CFG	GPO1_PO L_CFG			
			A: 0x00	0	0	0	0	0	0	0	0			
			B: 0x00	0	0	0	0	0	0	0	0			

STPMIC1LA/B/D default NVM shadow register map											
Reg (Hex)	Register Name	R/W	(1)Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0x9F	NVM_MAIN_CTRL_SHR3	R/W	D:0x00	0	0	0	0	0	0	0	0
0xA0	NVM_RANK_SHR9	R/W		-	-	GPO2_RANK[2:0]			GPO1_RANK[2:0]		
			A: 0x03	0	0	0	0	0	0	1	1
			B: 0x03	0	0	0	0	0	0	1	1
			D: 0x05	0	0	0	0	0	1	0	1
0xA3	NVM_LDO2_SHR	R/W		-	-	NVM_VOUT[4:0]				-	
			A: 0x30	0	0	1	1	0	0	0	0
			B: 0x12	0	0	0	1	0	0	1	0
			D: 0x30	0	0	1	1	0	0	0	0
0xA4	NVM_LDO3_SHR	R/W		NVM_SNK_SRC	-	NVM_VOUT[4:0]				-	
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0xA5	NVM_LDO5_SHR	R/W		-	-	NVM_VOUT[4:0]				-	
			A: 0x30	0	0	1	1	0	0	0	0
			B: 0x28	0	0	1	0	1	0	0	0
			D: 0x30	0	0	1	1	0	0	0	0
0xA9	NVM_PD_SHR1	R/W		-	-	-	-	NVM_BUCK2_PD[1:0]		NVM_BUCK1_PD[1:0]	
			A: 0x09	0	0	0	0	1	0	0	1
			B: 0x09	0	0	0	0	1	0	0	1
			D: 0x05	0	0	0	0	0	1	0	1
0xAB	NVM_PD_SHR3	R/W		-	-	-	NVM_LDO5_PD	NVM_LDO4_PD	NVM_LDO3_PD	NVM_LDO2_PD	-
			A: 0x1E	0	0	0	1	1	1	1	0
			B: 0x1E	0	0	0	1	1	1	1	0
			D: 0x1E	0	0	0	1	1	1	1	0
0xAC	NVM_BUCKS_IOUT_SHR1	R/W		-	-	-	-	BUCK2_ILIM[1:0]		BUCK1_ILIM[1:0]	
			A: 0x06	0	0	0	0	0	1	1	0
			B: 0x06	0	0	0	0	0	1	1	0
			D: 0x05	0	0	0	0	0	1	0	1
0xAD	NVM_BUCKS_IOUT_SHR2	R/W		HICCUP_DLY[1:0]		-	-	-	-	-	-
			A: 0x40	0	1	0	0	0	0	0	0
			B: 0x40	0	1	0	0	0	0	0	0
			D: 0x40	0	1	0	0	0	0	0	0
0xAE	NVM_LDO_S_IOUT_SHR	R/W		-	-	-	-	LDO5_ILIM[1:0]		LDO2_ILIM[1:0]	
			A: 0x0F	0	0	0	0	1	1	1	1
			B: 0x0F	0	0	0	0	1	1	1	1
			D: 0x0F	0	0	0	0	1	1	1	1
0xAF	NVM_FS_OCP_SHR1	R/W		-	-	-	-	-	-	NVM_FS_OCP_BUC	NVM_FS_OCP_BUC
										K2	K1
			A: 0x03	0	0	0	0	0	0	1	1
			B: 0x03	0	0	0	0	0	0	1	1
	D: 0x03	0	0	0	0	0	0	1	1		

STPMIC1LA/B/D default NVM shadow register map												
Reg (Hex)	Register Name	R/W	(1)Hex	BITS[7:0]								
				7	6	5	4	3	2	1	0	
0xB0	NVM_FS_OCP_SHR2	R/W		-	-	-		NVM_FS_OCP_LD05	NVM_FS_OCP_LD04	NVM_FS_OCP_LD03	NVM_FS_OCP_LD02	-
			A: 0x06	0	0	0	0	0	0	1	1	0
			B: 0x06	0	0	0	0	0	0	1	1	0
			D: 0x02	0	0	0	0	0	0	0	1	0
0xB1	NVM_FS_SHR1	R/W		VIN_FLT_CNT_MAX[3:0]				PKEY_FLT_CNT_MAX[3:0]				
			A: 0xFF	1	1	1	1	1	1	1	1	1
			B: 0xFF	1	1	1	1	1	1	1	1	1
			D: 0xFF	1	1	1	1	1	1	1	1	1
0xB2	NVM_FS_SHR2	R/W		TSHDN_FLT_CNT_MAX[3:0]				OCP_FLT_CNT_MAX[3:0]				
			A: 0xFF	1	1	1	1	1	1	1	1	
			B: 0xFF	1	1	1	1	1	1	1	1	
			D: 0xFF	1	1	1	1	1	1	1	1	
0xB3	NVM_FS_SHR3	R/W		-	FS_LOCK_DIS	RST_FLT_CNT_TMR[1:0]		WDG_FLT_CNT_MAX[3:0]				
			A: 0x4F	0	1	0	0	1	1	1	1	
			B: 0x4F	0	1	0	0	1	1	1	1	
			D: 0x4F	0	1	0	0	1	1	1	1	
0xB5	NVM_I2C_ADDR_SHR	R/W		LOCK_NVM			I2C_ADDR[6:0]					
			A: 0x33	0	0	1	1	0	0	1	1	
			B: 0x33	0	0	1	1	0	0	1	1	
			D: 0x33	0	0	1	1	0	0	1	1	
0xB6	NVM_USER_SHR1	R/W		NVM_USER1[7:0]								
			A: 0x00	0	0	0	0	0	0	0	0	
			B: 0x00	0	0	0	0	0	0	0	0	
			D: 0x00	0	0	0	0	0	0	0	0	
0xB7	NVM_USER_SHR2	R/W		NVM_USER2[7:0]								
			A: 0x00	0	0	0	0	0	0	0	0	
			B: 0x00	0	0	0	0	0	0	0	0	
			D: 0x00	0	0	0	0	0	0	0	0	
0xB9	NVM_MAIN_CTRL_SHR4	R/W		VIN_DLY[1:0]		-	-	NVM_PKEY_EN_PULL[1:0]		EN_POL_CFG	PKEY_EN_CFG	
			A: 0x46	0	1	0	0	0	1	1	0	
			B: 0x46	0	1	0	0	0	1	1	0	
			D: 0x46	0	1	0	0	0	1	1	0	

1. This column contains the STPMIC1L default values of the NVM content shadow register in hexadecimal format.

## Revision history

**Table 6. Document revision history**

Date	Version	Changes
24-Nov-2025	1	Initial release.

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