STPMIC1L application hints

Introduction

How to connect unused pins

In some STPMIC1L + STM32MP13x family MPU applications, not all the peripherals and functions may be required, and to minimize any possible issues and unnecessary power consumption, the relevant pins must be connected correctly.

The following tables provide guidance on how to connect unused pins of the STPMIC1L, and they are valid for all pins except VIN, VIO, and all GNDs.

Note 1: To avoid any damage to the STPMIC1L, VIN must be the first and highest input supply.

Note 2: The DC-DC converter input pins (pins #11 and #25) cannot be separated from the main input pin (pin #11).

Figure 1. Pin configuration, VFQFPN 28L (top view)

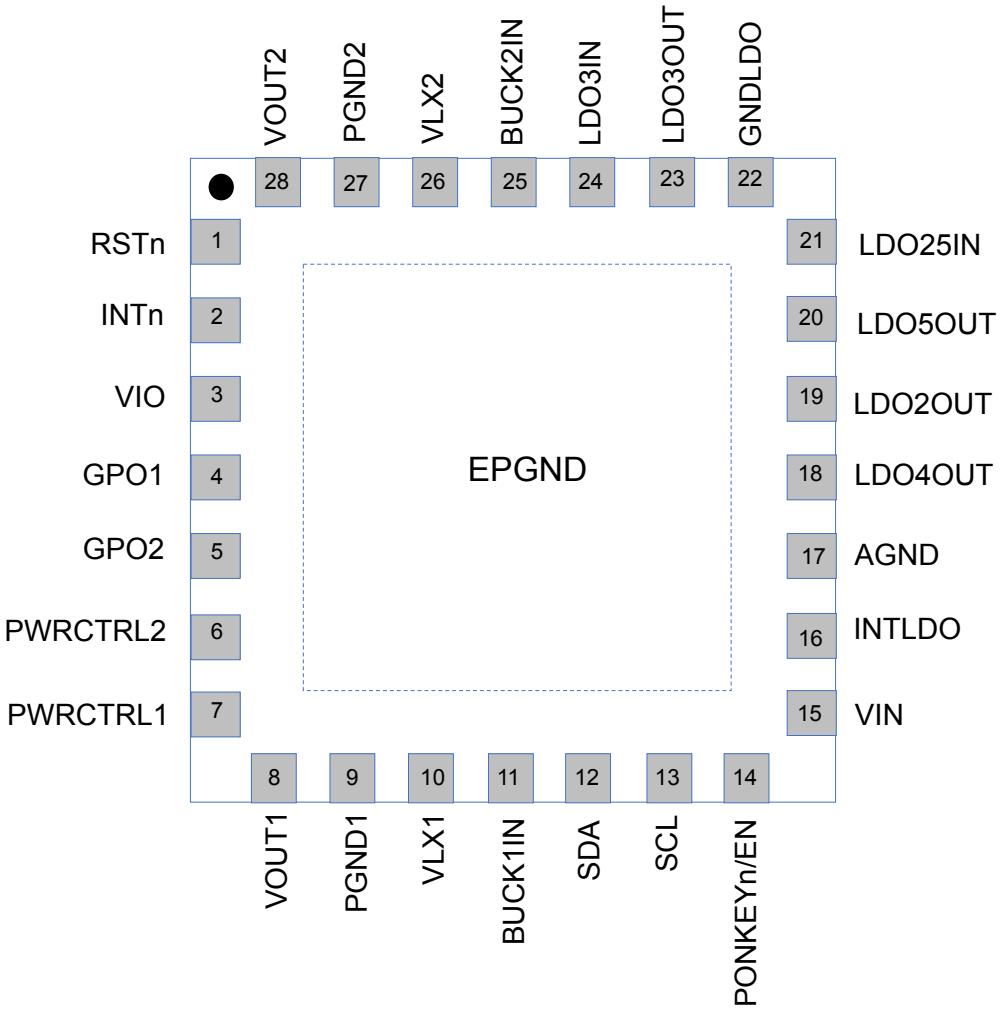

Table 1 shows the pin description of STPMIC1L and the possible configuration if they are not used in the final application:

Table 1. Pin description

Pin name	A/D [1]	I/O [1]	Location	Description (default configuration)	Unused pin connection
RSTn	D	I/O	1	Bidirectional reset (active low with internal pull-up)	Floating
INTn	D	O	2	Interrupt (active low with internal pull-up)	Floating
VIO	A	I	3	I/O voltage (for all digital signals except PONKEYn/En)	VIO
GPO1	D	O	4	External control 1	Floating
GPO2	D	O	5	External control 2	Floating
PWRCTRL2	D	I	6	Power control 2 mode (pull-up and pull-down, pull-up active by default)	VIO or floating
PWRCTRL1	D	I	7	Power control 1 mode (pull-up and pull-down, pull-up active by default)	VIO or floating
VOUT1	A	I	8	Input feedback signal buck converter 1	Floating
PGND1	A	-	9	Power ground buck converter 1	GND
VLX1	A	O	10	LX node buck converter 1	Floating
BUCK1IN	A	I	11	Power input buck converter 1	VIN
SCL	D	I	12	I²C serial clock	VIO
SDA	D	I/O	13	I²C serial data	VIO
PONKEYn/En	D	I	14	User power ON key / Enable (active low with internal pull-up by default)	Floating
VIN	A	I	15	Main power input - power input LDO4, VREF	VIN
INTLDO	A	O	16	Internal LDO	4.7 µF capacitor
AGND	A	-	17	Main analog ground	GND
LDO4OUT	A	O	18	Output voltage LDO4	Floating
LDO2OUT	A	O	19	Output voltage LDO2	Floating
LDO5OUT	A	O	20	Output voltage LDO5	Floating
LDO25IN	A	I	21	Power input LDO2 and LDO5	VIN
GNDLDO	A	-	22	LDO GND	GND
LDO3OUT	A	O	23	Output voltage LDO3	VIN
LDO3IN	A	I	24	Power input LDO3	VIN
BUCK2IN	A	I	25	Power input buck converter 2	VIN
VLX2	A	O	26	LX node buck converter 2	Floating
PGND2	A	-	27	Power ground buck converter 2	GND
VOUT2	A	I	28	Input feedback signal buck converter 2	Floating
EPGND	A	-	ePad	Exposed pad to be connected to ground	GND

1. A: analog; D: digital; I/O: input/Output

If the passive components (inductors, capacitors) of the unused LDOs and buck converters are not mounted (for cost constraints, to reduce the occupied area around the STPMIC1L, etc.), it is mandatory to disable these IPs by setting their respective ranks to 0 in the NVM. This avoids any possible oscillation or saturation of the internal circuitry, and ensures that, at each power-on cycle, the unused IPs are not automatically turned on.

1 STPMIC1L NVM configuration

The table below shows the default NVM content shadow register map of the STPMIC1LA, STPMIC1LB, and STPMIC1LD versions.

Table 2. NVM shadow register map

			STPMIC1LA/B/D default NVM shadow register map									
Reg (Hex)	Register Name	R/W	(1) Hex	BITS[7:0]								
				7	6	5	4	3	2	1	0	
0x90	NVM_MAIN_CTRL_SHR1	R/W		VINOK_HYST[1:0]		VINOK_RISE[1:0]		NVM_WDG_TMR_SET[1:0]		NVM_WD G_EN	AUTO_TU RNON	
			A: 0xF1	1	1	1	1	0	0	0	1	
			B: 0xD1	1	1	0	1	0	0	0	1	
			D: 0xF1	1	1	1	1	0	0	0	1	
0x91	NVM_MAIN_CTRL_SHR2	R/W		RANK_DLY[1:0]		RST_DLY[1:0]		NVM_PKEY_ LKP_CON FIG	NVM_PKEY_ LKP_FSLS	NVM_PKEY_LKP_TM R[1:0]		
			A: 0x0A	0	0	0	0	1	0	1	0	
			B: 0x0A	0	0	0	0	1	0	1	0	
			D: 0x0A	0	0	0	0	1	0	1	0	
0x92	NVM_RAN K_SHR1	R/W		-	-	BUCK2_RANK[2:0]			BUCK1_RANK[2:0]			
			A: 0x02	0	0	0	0	0	0	1	0	
			B: 0x02	0	0	0	0	0	0	1	0	
			D: 0x1A	0	0	0	1	1	0	1	0	
0x96	NVM_RAN K_SHR5	R/W		-	-	LDO2_RANK[2:0]			-	-	-	
			A: 0x08	0	0	0	0	1	0	0	0	
			B: 0x08	0	0	0	0	1	0	0	0	
			D: 0x08	0	0	0	0	1	0	0	0	
0x97	NVM_RAN K_SHR6	R/W		-	-	LDO4_RANK[2:0]			LDO3_RANK[2:0]			
			A: 0x28	0	0	1	0	1	0	0	0	
			B: 0x28	0	0	1	0	1	0	0	0	
			D: 0x28	0	0	1	0	1	0	0	0	
0x98	NVM_RAN K_SHR7	R/W		-	-	-	-	-	LDO5_RANK[2:0]			
			A: 0x04	0	0	0	0	0	1	0	0	
			B: 0x04	0	0	0	0	0	1	0	0	
			D: 0x04	0	0	0	0	0	1	0	0	
0x9A	NVM_BUC K_MODE_SHR1	R/W		-	-	-	-	BUCK2_PREG_MODE[1:0]		BUCK1_PREG_MODE[1:0]		
			A: 0x00	0	0	0	0	0	0	0	0	

			STPMIC1LA/B/D default NVM shadow register map								
Reg (Hex)	Register Name	R/W	(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0x9A	NVM_BUCK_MODE_SHR1	R/W	B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0x9C	NVM_BUCK1_VOUT_SHR	R/W		BUCK1_VRANGE_CFG	NVM_VOUT[6:0]						
			A: 0x48	0	1	0	0	1	0	0	0
			B: 0x48	0	1	0	0	1	0	0	0
			D: 0x4B	0	1	0	0	1	0	1	1
0x9D	NVM_BUCK2_VOUT_SHR	R/W		BUCK2_IRANGE_CF G	NVM_VOUT[6:0]						
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x4B	0	1	0	0	1	0	1	1
0x9F	NVM_MAIN_CTRL_SHR3	R/W		-	-	-	-	-	-	GPO2_POL_CFG	GPO1_POL_CFG
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0xA0	NVM_RANK_SHR9	R/W		-	-	GPO2_RANK[2:0]			GPO1_RANK[2:0]		
			A: 0x03	0	0	0	0	0	0	1	1
			B: 0x03	0	0	0	0	0	0	1	1
			D: 0x05	0	0	0	0	0	1	0	1
0xA3	NVM_LDO2_SHR	R/W		-	-	NVM_VOUT[4:0]					-
			A: 0x30	0	0	1	1	0	0	0	0
			B: 0x12	0	0	0	1	0	0	1	0
			D: 0x30	0	0	1	1	0	0	0	0
0xA4	NVM_LDO3_SHR	R/W		NVM_SNK_SRC	-	NVM_VOUT[4:0]					-
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0xA5	NVM_LDO5_SHR	R/W		-	-	NVM_VOUT[4:0]					-
			A: 0x30	0	0	1	1	0	0	0	0
			B: 0x28	0	0	1	0	1	0	0	0

STPMIC1LA/B/D default NVM shadow register map											
Reg (Hex)	Register Name	R/W	(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0xA5	NVM_LDO5_SHR	R/W	D: 0x30	0	0	1	1	0	0	0	0
0xA9	NVM_PD_S HR1	R/W		-	-	-	-	NVM_BUCK2_PD[1:0]		NVM_BUCK1_PD[1:0]	
			A: 0x09	0	0	0	0	1	0	0	1
			B: 0x09	0	0	0	0	1	0	0	1
			D: 0x05	0	0	0	0	0	1	0	1
0xAB	NVM_PD_S HR3	R/W		-	-	-	NVM_LDO5_PD	NVM_LDO4_PD	NVM_LDO3_PD	NVM_LDO2_PD	-
			A: 0x1E	0	0	0	1	1	1	1	0
			B: 0x1E	0	0	0	1	1	1	1	0
			D: 0x1E	0	0	0	1	1	1	1	0
0xAC	NVM_BUC KS_IOUT_SHR1	R/W		-	-	-	-	BUCK2_ILIM[1:0]		BUCK1_ILIM[1:0]	
			A: 0x06	0	0	0	0	0	1	1	0
			B: 0x06	0	0	0	0	0	1	1	0
			D: 0x05	0	0	0	0	0	1	0	1
0xAD	NVM_BUC KS_IOUT_SHR2	R/W		HICCUP_DLY[1:0]		-	-	-	-	-	-
			A: 0x40	0	1	0	0	0	0	0	0
			B: 0x40	0	1	0	0	0	0	0	0
			D: 0x40	0	1	0	0	0	0	0	0
0xAE	NVM_LDO S_IOUT_SHR	R/W		-	-	-	-	LDO5_ILIM[1:0]		LDO2_ILIM[1:0]	
			A: 0x0F	0	0	0	0	1	1	1	1
			B: 0x0F	0	0	0	0	1	1	1	1
			D: 0x0F	0	0	0	0	1	1	1	1
0xAF	NVM_FS_O CP_SHR1	R/W			-	-	-	-	-	NVM_FS_OCP_BUC K2	NVM_FS_OCP_BUC K1
			A: 0x03	0	0		0	0	0	1	1
			B: 0x03	0	0		0	0	0	1	1
			D: 0x03	0	0		0	0	0	1	1
0xB0	NVM_FS_O CP_SHR2	R/W		-	-		-	NVM_FS_OCP_LD O5	NVM_FS_OCP_LDO4	NVM_FS_OCP_LDO 3	NVM_FS_OCP_LDO2	-
			A: 0x06	0	0		0	0	0	1	1	0
			B: 0x06	0	0		0	0	0	1	1	0
			D: 0x02	0	0		0	0	0	1	1	0

			STPMIC1LA/B/D default NVM shadow register map								
Reg (Hex)	Register Name	R/W	(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0xB1	NVM_FS_S HR1	R/W		VIN_FLT_CNT_MAX[3:0]				PKEY_FLT_CNT_MAX[3:0]			
			A: 0xFF	1	1		1	1	1	1	1
			B: 0xFF	1	1		1	1	1	1	1
			D: 0xFF	1	1		1	1	1	1	1
0xB2	NVM_FS_S HR2	R/W		TSHDN_FLT_CNT_MAX[3:0]				OCP_FLT_CNT_MAX[3:0]			
			A: 0xFF	1		1	1	1	1	1	1
			B: 0xFF	1		1	1	1	1	1	1
			D: 0xFF	1		1	1	1	1	1	1
0xB3	NVM_FS_S HR3	R/W		-		FS_LOCK_DIS	RST_FLT_CNT_T MR[1:0]	WDG_FLT_CNT_MAX[3:0]			
			A: 0x4F	0		1	0	0	1	1	1	1
			B: 0x4F	0		1	0	0	1	1	1	1
			D: 0x4F	0		1	0	0	1	1	1	1
0xB5	NVM_I²C_A DDR_SHR	R/W		LOCK_NVM		I2C_ADDR[6:0]					
			A: 0x33	0		0	1	1	0	0	1	1
			B: 0x33	0		0	1	1	0	0	1	1
			D: 0x33	0		0	1	1	0	0	1	1
0xB6	NVM_USE R_SHR1	R/W		NVM_USER1[7:0]							
			A: 0x00	0	0		0	0	0	0	0	0
			B: 0x00	0	0		0	0	0	0	0	0
			D: 0x00	0	0		0	0	0	0	0	0
0xB7	NVM_USE R_SHR2	R/W		NVM_USER2[7:0]							
			A: 0x00	0	0		0	0	0	0	0	0
			B: 0x00	0	0		0	0	0	0	0	0
			D: 0x00	0	0		0	0	0	0	0	0
0xB9	NVM_MAIN_CTRL_SHR4	R/W		VIN_DLY[1:0]			-	-	NVM_PKEY_EN_PULL[1:0]	EN_POL_C FG	PKEY_EN_CFG	
			A: 0x46	0	1		0	0	0	1	1	0
			B: 0x46	0	1		0	0	0	1	1	0
			D: 0x46	0	1		0	0	0	1	1	0

1. *This column contains the STPMIC1L default values of the NVM content shadow register in hexadecimal format.*

Revision history

Table 3. **Document revision history**

Date	Version	Changes
03-Dec-2025	1	Initial release.

Contents

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