Non-volatile Memory (NVM) feature of L99SP08

Introduction

This document is an application note about the L99SP08 smart octal P-channel for ultra-low current consumption automotive systems.

The aim of the document is to describe how to deal with non-volatile memory (NVM) customer programming.

Typical application diagrams for 3.3 V and 5.0 V applications are reported in the datasheet of L99SP08 (see DS14248).

All tests were conducted on a typical sample representative of the standard population.

1 System Overview

1.1 Device Description

The L99SP08 Smart P-channel is an octal-channel device made using STMicroelectronics BCD9sL technology, housed in a small QFN 5x5x0.9 mm 32+4L wettable-flanks package. It is designed to support standby-on functionality when interacting with hybrid and monolithic STi²Fuse product family, as well as to drive loads in standalone mode, up to I_{OUTX} DC current per channel.

By integrating a deep standby mode, the device fulfills highly stringent requirements for all always-active battery lines, providing ultra-low current consumption with the car in parking mode. Real-time diagnostics are available through the SPI bus (communication error, oscillator stuck, over-temperature, VCC, and VOUT monitoring). In case of over-temperature, VDS over-voltage, or I_{PEAK} triggering, the device sets the EN pin high, allowing the turn-on of external devices such as STi²Fuse hybrid and monolithic devices.

Built-in self-tests (BIST) are integrated to check the correct behavior of the device during its working life, allowing customer on-demand activation and testing of the current ADC, voltage ADC, standby-on current sense chain, and P-channel stuck-on protection.

The device is also equipped with a non-volatile memory (NVM) to allow the customer to set current thresholds (I_{THRx}) parameters, managing the standby-on exit strategy.

1.2 Block diagram and pin description

Figure 1. Block diagram

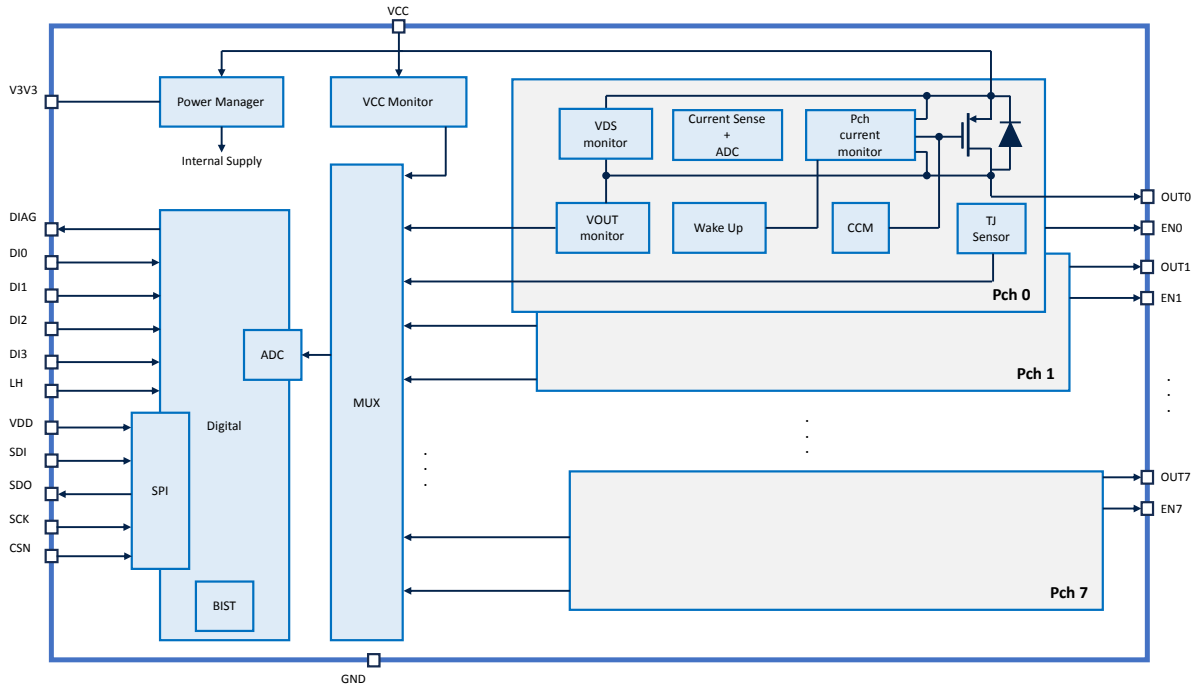
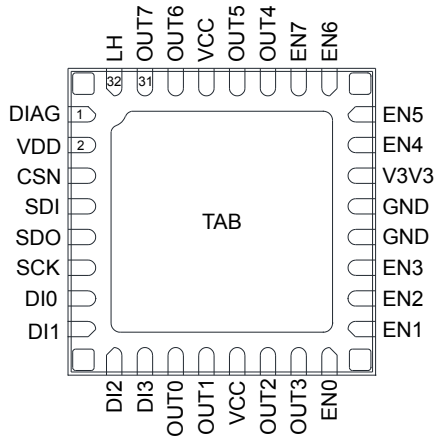


Figure 2. Configuration diagram (top through view)



Note: TAB connection must be connected to the ground. TAB is not intended as the device reference ground (a dedicated pin shall be used).

Table 1. Pin functions

Pin#	Name	Function
1	DIAG	Open drain logic output, active low. Diagnostic feedback
2	VDD	DC supply input for the SPI interface. 3.3 V and 5 V compatible
3	CSN	Chip select not (active low) for SPI communication. It is the selection pin of the device. CMOS compatible input
4	SDI	Serial data input for SPI communication. Data is transferred serially into the device on SCK rising edge
5	SDO	Serial data output for SPI communication. Data is transferred serially out of the device on SCK falling edge
6	SCK	Serial clock for SPI communication. It is a CMOS compatible input
7, 8, 9, 10	DI_x	4 direct inputs for fail-safe operation
11, 12, 14, 15, 27, 28, 30, 31	OUT_x	8 output pins (1 per channel)
13, 29	VCC	Input supply pin. Connect to the 12 V battery voltage
16, 17, 18, 19, 23, 24, 25, 26	EN_x	Open drain logic outputs, active high. 8 enable pins (1 per channel)
20, 21	GND	Ground connection.
22	V3V3	Output of the 3.3 V internal LDO voltage regulator (logic and I/O supply) Connect a low ESR capacitor (1 µF) close to this pin
32	LH	Active high input pin compatible with 3 V and 5 V CMOS; it activates limp-home mode
	TAB	Pin connected to internal ground through high resistive path. To be connect to GND

2 Non-volatile memory (NVM) customer programming

The L99SP08 is equipped with a 2-kbit EEPROM, also used to store device configuration data. The device can work on its own (without a microcontroller) because its NVM (non-volatile memory) can be fully configured using the FTPs (few times programmable) procedure described in this document with some simple operative examples.

The NVM is arranged in 15 rows (from ROW 0 to ROW 14), with 16 bytes for each row. Only ROW 0 is available for customer configuration. The remaining 14 rows are for STMicroelectronics restricted use. Table 2 reports the 16 bytes of ROW 0 and the name of the RAM registers where the corresponding information is available.

Table 2. Customer data map (ROW 0 of NVM) and corresponding RAM registers (NVMD0 to NVMD7)

Reg name	Byte#	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
NVMD0	Byte0	WrCount [7:0]							
	Byte1	DITH_STEP[2:0]			WD_TIME		DEEP_STANDBY_DIS	WrCount [9:8]	
NVMD1	Byte2	I_{OUT} threshold [5:0]						EMPTY	
	Byte3	I_{OUT} threshold [13:6]							
NVMD2	Byte4	ENCTRL_STDBY [3:0]				I_{OUT} threshold [15:14]		EMPTY	
	Byte5	OUT_CTRL [7:0]							
NVMD3	Byte6	ENCTRL_STDBY [7:4]				EN_CONF_STDBY	EMPTY		
	Byte7	TMAX [7:0]							
NVMD4	Byte8	ENCTRL [3:0]				DIS_CONF_FS	DIS_CONF_OUT_FS	EMPTY	
	Byte9	DIN Mask [7:0]							
NVMD5	Byte10	ENCTRL [7:4]				EMPTY			
	Byte11	DIN Mask [15:8]							
NVMD6	Byte12	EMPTY							
	Byte13	OUTCTRL_FS [7:0]							
NVMD7	Byte14	EMPTY							
	Byte15	CRC							

For the registers corresponding to the bytes defined in the previous table, please refer to the device datasheet (DS14248), from section "*NVM CTM/ST programming–data0 (byte1 and byte0) (NVMD0)*" to section "*NVM CTM/ST programming–data7 (byte15 and byte14) (NVMD7)*".

The NVM can be programmed via the SPI interface by a dedicated FTP (few times programmable) procedure. This procedure is described in the chapter *NVM FTP programming mode* in the datasheet DS14248. In general, the procedure to access to the NVM differs if write or read operation is necessary. For the NVM configuration, the write operation must be followed, consisting of sending via SPI a set of commands with key words that enable access to the NVM, followed by the addresses and data of the NVMDx of interest, and then sending the final exit key to confirm the NVM upload with the data in the NVMDx registers.

The number of write cycles is limited by the datasheet parameter NFTP, and it is automatically updated by the device itself and stored in the WrCount field (9 bits field, split between byte 0 and byte 1 of ROW 0). The same value can be read from the WR_COUNT[9:0] field in the NVMD0 register (address 0x61).

The CRC field in the customer data map is used to read the 15th byte when a read operation is requested, while it is not required for a write operation (since the CRC will be automatically calculated and written into the NVM by the device itself, using the polynomial is 0x7, that is, x^2 + x + 1).

The registers allocated for NVM read and write operations are mapped to addresses above 0x40. Therefore, it is necessary to perform a page switch, which can be achieved by modifying the CURR_PAGE field (bit 2) of the register CR0–PAGECR (address 0x00).

The default value of the CURR_PAGE bit is set to 0b, in this way, at the switch-on, the device is set to address page “0”.

To move to page “1”, to address a register between 0x40 and 0x7F, a dedicated write operation on register 0x00 is required to set the CURR_PAGE bit to 1b.

3 NVM write operation

The NVM writing can be performed in Normal mode or in Fail-safe mode through SPI frames.
The steps for programming/write execution are the following:

1. Enter in Fail-safe or Normal mode
2. Write the CTM first key word 0xF5AE to address 0x39
3. Write the CTM second key word 0x0A51 to address 0x39
4. Move from page 0 to page 1 by writing the CURR_PAGE bit to 1b to address 0x00
5. Write data to store in the NVM to registers from NVMD0 to NVMD7
6. Write NVM OP_REG = 1011b and NVMADDR = 0000b to register NVMCMD (0x60 → 0x20 in page 1)
7. Wait for about 10 ms, time needed to write NVM
8. Write the CTM exit key word 0xBAC0 to address 0x39
9. Move from page 1 to page 0 by writing the CURR_PAGE bit to 0b to address 0x00

Example:
Let us suppose the following scenario:

- R_{LOAD} on OUT_0 is 47 Ω
- OUT_0 is enabled in Fail-safe mode (OUTCTRL_FS0 = 1b [bit 8] to register 0x67 that is 0x27 in page 1)
- I_THR0 = 00b (100 mA)

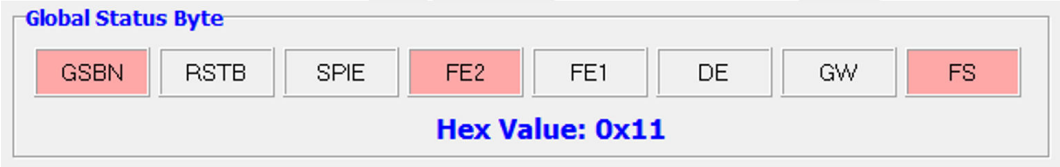
Environment setup:

- Temp = Ambient
- Device in Normal mode
- V_{BATT} = 13 V

Execution:
In this scenario, upon transitioning from Normal mode to Fail-safe mode, OUT_0 is activated due to the bit OUTCTRL_FS0 = 1b (bit 8 of register 0x67 that is 0x27 in page 1) in the NVM. However, a 47 Ω resistor is present on OUT_0, resulting in a current of approximately 260 mA, which exceeds the I_{OUT} threshold of channel 0 (100 mA). So, after the state transition, the I_{THR} protection is triggered and consequently the OUT_0 is shut down, as shown in Figure 3.
After the SPI frame for the state transition from Normal to Fail-safe (labeled as 0x010000, which writes 0x0000 to the CR1–CTRLR1 register at address 0x01), the OUT_0 remains in a high state for approximately 134 µs before shutting down, as expected due to the trigger of the I_{THR} fault flag.
The global status byte (GSB) changes from 0x80 (indicating the device is in Normal mode) to 0x11 (indicating with FE2 = 1b the output current threshold violation, and the Fail-state operation by FS bit = 1b).

Figure 3. **Device state transition (Normal to Fail-safe mode) and OUT_0 shut-down**

Figure 4. **GSB fault**



To prevent the channel from shutting down during the transition from Normal mode to Fail-safe mode, it is necessary to set the output current threshold of channel 0 above 260 mA.

The example below shows the frames to be sent sequentially to write an I_{THR} threshold at 300 mA in the NVM (as previously listed):

- Write the CTM first key word 0xF5AE to address 0x39

OP		ADDRESS						Data Byte 1								Data Byte 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	1	1	1	1	1	0	1	0	1	1	0	1	0	1	1	1	0

- Write the CTM second key word 0x0A51 to address 0x39

OP		ADDRESS						Data Byte 1								Data Byte 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	1	0	0	0	0	1	0	1	0	0	1	0	1	0	0	0	1

- Move from page 0 to page 1 by writing the CURR_PAGE bit to 1b in the CR0–PAGECR1/2 register (address 0x00). So, the corresponding frame to write is 0x000004.

OP		ADDRESS						Data Byte 1								Data Byte 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	P

- Set output current threshold of channel 0 to 300 mA. The frame to send is 0x220004.
Setting the output current threshold to 300 mA for channel 0 requires setting 10b (0x04) in the I_THR0 field of the NVMD1 register. The address of the NVMD1 register is 0x62, which corresponds to address 0x22 of page 1 (already set by the previous SPI command).

OP		ADDRESS						Data Byte 1								Data Byte 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	P

- The operation (read or write) in the NVM is specified by setting the OP_REG four-bit field in the NVMCM register. Send the frame 0x200B01 to set the write operation (OP_REG = 1011b) in the NVMCMD register (address 60h, which corresponds to address 20 on page 1).

OP		ADDRESS						Data Byte 1								Data Byte 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	P

- Write the CTM exit key word 0xBAC0 on address 0x39.

OP		ADDRESS						Data Byte 1								Data Byte 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	1	1	0	1	1	1	0	1	0	1	1	0	0	0	0	0	0

- Move back to page 1 by writing the CURR_PAGE bit to 0b in the CR0–PAGECR1/2 register (address 0x00). So, the corresponding frame to write is all zeros except for the LSB, which is 1b due to the parity bit toggling.

OP		ADDRESS						Data Byte 1								Data Byte 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P

Note: Bit0 (P) must be set according to the relevant microcontroller task for parity bit check.

The NVM writing steps are defined in Figure 5 (the SDI message is in pink and the SDO message is in blue):

Figure 5. NVM write: SPI log

Index	Time	Protocol	Message	
1	-41.398 µs	SPI	0x39f5ae	1st CTM key word
2	-41.398 µs	SPI	0x800000	
3	83.642 µs	SPI	0x390a51	2nd CTM key word
4	83.642 µs	SPI	0x800000	
5	198.202 µs	SPI	0x000004	Frame to move from page 0 to page 1 by writing CURR_PAGE bit to 1
6	198.202 µs	SPI	0x800000	
7	315.692 µs	SPI	0x220008	Write an IOUT threshold of 300 mA for channel 0 in the NVMD1 register at address 0x22h
8	315.692 µs	SPI	0x800000	
9	441.002 µs	SPI	0x200b01	Write NVM OP_REG=1011 and NVMADDR=0000 in register NVMCMD (0x20h) to write NVM
10	441.002 µs	SPI	0x800000	
11	553.392 µs	SPI	0x39bac0	Write the CTM exit key word
12	553.392 µs	SPI	0x800000	
13	668.182 µs	SPI	0x000001	Move from page 1 to page 0 by writing CURR_PAGE bit to 0
14	668.182 µs	SPI	0x800005	

After programming the output current threshold to 300 mA for channel 0 within the NVM, OUT_0 does not shut down and remains active upon transitioning from Normal mode to Fail-safe mode as shown in Figure 6. In this case, the GSB moves from 0x80 to 0x01 confirming the transition from Normal to Fail-safe mode without any other flagged bits.

Figure 6. Device state transition (Normal to Fail-safe mode) without OUT_0 shut-down

4 NVM read operation

The NVM reading can be performed in Normal mode or in Fail-safe mode through SPI frames.
The steps for direct read execution are the following:

1. Enter in Fail-safe or Normal mode
2. Write the CTM first key word 0xF5AE to address 0x39
3. Write the CTM second key word 0x0A51 to address 0x39
4. Move from page 0 to page 1 by writing the CURR_PAGE bit to 1b to address 0x00
5. Write NVM OP_REG = 1010b and NVMADDR = 0000b in register NVMCMD (0x60 → 0x20 in page 1)
6. Wait for about 30 µs, then read the NVM Sector0 data to registers from NVMD0 to NVMD7
7. Write the CTM exit key word 0xBAC0 to address 0x39
8. Move from page 1 to page 0 by writing the CURR_PAGE bit to 0b to address 0x00

Example:
Let us suppose that the following fields were previously written in the NVM:

- I_THR0 (bits [3:2] at address 0x62 that is 0x22 in page 1) set to 300 mA (I_THR0 = 10b)
- I_THR7 (bits [3:2] at address 0x63 that is 0x23 in page 1) set to 200 mA (I_THR7 = 01b)
- OUTCTRL_FS0 (bit 8 at address 0x67 that is 0x27 in page 1) set to 1b.

Environment setup:

- Temp = Ambient
- Device in Normal mode
- V_{BATT} = 13 V

Execution:
Frames to be sent sequentially to perform NVM reading (as previously listed):

- Write the CTM first key word 0xF5AE on address 0x39.

OP		ADDRESS						Data Byte 1								Data Byte 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	1	1	1	1	1	0	1	0	1	1	0	1	0	1	1	1	0

- Write the CTM second key word 0x0A51 on address 0x39.

OP		ADDRESS						Data Byte 1								Data Byte 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	1	0	0	0	0	1	0	1	0	0	1	0	1	0	0	0	1

- Move from page 0 to page 1 by writing the CURR_PAGE bit to 1b in the CR0–PAGECR1/2 register (address 0x00). So, the corresponding frame to write is 0x000004.

OP		ADDRESS						Data Byte 1								Data Byte 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	P

- Write NVM OP_REG = 1010b (read) and NVMADDR = 0000b to register NVMCMD (0x20) writing 0x200A00.

OP		ADDRESS						Data Byte 1								Data Byte 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	P

- Write the CTM exit key word 0xBAC0 to address 0x39.

OP		ADDRESS						Data Byte 1								Data Byte 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	1	1	0	1	1	1	0	1	0	1	1	0	0	0	0	0	0

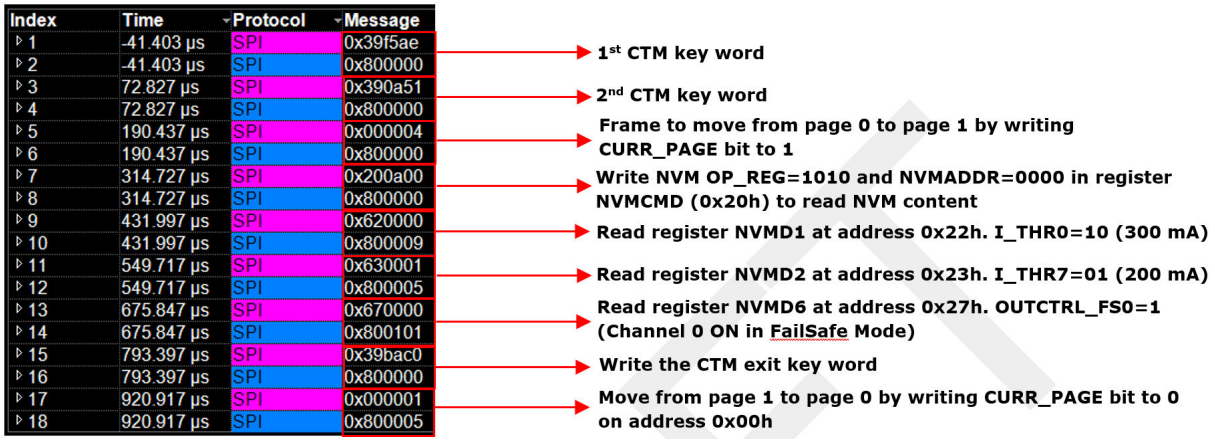
- Move from page 1 to page 0 by writing the CURR_PAGE bit as 0b at address 0x00, and so writing 0x000001 (all zeroes except LSB = 1b for parity bit toggling).

OP		ADDRESS						Data Byte 1								Data Byte 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P

Note: Bit0 (P) must be set according to the relevant microcontroller task for parity bit check.

The NVM reading steps are defined in Figure 7 (the SDI message is in pink and the SDO message is in blue):

Figure 7. NVM read: SPI log



Revision history

Table 3. **Document revision history**

Date	Revision	Changes
08-Jan-2026	1	First release.

Contents

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