AN6476

Application note

# Circuit guidelines for multiple STi²Fuse and M0-9 devices sharing a common SPI bus

## Introduction

Multiple high-side driver devices are typically used in automotive power distribution units (PDUs), which manage the distribution of electrical power within the vehicle. Different combinations of M0-9 HSDs (High-Side drivers) and STi2Fuse devices can be used to supply various electronic subsystems and loads, including control units, sensors, actuators, lighting, and infotainment systems.

This document presents different combinations of the STi2Fuse family devices and standard SPI high-side drivers to support system design.

# 1 M0-9 SPI standard circuit

**Case description:** Only M0-9 SPI standard devices share the same SPI bus(1).

**Conditions:**

- One SPI bus per KL30_x supply line.
- SDI serial resistor: N × 2.2 kΩ
- CLK serial resistor: N × 2.2 kΩ

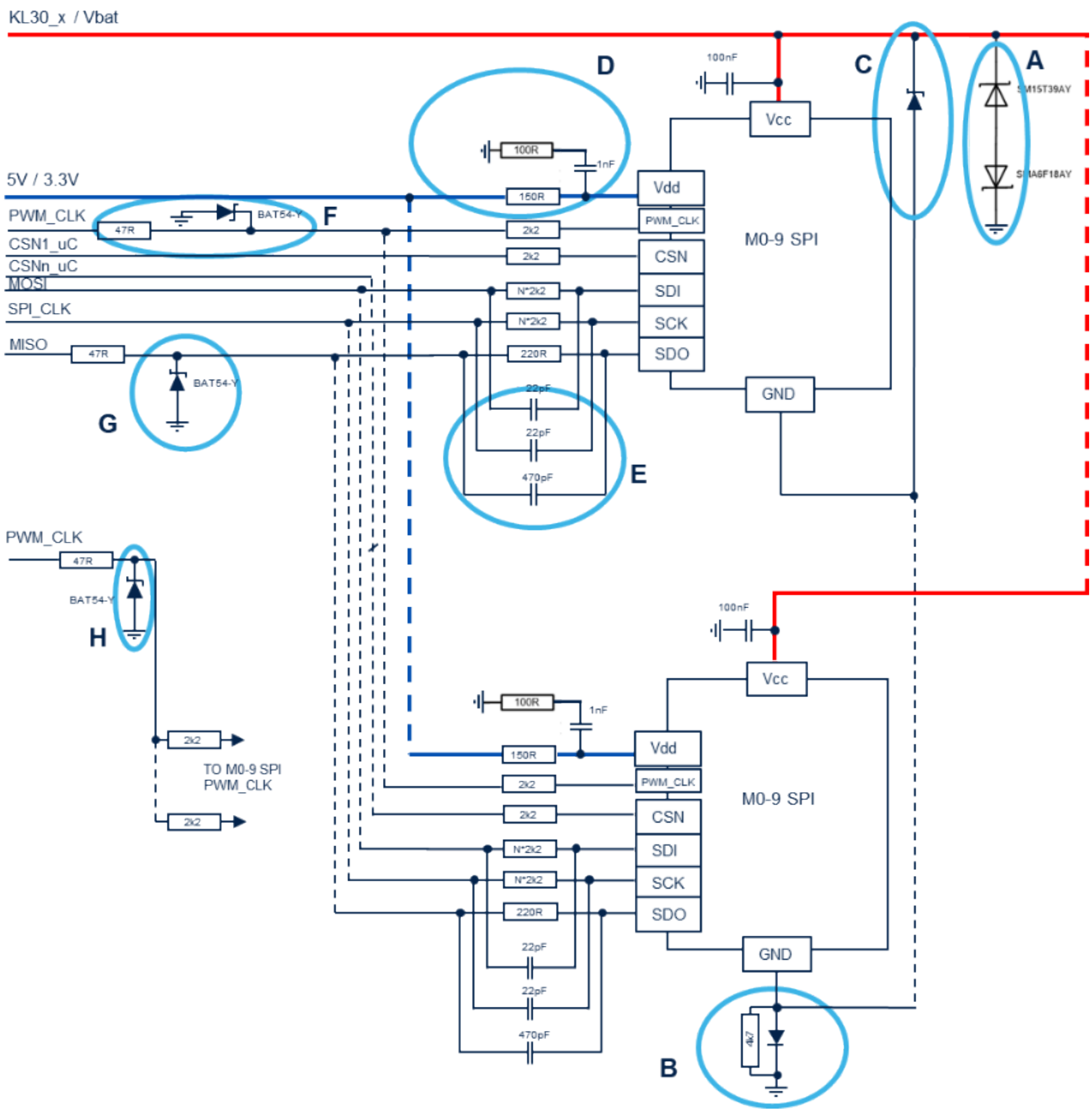
Where N is the number of devices on the SPI bus.

To limit reverse-battery current into the MCU and ensure compliance with pulse 1, as defined in ISO 7637-2:2011, the equivalent resistance of the parallel network, as seen from the MCU pin, shall not be lower than 2.2 kΩ (see UM3631).

To support higher SPI operating frequency, the following speed-up capacitors are recommended:

- SDI and SCK speed-up capacitor: 22 pF
- SDO speed-up capacitor: 470 pF

**Figure 1.** ***Schematic of M0-9 SPI standard devices sharing the same SPI bus(2).***



*Note:*
1. *This case has been validated with no more than 10 devices and an ST SPC582B family MCU.*
2. *DIx and output pins are not shown for simplicity. For the Dix Rprot value calculations, refer to the application schematic in UM3631.*

**Circuit blocks description**

**A:**

SM6F18AY clamp for ISO 7637-2 pulse 1 transients.

SMA6T33AY clamp for ISO 7637-2 pulse 2a transients.

**B:**

Reverse-battery protection network for a single device: BAS21 with 4.7 kΩ for $V_{DD}$ = 5 V, BAT54-Y with 4.7 kΩ for $V_{DD}$ = 3.3 VV.

For multiple devices, this diode can be shared with other devices of the same family on the same power supply.

The Schottky diode shall provide a forward voltage lower than 0.35 V at -40°C under the total flowing current, which is approximately 6.5 mA per device, to guarantee $V_{DD} \geq 2.7$ V under all operating conditions.

If this requirement cannot be met with a diode, a MOSFET-based solution or another equivalent protection solution shall be used.

**C:**

STPS1L40-Y diode to prevent the internal parasitic NPN transistor from being triggered during ISO 7637-2 pulse 1 transients, preserving RAM register content.

**D:**

1 nF capacitor in series with 100 Ω, one per device.

The capacitor acts as a current source to charge the MISO bus capacitance and is required for larger bus capacitances, typically above four devices on the bus.

The 100 Ω resistor is required to limit the injected current during the ISO 7637-2 test.

**E:**

Optional speed-up capacitors are used to maximize the SPI frequency.

**F:**

Diode and 47 Ω resistor for MCU pin protection, used only for N > 1.

**G:**

For N > 5, it is recommended to size the diode so that it can support the total forward DC current ($I_{D\_SDO\_total}$) of the SDO path, according to:

$I_{D\_SDO\_total}$ = -N × (12 V - 0.5 V) / 220 Ω = -N × 52 mA, during reverse-battery conditions.

**H:**

Diode and 47 Ω MCU protection network to prevent the current on the microcontroller pin from reaching the absolute maximum rating (AMR). Assuming a typical GPIO AMR of approximately 10 mA, this network shall be considered only for N > 4, as the reverse current to the PWM_CLK pin is approximately 2.3 mA max per device at VBAT = -14 V.

# 2 STi2Fuse  monolithic circuit

**Case description:** Only STi2Fuse  monolithic devices share the same SPI bus [1].

**Conditions:**

- One SPI bus per KL30_x supply line.
- SDI serial resistor: N × 2.2 kΩ
- CLK serial resistor: N × 2.2 kΩ

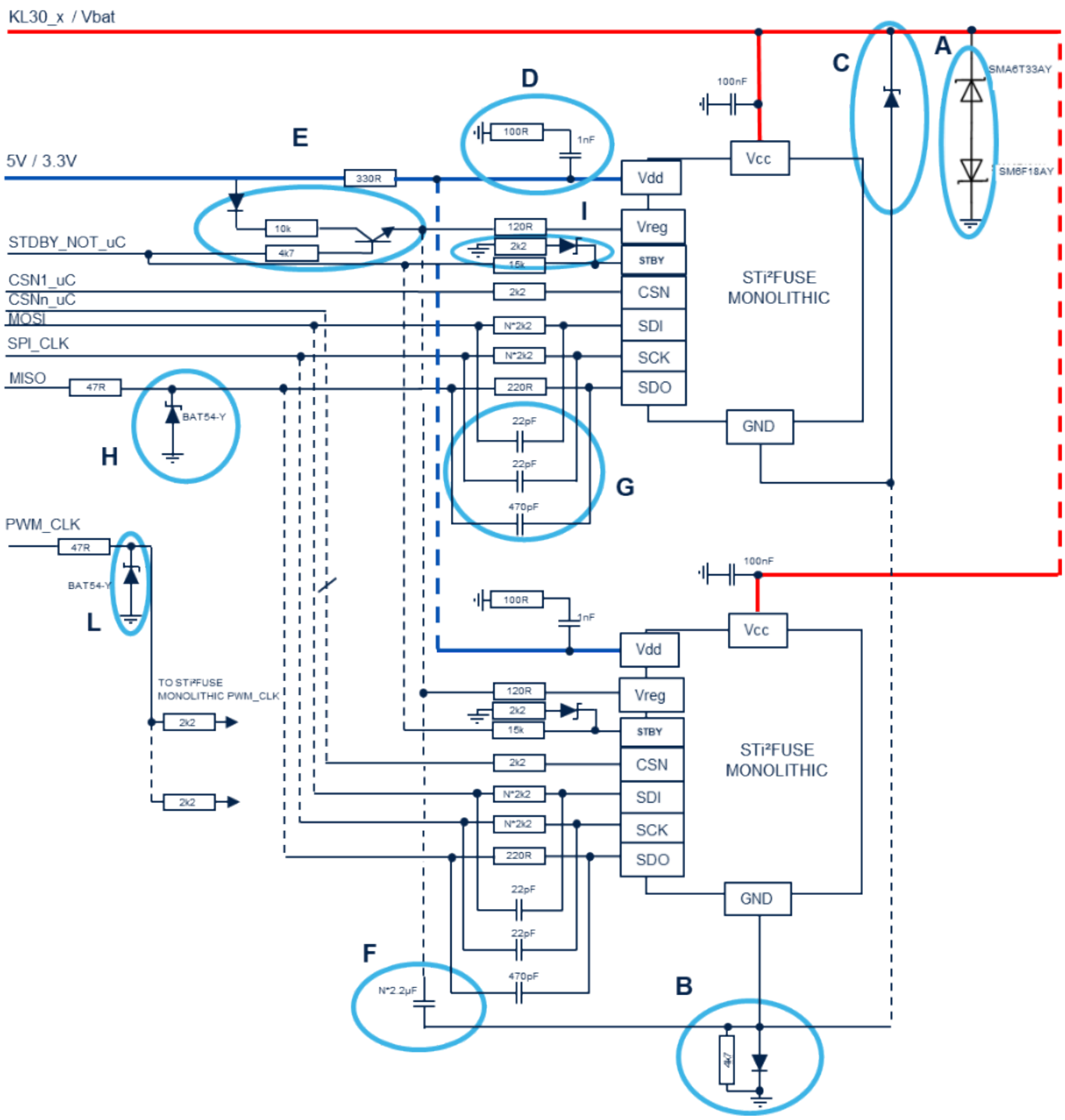
Where N is the number of devices on the SPI bus.

To limit reverse-battery current into the MCU and ensure compliance with pulse 1, as defined in ISO 7637-2:2011, the equivalent resistance of the parallel network, as seen from the MCU pin, shall not be lower than 2.2 kΩ (see UM3631).

To support higher SPI operating frequency, the following speed-up capacitors are recommended:

- SDI and SCK speed-up capacitor: 22 pF
- SDO speed-up capacitor: 470 pF

**Figure 2.** ***Schematic of STi2Fuse  monolithic sharing the same SPI bus [2].***



*Note:*
1. *This case has been validated with no more than 10 devices and an ST SPC582B family MCU.*
2. *DIx and output pins are not shown for simplicity. For the Dix Rprot value calculations, refer to the application schematic in UM3631.*

**Circuit block description**

**A:**

SM6F18AY clamp for ISO 7637-2 pulse 1 transients.

SMA6T33AY clamp for ISO 7637-2 pulse 2a transients.

**B:**

Reverse-battery protection network for a single device: BAS21 with 4.7 kΩ kΩ for $V_{DD}$ = 5 V, BAT54-Y with 4.7kΩ for $V_{DD}$ = 3.3 VV.

For multiple devices, this diode can be shared with other devices of the same family on the same power supply.

The Schottky diode shall provide a forward voltage lower than 0.35 V at -40°C under the total flowing current, which is approximately 6.5 mA per device, to guarantee $V_{DD}$ ≥ 2.7 V under all operating conditions.

If this requirement cannot be met with a diode, a MOSFET -based solution or another equivalent protection solution shall be used.

**C:**

STPS1L40-Y diode to prevent the internal parasitic NPN transistor from being triggered during ISO 7637-2 pulse 1 transients, preserving RAM register content.

**D:**

1 nF capacitor in series with 100 Ω, one per device.

The capacitor acts as a current source to charge the MISO bus capacitance and is required for larger bus capacitances, typically above four devices on the bus.

The 100 Ω resistor is required to limit the injected current during the ISO 7637-2 test.

**E:**

Switchable diode from $V_{DD}$ to VREG, required to preserve RAM register content during ISO 7637-2 pulse 1. The switch is needed to allow the devices to enter standby mode while $V_{DD}$ remains active at module level.

The circuit described includes an NPN BJT and a diode used for standby and VREG control functions. The following requirements apply to these components:

- Current capability: approximately 5 mA per device
- The diode shall block reverse current
- VCE shall withstand approximately 25 V during ISO 7637-2 pulse 1
- The base resistor shall limit the current when the emitter goes negative during ISO 7637-2 pulse 1
- Recommended part number: BC847

These characteristics apply to all circuits described in the other cases.

**F:**

2.2 μF capacitor on the VREG pin through a 120 Ω resistor. The capacitor value is required to maintain RAM register content during ISO 7637-2 pulse 1. A shared capacitor sized as N × 2.2 μF increases the wake-up time if not all devices are woken up at the same time. Devices can enter standby mode only if all devices sharing the capacitor are commanded to enter standby. One device wakes up all devices. If these conditions are too restrictive, a 2.2 μF capacitor through a 120 Ω resistor can be connected to each device individually.

**G:**

Optional speed-up capacitors are used to maximize the SPI frequency.

**H:**

For N > 5, it is recommended to size the diode so that it can support the total forward DC current ($I_{D\_SDO\_total}$) of the SDO path, according to:

$I_{D\_SDO\_total}$ = -N × (12 V - 0.5 V) / 220 Ω = -N × 52 mA, during reverse-battery conditions.

**I:**

2.2 kΩ resistor in series with the BAT54 diode to ensure proper activation of the reverse turn-on function.

**L:**

Diode and 47 Ω MCU protection network to prevent the current on the microcontroller pin from reaching the absolute maximum rating (AMR). Assuming a typical GPIO AMR of approximately 10 mA, this network shall be considered only for N > 4, as the reverse current to the PWM_CLK pin is approximately 2.3 mA max per device at VBAT = -14 V .

# 3 STi²Fuse hybrid circuit

**Case description:** Only STi2Fuse  hybrid devices share the same SPI bus [(1)].

**Conditions:**

- One SPI bus per KL30_x supply line.
- SDI serial resistor: N × 2.2 kΩ
- CLK serial resistor: N × 2.2 kΩ

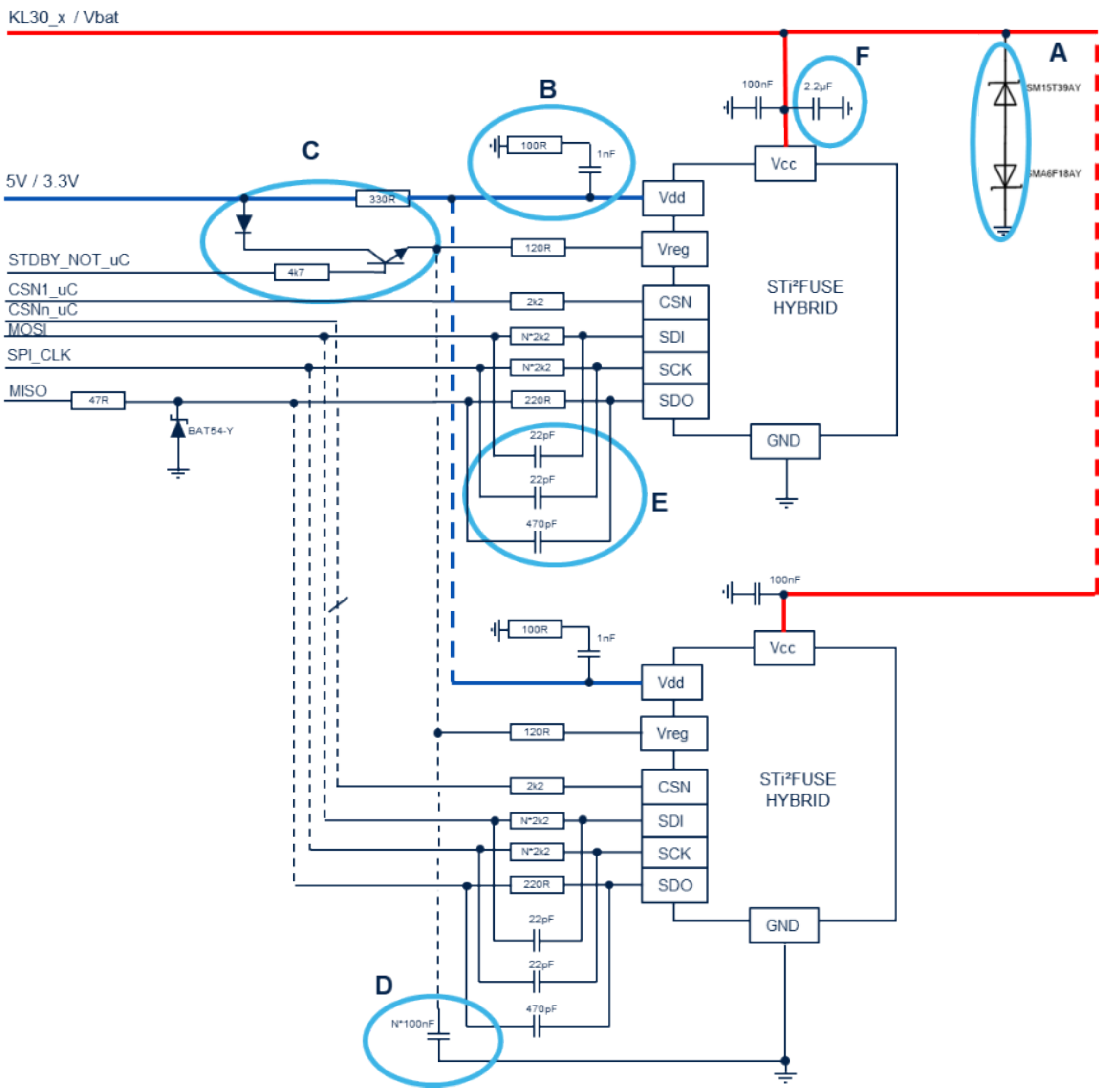
Where N is the number of devices on the SPI bus.

To limit reverse-battery current into the MCU and ensure compliance with pulse 1, as defined in ISO 7637-2:2011, the equivalent resistance of the parallel network, as seen from the MCU pin, shall not be lower than 2.2 kΩ (see UM3631).

To support higher SPI operating frequency, the following speed-up capacitors are recommended:

- SDI and SCK speed-up capacitor: 22 pF
- SDO speed-up capacitor: 470 pF

**Figure 3.** ***Schematic of STi2Fuse  hybrid sharing the same SPI bus [(2)].***



*Note:*
1. *This case has been validated with no more than 10 devices and an ST SPC582B family MCU.*
2. *DIx and output pins are not shown for simplicity. For the Dix Rprot value calculations, refer to the application schematic in UM3631.*

**Circuit block description**

**A:**

SM6F18AY clamp for ISO 7637-2 pulse 1 transients.

SMA6T33AY clamp for ISO 7637-2 pulse 2a transients.

**B:**

1 nF capacitor in series with 100 Ω, one per device.

The capacitor acts as a current source to charge the MISO bus capacitance and is required for larger bus capacitances, typically above four devices on the bus.

The 100 Ω resistor is required to limit the injected current during the ISO 7637-2 test.

**C:**

Switchable diode from $V_{DD}$ to VREG, required to preserve RAM register content during ISO 7637-2 pulse 1. The switch is needed to allow the devices to enter standby mode while $V_{DD}$ remains active at module level.

**D:**

100 nF capacitor on the VREG pin through a 120 Ω resistor. The capacitor value is required to maintain RAM register content during ISO 7637-2 pulse 1. A shared capacitor sized as N × 100 nF increases the wake-up time if not all devices are woken up at the same time. Devices can enter standby mode only if all devices sharing the capacitor are commanded to enter standby. One device wakes up all devices. If these conditions are too restrictive, a 100 nF capacitor through a 120 Ω resistor can be connected to each device individually.

**E:**

Optional speed-up capacitors are used to maximize the SPI frequency.

**F:**

2.2 µF capacitor to slow down the ISO 7637-2 pulse 1 dV/dt, preventing activation of parasitic effects during the transient.

# 4 STi²Fuse hybrid and monolithic circuit

**Case description:** STi²Fuse hybrid and monolithic devices share the same SPI bus (1).

**Conditions:**

- One SPI bus per KL30_x supply line.
- $N_m$ = number of monolithic devices on the SPI bus
- $N_h$ = number of hybrid devices on the SPI bus
- SDI serial resistor: N × 2.2 kΩ
- CLK serial resistor: N × 2.2 kΩ

Where N is the total number of devices on the SPI bus ($N_m + N_h$).

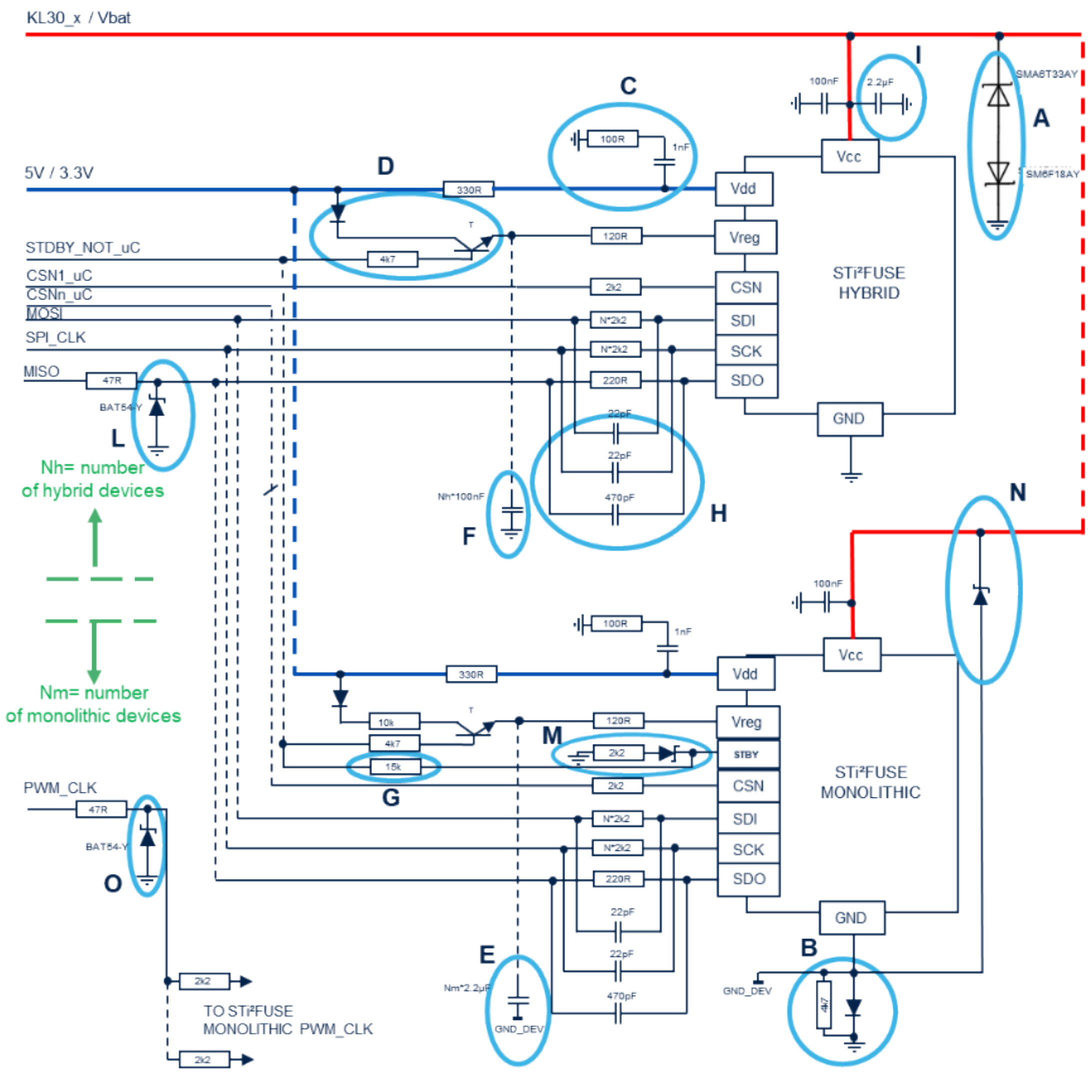
Monolithic and hybrid devices shall have separate VREG capacitors in all cases.

For monolithic devices only, to limit reverse-battery current into the MCU and ensure compliance with pulse 1, as defined in ISO 7637-2:2011, the equivalent resistance of the parallel network, as seen from the MCU pin, shall not be lower than 2.2 kΩ (see UM3631).

To support higher SPI operating frequency, the following speed-up capacitors are recommended:

- SDI and SCK speed-up capacitor: 22 pF
- SDO speed-up capacitor: 470 pF

Figure 4. ***Schematic of STi2Fuse hybrid and monolithic sharing the same SPI bus (2).***



*Note:*
1. *This case has been validated with no more than 10 devices and an ST SPC582B family MCU.*
2. *DIx and output pins are not shown for simplicity. For the Dix Rprot value calculations, refer to the application schematic in UM3631.*

**Circuit block description**

**A:**

SM6F18AY clamp for ISO 7637-2 pulse 1 transients.

SMA6T33AY clamp for ISO 7637-2 pulse 2a transients.

**B**: (For monolithic devices only)

Reverse-battery protection network for a single device: BAS21 with 4.7 kΩ kΩ for $V_{DD}$ = 5 V, BAT54-Y with 4.7kΩ for $V_{DD}$ = 3.3 VV.

For multiple devices, this diode can be shared with other devices of the same family on the same power supply.

The Schottky diode shall provide a forward voltage lower than 0.35 V at -40°C under the total flowing current, which is approximately 6.5 mA per device, to guarantee $V_{DD}$ ≥ 2.7 V under all operating conditions.

If this requirement cannot be met with a diode, a MOSFET -based solution or another equivalent protection solution shall be used.

**C**:

1 nF capacitor in series with 100 Ω, one per device.

The capacitor acts as a current source to charge the MISO bus capacitance and is required for larger bus capacitances, typically above four devices on the bus.

The 100 Ω resistor is required to limit the injected current during the ISO 7637-2 test.

**D**:

Switchable diode from $V_{DD}$ to VREG, required to preserve RAM register content during ISO 7637-2 pulse 1. The switch is needed to allow the devices to enter standby mode while $V_{DD}$ remains active at module level.

**E**: (For monolithic devices only)

2.2 µF capacitor on the VREG pin through a 120 Ω resistor. The capacitor value is required to maintain RAM register content during ISO 7637-2 pulse 1. A shared capacitor sized as $N_m$ × 2.2 µF increases the wake-up time if not all devices are woken up at the same time. Devices can enter standby mode only if all devices sharing the capacitor are commanded to enter standby. One device wakes up all devices. If these conditions are too restrictive, a 2.2 µF capacitor through a 120 Ω resistor can be connected to each device individually.

**F:** (For hybrid devices only)

100 nF capacitor on the VREG pin through a 120 Ω resistor. The capacitor value is required to maintain RAM register content during ISO 7637-2 pulse 1. A shared capacitor sized as $N_h$ × 100 nF increases the wake-up time if not all devices are woken up at the same time. Devices can enter standby mode only if all devices sharing the capacitor are commanded to enter standby. One device wakes up all devices. If these conditions are too restrictive, a 100 nF capacitor through a 120 Ω resistor can be connected to each device individually.

**G:**

15 kΩ STDBY_NOT pin protection resistor, used to minimize interference from the monolithic devices on the STDBY_NOT_uC signal during ISO 7637-2 pulse 1.

This resistor value shall not be lower than 15 kΩ.

**H:**

Optional speed-up capacitors are used to maximize the SPI frequency.

**I:**

2.2 µF capacitor to slow down the ISO 7637-2 pulse 1 dV/dt, preventing activation of parasitic effects during the transient.

**L:**

For $N_m$ > 5, it is recommended to size the diode so that it can support the total forward DC current ($I_{D\_SDO\_total}$) of the SDO path, according to:

$I_{D\_SDO\_total}$ = - N × (12 V - 0.5 V) / 220 Ω =-Nm=-Nm × 52 mA, during reverse-battery conditions.

**M:**

2.2 kΩ resistor in series with the BAT54 diode to ensure full activation of the reverse turn-on function of the channels during reverse-battery conditions on the STi2Fuse  monolithic devices.

**N:**

STPS1L40-Y diode to prevent the internal parasitic NPN transistor from being triggered during ISO 7637-2 pulse 1 transients, preserving RAM register content.

**O:**

Diode and 47 Ω MCU protection network to prevent the current on the microcontroller pin from reaching the absolute maximum rating (AMR). Assuming a typical GPIO AMR of approximately 10 mA, this network shall be considered only for $N_m > 4$, as the reverse current to the PWM_CLK pin is approximately 2.3 mA max per device at VBAT = -14 V.

# 5 STi²Fuse hybrid, monolithic, and M0-9 SPI

**Case description:** STi2Fuse  hybrid, monolithic and M0-9 SPI standard devices share the same SPI bus (1).

**Conditions:**

- One SPI bus per KL30_x supply line.
- $N_m$ = number of monolithic devices on the SPI bus
- $N_h$ = number of hybrid devices on the SPI bus
- $N_{M09}$ = number of M0-9 SPI devices on the SPI bus
- SDI serial resistor: N × 2.2 kΩ
- CLK serial resistor: N × 2.2 kΩ

Where N is the total number of devices on the SPI bus ($N_m + N_h + N_{M09}$).

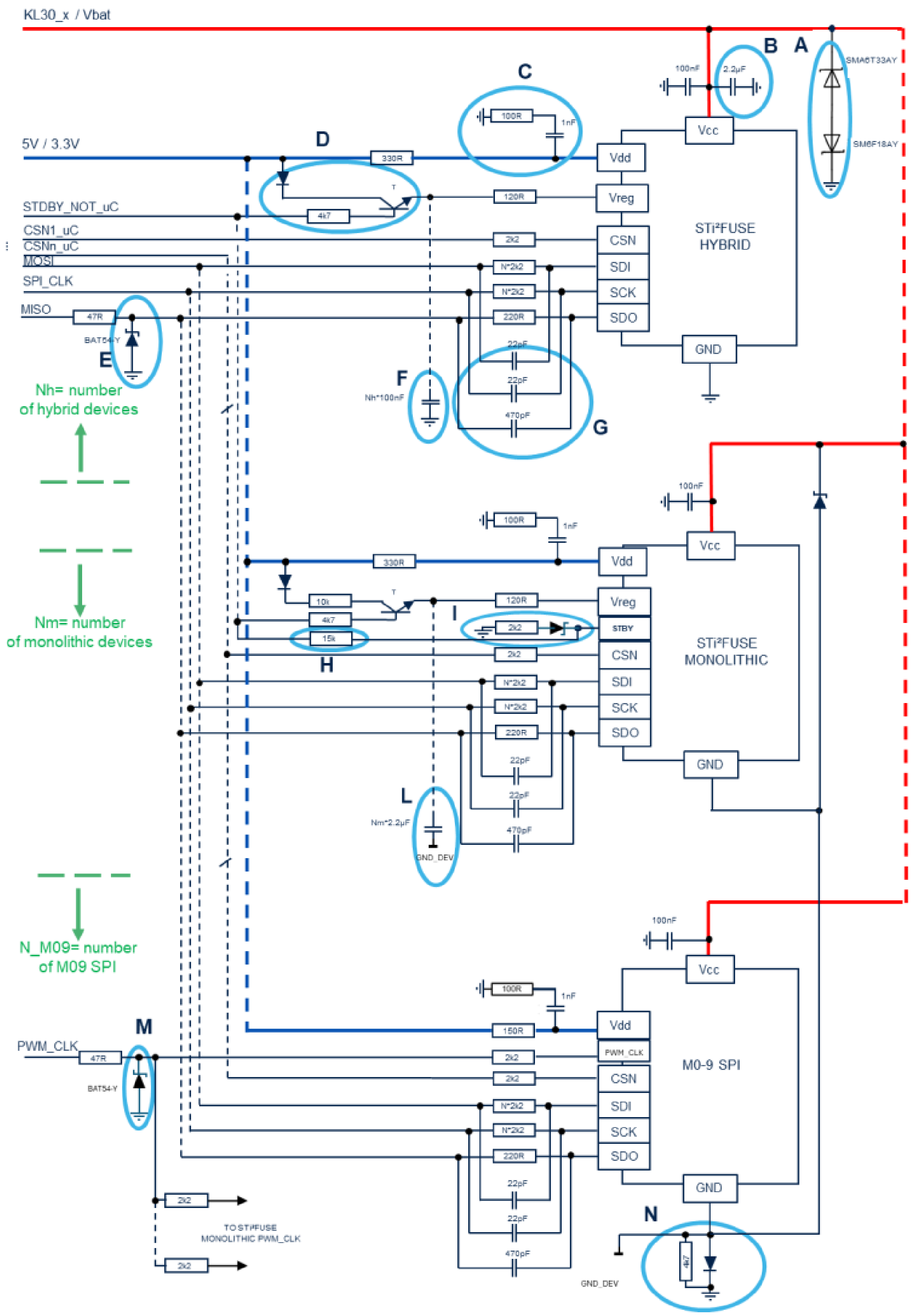
Monolithic and hybrid devices shall have separate VREG capacitors in all cases.

For monolithic and M0-9 SPI devices only, to limit reverse-battery current into the MCU and ensure compliance with pulse 1, as defined in ISO 7637-2:2011, the equivalent resistance of the parallel network, as seen from the MCU pin, shall not be lower than 2.2 kΩ (see UM3631).

To support higher SPI operating frequency, the following speed-up capacitors are recommended:

- SDI and SCK speed-up capacitor: 22 pF
- SDO speed-up capacitor: 470 pF

Figure 5. *Schematic of STi2Fuse hybrid, monolithic, and M0-9 SPI sharing the same SPI bus [2].*




*Note:*

1. *This case has been validated with no more than 10 devices and an ST SPC582B family MCU.*
2. *DIx and output pins are not shown for simplicity. For the Dix Rprot value calculations, refer to the application schematic in UM3631.*

**Circuit block description**

**A:**

SM6F18AY clamp for ISO 7637-2 pulse 1 transients.

SMA6T33AY clamp for ISO 7637-2 pulse 2a transients.

**B:** (For hybrid devices only)

2.2 µF capacitor to slow down the ISO 7637-2 pulse 1 dV/dt, preventing activation of parasitic effects during the transient.

**C:**

1 nF capacitor in series with 100 Ω, one per device.

The capacitor acts as a current source to charge the MISO bus capacitance and is required for larger bus capacitances, typically above four devices on the bus.

The 100 Ω resistor is required to limit the injected current during the ISO 7637-2 test.

**D:**

Switchable diode from $V_{DD}$ to VREG, required to preserve RAM register content during ISO 7637-2 pulse 1. The switch is needed to allow the devices to enter standby mode while $V_{DD}$ remains active at module level.

**E:**

For $(N_m + N_{M09}) > 5$, it is recommended to size the diode so that it can support the total forward DC current ($I_{D\_SDO\_total}$) of the SDO path, according to: $I_{D\_SDO\_total} = -(N_m + N_{M09}) \times (12\ V - 0.5\ V) / 220\ \Omega = -(N_m + N_{M09}) \times 52\ mA$, during reverse-battery conditions.

**F:** (For hybrid devices only)

100 nF capacitor on the VREG pin through a 120 Ω resistor. The capacitor value is required to maintain RAM register content during ISO 7637-2 pulse 1. A shared capacitor sized as $N_h$ × 100 nF increases the wake-up time if not all devices are woken up at the same time. Devices can enter standby mode only if all devices sharing the capacitor are commanded to enter standby. One device wakes up all devices. If these conditions are too restrictive, a 100 nF capacitor through a 120 Ω resistor can be connected to each device individually.

**G:**

Optional speed-up capacitors are used to maximize the SPI frequency.

**H:**

15 kΩ STDBY_NOT pin protection resistor, used to minimize interference from the monolithic devices on the STDBY_NOT_uC signal during ISO 7637-2 pulse 1. This resistor value shall not be lower than 15 kΩ.

**I:**

2.2 kΩ resistor in series with the BAT54 diode to ensure full activation of the reverse turn-on function of the channels during reverse-battery conditions on the STi2Fuse  monolithic devices.

**L:**

2.2 µF capacitor on the VREG pin through a 120 Ω resistor. The capacitor value is required to maintain RAM register content during ISO 7637-2 pulse 1. A shared capacitor sized as $N_m$ × 2.2 µF increases the wake-up time if not all devices are woken up at the same time. Devices can enter standby mode only if all devices sharing the capacitor are commanded to enter standby. One device wakes up all devices. If these conditions are too restrictive, a 2.2 µF capacitor through a 120 Ω resistor can be connected to each device individually.

**M:**

Diode and 47 Ω MCU protection network to prevent the current on the microcontroller pin from reaching the absolute maximum rating (AMR). Assuming a typical GPIO AMR of approximately 10 mA, this network shall be considered only for $(N_m + N_{M09}) > 4$, as the reverse current to the PWM_CLK pin is approximately 2.3 mA max per device at VBAT = -14 V.

**N:** (For monolithic STi$^2$Fuse and M0-9 SPI devices)

Reverse-battery protection network for a single device: BAS21 with 4.7 kΩ kΩ for $V_{DD}$ = 5 V, BAT54-Y with 4.7kΩ for $V_{DD}$ = 3.3 VV.

For multiple devices, this diode can be shared with other devices of the same family on the same power supply.

The Schottky diode shall provide a forward voltage lower than 0.35 V at -40°C under the total flowing current, which is approximately 6.5 mA per device, to guarantee $V_{DD} \geq 2.7$ V under all operating conditions.

If this requirement cannot be met with a diode, a MOSFET -based solution or another equivalent protection solution shall be used.

# 6 Optional circuit to reduce $V_{DD}$ current consumption and prevent MCU reset during ISO 7637-2 pulse 1

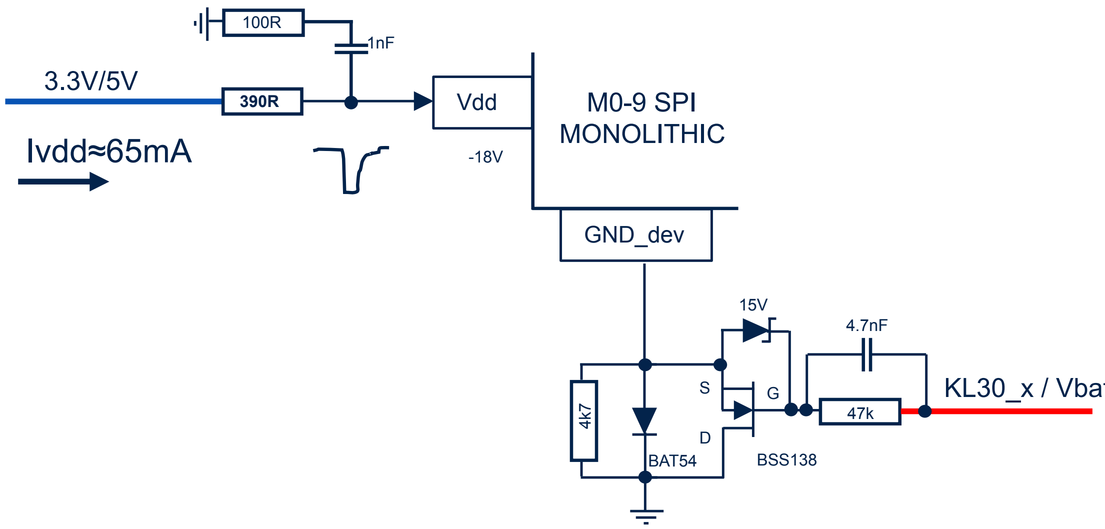
During reverse-battery and ISO 7637-2 pulse 1 negative events, the current demand on the 3.3 V/5 V line increases and shall be supplied by the MCU-side LDO. This transient current, multiplied by the number of devices connected to the same rail, may exceed the maximum current capability of the LDO and cause a microcontroller reset due to excessive voltage drop.

This section presents the solutions used to limit the current drawn from the MCU $V_{DD}$ supply during ISO 7637-2 pulse 1 events, with reference to M0-9 SPI standard devices and STi2Fuse monolithic devices. Since the implementation differs between the two families, the corresponding circuits are described in the following subsections.

## 6.1 Current reduction on the $V_{DD}$ line for standard M0-9 SPI devices

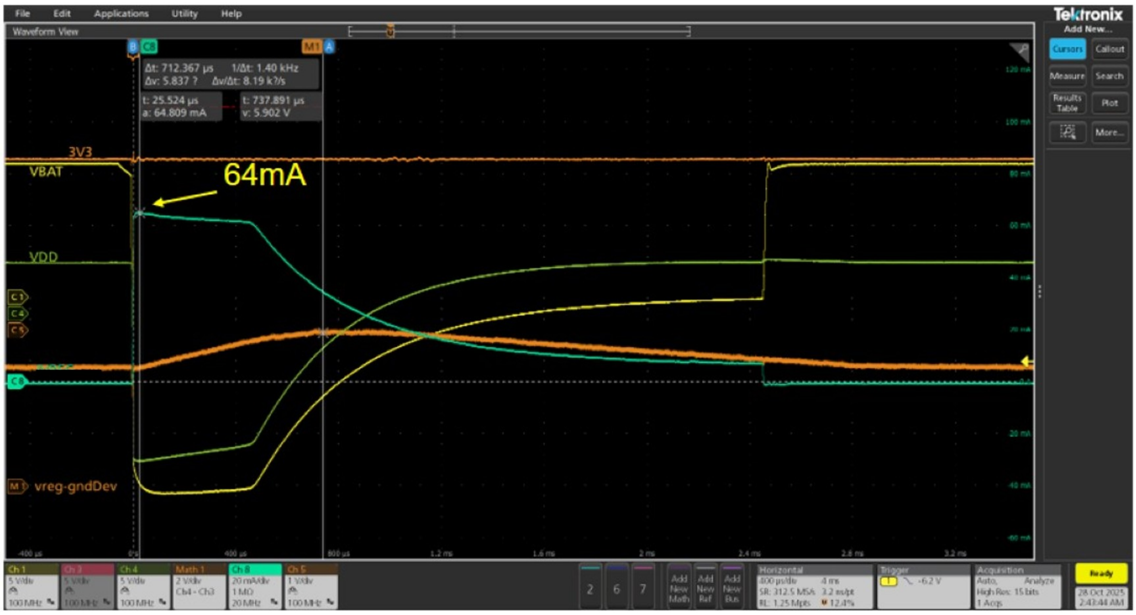
To mitigate this current demand, one solution is to replace the 150 Ω resistor on the $V_{DD}$ line with a 390 Ω resistor, while using a MOSFET on GND_Device, as detailed in UM3631 (VIPower M0-9 SPI standard high-side drivers), to ensure that $V_{DD}$ is not lower than 2.7 V, as specified in the datasheets of all M0-9 family devices.

**Figure 6.** ***Circuit solution for reducing the current on the 3.3 V line during reverse-battery conditions and ISO 7637-2 pulse 1 transient.***




With this countermeasure, as shown in Figure 6, the current is reduced to less than half of the current obtained with the standard schematic. The resulting $V_{DD}$ current during the ISO 7637-2 pulse 1 transient is approximately 65 mA for each device connected to the same supply rail, as shown in Figure 7.

Figure 7. *$V_{DD}$ pin current during ISO 7637-2 pulse 1 negative transient with the proposed circuit.*




## 6.2 Current reduction on the $V_{DD}$ line for STi²Fuse monolithic devices

An optional method to reduce the current injected into the $V_{DD}$ pin during ISO 7637-2 pulse 1 is to split the 330 Ω VDD Rprot resistor into two separate resistors and add a diode to GND, as shown in Figure 8. This circuit reduces the current on the 3.3 V/5 V line during the negative transient, while maintaining the VDD operating conditions required by the STi2Fuse monolithic device.

Figure 8. *Split $V_{DD}$ Rprot network used to reduce current on the 3.3 V/5 V line during ISO 7637-2 pulse 1*

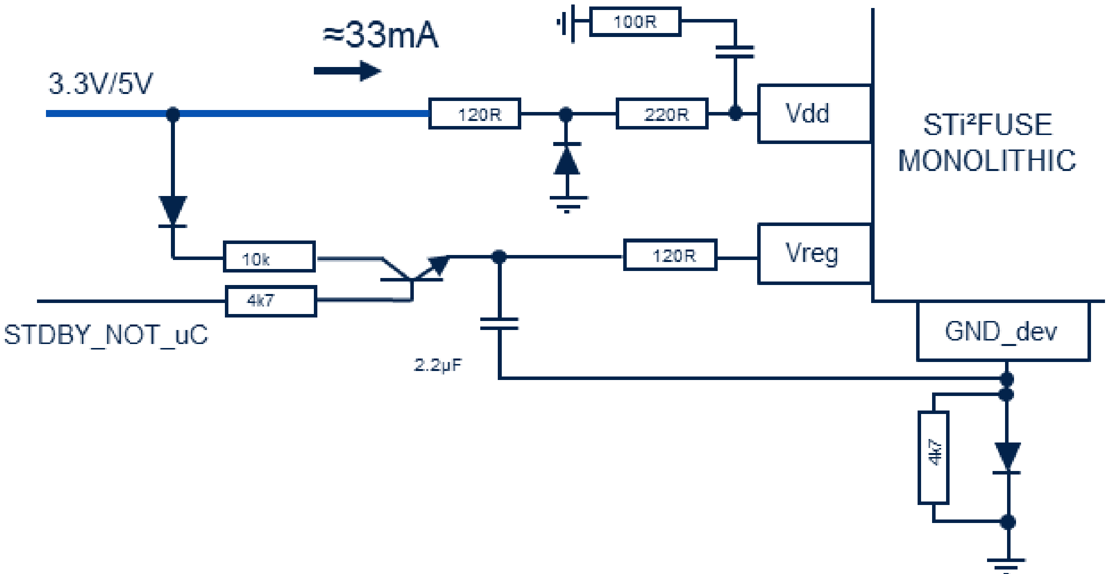


**Figure 9.** ***Current on the 3.3 V line during ISO 7637-2 pulse 1 negative transient with the split resistor network.***

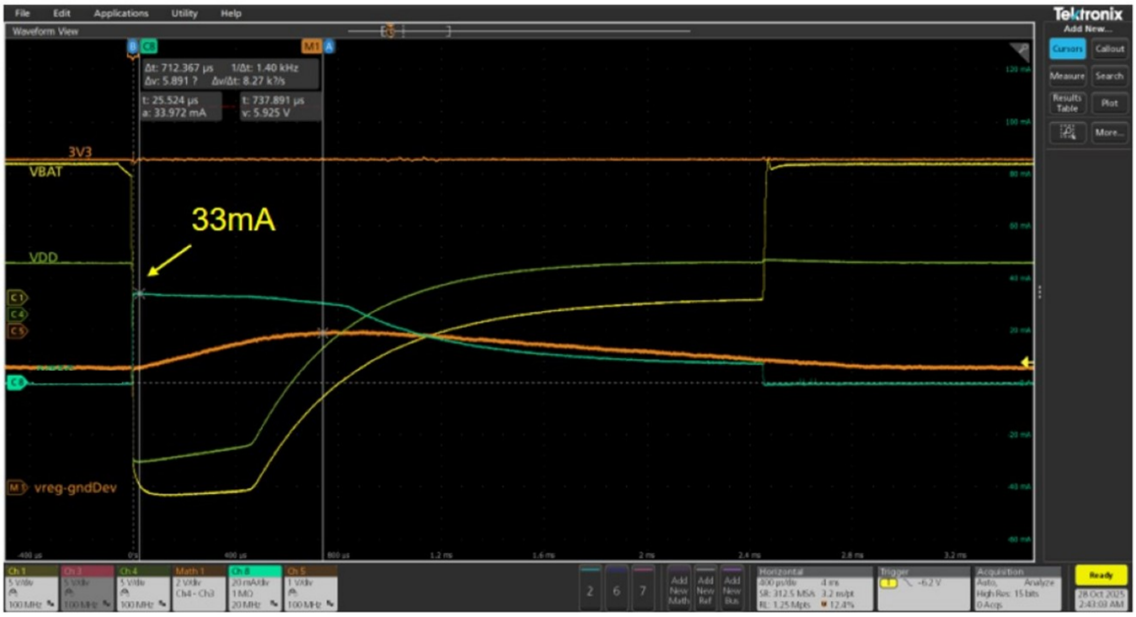
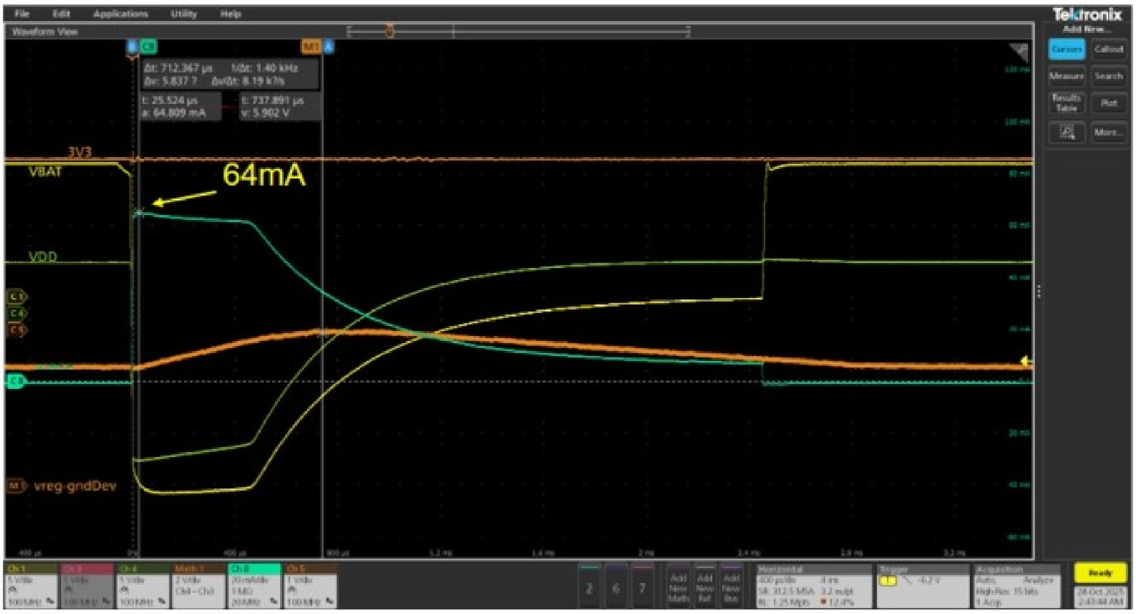



**Figure 10.** ***Current on 3.3 V line during negative ISO pulse 1 with single 330 R resistor.***

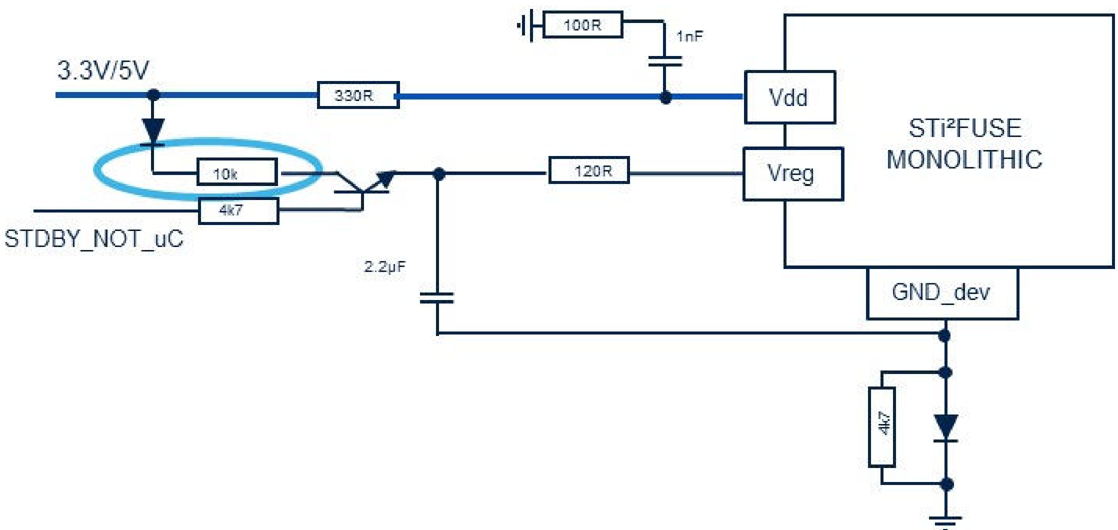


# 7 Overvoltage reduction on the $V_{REG}$ pin during ISO 7637-2 pulse 1 for monolithic STi²Fuse devices

During ISO 7637-2 pulse 1 negative events, an overvoltage is applied to the VREG pin with respect to GND_dev. This overvoltage depends on the amount of current injected into the $V_{REG}$ pin through the series transistor collector resistance. The resistor value shall therefore be selected as a trade-off: it shall not be too high, in order to ensure proper supply of the $V_{REG}$ pin, and it shall not be too low, in order to limit the injected current and prevent the $V_{REG}$ pin from reaching its AMR of 6 V.

As shown in Figure 11, a resistor value of 10 kΩ provides a good compromise between these two requirements.

**Figure 11.** ***Series resistor on the transistor collector to reduce VREG overvoltage during ISO 7637-2 pulse 1.***

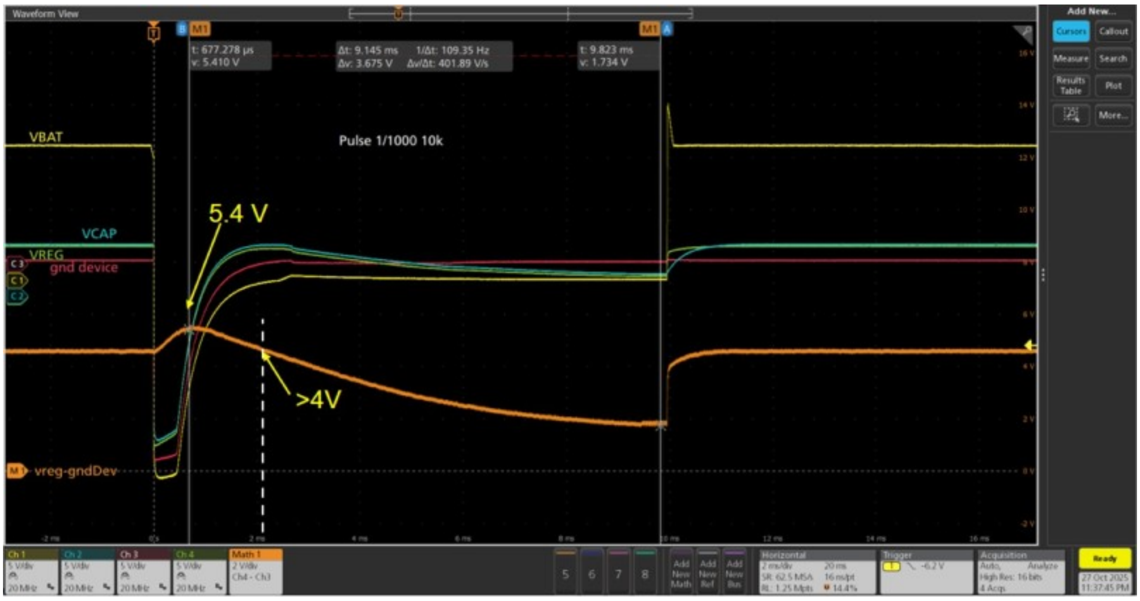



Two examples are shown in Figure 12 and Figure 13, with resistor values of 2.2 kΩ and 10 kΩ, respectively. With a 2.2 kΩ resistor, the VREG overvoltage is approximately 6.8 V, which exceeds the $V_{REG}$ pin AMR.

**Figure 12.** ***$V_{REG}$ overvoltage during ISO 7637-2 pulse 1 with a 2.2 kΩ series resistor on the NPN collector.***

With a 10 kΩ resistor, the $V_{REG}$ overvoltage is 5.4 V, which is sufficiently far from the pin AMR and provides an adequate safety margin.

**Figure 13.** ***$V_{REG}$ overvoltage during ISO 7637-2 pulse 1 with a 10 kΩ series resistor on the NPN collector***



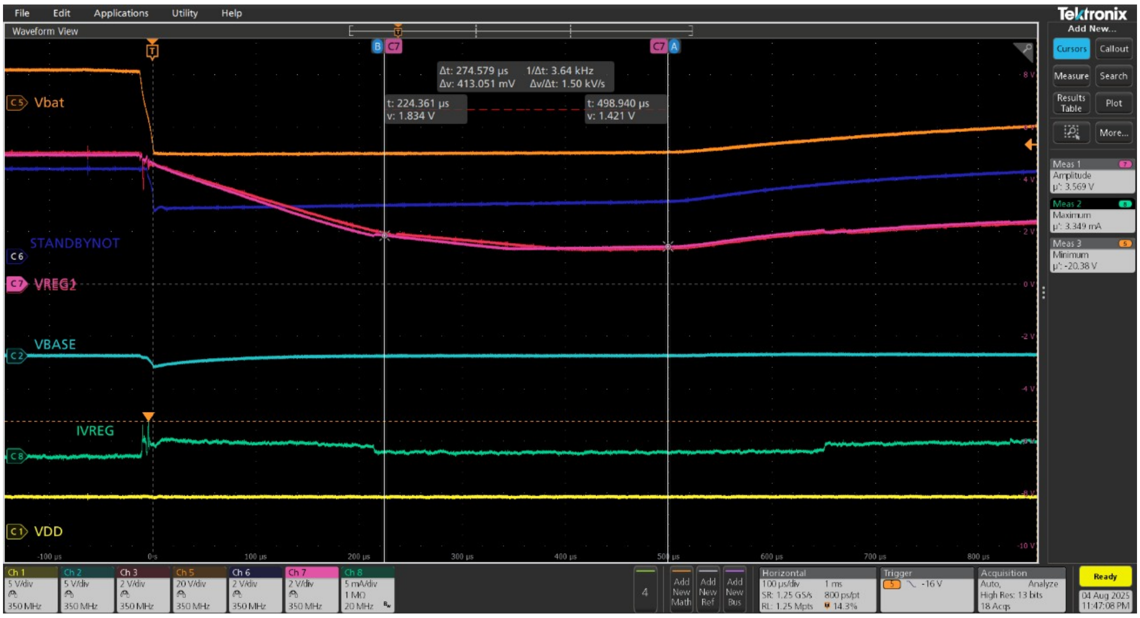
# 8 RAM data retention on hybrid and monolithic STi²Fuse devices

To ensure RAM data retention when a combination of hybrid and monolithic STi2Fuse devices is present, excessive current injection through the Rprot resistor connected between the STDBY_NOT pin and the STDBY_NOT_uC signal shall be avoided during ISO 7637-2 pulse 1.

The STDBY_NOT signal drives the base of the NPN switchable diode to keep the VREG pin voltage high, thereby preserving the data stored in the RAM registers. To guarantee this behavior, the STDBY_NOT_uC signal shall be always held high during ISO 7637-2 pulse 1. The recommended Rprot (STDBY_NOT) value is 15 kΩ.

During ISO 7637-2 pulse 1, the STDBY_NOT pin of the monolithic device drops to approximately -18 V. If the Rprot (STDBY_NOT) value is lower than recommended, the voltage at this pin also drops, reducing the base current of the NPN transistor and may cause the VREG voltage of the hybrid devices to fall below the POR threshold, as shown in the example below.

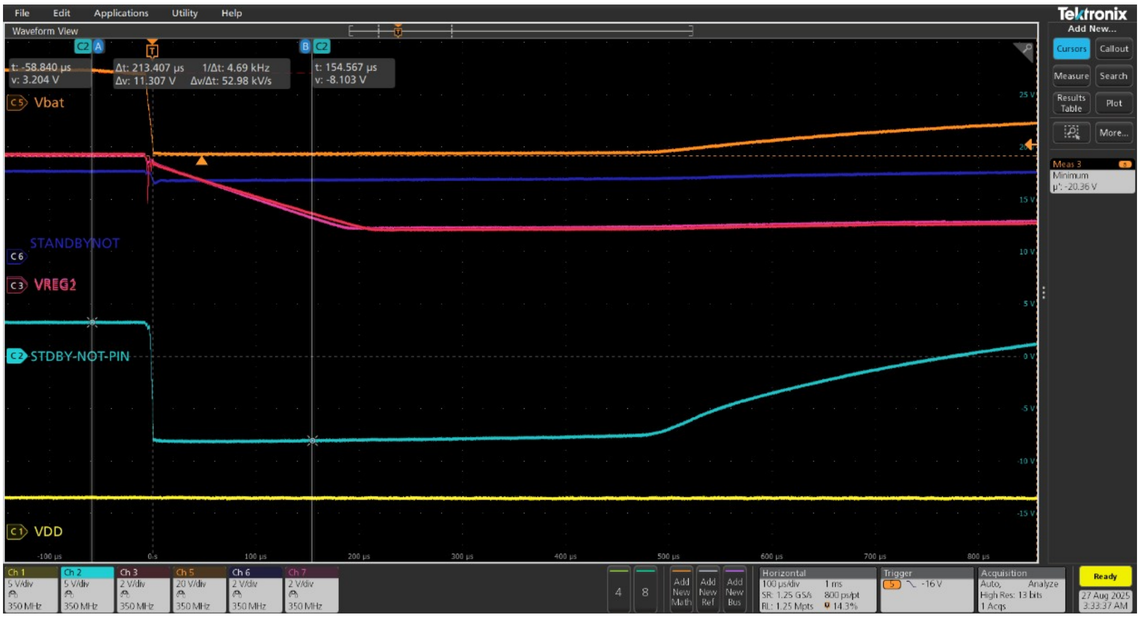
**Figure 14.** ***VREG on hybrid devices with Rprot (STDBY_NOT) = 1 kΩ during ISO 7637-2 pulse 1, RAM data not preserved.***




In fact, with a low Rprot (STDBY_NOT) value of 1 kΩ, the signal is affected by the monolithic eFuse during ISO 7637-2 pulse 1, causing an overload on the STDBY_NOT_uC line, with VREG falling below the POR threshold. As a result, RAM register retention cannot be guaranteed.

To avoid this impact on the control signal, a higher Rprot (STDBY_NOT) value is required to minimize interaction on the STDBY_NOT signal during ISO 7637-2 pulse 1. This ensures a higher VREG voltage, above 1.9 V, and therefore RAM content preservation on hybrid and monolithic STi2Fuse devices. The plot below shows the results with Rprot (STDBY_NOT) = 15 kΩ.

**Figure 15.** ***VREG on hybrid devices with Rprot (STDBY_NOT) = 15 kΩ during ISO 7637-2 pulse 1, with RAM data preserved.***



## Revision history

Table 1. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 10-Jun-2026 | 1 | Initial release. |

# Contents

# List of tables

# List of figures