
Automotive L9988 12 V battery management system open load diagnostic

Introduction

The *Open Load Detection* function is essential for the safety of the battery management systems (BMS). Given its significant importance, it is highly recommended to fully understand this function.

In a battery management system (BMS), a large amount of wiring connections between individual cells and cell monitor circuits is crucial. These connections enable monitoring of cell parameters such as voltage, current, temperature, and more than, for example, implement also as the current path for cell passive balancing discharge.

- Risks and Challenges of Open Wires

The occurrence of open wires in the BMS must be avoided. Open load conditions can be caused by weakened or lost connections in the cell wiring, representing a safety risk to the entire BMS. Unmonitored cells can become a risk to the system at any unknown time.

- Addressing Open Wire Issues

When open wires do occur, it is essential to quickly, accurately, and efficiently determine their location and provide timely notifications. This prompt response is crucial to maintaining the safety of the BMS.

The aim of this document is to help the customer to implement the open-load diagnosis procedure as well as to highlight the special cases that require attention.

1 Open load diagnostic

The Open Load Diagnostic is a crucial feature that allows for the detection of three different open load failure conditions:

1. A cell sense lines (C_x)
2. A cell balancing lines (S_x)
3. A cell harness connected to the PCB.

The DIAG_STEP command is enabled to verify any open wires between the ADCs of the L9988 and the external cells.

When this diagnostic is triggered, the routine is executed in parallel on all cell analog front-end pins, similar to measuring cell voltages. However, there are internal current sources that either sink or source current into the C_x/S_x pins while they are being measured. A pull-up or pull-down generator determines if the current sources are sinking or sourcing 100 μA /50 μA .

The IC performs a conversion of the cell voltage at C_x pins using the temporal window TADCV_START (60 μs) + TADCV_OPEN_DIAG (programmable time).

The following procedure is used to check for an open wire on any of the C_x and S_x pins:

- The ICELL_OPEN_DIAG (typically 100 μA) pull down current is enabled on C_x pins ranging from 1 to 4.
- The IBAL_OPEN_DIAG (typically 100 μA) pull down current is enabled on S_x pins ranging from 1 to 4.
- The ICELL_OPEN_DIAG_FIRST (typically 50 μA) pullup current is enabled on C_0 .
- The IBAL_OPEN_DIAG_FIRST (typically 50 μA) pullup current is enabled on S_0 .

Figure 1 shows the schematic of Open Load Diagnostic procedure to help customers visualize the complexities of the procedure more intuitively.

Figure 1. Open load diagnostic

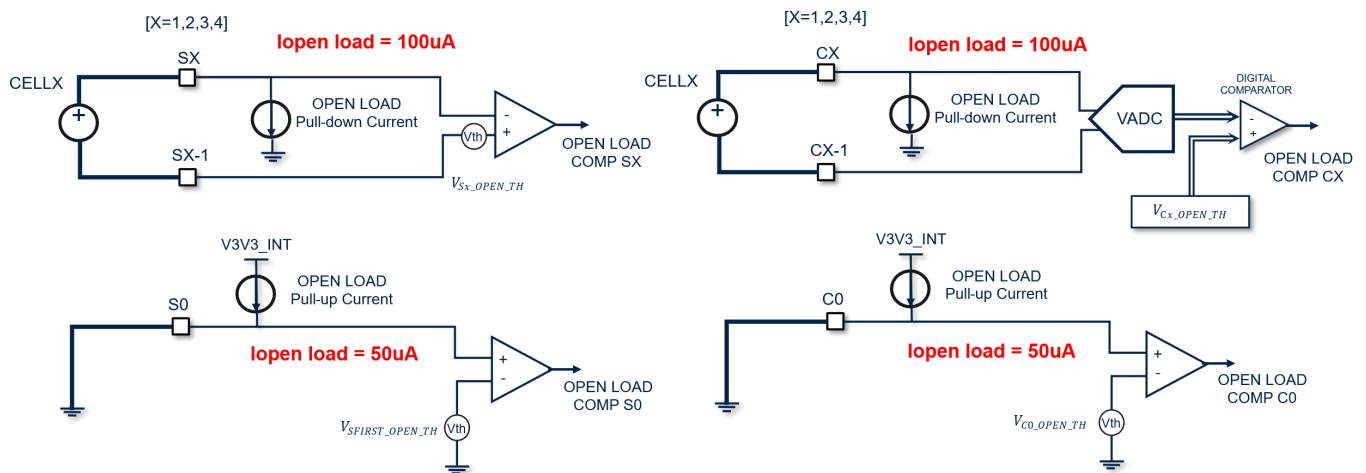
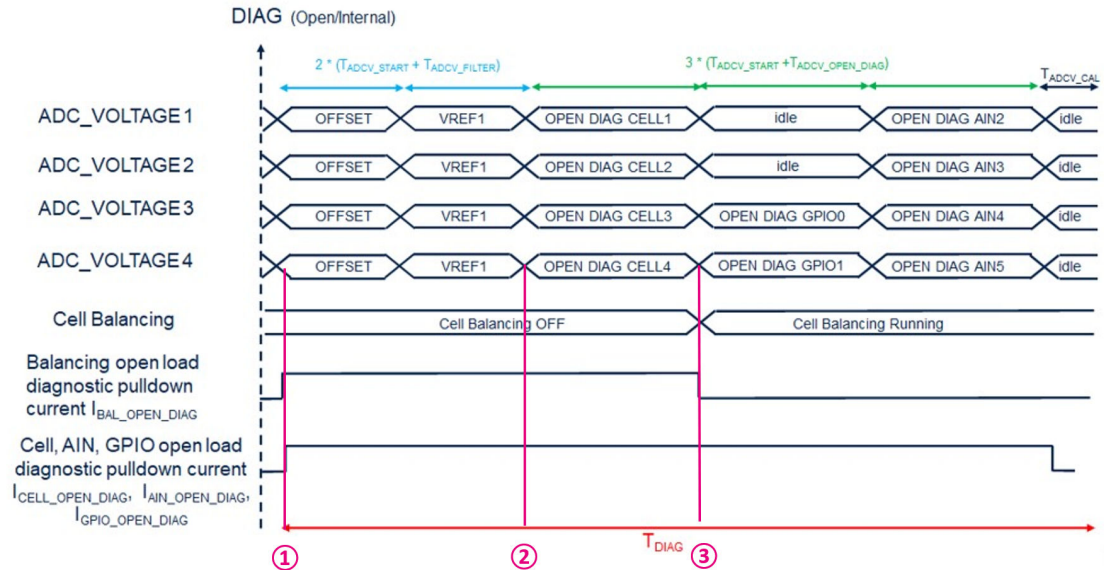


Figure 2. Open Load Diagnostic - Procedure sequence shows the procedure sequence of Open Load Diagnostic.

Figure 2. Open Load Diagnostic - Procedure sequence



1. I_{OPEN_DIAG} pull-down/pull-up currents are enabled on C_x and S_x pins [$x=1,2,3,4$].
2. After $2 * (T_{ADC_START} + T_{ADC_FILTER})$ a conversion of the cell voltage at C_x pins using the ADC_FIL filter window is started.
3. After $3 * (T_{ADC_START} + T_{ADC_FILTER})$ the S_x [$x=0,1,2,3,4$] pins analog comparators, the C_0 analog comparator and the C_x [$x=1,2,3,4$] digital comparators are unmasked, and output are sampled. At the same time, the pull-down/pull-up currents on the S_x pin are disabled.

2 Device configuration

Before enabling the open load diagnostic, the L9988 needs to be configured for normal BMS operation. Here following an example of device configuration.

2.1 NVM configuration (write command)

The MCU shall write the following commands to configure the NVM:

1. Write 0x55 in the SPECIAL_KEY register for partial unlock.
2. Write 0x33 in the SPECIAL_KEY register for full unlock.
3. Write proper NVM configuration, according to customer application requirements.
4. Write 0x3 in the NVM_OP_CMD field in the GENERAL_REG register to upload data into the NVM.
5. Write 0xAA in the SPECIAL_KEY register for lock restoring or wait $t_{CFG_TIMEOUT}$ expiration for automatic locking.

Every time the NVM is written, the *NVM_UPLOAD_COUNT* increases by 1, starting from 0x00.

Please note that the *NVM_UPLOAD_COUNT* cannot exceed 0x1F, so in general it must be written just once during the first power-up.

2.2 BITs configuration

Various thresholds or bits could be set to ensure that the device is configured with no faults at the start of the AFE Open Load Diagnostic.

Table 1. Thresholds configuration

Field	Register	Note ⁽¹⁾
VCELL<x>_EN	BOARD_CFG	All cells X enabled
CELL_OV_TH	CELL_BAL_TH_CFG	Set the OV threshold not to have any OV faults (although this is not critical for the test)
CELL_UV_TH	CELL_UV_TH_CFG	Set the UV threshold not to have any UV faults (although this is not critical for the test)
CELL_DEEP_UV_TH	CELL_UV_TH_CFG	Set a deep UV threshold not to have any UV faults (although this is not critical for the test)
SUM_UV_TH	SUM_TH_CFG	Set the SUM_UV threshold not to have any UV faults (although this is not critical for the test)
SUM_OV_TH	SUM_TH_CFG	Set the SUM_OV threshold not to have any OV faults (although this is not critical for the test)
VBS_OV_TH	VBS_CFG	Set the VBS_OV threshold not to have any OV faults (although this is not critical for the test)
VBS_UV_TH	VBS_CFG	Set the VBS_UV threshold not to have any UV faults (although this is not critical for the test)
CX_OPEN_TH	DEV_GEN3_CFG	Set CX_OPEN threshold in according to the application.
ADCV_FIL	GEN_CFG2	ADCV_FIL=000 136 μ s
		ADCV_FIL=001 264 μ s
		ADCV_FIL=010 1.04 ms
		ADCV_FIL=100 2.08 ms
		ADCV_FIL=011 4.16 ms
		ADCV_FIL=100 8.32 ms
		ADCV_FIL=101 16.64 ms
		ADCV_FIL=110 33.28 ms

1. *TADCV_OPEN_DIAG_xxx* is equal to *TADCV_FILTER_xxx*.

3 Procedure open load diagnostic

The IC can perform two procedures of the Voltage Conversion Routine (VCR). The first uses the command SoC by SPI and the second uses an internal timer to cyclically set the SoC. The cycle timer can be configured by 3 bits (for more details refer to the datasheet).

Procedure for activation of the Open Load diagnostic by SOC_SPI:

Table 2. Open Load Diagnostic procedure by SOC_SPI

Field	Register	Bit
VOLT_STEP	GEN_CFG2	Set to 1
DIAG_STEP	GEN_CFG2	Set to 1
SOC_SPI	CONV_SOC	Set to 1

Procedure for activation of the Open Load diagnostic by internal timer:

Table 3. Open Load Diagnostic procedure by internal timer

Field	Register	Bit
VOLT_STEP	GEN_CFG2	Set to 1
DIAG_STEP	GEN_CFG2	Set to 1
SOC_SEL	CYCLE_CONFIG_REG1	Set to 1
CYCLE_NORMAL	CYCLE_CONFIG_REG1	3-bit selection activates the internal timer for the SOC cycle

3.1 Open Load Detection

The CELL_OPEN_DIAG flags register are then assessed as indicated in the following table conditions (Table 4. Open Load Diagnostic conditions).

Table 4. Open Load Diagnostic conditions

Field	Bits	Conditions	Fault condition
CELL_OPEN_DIAG<x>	00	No open detection	
CELL_OPEN_DIAG<x>	01	Cell C _x open detection	$V_{Cx} - V_{Cx-1} < V_{Cx_OPEN_TH} V_{Sx} - V_{Sx-1} > V_{Sx_OPEN_TH}$
CELL_OPEN_DIAG<x>	10	Balancing S _x open detection	$V_{Cx} - V_{Cx-1} > V_{Cx_OPEN_TH} V_{Sx} - V_{Sx-1} < V_{Sx_OPEN_TH}$
CELL_OPEN_DIAG<x>	11	PCB open detection	$V_{Cx} - V_{Cx-1} < V_{Cx_OPEN_TH} V_{Sx} - V_{Sx-1} > V_{Sx_OPEN_TH}$
C0_OPEN	0	No C ₀ open detection	
C0_OPEN	1	C ₀ open detection	$V_{C0} > V_{C0_OPEN_TH}$
SFIRST_OPEN	0	No S ₀ open detection	$V_{S0} > V_{SFIRST_OPEN_TH}$
SFIRST_OPEN	1	S ₀ open detection	

Where:

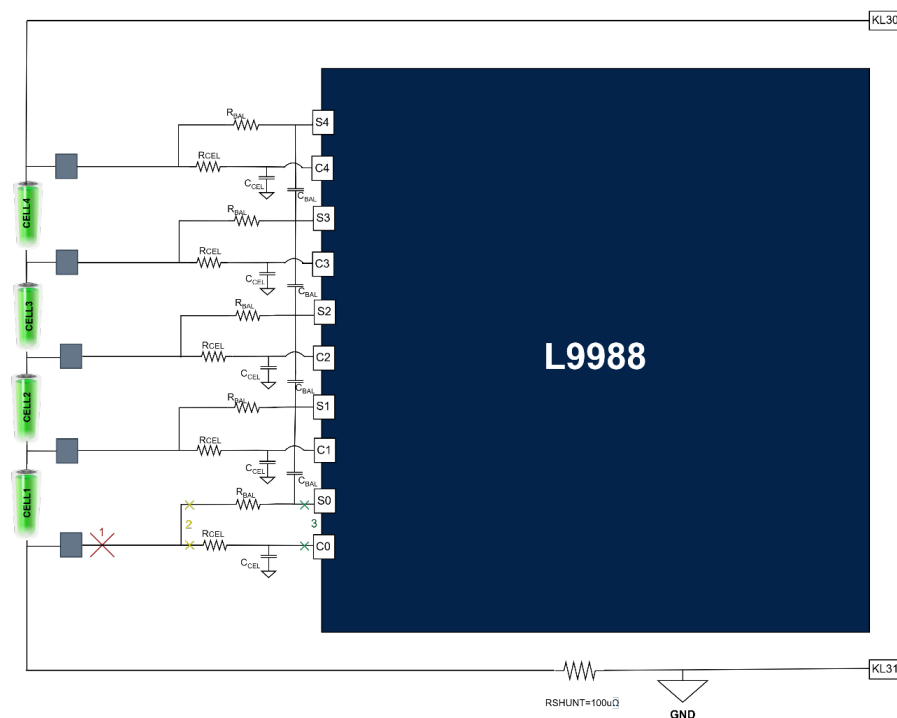
- $V_{Cx_OPEN_TH} = 2048 * V_{ADC_RES} * CODE \rightarrow 0V < V_{Cx_OPEN_TH} < 6V$
- $V_{Sx_OPEN_TH} = 0.6V$
- $V_{SFIRST_OPEN_TH} = 0.6V$
- $V_{C0_OPEN_TH} = 0.2V$

3.2 Settling time

Many factors impact on the correct Open Load Detection and influence the settling time. The $T_{SETTLING}$ is settling time of the C_x-S_x nodes voltage in Open Load condition and depends on:

- *Fault injection point:*
 - Battery connector (1) - worst case
 - Cell resistance (2)
 - L9988 pin (3) - best case
- *Fault injection multiplicity:*
 - Multiple point faults - worst case
 - Single point fault - best case
- *Cell voltage:*
 - 5 V - worst case
 - 1 V - best case
 - The cell and balancing capacitance and ESD capacitance
 - C_{xopen} threshold

Figure 3. Open Load Diagnostic - Cell voltage and balance schematic Board



For a correct Open Load detection, the following timing constraint shall be fulfilled:

1. $C_x [x=1,2,3,4] \rightarrow T_{SETTLING} < 2 * (T_{ADCV_START} + T_{ADCV_FILTER})$
2. $S_x [x=0,1,2,3,4] \& C_0 \rightarrow T_{SETTLING} < T_{ADC} < 3 * (T_{ADCV_START} + T_{ADCV_FILTER})$

To ensure proper Open Load Detection under all conditions the following conditions should be met:
 $2 * (T_{ADCV_START} + T_{ADCV_FILTER}) > 10 \text{ ms}$ (*)

In case T_{ADCV_FILTER} cannot be set to satisfy the previous inequation, a multiple DIAG step conversion could be requested instead.

(*) The 10ms limit depends on the injection point, fault multiplicity, and cell voltage considered. If some of the considered corners are not realistic and could be excluded, this limit (10 ms) may be reduced.

3.3

Example of settling time

In the following chapter, an example of settling time is shown that influences the PCB Open Diagnostic. Suppose that:

So, the time that occurs to discharge the voltage on cell and ESD capacitors is:

$$\Delta T = \frac{C_{AV}}{I_{cell_open_diag}} = \frac{(C_{cell} + C_{ESD})(V_{cc} \times C_{open_th})}{I_{cell_open_diag}} = \frac{94nF(4.5 - 1)V}{100\mu A} \approx 3.29ms$$

Figure 4. Open Load Diagnostic - Timing diagram with ADCV_FIL of 264 μs

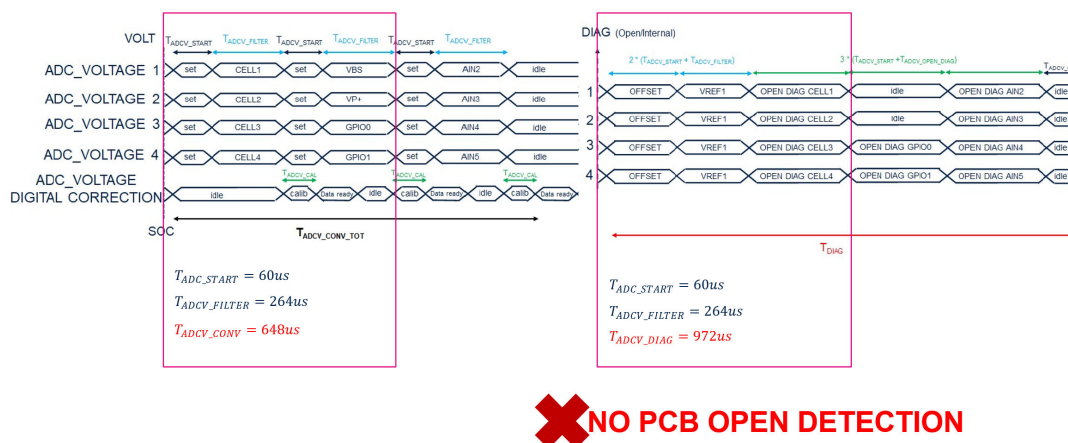
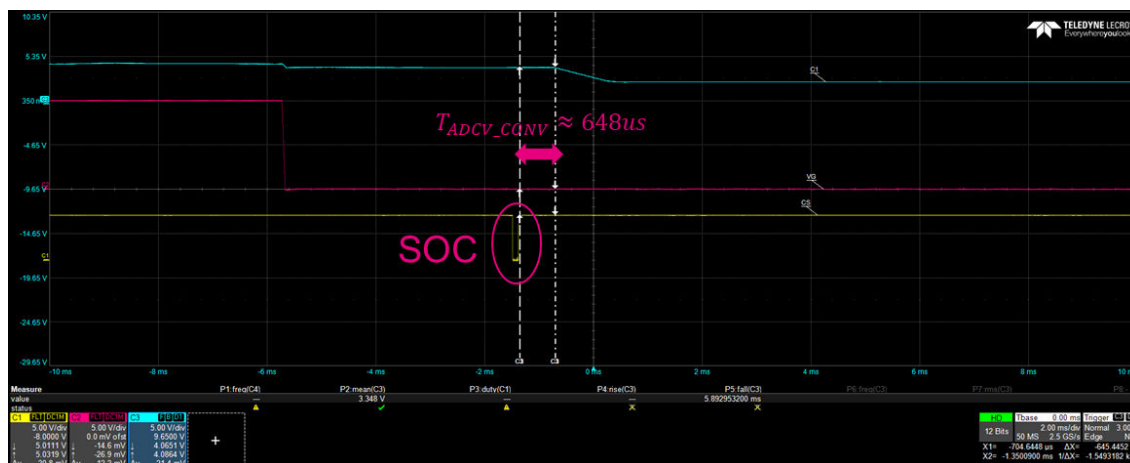


Figure 4. Open Load Diagnostic - Timing diagram with ADCV_FIL of 264 μs shows the timing diagram of VCR and DIAG_STEP when the TADCV_FIL is set to 264 μs .

When the SoC is enabled, the Voltage Conversion Routine is started, and its duration is 684 μs ($2 \times (T_{ADCV_START} + T_{ADCV_FILTER})$). After the VCR, there is a time where the OFFSET and VREFx steps are always executed during DIAG_STEP, and its duration is 648 μs ($2 \times (T_{ADCV_START} + T_{ADCV_FILTER})$). Only after 972 μs ($3 \times (T_{ADCV_START} + T_{ADCV_FILTER})$) the Open Load Diagnostic has been made but the settling time to discharge the capacitor is 3 ms so the nodes voltage is more than the open threshold and PCB open is not detected.

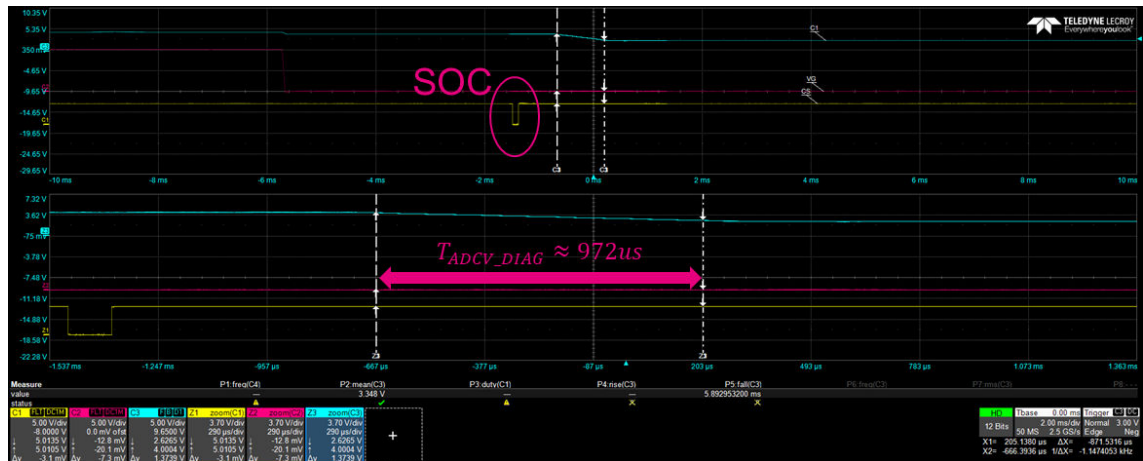
Figure 5. Open Load Diagnostic - Oscilloscope time of VCR with ADCV_FIL of 264 μs shows that the voltage on C₁ is about 4 V and the time that occurs since the SoC is set and the beginning of the decrease of C₁ voltage is the time of conversion. The voltage beginning to decrease because the pullup/pulldown current generators are active.

Figure 5. Open Load Diagnostic - Oscilloscope time of VCR with ADCV_FIL of 264 μs



The time estimated to Open Diagnostic is 972 μ s but after this time, the C₁ voltage is about 2.5 V. The voltage is over the open threshold therefore the Open Load Diagnostic is not detected as shown in Figure 6. Open Load Diagnostic - Oscilloscope time of DIAG STEP with ADCV_FIL of 264 μ s

Figure 6. Open Load Diagnostic - Oscilloscope time of DIAG STEP with ADCV_FIL of 264 μ s

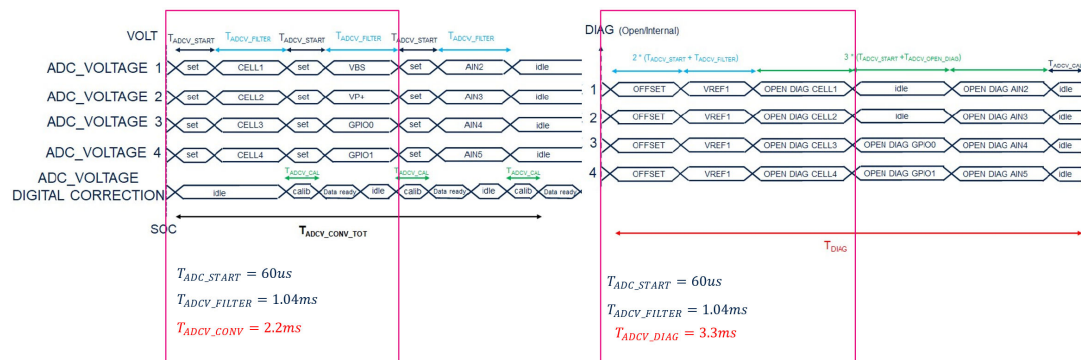


There are two solutions for correctly detect the Open Load:

- Launch VCR and DIAG step again
- Choose a longer ADCV_FIL filtering time

If a longer filtering time is considered, for example, ADCV_FIL= 1.04 ms, the Open Load Diagnostic is determined as shown in Figure 7. Open Load Diagnostic - Timing diagram with ADCV_FIL of 1.04 ms.

Figure 7. Open Load Diagnostic - Timing diagram with ADCV_FIL of 1.04 ms



PCB OPEN DETECTION

With ADCV_FIL of 1.04 ms the detection time of the Open Load Diagnostic is about 3.3 ms so the voltage on the nodes has time to discharge as shown Figure 9. Open Load Diagnostic - Oscilloscope time of DIAG STEP with ADCV_FIL of 1.04 ms.

Figure 8. Open Load Diagnostic - Oscilloscope time of VCR with ADCV_FIL of 1.04 ms

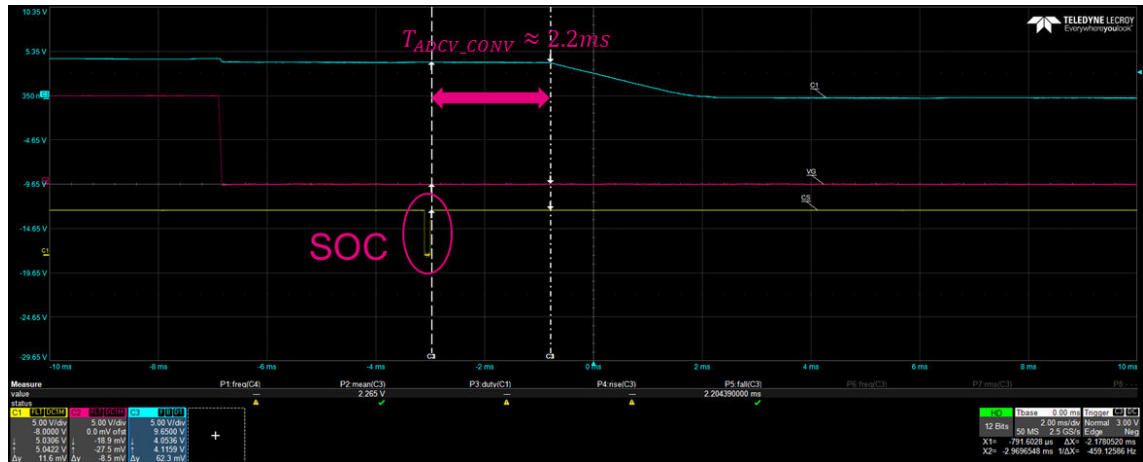
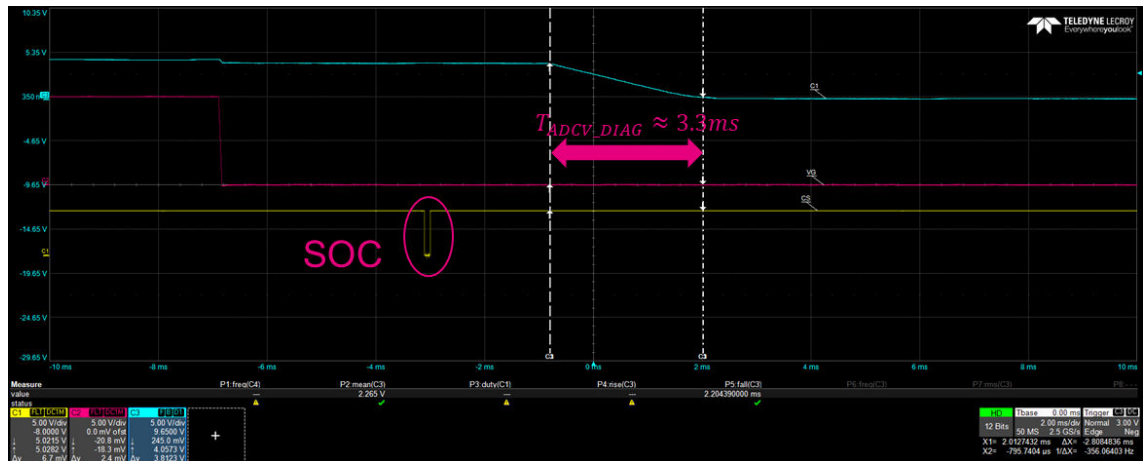


Figure 9. Open Load Diagnostic - Oscilloscope time of DIAG STEP with ADCV_FIL of 1.04 ms



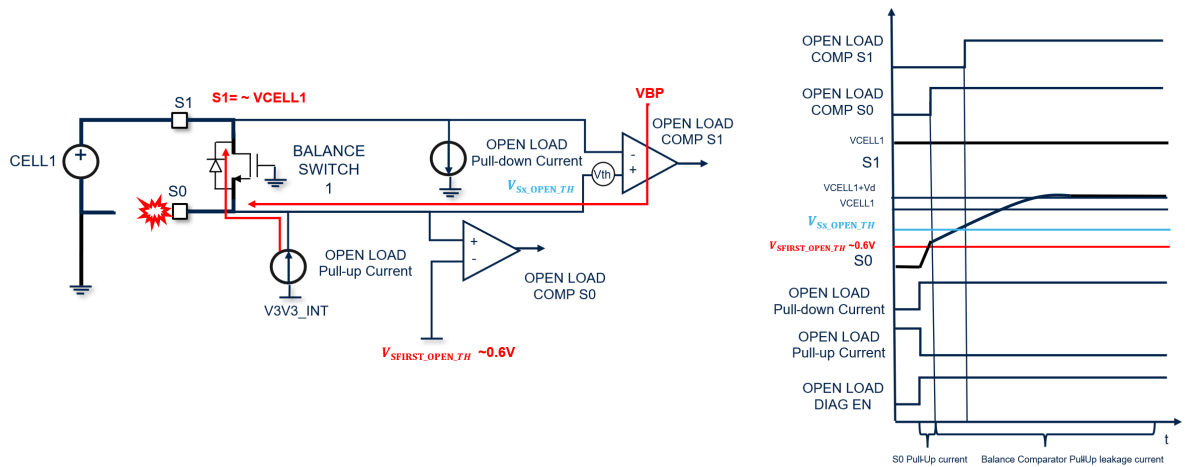
4 Open Load Diagnostic – Special behavior scenario

In the following chapter, some special cases will be analyzed where the Open Load Detection may not be correctly detected.

4.1 Special case 1

In this scenario:

Figure 10. Open Load Diagnostic - Special case 1



S_0 pin voltage is not limited to minor voltage from internal 3V3 but is pulled up by the leakage current from the balance comparator from VBP supply. S_0 voltage is then clamped by the S_1 balance switch to $V_{C1} + V_d$ (V_d diode forward voltage) that is higher than V_{th} thus triggering the S_1 open load comparator detection.

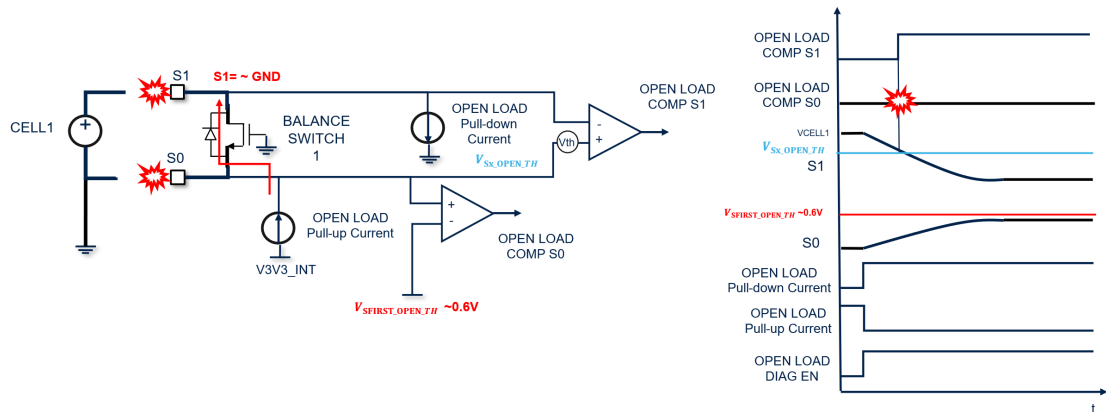
CONCLUSION:

- Open Load diagnosis on S_1 and S_0 is ensured by the combination of both SFIRST_OPEN and CELL_OPEN_DIAG1 flag results.
- Open Load is detected when either SFIRST_OPEN = '1' OR CELL_OPEN_DIAG1 = '11' OR CELL_OPEN_DIAG1 = '10'.

4.2 Special case 2

In this scenario:

Figure 11. Open Load Diagnostic - Special case 2



Since S_1 pull-down current is higher than S_0 pull-up current, the S_0 voltage is clamped by the S_1 balance switch to $GND + V_d$ (V_d diode forward voltage).

Depending on process spread and temperature, the S_0 voltage could be either above or below V_{REF} .

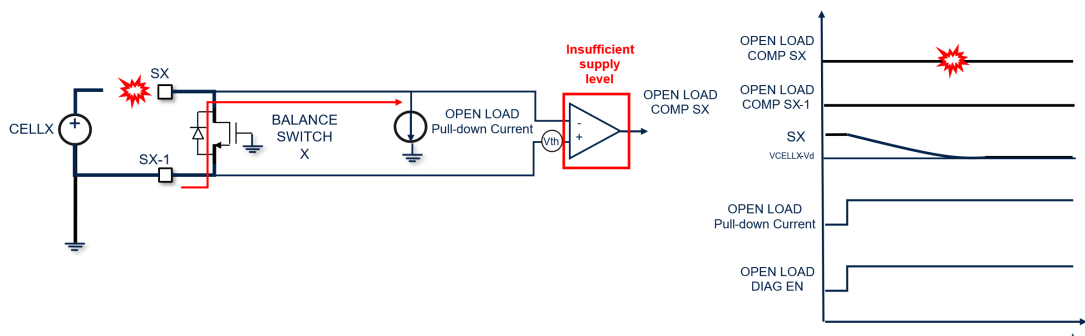
CONCLUSION:

- Open Load diagnosis on S_1 and S_0 is ensured by the combination of both SFIRST_OPN and CELL_OPEN_DIAG1 flag results.
- Open Load is detected when either SFIRST_OPEN = '1' OR CELL_OPEN_DIAG1 = '11' OR CELL_OPEN_DIAG1 = '10'.

4.3 Special case 3

In this scenario:

Figure 12. Open Load Diagnostic - Special case 3



The balance open diagnostic is supplied by VBP [S_1, S_2, S_3] and by VCP [S_4] and cells open diagnostic is supplied by VCP [C_1, C_2, C_3, C_4].

An insufficient voltage level of VBP or VCP may result in wrong diagnosis behavior [missed detection]

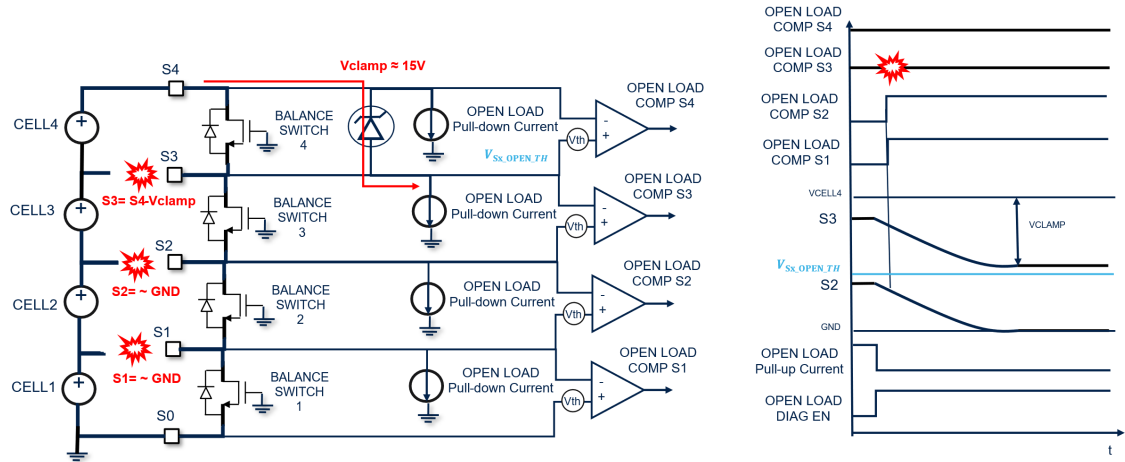
CONCLUSION:

- Open Load diagnosis is not reliable and should not be run under VBP UV or VCP UV.

4.4 Special case 4

In this scenario:

Figure 13. Open Load Diagnostic - Special case 4



The S_1/S_2 pull-down current discharges S_1/S_2 nodes to GND.

The S_3 pull-down current tries to discharge the S_3 node to GND, balance switch 4 clamp activates and limits the voltage of S_3 to S_4-V_{clamp} .

CONCLUSION:

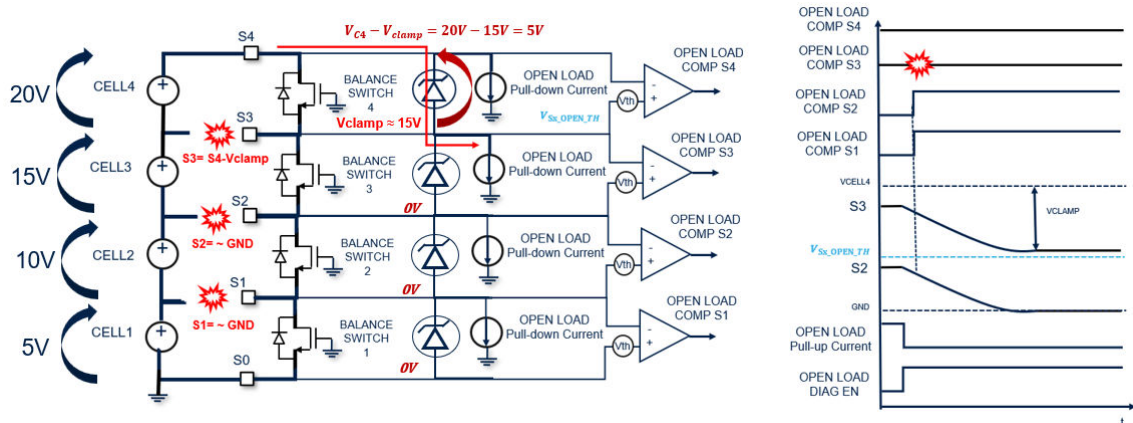
- Open Load diagnosis is not reliable for S_3

4.5 Deeper investigation on special case 4

In case of multiple open as 3 faults of Scenario 4:

- S_1 & S_2 & S_3 disconnected at any point
- $V_{C4} > 15\text{ V}$ (ex. $V_{CELL} = 5\text{ V}$)

Figure 14. Deeper investigation on special case 4



The S_1/S_2 pull-down current discharges S_1/S_2 nodes to GND. The S_3 pull-down current tries to discharge the S_3 node to GND, but the balance switch 4 clamp is activated and limits the voltage to $V_{C4}-V_{clamp}$.

4.5.1 CASE 1 - Sub case 1A

When:

- $V_{BS} > 15\text{ V}$

AND

- CELL_OPEN_DIAG1 = 1X (X = DON'T CARE)

AND

- CELL_OPEN_DIAG2 = 1X (X = DON'T CARE)

AND

- CELL_OPEN_DIAG4 = 0X (X = DON'T CARE)

All Open Load Flags are correct and can be trusted except CELL_OPEN_DIAG3.

To assess additional information VCELL3 voltage measure shall be performed. After the VCELL3 voltage measure, appears that CELL_OPEN_DIAG3 = 00, so C3 is connected and nothing can be concluded on S3 connection. So, the real state of Open Diagnostic for CELL3 is CELL_OPEN_DIAG3 = X0 (can be or balancing open or not open).

NB: SFIRST_OPEN and C0_OPEN values are always do not care.

4.5.2

CASE 1 - Sub case 1B

When:

- VBS > 15 V

AND

- CELL_OPEN_DIAG1 = 1X (X = DON'T CARE)

AND

- CELL_OPEN_DIAG2 = 1X (X = DON'T CARE)

AND

- CELL_OPEN_DIAG4 = 0X (X = DON'T CARE)

All Open Load Flags are correct and can be trusted except CELL_OPEN_DIAG3.

To assess additional information VCELL3 voltage measure shall be performed. After the VCELL3 voltage measure, it appears that CELL_OPEN_DIAG3 = 01, so C3 is connected and nothing can be concluded on S3 connection. So, the real state of Open Diagnostic for CELL3 is CELL_OPEN_DIAG3 = X0 (can be or balancing open or not open).

NB: SFIRST_OPEN and C0_OPEN value is always don't care.

4.5.3

CASE 2

When:

- VBS > 15 V (no scenario 4)

BUT

- CELL_OPEN_DIAG1 = 0X (X = DON'T CARE)

OR

- CELL_OPEN_DIAG2 = 0X (X = DON'T CARE)

OR

- CELL_OPEN_DIAG4 = 1X (X = DON'T CARE)

All Open Load Flags are correct and can be trusted: SFIRST_OPEN, C0_OPEN, CELL_OPEN_DIAG1, CELL_OPEN_DIAG2, CELL_OPEN_DIAG3, CELL_OPEN_DIAG4.

4.5.4

CASE 3

When:

- VBS < 15 V (no scenario 4)

All Open Load Flags are correct and can be trusted: SFIRST_OPEN, C0_OPEN, CELL_OPEN_DIAG1, CELL_OPEN_DIAG2, CELL_OPEN_DIAG3, CELL_OPEN_DIAG4.

5 Cell Open Detection

A battery emulator is used to generate the cell voltage for each cell (4.5 V) of L9988. The device board is equipped with switches that allow it to have different open conditions.

Chapters *Cell Open Detection–Single Open Wire* and *Cell Open Detection–Multiple Open Wire* show the results of Cell Open Detection in case of Single and Multiple Open Wire.

The results have been obtained with the following parameters:

- All cells enabled (C1, C2, C3, C4) and VBS enabled
- CX_OPEN_TH set to 1 V
- VBS_SUM_TH set to 200 mV
- CELL_DEEP_UV_TH set to 1 V
- CELL_UV_TH set to 2 V
- CELL_OV_TH set to 5 V
- SUM_UV_TH set to 8 V
- SUM_OV_TH set to 16 V
- VBS_UV_TH set to 8 V
- VBS_OV_TH set to 16 V
- ADCV_FIL set to 264 μ s, 1.04 ms, 2.04 ms, 4.16 ms, 8.32 ms, 16.64 ms and 66.56 ms.

5.1 Cell Open Detection – Single Open Wire

Figure 15. Result of CELL OPEN DIAG- single wire

	T_{ADCV_FILTR}			
	264 μ s		1.04ms	
C_0	C_0OPEN $SFIRST = 0$	C_0OPEN $SFIRST = 0$	-	-
C_1	NO CELL OPEN 1st VCR	CELL OPEN 2nd VCR	CELL OPEN 1st VCR	CELLOPEN 2nd VCR
C_2	NO CELL OPEN 1st VCR	CELL OPEN 2nd VCR	CELL OPEN 1st VCR	CELLOPEN 2nd VCR
C_3	NO CELL OPEN 1st VCR	CELL OPEN 2nd VCR	CELL OPEN 1st VCR	CELLOPEN 2nd VCR
C_4	NO CELL OPEN 1st VCR	CELL OPEN 2nd VCR	CELL OPEN 1st VCR	CELLOPEN 2nd VCR

As expected, with a minimum filter time of 264 μ s, the single cell open is not detected because the capacitors on the cell do not discharge in time. On the second SoC with the same filter time, the single open is detected because the capacitor discharge time has passed.

However, by selecting a longer filter time, such as 1.04 ms or higher, the single cell open is detected already on the first SoC.

5.2 Cell Open Detection – Multiple Open Wire

Figure 16. Result of CELL OPEN DIAG- double wire

	T_{ADC_FILTR}							
	264us		1.04ms		2.08ms		4.16ms	
$C_0 - C_1$	C_0 CELL OPEN C_1 NO CELL OPEN 1st VCR	C_0 CELL OPEN C_1 CELL OPEN 2nd VCR	C_0 CELL OPEN C_1 CELL OPEN 1st VCR	C_0 CELL OPEN C_1 CELL OPEN 2nd VCR	—	—	—	—
$C_0 - C_2$	C_0 CELL OPEN C_2 NO CELL OPEN 1st VCR	C_0 CELL OPEN C_2 CELL OPEN 2nd VCR	—	—	—	—	—	—
$C_0 - C_3$	C_0 CELL OPEN C_3 NO CELL OPEN 1st VCR	C_0 CELL OPEN C_3 CELL OPEN 2nd VCR	—	—	—	—	—	—
$C_0 - C_4$	C_0 CELL OPEN C_4 NO CELL OPEN 1st VCR	C_0 CELL OPEN C_4 CELL OPEN 2nd VCR	—	—	—	—	—	—
$C_1 - C_2$	C_1 NO CELL OPEN C_2 NO CELL OPEN 1st VCR	C_1 CELL OPEN C_2 NO CELL OPEN 2nd VCR	C_1 CELL OPEN C_2 NO CELL OPEN 1st VCR	C_1 CELL OPEN C_2 CELL OPEN 2nd VCR	C_1 CELL OPEN C_2 CELL OPEN 1st VCR	C_1 PCB OPEN C_2 PCB OPEN 2nd VCR	—	—
$C_1 - C_3$	C_1 NO CELL OPEN C_3 NO CELL OPEN 1st VCR	C_1 CELL OPEN C_3 CELL OPEN 2nd VCR	C_1 CELL OPEN C_3 CELL OPEN 1st VCR	C_1 CELL OPEN C_3 CELL OPEN 2nd VCR	—	—	—	—
$C_1 - C_4$	C_1 NO CELL OPEN C_4 NO CELL OPEN 1st VCR	C_1 CELL OPEN C_4 CELL OPEN 2nd VCR	C_1 CELL OPEN C_4 CELL OPEN 1st VCR	C_1 CELL OPEN C_4 CELL OPEN 2nd VCR	—	—	—	—
$C_2 - C_3$	C_2 NO CELL OPEN C_3 NO CELL OPEN 1st VCR	C_2 CELL OPEN C_3 NO CELL OPEN 2nd VCR	C_2 CELL OPEN C_3 NO CELL OPEN 1st VCR	C_2 CELL OPEN C_3 CELL OPEN 2nd VCR	C_2 CELL OPEN C_3 NO CELL OPEN 1st VCR	C_2 CELL OPEN C_3 CELL OPEN 2nd VCR	C_2 CELL OPEN C_3 CELL OPEN 1st VCR	C_2 CELL OPEN C_3 CELL OPEN 2nd VCR
$C_2 - C_4$	C_2 NO CELL OPEN C_4 NO CELL OPEN 1st VCR	C_2 CELL OPEN C_4 CELL OPEN 2nd VCR	C_2 CELL OPEN C_4 CELL OPEN 1st VCR	C_2 CELL OPEN C_4 CELL OPEN 2nd VCR	—	—	—	—
$C_3 - C_4$	C_3 NO CELL OPEN C_4 NO CELL OPEN 1st VCR	C_3 CELL OPEN C_4 NO CELL OPEN 2nd VCR	C_3 CELL OPEN C_4 NO CELL OPEN 1st VCR	C_3 CELL OPEN C_4 NO CELL OPEN 2nd VCR	C_3 CELL OPEN C_4 NO CELL OPEN 1st VCR	C_3 CELL OPEN C_4 CELL OPEN 2nd VCR	—	—

Figure 17. Result of CELL OPEN DIAG- triple wire

	$T_{ADC_V_FILTR}$							
	264us		1.04ms		2.08ms		4.16ms	
$C_0 - C_1 - C_2$	C_0 CELL OPEN C_1 NO CELL OPEN C_2 NO CELL OPEN 1st VCR	C_0 CELL OPEN C_1 CELL OPEN C_2 NO CELL OPEN 2nd VCR	C_0 CELL OPEN C_1 CELL OPEN C_2 NO CELL OPEN 1st VCR	C_0 CELL OPEN C_1 CELL OPEN C_2 CELL OPEN 2nd VCR	C_0 CELL OPEN C_1 CELL OPEN C_2 CELL OPEN 1st VCR	C_0 CELL OPEN C_1 CELL OPEN C_2 CELL OPEN 2nd VCR	-	-
$C_0 - C_1 - C_3$	C_0 CELL OPEN C_1 NO CELL OPEN C_3 NO CELL OPEN 1st VCR	C_0 CELL OPEN C_1 CELL OPEN C_3 CELL OPEN 2nd VCR	C_0 CELL OPEN C_1 CELL OPEN C_3 CELL OPEN 1st VCR	C_0 CELL OPEN C_1 CELL OPEN C_3 CELL OPEN 2nd VCR	-	-	-	-
$C_0 - C_1 - C_4$	C_0 CELL OPEN C_1 NO CELL OPEN C_4 CELL OPEN 1st VCR	C_0 CELL OPEN C_1 CELL OPEN C_4 CELL OPEN 2nd VCR	C_0 CELL OPEN C_1 CELL OPEN C_4 CELL OPEN 1st VCR	C_0 CELL OPEN C_1 CELL OPEN C_4 CELL OPEN 2nd VCR	-	-	-	-
$C_0 - C_2 - C_3$	C_0 CELL OPEN C_2 NO CELL OPEN C_3 NO CELL OPEN 1st VCR	C_0 CELL OPEN C_2 CELL OPEN C_3 NO CELL OPEN 2nd VCR	C_0 CELL OPEN C_2 CELL OPEN C_3 NO CELL OPEN 1st VCR	C_0 CELL OPEN C_2 CELL OPEN C_3 CELL OPEN 2nd VCR	C_0 CELL OPEN C_2 CELL OPEN C_3 CELL OPEN 1st VCR	C_0 CELL OPEN C_2 CELL OPEN C_3 CELL OPEN 2nd VCR	C_0 CELL OPEN C_2 CELL OPEN C_3 CELL OPEN 1st VCR	C_0 CELL OPEN C_2 CELL OPEN C_3 CELL OPEN 2nd VCR
$C_0 - C_2 - C_4$	C_0 CELL OPEN C_2 NO CELL OPEN C_4 NO CELL OPEN 1st VCR	C_0 CELL OPEN C_2 CELL OPEN C_4 CELL OPEN 2nd VCR	C_0 CELL OPEN C_2 CELL OPEN C_4 CELL OPEN 1st VCR	C_0 CELL OPEN C_2 CELL OPEN C_4 CELL OPEN 2nd VCR	-	-	-	-
$C_0 - C_3 - C_4$	C_0 CELL OPEN C_3 NO CELL OPEN C_4 NO CELL OPEN 1st VCR	C_0 CELL OPEN C_3 CELL OPEN C_4 NO CELL OPEN 2nd VCR	C_0 CELL OPEN C_3 CELL OPEN C_4 NO CELL OPEN 1st VCR	C_0 CELL OPEN C_3 CELL OPEN C_4 NO CELL OPEN 2nd VCR	C_0 CELL OPEN C_3 CELL OPEN C_4 NO CELL OPEN 1st VCR	C_0 CELL OPEN C_3 CELL OPEN C_4 CELL OPEN 2nd VCR	C_0 CELL OPEN C_3 CELL OPEN C_4 CELL OPEN 1st VCR	C_0 CELL OPEN C_3 CELL OPEN C_4 CELL OPEN 2nd VCR
$C_1 - C_2 - C_3$	C_1 NO CELL OPEN C_2 NO CELL OPEN C_3 NO CELL OPEN 1st VCR	C_1 CELL OPEN C_2 NO CELL OPEN C_3 NO CELL OPEN 2nd VCR	C_1 CELL OPEN C_2 NO CELL OPEN C_3 NO CELL OPEN 1st VCR	C_1 CELL OPEN C_2 CELL OPEN C_3 CELL OPEN 2nd VCR	C_1 CELL OPEN C_2 CELL OPEN C_3 CELL OPEN 1st VCR	C_1 CELL OPEN C_2 CELL OPEN C_3 CELL OPEN 2nd VCR	C_1 CELL OPEN C_2 CELL OPEN C_3 CELL OPEN 1st VCR	C_1 CELL OPEN C_2 CELL OPEN C_3 CELL OPEN 2nd VCR
$C_1 - C_2 - C_4$	C_1 NO CELL OPEN C_2 NO CELL OPEN C_4 CELL OPEN 1st VCR	C_1 CELL OPEN C_2 NO CELL OPEN C_4 CELL OPEN 2nd VCR	C_1 CELL OPEN C_2 NO CELL OPEN C_4 CELL OPEN 1st VCR	C_1 CELL OPEN C_2 CELL OPEN C_4 CELL OPEN 2nd VCR	C_1 CELL OPEN C_2 CELL OPEN C_4 CELL OPEN 1st VCR	C_1 CELL OPEN C_2 CELL OPEN C_4 CELL OPEN 2nd VCR	-	-
$C_1 - C_3 - C_4$	C_1 NO CELL OPEN C_3 NO CELL OPEN C_4 NO CELL OPEN 1st VCR	C_1 CELL OPEN C_3 CELL OPEN C_4 NO CELL OPEN 2nd VCR	C_1 CELL OPEN C_3 CELL OPEN C_4 NO CELL OPEN 1st VCR	C_1 CELL OPEN C_3 CELL OPEN C_4 NO CELL OPEN 2nd VCR	C_1 CELL OPEN C_3 CELL OPEN C_4 NO CELL OPEN 1st VCR	C_1 CELL OPEN C_3 CELL OPEN C_4 CELL OPEN 2nd VCR	C_1 CELL OPEN C_3 CELL OPEN C_4 CELL OPEN 1st VCR	C_1 CELL OPEN C_3 CELL OPEN C_4 CELL OPEN 2nd VCR
$C_2 - C_3 - C_4$	C_2 NO CELL OPEN C_3 NO CELL OPEN C_4 NO CELL OPEN 1st VCR	C_2 CELL OPEN C_3 NO CELL OPEN C_4 NO CELL OPEN 2nd VCR	C_2 CELL OPEN C_3 NO CELL OPEN C_4 NO CELL OPEN 1st VCR	C_2 CELL OPEN C_3 CELL OPEN C_4 NO CELL OPEN 2nd VCR	C_2 CELL OPEN C_3 CELL OPEN C_4 NO CELL OPEN 1st VCR	C_2 CELL OPEN C_3 CELL OPEN C_4 CELL OPEN 2nd VCR	C_2 CELL OPEN C_3 CELL OPEN C_4 CELL OPEN 1st VCR	C_2 CELL OPEN C_3 CELL OPEN C_4 CELL OPEN 2nd VCR

6 Balancing Open Detection

A battery emulator is used to generate the cell voltage for each cell (4.5 V) of L9988. The device board is equipped with switches that allow it to have different open conditions.

Chapters *Balancing Open Detection–Single Open Wire* and *Balancing Open Detection–Multiple Open Wire* show the results of Cell Open Detection in case of Single and Multiple Open Wire.

The results have been obtained with the following parameters:

- All cells enabled (C1, C2, C3, C4) and VBS enabled
- CX_OPEN_TH set to 1 V
- VBS_SUM_TH set to 200 mV
- CELL_DEEP_UV_TH set to 1 V
- CELL_UV_TH set to 2 V
- CELL_OV_TH set to 5 V
- SUM_UV_TH set to 8 V
- SUM_OV_TH set to 16 V
- VBS_UV_TH set to 8 V
- VBS_OV_TH set to 16 V

ADCV_FIL set to 264 μ s, 1.04 ms, 2.04 ms, 4.16 ms, 8.32 ms, 16.64 ms and 66.56 ms.

6.1 Balancing Open Detection – Single Open Wire

Figure 18. Result of BAL OPEN DIAG-single wire

	T_{ADCV_FILTR}			
	264 μ s		1.04ms	
S_0	<i>NO BAL OPEN</i> <i>1st VCR</i>	<i>S₀BAL OPEN</i> <i>SFIRST=1</i>	<i>S₀BAL OPEN</i> <i>SFIRST=1</i>	<i>S₀BAL OPEN</i> <i>SFIRST=1</i>
S_1	<i>NO BAL OPEN</i> <i>1st VCR</i>	<i>BAL OPEN</i> <i>2nd VCR</i>	<i>BAL OPEN</i> <i>1st VCR</i>	<i>BAL OPEN</i> <i>2nd VCR</i>
S_2	<i>NO BAL OPEN</i> <i>1st VCR</i>	<i>BAL OPEN</i> <i>2nd VCR</i>	<i>BAL OPEN</i> <i>1st VCR</i>	<i>BAL OPEN</i> <i>2nd VCR</i>
S_3	<i>NO BAL OPEN</i> <i>1st VCR</i>	<i>BAL OPEN</i> <i>2nd VCR</i>	<i>BAL OPEN</i> <i>1st VCR</i>	<i>BAL OPEN</i> <i>2nd VCR</i>
S_4	<i>NO BAL OPEN</i> <i>1st VCR</i>	<i>BAL OPEN</i> <i>2nd VCR</i>	<i>BAL OPEN</i> <i>1st VCR</i>	<i>BAL OPEN</i> <i>2nd VCR</i>

As expected, with a minimum filter time of 264 μ s, the single balancing open is not detected because the capacitors on the balancing path do not discharge in time. On the second SoC with the same filter time, the single open is detected because the capacitor discharge time has passed.

However, by selecting a longer filter time, such as 1.04 ms or higher, the single balancing open is detected already on the first SoC.

6.2 Balancing Open Detection – Multiple Open Wires

Figure 19. Result of BAL OPEN DIAG-double wire

	T_{ADCV_FILTR}							
	264us		1.04ms		2.08ms		4.16ms	
$S_0 - S_1$	S_0 NO BAL OPEN S_1 NO BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN 2nd VCR	S_0 NO BAL OPEN S_1 BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN 2nd VCR	S_0 NO BAL OPEN S_1 BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN 2nd VCR	S_0 NO BAL OPEN S_1 BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN 2nd VCR
$S_0 - S_2$	S_0 NO BAL OPEN S_2 NO BAL OPEN 1st VCR	S_0 BAL OPEN S_2 BAL OPEN 2nd VCR	S_0 BAL OPEN S_2 BAL OPEN 1st VCR	S_0 BAL OPEN S_2 BAL OPEN 2nd VCR	—	—	—	—
$S_0 - S_3$	S_0 NO BAL OPEN S_3 NO BAL OPEN 1st VCR	S_0 BAL OPEN S_3 NO BAL OPEN 2nd VCR	S_0 BAL OPEN S_3 BAL OPEN 1st VCR	S_0 BAL OPEN S_3 BAL OPEN 2nd VCR	—	—	—	—
$S_0 - S_4$	S_0 NO BAL OPEN S_4 NO BAL OPEN 1st VCR	S_0 BAL OPEN S_4 BAL OPEN 2nd VCR	S_0 BAL OPEN S_4 BAL OPEN 1st VCR	S_0 BAL OPEN S_4 BAL OPEN 2nd VCR	—	—	—	—
$S_1 - S_2$	S_1 BAL OPEN S_2 NO BAL OPEN 1st VCR	S_1 BAL OPEN S_2 NO BAL OPEN 2nd VCR	S_1 BAL OPEN S_2 BAL OPEN 1st VCR	S_1 BAL OPEN S_2 BAL OPEN 2nd VCR	—	—	—	—
$S_1 - S_3$	S_1 NO BAL OPEN S_3 NO BAL OPEN 1st VCR	S_1 BAL OPEN S_3 NO BAL OPEN 2nd VCR	S_1 BAL OPEN S_3 BAL OPEN 1st VCR	S_1 BAL OPEN S_3 BAL OPEN 2nd VCR	—	—	—	—
$S_1 - S_4$	S_1 NO BAL OPEN S_4 NO BAL OPEN 1st VCR	S_1 BAL OPEN S_4 BAL OPEN 2nd VCR	S_1 BAL OPEN S_4 BAL OPEN 1st VCR	S_1 BAL OPEN S_4 BAL OPEN 2nd VCR	—	—	—	—
$S_2 - S_3$	S_2 BAL OPEN S_3 NO BAL OPEN 1st VCR	S_2 BAL OPEN S_3 NO BAL OPEN 2nd VCR	S_2 BAL OPEN S_3 BAL OPEN 1st VCR	S_2 BAL OPEN S_3 BAL OPEN 2nd VCR	—	—	—	—
$S_2 - S_4$	S_2 NO CELL OPEN S_4 NO CELL OPEN 1st VCR	S_2 CELL OPEN S_4 CELL OPEN 2nd VCR	S_2 CELL OPEN S_4 CELL OPEN 1st VCR	S_2 CELL OPEN S_4 CELL OPEN 2nd VCR	—	—	—	—
$S_3 - S_4$	S_3 BAL OPEN S_4 BAL OPEN 1st VCR	S_3 BAL OPEN S_4 BAL OPEN 2nd VCR	—	—	—	—	—	—

The double open on when S_0 and S_1 (blue rectangle) is never detected and can be classified in Section 4.2: Special case 2.

Figure 20. Result of BAL OPEN DIAG-triple wire

	T_{ADCV_FILTR}							
	264us		1.04ms		2.08ms		4.16ms	
$S_0 - S_1 - S_2$	S_0 NO BAL OPEN S_1 NO BAL OPEN S_2 NO BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_2 NO BAL OPEN 2nd VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_2 BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_2 BAL OPEN 2nd VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_2 BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_2 BAL OPEN 2nd VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_2 BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_2 BAL OPEN 2nd VCR
$S_0 - S_1 - S_3$	S_0 NO BAL OPEN S_1 NO BAL OPEN S_3 NO BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 NO BAL OPEN S_3 NO BAL OPEN 2nd VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_3 BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_3 BAL OPEN 2nd VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_3 BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_3 BAL OPEN 2nd VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_3 BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_3 BAL OPEN 2nd VCR
$S_0 - S_1 - S_4$	S_0 NO BAL OPEN S_1 NO BAL OPEN S_4 NO BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 NO BAL OPEN S_4 BAL OPEN 2nd VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_4 BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_4 BAL OPEN 2nd VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_4 BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_4 BAL OPEN 2nd VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_4 BAL OPEN 1st VCR	S_0 NO BAL OPEN S_1 BAL OPEN S_4 BAL OPEN 2nd VCR
$S_0 - S_2 - S_3$	S_0 NO BAL OPEN S_2 BAL OPEN S_3 NO BAL OPEN 1st VCR	S_0 BAL OPEN S_2 BAL OPEN S_3 NO BAL OPEN 2nd VCR	S_0 BAL OPEN S_2 BAL OPEN S_3 BAL OPEN 1st VCR	S_0 BAL OPEN S_2 BAL OPEN S_3 BAL OPEN 2nd VCR	-	-	-	-
$S_0 - S_2 - S_4$	S_0 NO BAL OPEN S_2 NO BAL OPEN S_4 NO BAL OPEN 1st VCR	S_0 BAL OPEN S_2 BAL OPEN S_4 BAL OPEN 2nd VCR	S_0 BAL OPEN S_2 BAL OPEN S_4 BAL OPEN 1st VCR	S_0 BAL OPEN S_2 BAL OPEN S_4 BAL OPEN 2nd VCR	-	-	-	-
$S_0 - S_3 - S_4$	S_0 NO BAL OPEN S_3 BAL OPEN S_4 BAL OPEN 1st VCR	S_0 BAL OPEN S_3 BAL OPEN S_4 BAL OPEN 2nd VCR	S_0 BAL OPEN S_3 BAL OPEN S_4 BAL OPEN 1st VCR	S_0 BAL OPEN S_3 BAL OPEN S_4 BAL OPEN 2nd VCR	-	-	-	-
$S_1 - S_2 - S_3$	S_1 BAL OPEN S_2 NO BAL OPEN S_3 NO BAL OPEN 1st VCR	S_1 BAL OPEN S_2 BAL OPEN S_3 NO BAL OPEN 2nd VCR	S_1 BAL OPEN S_2 BAL OPEN S_3 NO BAL OPEN 1st VCR	S_1 BAL OPEN S_2 BAL OPEN S_3 NO BAL OPEN 2nd VCR	S_1 BAL OPEN S_2 BAL OPEN S_3 NO BAL OPEN 1st VCR	S_1 BAL OPEN S_2 BAL OPEN S_3 NO BAL OPEN 2nd VCR	S_1 BAL OPEN S_2 BAL OPEN S_3 NO BAL OPEN 1st VCR	S_1 BAL OPEN S_2 BAL OPEN S_3 NO BAL OPEN 2nd VCR
$S_1 - S_2 - S_4$	S_1 BAL OPEN S_2 NO BAL OPEN S_4 NO BAL OPEN 1st VCR	S_1 BAL OPEN S_2 NO BAL OPEN S_4 BAL OPEN 2nd VCR	S_1 BAL OPEN S_2 BAL OPEN S_4 BAL OPEN 1st VCR	S_1 BAL OPEN S_2 BAL OPEN S_4 BAL OPEN 2nd VCR	-	-	-	-
$S_1 - S_3 - S_4$	S_1 NO BAL OPEN S_3 BAL OPEN S_4 BAL OPEN 1st VCR	S_1 BAL OPEN S_3 BAL OPEN S_4 BAL OPEN 2nd VCR	S_1 BAL OPEN S_3 BAL OPEN S_4 BAL OPEN 1st VCR	S_1 BAL OPEN S_3 BAL OPEN S_4 BAL OPEN 2nd VCR	-	-	-	-
$S_2 - S_3 - S_4$	S_2 BAL OPEN S_3 BAL OPEN S_4 BAL OPEN 1st VCR	S_2 BAL OPEN S_3 BAL OPEN S_4 BAL OPEN 2nd VCR	S_2 BAL OPEN S_3 BAL OPEN S_4 BAL OPEN 1st VCR	S_2 BAL OPEN S_3 BAL OPEN S_4 BAL OPEN 2nd VCR	-	-	-	-

The triple opens on when S_0 , S_1 and S_2 or S_0 , S_1 and S_3 or S_0 , S_1 and S_4 (blue rectangle) are never detected and can be classified in [Section 4.2: Special case 2](#).

The triple opens on when S_1 , S_2 and S_3 (orange rectangle) is never detected and can be classified in [Section 4.4: Special case 4](#)

7 PCB Open Detection

A battery emulator is used to generate the cell voltage for each cell (4.5 V) of L9988. The device board is equipped with switches that allow it to have different open conditions.

Chapters *PCB Open Detection–Single Open Wire* and *PCB Open Detection–Multiple Open Wire* show the results of Cell Open Detection in case of Single and Multiple Open Wire.

The results have been obtained with the following parameters:

- All cells enabled (C1, C2, C3, C4) and VBS enabled
- CX_OPEN_TH set to 1 V
- VBS_SUM_TH set to 200 mV
- CELL_DEEP_UV_TH set to 1 V
- CELL_UV_TH set to 2 V
- CELL_OV_TH set to 5 V
- SUM_UV_TH set to 8 V
- SUM_OV_TH set to 16 V
- VBS_UV_TH set to 8 V
- VBS_OV_TH set to 16 V

ADCV_FIL set to 264 μ s, 1.04 ms, 2.04 ms, 4.16 ms, 8.32 ms, 16.64 ms and 66.56 ms

7.1 PCB Open Detection – Single Open Wire

Figure 21. Result of PCB OPEN DIAG-single wire

	T_{ADCV_FILTR}				
	264 μ s		1.04ms		2.08ms
PCB_0	<i>C₀ OPEN NO SFIRST</i>	<i>C₀ OPEN SFIRST = 1</i>	<i>C₀ OPEN SFIRST = 1</i>	<i>C₀ OPEN SFIRST = 1</i>	-
PCB_1	<i>NO PCB OPEN 1st VCR</i>	<i>PCB OPEN 2nd VCR</i>	<i>PCB OPEN 1st VCR</i>	<i>PCB OPEN 2nd VCR</i>	-
PCB_2	<i>NO PCB OPEN 1st VCR</i>	<i>PCB OPEN 2nd VCR</i>	<i>PCB OPEN 1st VCR</i>	<i>PCB OPEN 2nd VCR</i>	-
PCB_3	<i>NO PCB OPEN 1st VCR</i>	<i>CELL OPEN 2nd VCR</i>	<i>PCB OPEN 1st VCR</i>	<i>PCB OPEN 2nd VCR</i>	-
PCB_4	<i>NO PCB OPEN 1st VCR</i>	<i>PCB OPEN 2nd VCR</i>	<i>PCB OPEN 1st VCR</i>	<i>PCB OPEN 2nd VCR</i>	-

As expected, with a minimum filter time of 264 μ s, the single PCB open is not detected because the cell capacitors, balancing capacitors and ESD capacitors do not discharge in time. On the second SoC with the same filter time, the single PCB open is detected because the capacitors discharge time has passed.

However, by choosing a longer filter time, such as 1.04ms or higher, the single PCB open is detected already on the first SoC.

7.2 PCB Open Detection – Multiple Open Wires

Figure 22. Result of PCB OPEN DIAG-double wire

	T_{ADCV_FILTR}							
	264us		1.04ms		2.08ms		4.16ms	
$PCB_0 - PCB_1$	C_0 CELL OPEN SFIRST=0 PCB ₁ NO PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ NO PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN 2nd VCR
$PCB_0 - PCB_2$	C_0 CELL OPEN SFIRST=0 PCB ₂ NO PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₂ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=1 PCB ₂ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₂ PCB OPEN 2nd VCR	-	-	-	-
$PCB_0 - PCB_3$	C_0 CELL OPEN SFIRST=0 PCB ₃ NO PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₃ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=1 PCB ₃ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₃ PCB OPEN 2nd VCR	-	-	-	-
$PCB_0 - PCB_4$	C_0 CELL OPEN SFIRST=0 PCB ₄ NO PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₄ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=1 PCB ₄ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₄ PCB OPEN 2nd VCR	-	-	-	-
$PCB_1 - PCB_2$	S_1 BAL OPEN PCB ₂ NO PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₂ NO PCB OPEN 2nd VCR	PCB ₁ PCB OPEN S_2 BAL OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₂ PCB OPEN 2nd VCR	PCB ₁ PCB OPEN PCB ₂ PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₂ PCB OPEN 2nd VCR	-	-
$PCB_1 - PCB_3$	PCB ₁ NO PCB OPEN PCB ₃ NO PCB OPEN 1st VCR	PCB ₁ PCB OPEN C_3 CELL OPEN 2nd VCR	PCB ₁ PCB OPEN PCB ₃ PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₃ PCB OPEN 2nd VCR	-	-	-	-
$PCB_1 - PCB_4$	PCB ₁ NO PCB OPEN PCB ₄ PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₄ PCB OPEN 2nd VCR	PCB ₁ PCB OPEN PCB ₄ PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₄ PCB OPEN 2nd VCR	-	-	-	-
$PCB_2 - PCB_3$	S_2 BAL OPEN PCB ₃ NO PCB OPEN 1st VCR	PCB ₂ PCB OPEN PCB ₃ NO PCB OPEN 2nd VCR	PCB ₂ PCB OPEN S_3 BAL OPEN 1st VCR	PCB ₂ PCB OPEN PCB ₃ PCB OPEN 2nd VCR	PCB ₂ PCB OPEN PCB ₃ PCB OPEN 1st VCR	PCB ₂ PCB OPEN PCB ₃ PCB OPEN 2nd VCR	-	-
$PCB_2 - PCB_4$	PCB ₂ NO PCB OPEN PCB ₄ NO PCB OPEN 1st VCR	PCB ₂ PCB OPEN PCB ₄ PCB OPEN 2nd VCR	PCB ₂ PCB OPEN PCB ₄ PCB OPEN 1st VCR	PCB ₂ PCB OPEN PCB ₄ PCB OPEN 2nd VCR	-	-	-	-
$PCB_3 - PCB_4$	S_3 BAL OPEN S_4 BAL OPEN 1st VCR	PCB ₃ PCB OPEN S_4 BAL OPEN 2nd VCR	PCB ₃ PCB OPEN S_4 BAL OPEN 1st VCR	PCB ₃ PCB OPEN S_4 BAL OPEN 2nd VCR	PCB ₃ PCB OPEN S_4 BAL OPEN 1st VCR	PCB ₃ PCB OPEN PCB ₄ PCB OPEN 2nd VCR	PCB ₃ PCB OPEN PCB ₄ PCB OPEN 1st VCR	PCB ₃ PCB OPEN PCB ₄ PCB OPEN 2nd VCR

The double open on when PCB_0 and PCB_1 (blue rectangle) is never detected and can be classified in Section 4.2: Special case 2.

Figure 23. Result of PCB OPEN DIAG-triple wire

	T_{ADCV_FILTR}							
	264us		1.04ms		2.08ms		4.16ms	
$PCB_0 - PCB_1 - PCB_2$	C_0 CELL OPEN SFIRST=0 PCB ₁ NO PCB OPEN PCB ₂ NO PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₂ NO PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₂ NO PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₂ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₂ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₂ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₂ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₂ PCB OPEN 2nd VCR
$PCB_0 - PCB_1 - PCB_3$	C_0 CELL OPEN SFIRST=0 PCB ₁ NO PCB OPEN PCB ₃ NO PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ NO PCB OPEN PCB ₃ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₃ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₃ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₃ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₃ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₃ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₃ PCB OPEN 2nd VCR
$PCB_0 - PCB_1 - PCB_4$	C_0 CELL OPEN SFIRST=0 PCB ₁ NO PCB OPEN PCB ₄ NO PCB OPEN 1st VCR	C_0 NO CELL OPEN SFIRST=0 PCB ₁ NO PCB OPEN PCB ₄ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₄ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₄ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₄ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₄ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₄ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=0 PCB ₁ PCB OPEN PCB ₄ PCB OPEN 2nd VCR
$PCB_0 - PCB_2 - PCB_3$	C_0 CELL OPEN SFIRST=0 PCB ₂ NO PCB OPEN PCB ₃ NO PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₂ PCB OPEN PCB ₃ NO PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=1 PCB ₂ PCB OPEN PCB ₃ NO PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₂ PCB OPEN PCB ₃ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=1 PCB ₂ PCB OPEN PCB ₃ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₂ PCB OPEN PCB ₃ PCB OPEN 2nd VCR	-	-
$PCB_0 - PCB_2 - PCB_4$	C_0 CELL OPEN SFIRST=0 PCB ₂ NO PCB OPEN PCB ₄ NO PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₂ PCB OPEN PCB ₄ PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=1 PCB ₂ PCB OPEN PCB ₄ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₂ PCB OPEN PCB ₄ PCB OPEN 2nd VCR	-	-	-	-
$PCB_0 - PCB_3 - PCB_4$	C_0 CELL OPEN SFIRST=0 PCB ₃ NO PCB OPEN PCB ₄ NO PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₃ PCB OPEN PCB ₄ NO PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=1 PCB ₃ PCB OPEN PCB ₄ NO PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₃ PCB OPEN PCB ₄ NO PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=1 PCB ₃ PCB OPEN PCB ₄ NO PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₃ PCB OPEN PCB ₄ NO PCB OPEN 2nd VCR	C_0 CELL OPEN SFIRST=1 PCB ₃ PCB OPEN PCB ₄ PCB OPEN 1st VCR	C_0 CELL OPEN SFIRST=1 PCB ₃ PCB OPEN PCB ₄ PCB OPEN 2nd VCR
$PCB_1 - PCB_2 - PCB_3$	PCB ₁ NO PCB OPEN PCB ₂ NO PCB OPEN PCB ₃ NO PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₂ NO PCB OPEN PCB ₃ NO PCB OPEN 2nd VCR	PCB ₁ PCB OPEN PCB ₂ NO PCB OPEN PCB ₃ NO PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₂ PCB OPEN PCB ₃ NO PCB OPEN 2nd VCR	PCB ₁ PCB OPEN PCB ₂ PCB OPEN PCB ₃ NO PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₂ PCB OPEN PCB ₃ NO PCB OPEN 2nd VCR	PCB ₁ PCB OPEN PCB ₂ NO PCB OPEN PCB ₃ NO PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₂ NO PCB OPEN PCB ₃ NO PCB OPEN 2nd VCR
$PCB_1 - PCB_2 - PCB_4$	PCB ₁ NO PCB OPEN PCB ₂ NO PCB OPEN PCB ₄ NO PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₂ NO PCB OPEN PCB ₄ PCB OPEN 2nd VCR	PCB ₁ PCB OPEN PCB ₂ NO PCB OPEN PCB ₄ PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₂ PCB OPEN PCB ₄ PCB OPEN 2nd VCR	PCB ₁ PCB OPEN PCB ₂ PCB OPEN PCB ₄ PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₂ PCB OPEN PCB ₄ PCB OPEN 2nd VCR	-	-
$PCB_1 - PCB_3 - PCB_4$	PCB ₁ NO PCB OPEN PCB ₃ NO PCB OPEN PCB ₄ NO PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₃ PCB OPEN PCB ₄ NO PCB OPEN 2nd VCR	PCB ₁ PCB OPEN PCB ₃ PCB OPEN PCB ₄ NO PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₃ PCB OPEN PCB ₄ NO PCB OPEN 2nd VCR	PCB ₁ PCB OPEN PCB ₃ PCB OPEN PCB ₄ NO PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₃ PCB OPEN PCB ₄ NO PCB OPEN 2nd VCR	PCB ₁ PCB OPEN PCB ₃ PCB OPEN PCB ₄ PCB OPEN 1st VCR	PCB ₁ PCB OPEN PCB ₃ PCB OPEN PCB ₄ PCB OPEN 2nd VCR
$PCB_2 - PCB_3 - PCB_4$	PCB ₂ NO PCB OPEN PCB ₃ NO PCB OPEN PCB ₄ NO PCB OPEN 1st VCR	PCB ₂ PCB OPEN PCB ₃ NO PCB OPEN PCB ₄ NO PCB OPEN 2nd VCR	PCB ₂ PCB OPEN PCB ₃ NO PCB OPEN PCB ₄ NO PCB OPEN 1st VCR	PCB ₂ PCB OPEN PCB ₃ PCB OPEN PCB ₄ NO PCB OPEN 2nd VCR	PCB ₂ PCB OPEN PCB ₃ PCB OPEN PCB ₄ NO PCB OPEN 1st VCR	PCB ₂ PCB OPEN PCB ₃ PCB OPEN PCB ₄ NO PCB OPEN 2nd VCR	PCB ₂ PCB OPEN PCB ₃ PCB OPEN PCB ₄ PCB OPEN 1st VCR	PCB ₂ PCB OPEN PCB ₃ PCB OPEN PCB ₄ PCB OPEN 2nd VCR

The triple opens on when PCB₀, PCB₁ and PCB₂ or PCB₀, PCB₁ and PCB₃ or PCB₀, PCB₁ and PCB₄ (blue rectangle) are never detected and can be classified in [Section 4.2: Special case 2](#).

The triple opens on when PCB₁, PCB₂ and PCB₃ (orange rectangle) is never detected and can be classified in [Section 4.4: Special case 4](#).

Revision history

Table 5. Document revision history

Date	Version	Changes
04-Aug-2026	1	Initial release.

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