AN6533

Application note

Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages

Introduction

This application note provides guidelines for the handling and board mounting of QFN and SON packages including recommendations for printed-circuit board (PCB) design, board mounting, and rework. Generic information of package properties such as moisture sensitivity level (MSL) rating, board level reliability, mechanical and thermal resistance data are also provided. Semiconductor components are electrical (ESD) and mechanical sensitive devices. Proper precautions for handling, packing and processing are described.

1 SON and QFN packages

1.1 Package description

The small outline no-lead (SON)/quad flat no-lead (QFN) is a small size, lead-less plastic package with a low profile, moderate thermal dissipation, and good electrical performance. It is a surface mount package with metallized terminal pads located at the bottom surface of the package. SON have terminal pads along two opposite edges of the package versus QFN with terminal pads along the four edges of the bottom surface. SON is sometimes also referred as DFN: dual flat no-lead package.

QFN/SON are also designed with the die attach pad exposed at the bottom side to create an efficient heat path to the PCB. Heat transfer can be further facilitated by metal vias in the thermal land pattern of the PCB. The exposed pad also enables ground connection.

QFN/SON are suitable for a broad range of applications in consumer, industrial, and automotive area, including sensor and power applications.

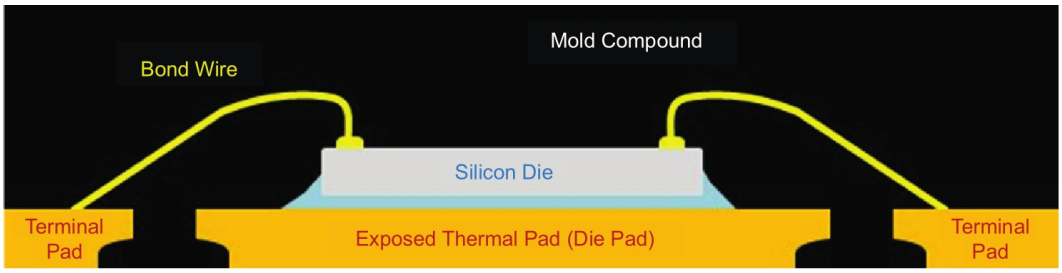
QFN/SON main features are:

- Package size: 1 × 1 mm² to 6 × 6 mm²
- Maximum seated height: 0.35 mm to 2.10 mm (standard: 0.85 mm)
- Terminal counts: Single row 4 to 72
- Terminal pitch: 0.4 mm to 1 mm
- Terminal plating: Ni-Pd-Au, Sn
- Meets RoHS, ELV and REACH
- Halogen-free and lead-free compliant

1.2 Package design

Figure 1. Cross-section of a sawn QFN with exposed pad shows a cross-section of a typical sawn QFN/SON. The package design is leadframe based. The die is usually glued to the die pad of the leadframe, either with a conductive or nonconductive adhesive. Electrical interconnections from the die to the terminal pads are made with wire bonding. The die pad is exposed external to the package.

Figure 1. Cross-section of a sawn QFN with exposed pad



Chip-on-lead (COL) package designs enable a near chip-scale integration (Figure 2. Chip-on-lead (COL) package design). The die is placed on internally extended terminal fingers using an insulating, but thermally conductive adhesive. This allows a larger die to be assembled in the same package size using conventional wire bonding, and also enables flip chip interconnects with solder bumps or copper pillars.

Figure 2. **Chip-on-lead (COL) package design**

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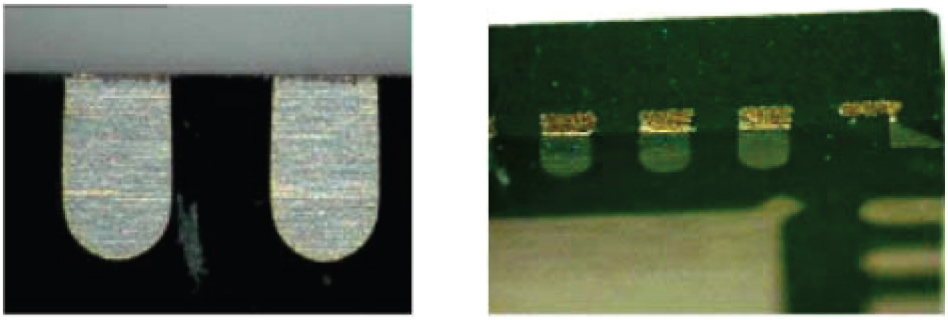
1.3 Package terminal types

QFN/SON terminal pads can vary in design, shape, and dimensions. Two different terminal designs are common for sawn QFN distinguishable by the geometry of the outer terminal ends.

1.3.1 Fully-exposed terminal ends

This is the standard design of QFN/SON packages (Figure 3. Fully-exposed terminal ends (package bottom and side view)). Terminal ends are exposed all the way to the edge of the package when viewed from the bottom of the package. The lead ends are fully exposed to the side of the package. It is possible that a solder fillet is formed up the side of the component if the terminal end is properly wetted. This may not be the case if the bare copper has been oxidized during the dry-bake step or during customer storage.

Figure 3. **Fully-exposed terminal ends (package bottom and side view)**



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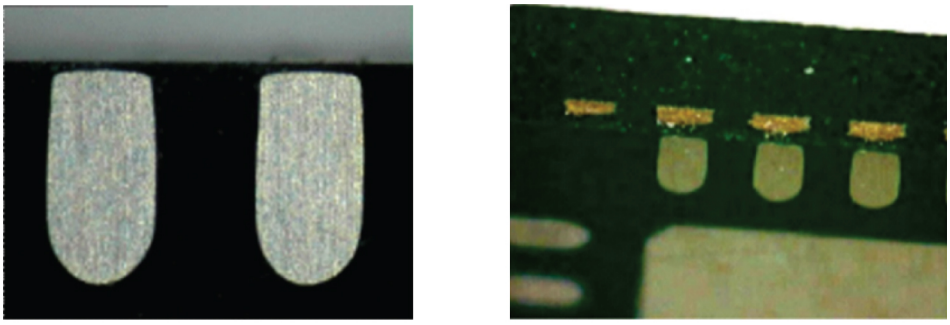
1.3.2 Pull-back terminal ends

The terminal ends are pulled back from the package edge (Figure 4. Pull-back terminal ends (package bottom and side view)). Mold compound is visible at the package edge between the edge and the end of the terminal when viewed from the package bottom side. The terminal end is slightly recessed, no solder fillet is expected after the solder reflow process.

Figure 4. **Pull-back terminal ends (package bottom and side view)**



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1.3.3 Terminal ends with side wettable flank

Wettable flanks (WF) are modifications to the fully-exposed terminal ends, which promote solder wetting for the formation of a solder fillet. Uniform solder fillets are needed to enable inspection for solder failures using automatic optical inspection (AOI) and avoids the need for x-ray inspection, with additional cost and layout restrictions for the PCB.

Figure 5. Wettable flank (WF) features of QFN/SON terminal ends shows that the primary WF features are step cuts and dimples at the terminal ends. The step cut is formed during the package singulation process, while the “dimpled” terminal is formed during the half-etching step of the leadframe fabrication process. The fillets are formed and should be visible on the PCB after the solder reflow process, as shown in Figure 6. Solder fillets cross-sections after reflow and Figure 7. SEM Images of solder fillets cross-sections after reflow.

Fillet formation, size and shape is highly dependent upon solder paste, stencil design, board layout, reflow profile, and other PCB assembly parameters. To get optimal results, follow the guidelines in Section 2.2.

Figure 5. Wettable flank (WF) features of QFN/SON terminal ends

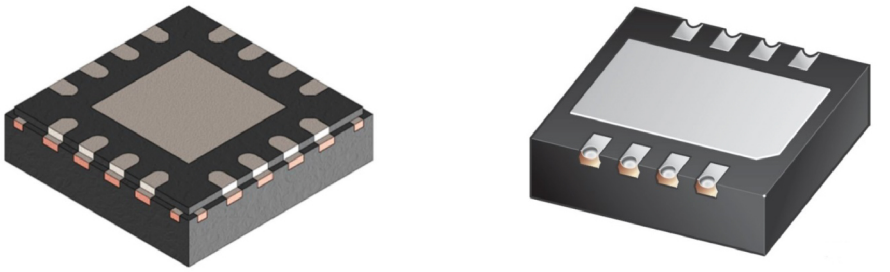


Figure 6. Solder fillets cross-sections after reflow

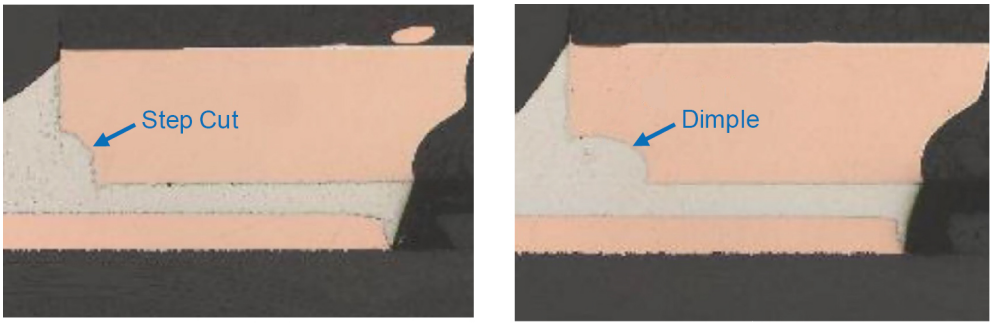
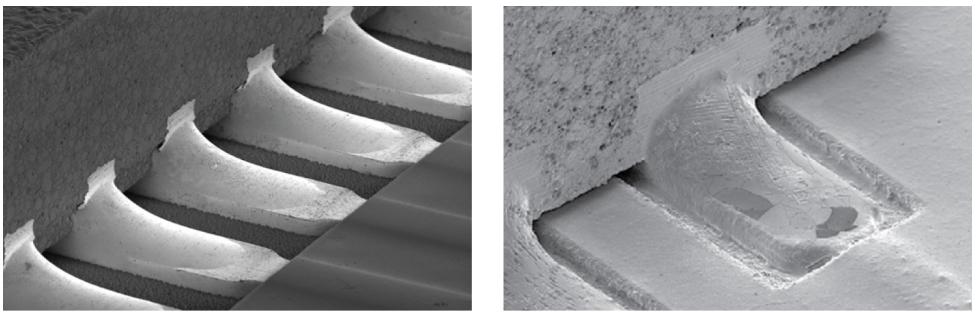


Figure 7. SEM Images of solder fillets cross-sections after reflow



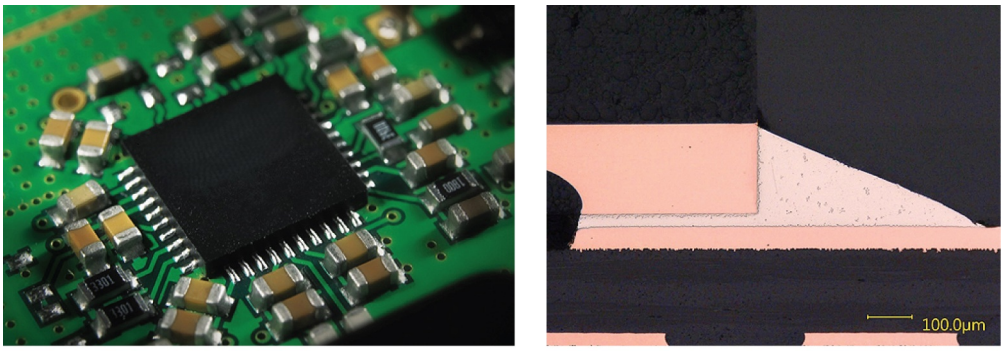
2 Printed-circuit board (PCB) guidelines

2.1 PCB design guidelines and requirements

As the package size shrinks and the terminal count increases, the dimensional tolerance and positioning accuracy affects subsequent processes. Part interchangeability is also a concern when two separate suppliers provide production parts for the PCB. The optimized PCB layout for one supplier may have issues (manufacturing yield and/or solder joint life) with the other supplier's parts. When more than one source is expected, the PCB layout should be optimized for both parts. Additional information of this topic is provided in this section.

A proper PCB footprint and stencil design is critical to surface mount assembly yields and subsequent electrical and mechanical performance of the mounted package. The design starts with obtaining the correct package drawing. Refer to the package outline drawing in the device datasheet.

Figure 8. A well-soldered QFN/SON package



PCB assembly with QFN

Cross-section of toe solder fillet

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The cross-section picture in Figure 8. A well-soldered QFN/SON package shows the goal of a well-soldered QFN/SON terminal, void-free solder joint and a smooth solder fillet.

2.2 PCB footprint design

2.2.1 Guidelines for perimeter land patterns

A land is the conductive pattern on the PCB used for the solder connection of a component. The land pattern is a combination of lands intended for the board mounting of a particular component. Land patterns are also referred to as footprint for reflow soldering.

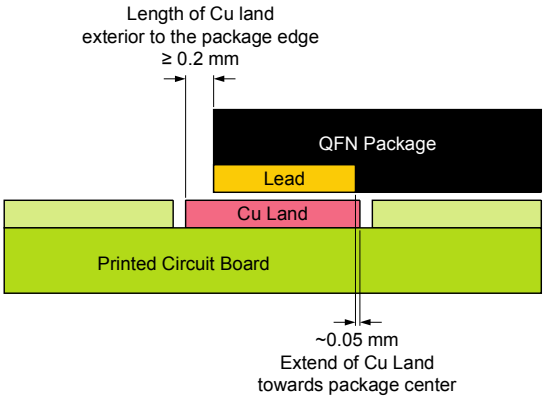
2.2.1.1 Guidelines for size of perimeter Cu-lands:

All PCB land calculation should be based on the nominal size of the package terminal.

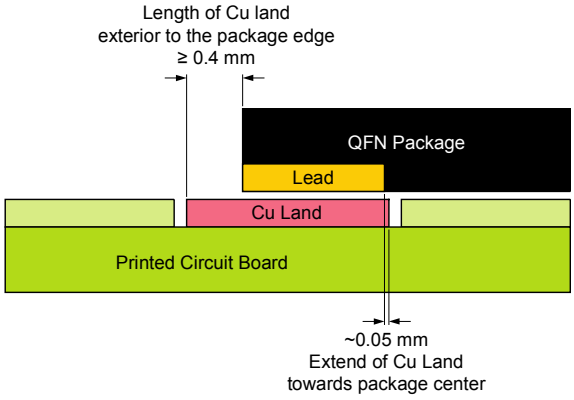
Length of perimeter lands:

- The land should extend ~0.05 mm towards the center of the package (Figure 9. Length of perimeter copper lands).
- The land should extend ≥ 0.20 mm from the package edge to the exterior for QFN/SON with fully-exposed lead ends.
- The land should extend ≥ 0.40 mm from the package edge to the exterior for QFN/SON with side wettable flanks to form inspectable toe solder fillets (Figure 9. Length of perimeter copper lands). If board space allows, a longer land extension (such as 0.60 mm) will generally result in more consistent fillet formation because it will be influenced less by PCB assembly issues (e.g. misalignment).
- The PCB land should not extend beyond the package edge for packages with pull-back terminal ends.

Figure 9. Length of perimeter copper lands



Fully exposed lead ends



Lead ends with side wettable flank

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Width of perimeter lands:

- The PCB land width should be approximately the same as the nominal package terminal width (see Table 1. Recommended land width as a function of terminal pitch).
- Terminal pitch needs to be designed using the exact dimensions of 0.40, 0.50, 0.65, 0.80, and 1.00 mm.

Table 1. Recommended land width as a function of terminal pitch

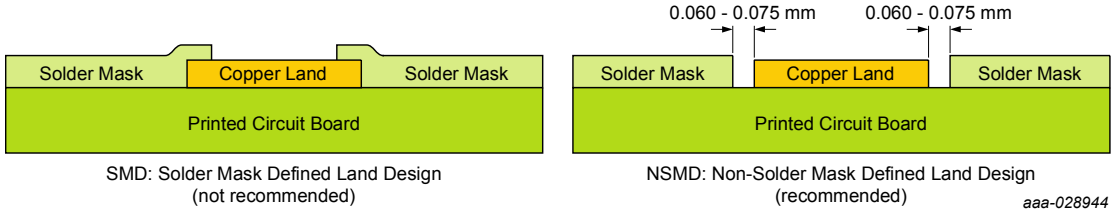
Terminal pitch (mm)	Land width (mm)
0.40	0.200
0.50	0.250
0.65	0.370
0.80	0.400
1.00	0.500

2.2.1.2 *Solder mask guidelines for perimeter lands*

For perimeter PCB lands, it is recommended to use non-solder mask-defined (NSMD), because they provide significant advantages over solder mask-defined (SMD) lands in terms of dimensional tolerances and registration accuracy. The NSMD has a solder mask opening that is larger than the copper land, and the PCB pad area is controlled by the size of the copper land. Since the copper etching process is capable and stable, a smaller size copper land can be defined more accurately. Figure 10. SMD and NSMD land designs shows the pad design concepts.

The solder mask should be pulled away from the perimeter lands to account for the registration tolerance of the solder mask. The opening should be 0.12 to 0.15 mm larger than the land size resulting in 0.060 to 0.075 mm clearance between the copper land and solder mask (IPC-7351).

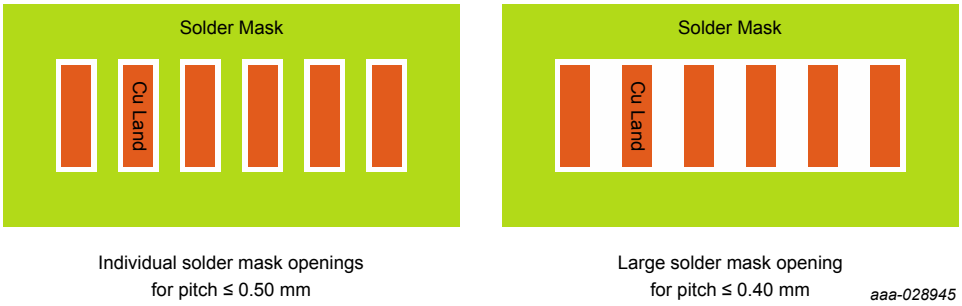
Figure 10. SMD and NSMD land designs



Each land should have its own solder mask opening with a web of solder mask between two adjacent leads (Figure 11. Solder mask design for perimeter land pattern). IPC-7351 recommends having at least 0.075 mm of web width to ensure adhesion to the PCB surface is sufficient. Minimum solder mask width will also depend on PCB manufacturer capabilities.

Individual solder mask openings will not work for pitches ≤ 0.40 mm, taking requirements for minimum spacing and width of solder mask into account. A single large solder mask opening for all lands can be used as an alternative design for small pitches (Figure 11. Solder mask design for perimeter land pattern).

Figure 11. Solder mask design for perimeter land pattern



2.2.1.3 *Clearance to vias and adjacent components*

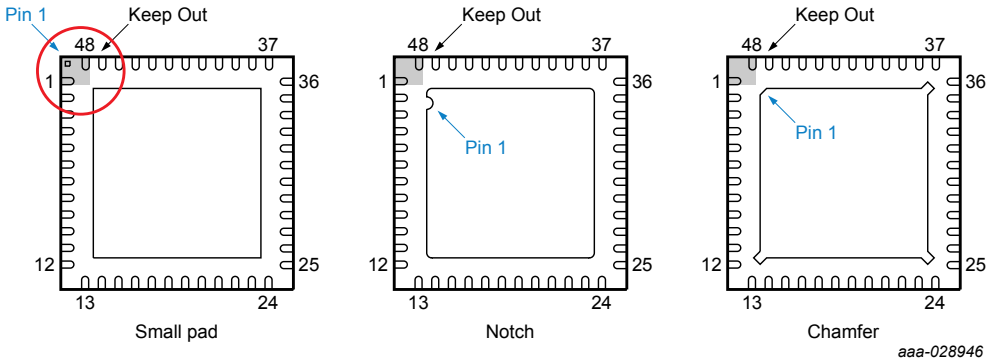
Placement of exposed, not covered by solder mask, PCB vias and traces near package corners should be avoided to eliminate potential shorting between exposed package tie-bar features.

Other surface mount devices and insertion components (THT or through hole technology) should be placed sufficiently away from package land pattern area to avoid potential package and board defects.

2.2.1.4 *Pin 1 keep out area*

Different design features are used to identify the package orientation and location of “Pin 1” on package bottom side. This can either be a small square pad (left), a notch in the exposed pad (middle), or a chamfer in the exposed pad corner (right) as shown in Figure 12. Gray “Pin 1” keep out area (package transparent top view). The feature is not necessarily included in the package outline drawing as published. In the event of an open trace on the PC-board, there may be unintentional contact between this trace and the small square pad, leading to a malfunction. To prevent this, ST prescribes a “keep out” area for the corner/pin 1 area of the PC-board, as indicated in Figure 12. Gray “Pin 1” keep out area (package transparent top view), which applies to all designs.

Figure 12. **Gray "Pin 1" keep out area (package transparent top view)**



2.2.1.5 *Keep out areas for QFN accelerometer sensors*

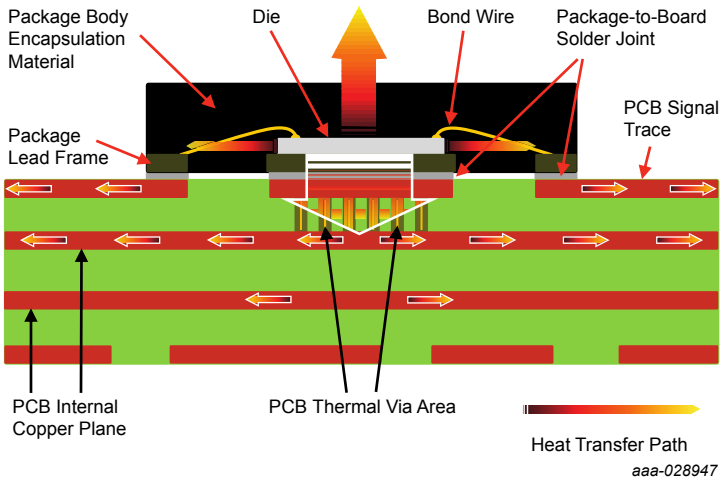
Avoid positioning screw holes for PCB attachment near the accelerometer location. Doing so may flex the PCB and affect product performance.

To prevent the risk of package tie-bar shorting with PCB traces, it is recommended that vias and other insertion components are kept at least 2mm away from the package edge.

2.2.2 Guideline for exposed pad land patterns

QFN/SON packages with an exposed pad (EP) on the bottom, enhance the thermal and electrical performance of the package. The die is attached directly to the exposed pad thus providing an efficient heat removal path, as well as excellent electrical grounding to the PCB as shown in Figure 13. Cross-section of QFN/SON package and PCB showing heat transfers. To further optimize thermal performance, the PCB design should include thermal vias and a thermal plane(s).

Figure 13. **Cross-section of QFN/SON package and PCB showing heat transfers**



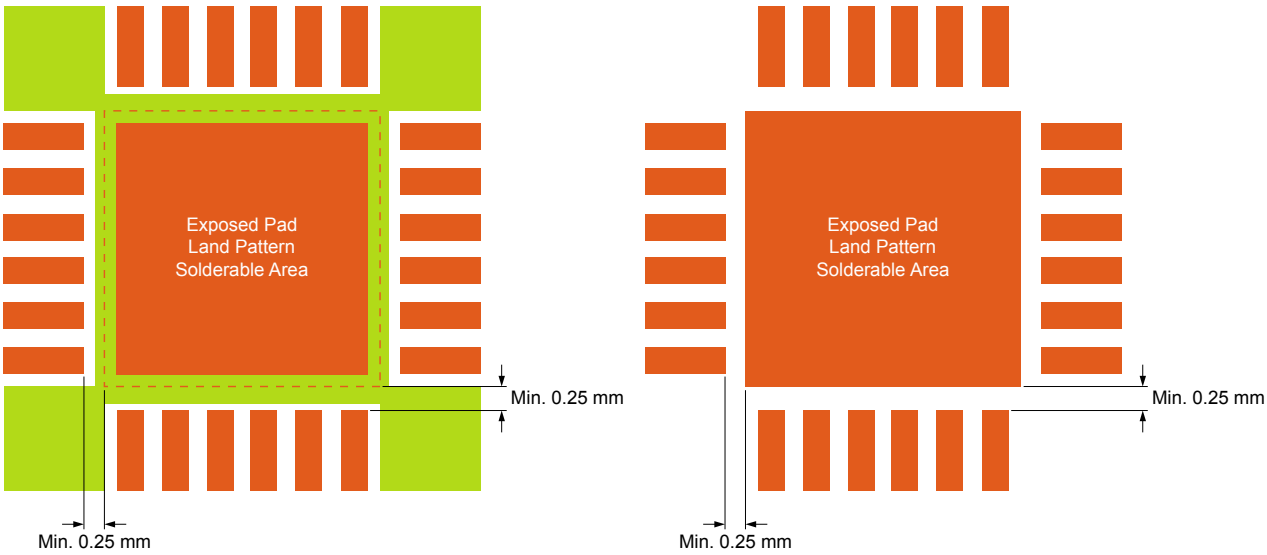
Although the land pattern design of the perimeter lands for exposed pad packages should be the same as that for non-thermally/electrically enhanced packages, extra features are required during the PCB design and assembly stage for effectively mounting thermally/electrically enhanced packages. In addition, repair and rework of assembled exposed pad packages may involve some extra steps, depending upon the current rework practice within the company.

2.2.2.1 *Spacing between perimeter and exposed pad land pattern*

The design of the land pattern and the size of the exposed thermal pad depends strongly on the thermal characteristics and power dissipation of the specific product and application. To maximize both removal of heat from the package and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad (as shown in Figure 14. Minimum clearance between perimeter and exposed pad land pattern).

The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. However, the area that can be soldered (which should be defined by the solder mask) should be approximately the same size/shape as the exposed pad area on the package to maximize the thermal/electrical performance. A clearance of at least 0.25mm should be designed on the PCB between the outer edges of the exposed pad land pattern and the inner edges of perimeter land pattern to avoid any shorts.

Figure 14. Minimum clearance between perimeter and exposed pad land pattern



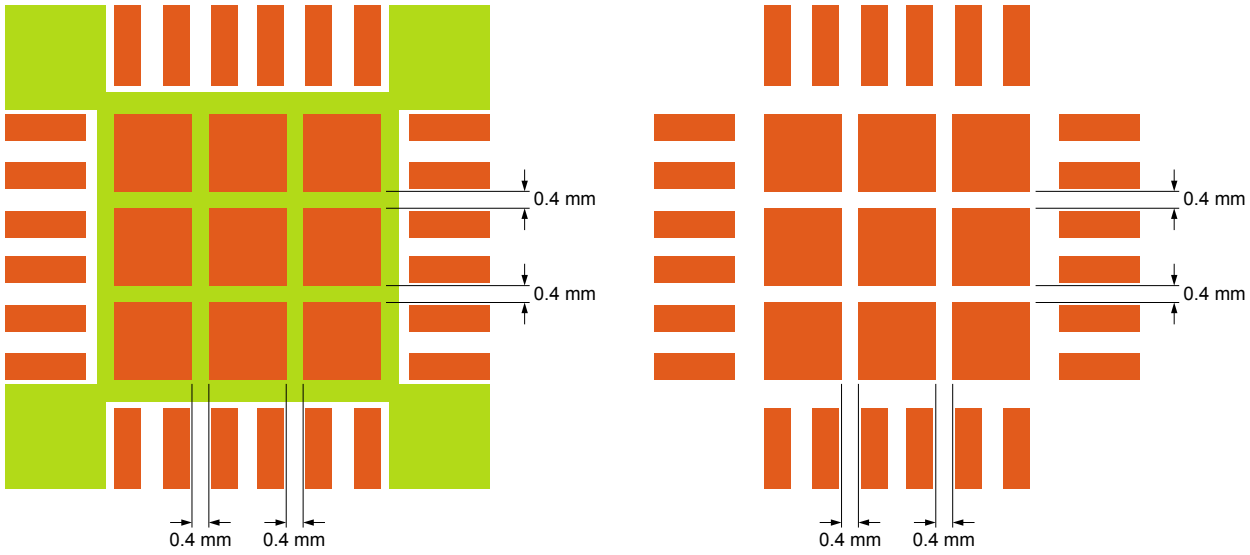
2.2.2.2 *Segmented exposed pad land pattern design*

Alternatively, the land pattern for the exposed pad can be segmented into a symmetric array of square or rectangular lands, as shown in Figure 15. Segmented exposed pad land patterns. The land array can be created either by segmentation of a full copper area by solder mask openings, or by NSDM defined copper lands.

- Recommended edge length/width of a matrix land is between 1.0 to 2.0 mm
- Distance between the lands should be 0.40 mm

The segmented PCB design facilitates the solder paste flux outgassing during reflow, thereby promoting a lower voiding level of the completed solder joint. The maximum size of a single solder void is limited by the dimensions of a single matrix segment at the same time.

Figure 15. **Segmented exposed pad land patterns**

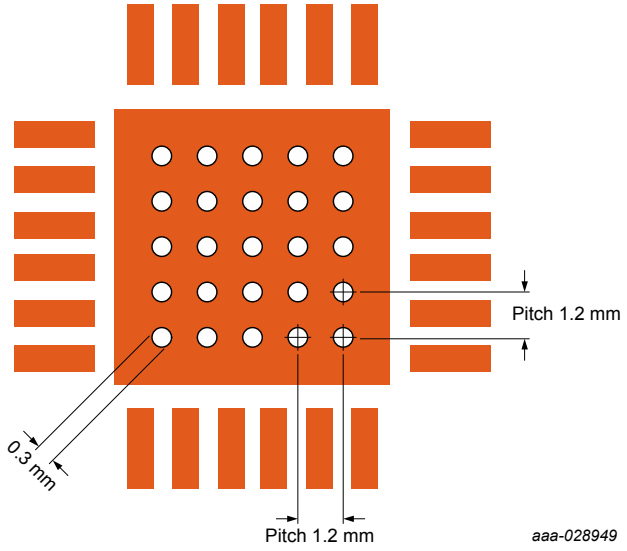


2.2.2.3 *Thermal vias in the exposed pad land pattern*

While the land pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct the heat from the surface of the PCB to the ground plane(s). These vias act as “heat pipes”. The number of vias is application specific and depends upon the product power dissipation and electrical conductivity requirements.

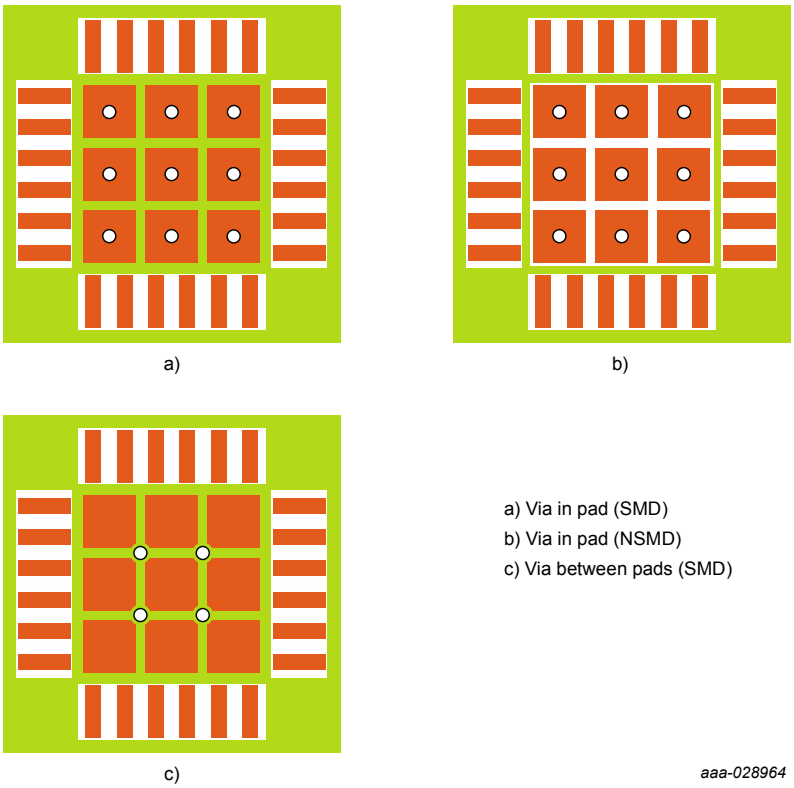
- Thermal and electrical analysis and/or testing are recommended to determine the minimum number of vias required.
- Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern at a 1.20 mm grid, as shown in Figure 16. Exposed pad land pattern with array of thermal vias.
- It is recommended that the via diameter be 0.30 to 0.33 mm with 35 µm Cu plating thickness (1.0 oz/ft^2). This is desirable to avoid any solder-wicking inside the via during the soldering process, which may result in solder voids in the joint between the exposed pad and the thermal land.
- If the copper plating does not plug the vias, then the thermal vias can be “tented” with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 0.10 mm larger than the via diameter.

Figure 16. **Exposed pad land pattern with array of thermal vias**



Design options for combination of vias with a segmented exposed pad land pattern are shown in Figure 17. Segmented exposed pad land pattern with vias.

Figure 17. Segmented exposed pad land pattern with vias



2.2.3 Pad surface finish

Almost all PCB finishes are compatible with QFN/SONs, including:

- Organic solderability protectant (OSP)
- Electroless nickel immersion gold (ENIG)
- Immersion Sn
- Immersion Ag

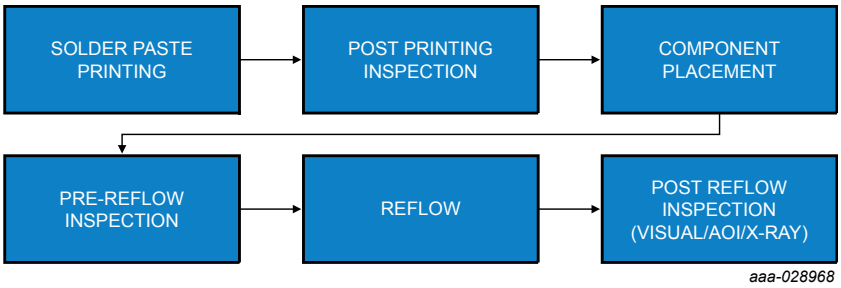
Hot air solder leveled (HASL) finish may cause uneven surface issues and extra caution is required.

3 Board assembly

3.1 Assembly process flow

Figure 18. SMT process flow shows a typical surface mount technology (SMT) process flow. Use of standard pick and place process and equipment is recommended and manual or hand soldering should be avoided.

Figure 18. SMT process flow



3.2 Solder paste printing

3.2.1 Solder paste

Solder paste is a homogenous mixture of fine metal alloy particles, flux, and viscosity modifiers to adjust printing and reflow properties. The main features of solder pastes are:

- Solder alloy:
  Lead-free solder paste is recommended, in line with environment legislation (RoHS, ELV). A variety of lead-free alloys is available for PCB assembly, with different physical properties and melting temperatures. Common solders alloys are combinations of Tin, Silver, and Copper: SnAg3Cu0.5 (SAC305), SnAg4Cu0.5 (SAC405), or SnAg3.8Cu0.7 (SAC387), with a melting range between 217 to 220°C. The peak reflow temperature for these alloys shall be > 235°C.
- Solder spheres:
  A main component of the paste is the low-oxide spherical powder made from the solder alloy. The amount of solder powder in the paste is referred to as the metal load and is typically in the range of 83 to 92 % by weight. The spherical shape and controlled size of the powder particles ensures a uniform printing and a stable paste volume for each solder land. The solder pastes are classified by spheres size according to IPC standard J-STD-005 (see Table 2. Solder paste type). Smaller spheres allow higher printing resolution and smaller pitches. The rule of thumb is that the minimum dimension of the smallest stencil opening shall be larger than 4 to 6 sphere diameters.

Table 2. Solder paste type

Paste type	Sphere diameter	
	Min. (µm)	Max. (µm)
3	25	45
4	20	38
5	10	25
6	5	15

- Flux:
  Flux is needed to remove surface oxidation, prevents oxidation during reflow and improves the wetting of the solder alloy. Solder pastes are classified into three types based on the flux type according to IPC standard J-STD-004:
  - Rosin-based flux
  - Water-soluble flux
  - No-clean flux
    Rosin-based and water-soluble fluxes require cleaning of the PCB after reflow process. Standard rosin chemistries are normally cleaned with solvents, semi-aqueous solutions or aqueous/saponifier solutions, while the water-soluble chemistries are cleaned with pure water.
    No-clean flux doesn't require cleaning, but normally a little residue remains on the PCB after soldering. In general, it is recommended to use a no-clean solder paste, because cleaning of flux residues from underneath the package is not feasible for a QFN/SON-style package (due to the low package standoff).

3.2.2 Stencil thickness

The thickness of the stencil determines the amount of solder paste deposited onto the printed circuit board land pattern. Due to the fine pitch and small terminal geometry used, care must be taken when printing the solder paste on to the PCB. Typical stencil thicknesses are given in Table 3. Typical Stencil Thickness.

Table 3. Typical Stencil Thickness

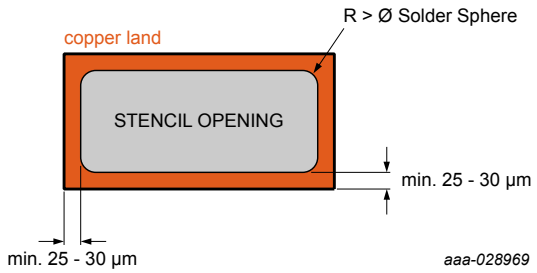
Package pitch (mm)	Stencil thickness (µm)
0.50	150
0.40	100 to 125

Since QFN/SON are (most likely) not the only package on the actual production PCB, the recommended stencil thickness for the other packages may be thicker than desired. For such a case, a step-down stencil is recommended, where most of the stencil for the PCB has a typical thickness, but the area for the QFN/SON would be reduced to 100 to 150µm, depending on the package pitch.

3.2.3 Stencil design

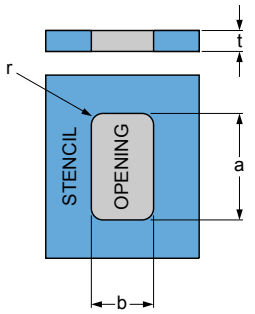
The dimension of the stencil openings should be a minimum 25 to 30 µm (5 to 10 %) smaller than the size of the corresponding copper lands to account for alignment and PCB tolerances. A fillet at the corners reduces the adhesion to the solder paste and improves the paste release (Figure 19. Stencil opening size and corner radius). The fillet radius depends on the solder paste type; i.e. it should be larger than the diameter of the solder spheres.

Figure 19. Stencil opening size and corner radius



A minimum aperture size is needed to ensure the proper release of the solder paste during stencil printing (Figure 19. Stencil opening size and corner radius). The area ratio and the aspect ratio between stencil opening and stencil thickness are used to determine the minimum dimensions, respectively.

Figure 20. Area ratio and aspect ratio



Aperture Dimensions

$$\text{Aspect Ratio} = \frac{\text{smallest aperture dimension (a or b)}}{\text{stencil thickness}}$$

$$\text{Aspect Ratio} = \frac{\min [a, b]}{t} > 1.5$$

Example: Minimum width for stencil thickness 150 µm

$$\frac{b}{150\ \mu m} > 1.5 = > b > 1.5 \times 150\ \mu m = > b > 225\ \mu m$$

$$\text{Area Ratio} = \frac{\text{projected aperture area}}{\text{aperture side wall area}}$$

$$\text{Area Ratio} = \frac{ab - r2\,(4 - \pi)}{2t\,[a + b + r\,(\pi - 4)]} > 0.66$$

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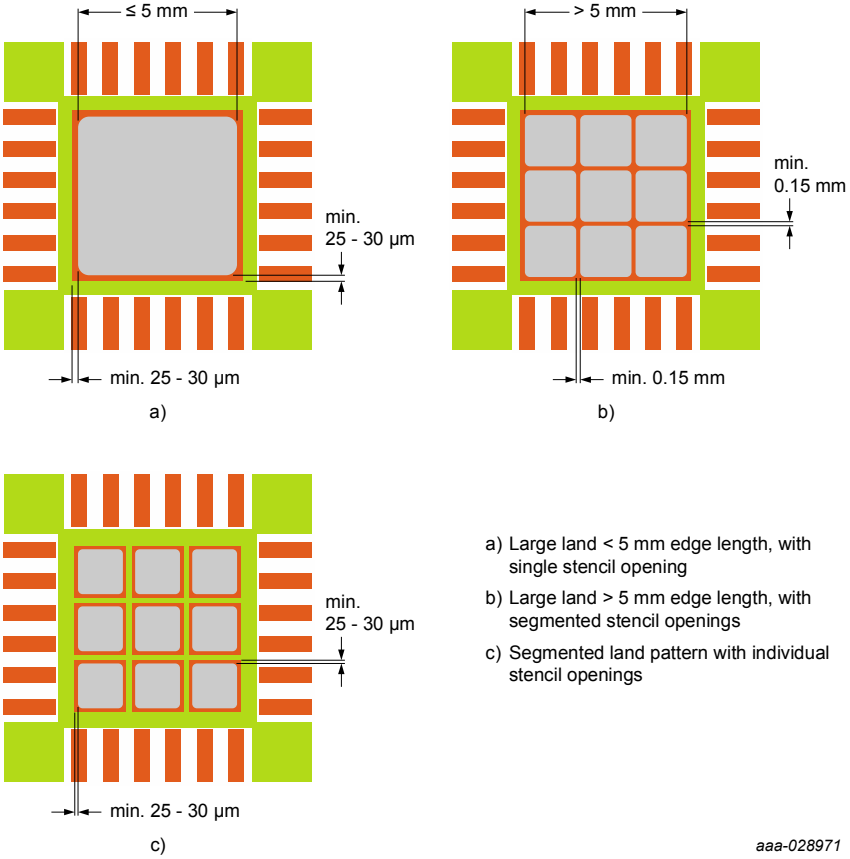
Maximum thermal/electrical performance requires that the exposed pad of the package is soldered to the land pattern on the PCB. The maximum aperture size of the stencil should not exceed > 5 mm on either side (Figure 21. Figure 26a). Larger openings should be subdivided into an array of smaller openings as shown in Figure 21. Figure 26b. The spacing between segments on the stencil should be 0.150 mm or more. Narrower spacing between segments can become a manufacturing issue.

Figure 21. Stencil design for exposed pad



a) Large land < 5 mm edge length, with single stencil opening

b) Large land > 5 mm edge length, with segmented stencil openings

c) Segmented land pattern with individual stencil openings

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An array of smaller paste deposits for exposed pad land supports outgassing of the flux during reflow. Otherwise the evaporated flux is entrapped in the solder joint and creates large solder voids. Smaller QFN/SON packages can take advantage of this stencil design even for exposed pad size < 5 mm.

The target solder paste coverage of the land should be about 60 % to 65 % of the lands area to achieve a good solder joint. Smaller solder paste volumes could have adverse effects on the solder joint reliability. If the product dissipates a large amount of heat, the solder paste deposit can be increased. Too much paste can cause the component to float and have misconnections of terminals. Solder paste deposits should be arranged so that paste is never printed directly over an unplugged via.

3.3 Component placement

Increased package interconnection density requires precise and accurate pick and place tools. To meet this tight requirement, a placement machine equipped with an optical recognition system for the centering of the PCB and the components during the pick-and-place motion is recommended. A placement accuracy study is suggested to calculate compensations required.

Packages with the same outline can have different design features to identify the package orientation and location of pin 1 when the package is viewed from bottom side (see Section 2.2.1.4). Also, the leadframe finish may reflect differently in the vision system. If parts are supplied by more than one assembly line, then it is necessary to create dedicated equipment recipes.

Refer to Section 5.4, for package orientation and location of pin 1 in JEDEC trays or tape and reel carriers.

3.4 Reflow soldering

The temperature profile is the most important control in reflow soldering, and it must be fine tuned to establish a robust process. The actual profile parameters depend upon the solder paste and alloy used; the recommendations from paste manufacturers should be followed. Nitrogen reflow is recommended to improve solderability and to reduce defects (like solder balls).

When a board is exposed to the reflow oven temperature, certain areas on the board will heat faster than others depending on the thermal mass. Large components and large copper areas in the board will heat up slower than small components and board areas with little copper. The actual temperature shall be measured with thermocouples at various places on the PCB surface to ensure that the reflow temperature is reached everywhere on the board.

The temperature of package top surface shall be monitored at the same time, to validate that the peak package body temperature (T_P) does not exceed the MSL classification of individual devices (see IPC/JEDEC J-STD020).

Figure 22. Typical reflow profile for QFN with lead-free SAC solder

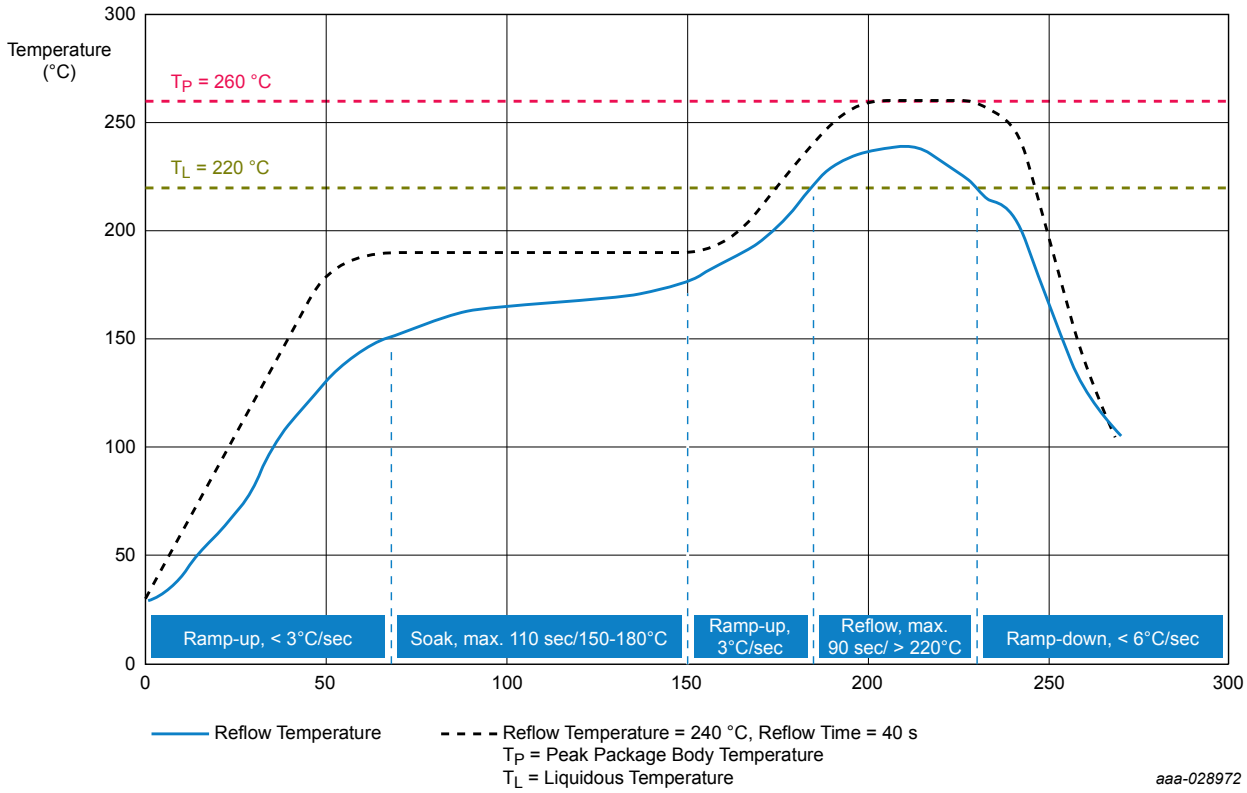


Figure 22. Typical reflow profile for QFN with lead-free SAC solder shows a typical time/temperature profile (blue) for reflow soldering with lead-free SAC solder alloys using a multi-zone reflow oven. The maximum allowed package body temperature at every stage of the process (depending on the IPC/JEDEC J-STD-020 classification of the package) is represented by the dashed gray line.

The reflow profile is divided into five stages:

- Ramp-up to soak
  The printed circuit board should be heated evenly to avoid overheating of components. Volatile solvents in the solder paste start to outgas during ramp up. Too fast temperature increase could cause solder balling. The maximum ramp-up rate shall not exceed 3 °C/second to avoid overstress to the package.
- Pre-heat and soak
  The PCB assembly is held at 150 to 180 °C temperature for 60 to 120 seconds during thermal soak. The volatiles in the solder paste will be removed and the flux is being activated to reduce oxides from the pads and lands. Time and temperature are recommended by the paste supplier depending on the flux type.
- Ramp-up to reflow
  The PCB assembly is uniformly heated above the liquidous temperature of the solder alloy. Again, the maximum ramp-up rate shall not exceed 3 °C/second to avoid overstress to the package.
- Reflow
  The recommended peak reflow temperature for SAC alloys shall be > 235 °C. The period above the liquidous temperature (T_L) is called the reflow time. It shall be long enough to allow the liquid solder to uniformly wet the pad and land surfaces and to form an intermetallic phase. Too long reflow time may lead to brittle solder joints and could cause damage to the board and components. The peak package body temperature (T_P) must not exceed 260 °C and the time above 255 °C must not exceed 30 seconds depending on IPC/JEDEC classification.
- Cool down
  Fast cool down prevents excess intermetallic formation and creates a fine grain structure of the solder alloy. The ramp-down rate can be faster than the ramp-up, but shall not exceed 6 °C/second to avoid overstress.

The reflow profile for exposed pad packages need not be any different than the one used for non-thermally/electrically enhanced packages.

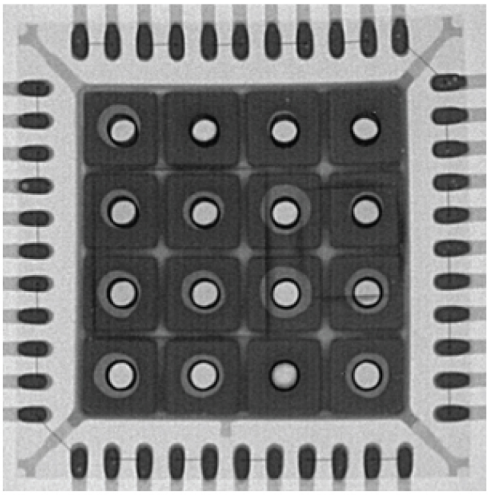
Cross referencing with the device data sheet is recommended for any additional board assembly guidelines specific to the exact product used.

3.5 Inspection

Unlike traditional leaded components, the solder joints of QFN/SON are formed primarily underneath the package. To verify any open or short circuits (bridging) after reflow soldering, optical inspection and x-ray inspection are recommended. Micro-sectioning is another method of inspecting solder joint quality during process optimizations, but it is less suitable to production inspection (due to slow processing).

Figure 23. X-ray inspection of a QFN package after soldering shows the x-ray image of a soldered QFN44 package with exposed pad and pull-back terminal ends. The dark gray areas represent the solder joints. Light gray spots within the solder joints are due to solder voids. The perimeter lands are well soldered with very little voiding. The land pattern for the exposed pad is segmented with a thermal via within each square. The voids around the vias are not regarded as defects.

Figure 23. X-ray inspection of a QFN package after soldering



HVQFN44 9x9 with segmented exposed pad land pattern, thermal vias in the exposed pad land, and a daisy-chain wire bond configuration

aaa-028973

Figure 24. Visual optical inspection of QFN after assembly shows an example of shorted solder joints caused by excess spread of solder paste during reflow or high solder amount.

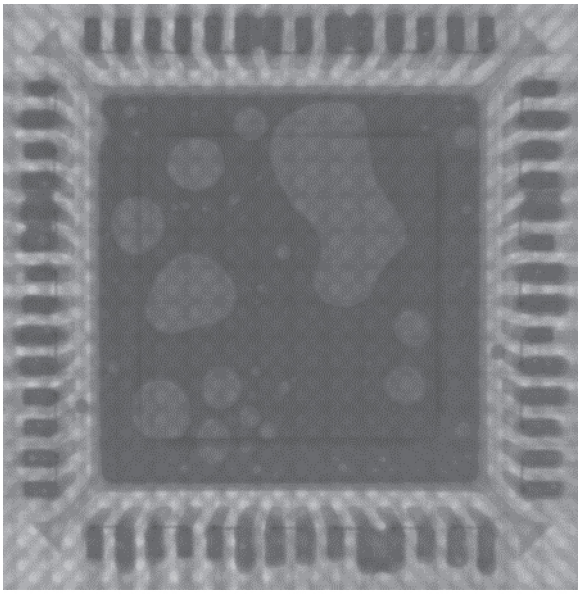
Figure 24. Visual optical inspection of QFN after assembly

Shorts and Bridging on Perimeter Pads (Side View)

aaa-028974

Figure 25. X-ray of QFN package after assembly shows an issue with excess solder voids at the exposed pad. The large single copper land used for the exposed pad prevents the proper outgassing of volatile solvents from the solder paste. The perimeter solder joints show either poor wetting or shorts between terminals.

Figure 25. **X-ray of QFN package after assembly**



Not segmented exposed pad with large solder voids and terminals with shorts/bridging

aaa-028975

3.6 Board level reliability results

To get results from ST board level reliability tests, contact the ST sales team.

4 Package thermal characteristics

4.1 General thermal performance

Since the thermal performance of the package in the final application will depend on a number of factors (like board design, power dissipation of other components on the same board, ambient temperature), the thermal package properties provided should only serve as a reference.

Exposed pad packages may require the exposed pad to be connected to the PCB for thermal and/or electrical measurement. For optimized thermal performance, it is recommended to form a thermal pass into the PCB, by connecting the exposed pad to the top and/or bottom and/or inner copper layers of the PCB. The PCB copper area and number of thermal vias connected to the exposed pad required to achieve the proper thermal performance on the PCB is application specific, and depends on the package power dissipation and the individual board properties (thermal resistance of the application PCB).

4.2 Package thermal characteristics

Junction temperature is a function of die size, on-chip power dissipation, package characteristics, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal technology.

Additional factors to be considered in PCB design and the thermal rating of the final application (amongst others) are:

- Thermal characteristics of the PCB (metal density, number of thermal vias, thermal conductivity of thermal vias)
- Quality and size of PCB solder joints (effective PCB pad size, potential solder voiding in the thermal path solder joints that may reduce the effective solder area)

The stated values are meant to define the package thermal performance in a standardized environment (one package on a standardized board).

Thermal properties of the individual products are usually given in the product datasheets as appropriate. Product datasheets are available at http://www.st.com. For more details on thermal properties, contact your local ST sales office.

4.3 Package thermal properties definition

The thermal performance of QFN/SON packages with and without exposed pads is typically specified by thermal properties such as $R_{\theta JA}$, $R_{\theta JC}$ and Ψ_{JT} (in °C/W). Thermal characterization is performed by physical measurement and by running complex simulation models under the following conditions:

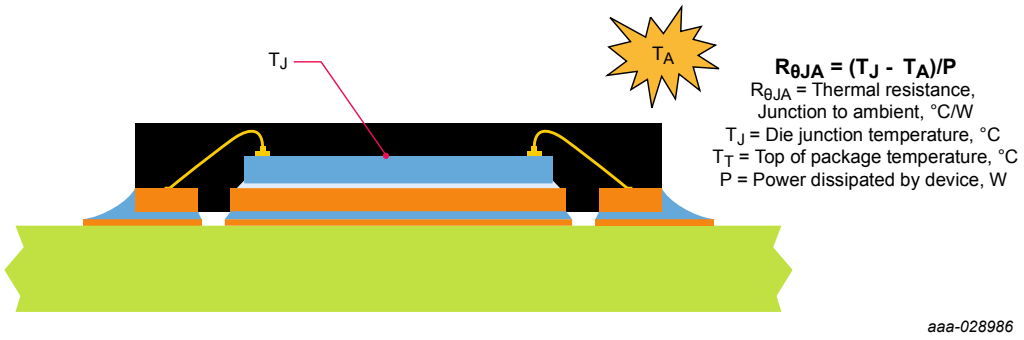
- One thermal board type:
  - Four-layer board (2s2p), per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only)
- Two boundary conditions:
  - Natural convection (still air), per JEDEC JESD51-2
  - Cold plate method, per MIL SPEC-883 method 1012.1

4.3.1 $R_{\theta JA}$: Theta junction-to-ambient natural convection (still air)

Junction-to-ambient thermal resistance (Theta-JA or $R_{\theta JA}$ per JEDEC JESD51-2) is a one-dimensional value that measures the conduction of heat from the junction (of the hottest temperature on die) to the environment (ambient) near the package in a still air environment. The heat that is generated on the die surface reaches the immediate environment along two paths:

- Convection and radiation off the exposed surface of the package, and
- Conduction into-and-through the test board, followed by convection and radiation off the exposed board surfaces.

Figure 26. **Junction and ambient temperature (still air)**



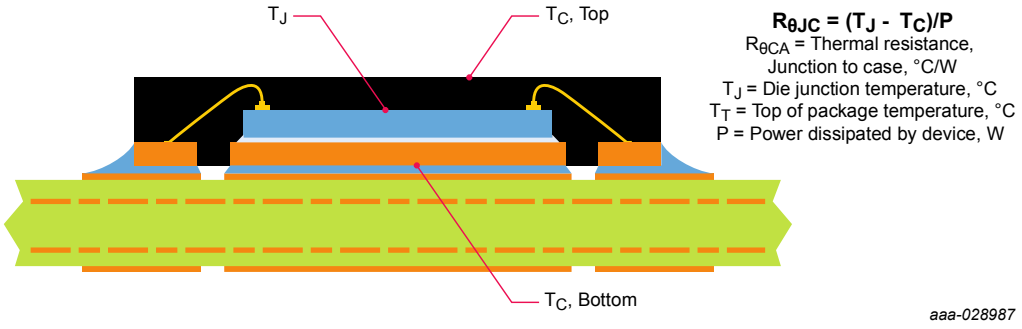
4.3.2 $R_{\theta JC}$: Theta junction-to-case

Junction-to-case thermal resistance (Theta-JC or $R_{\theta JC}$ per MIL SPEC-883 Method 1012.1) indicates the average thermal resistance between the die and the case top surface, as measured by the cold plate method per MIL SPEC-883 Method 1012.1, with the cold plate temperature used for the case temperature. The case temperature is defined as

- Either the temperature at the top of the package (for non-exposed pad packages), or
- The temperature at the bottom of the exposed pad surface (for exposed pad packages).

For exposed pad packages where the pad would be expected to be soldered, the junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance. $R_{\theta JC}$ can be used to estimate the thermal performance of a package when the board is adhered to a metal housing or heat sink, or when a complete thermal analysis is done.

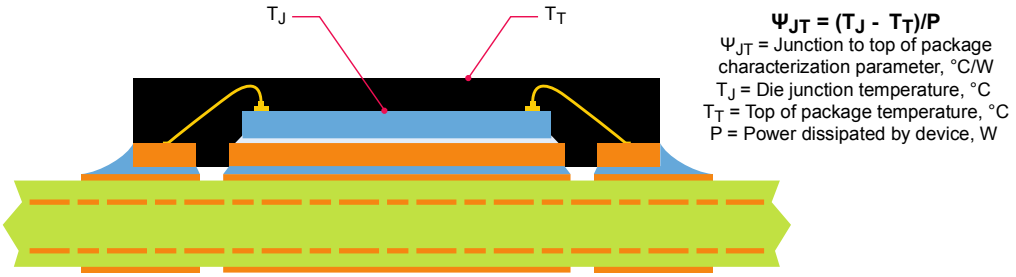
Figure 27. **Junction and case temperatures (top and bottom side)**



4.3.3 Ψ_{JT} (Psi JT): Junction-to-package top

Junction-to-package top (Psi JT or Ψ_{JT}) indicates the temperature difference between the package top and the junction temperature, optionally measured in a still air condition (per JEDEC JESD51-2) or in a forced convection environment (per JEDEC JESD51-6). Ψ_{JT} must not be confused with the parameter $R_{\theta JC}$: $R_{\theta JC}$ is the thermal resistance from the device junction to the external surface of the package, with the package surface held at a constant temperature, while Ψ_{JT} is the value of the temperature difference between the package surface and the junction temperature, usually in natural convection.

Figure 28. **Junction and package top temperatures**



5 Package handling

5.1 Handling of ESD sensitive devices

Semiconductor integrated circuits (ICs) and components are electrostatic discharge sensitive (ESDS) devices, so proper precautions are required for handling and processing them. Electrostatic discharge (ESD) is one of the significant factors leading to damage and failure of semiconductor ICs and components, and comprehensive ESD controls to protect ESDS devices during handling and processing should be considered.

The following industry standards describe detailed requirements of proper ESD controls; it is recommended to meet the standards before handling and processing ESDS devices. Detailed ESD specifications of devices are available in each device datasheet.

- JEDEC JESD625: Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- IEC-61340-5-1: Protection of electronic devices from electrostatic phenomena - General requirements

5.2 Handling of moisture-sensitive surface mount devices

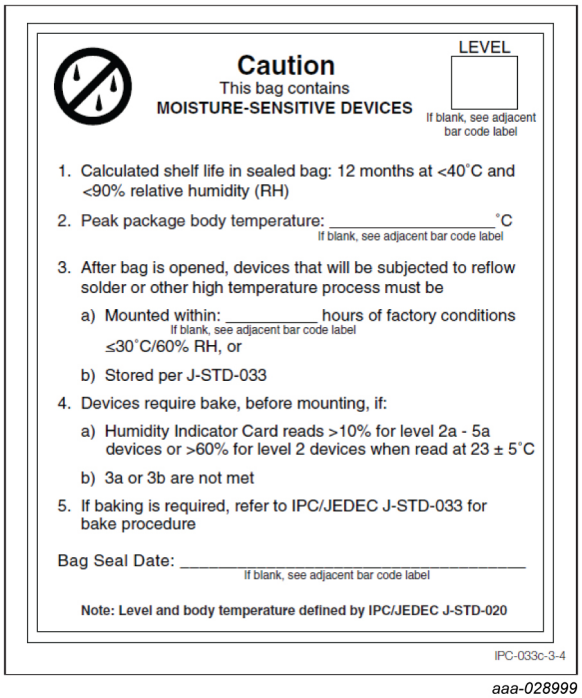
Some SON/QFN packages are moisture sensitive surface mount devices (SMD) and proper precautions are required for handling, packing, shipping and use.

Moisture from atmospheric humidity enters permeable plastic package materials by diffusion. When the package is exposed to rapid temperature rise and high temperature during reflow solder process, moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or de-lamination of critical interfaces (“popcorn” effect).

Therefore, moisture-sensitive components are dried and sealed in a moisture barrier bags (MBB) before shipping per IPC/JEDEC J-STD-033. The components are stored together with a desiccant and a moisture indicator card in the vacuum sealed bag. Only remove the moisture-sensitive components immediately prior to assembly onto the PCB. If partial lots are used, the remaining SMD packages must be resealed or placed in safe storage within one hour of bag opening.

A label on the moisture barrier bag (MBB) indicates that it contains moisture sensitive components (Figure 29. Example of moisture-sensitive caution label (IPC/JEDEC J-STD-033)). The “Moisture Sensitivity Caution Label” contains information about the moisture sensitivity level (MSL) and maximum allowed peak body temperature of the products. Same information is shown on the barcode labels of the shipping box and reels.

Figure 29. Example of moisture-sensitive caution label (IPC/JEDEC J-STD-033)



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The MSL indicates the floor life of the component, its storage conditions, and handling precautions after the original container has been opened. The permissible time, from opening the moisture barrier bag until the final solder reflow process, that a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity.

Table 4. Moisture classification level of floor live (IPC/JEDEC J-STD-033) presents the floor life definitions per IPC/JEDEC J-STD-033. Components must be mounted and reflowed within the allowable period of time (floor life out of the bag), and component temperature must not exceed the maximum peak body temperature during reflow process at the customer's facility.

Table 4. Moisture classification level of floor live (IPC/JEDEC J-STD-033)

Moisture sensitivity level	Floor life (out of bag) at factory ambient ≤ 30 °C/60 % RH or as stated
1	Unlimited at ≤ 30 °C/85 % RH
2	1 Year
2a	4 Weeks
3	168 Hours
4	72 Hours
5	48 Hours
5a	24 Hours
6	Mandatory bake before use. After bake, must be reflowed within the limit specified on the label.

Upon opening the MBB, the floor-life clock starts. If components have been exposed to ambient air for longer than the specified time, or if the humidity indicator card indicates too much moisture after opening a moisture barrier bag, then the components are required to be rebaked prior to the assembly process. Refer to IPC/JEDEC J-STD-033 for bake procedure.

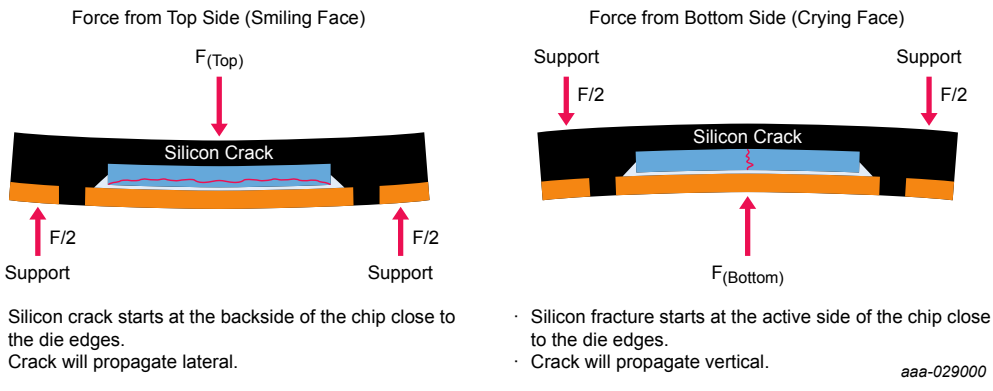
5.3 Handling of thin QFN/SON packages

The small, near chip scale size of QFN/SON packages enables higher integration on board level compared to leaded type packages. Care must be taken, especially with thin QFN/SON package types ≤ 0.50 mm maximum seated height, to avoid overstressing the parts during handling, e.g. pick and place or test.

Figure 30. Load cases for package handling shows two load cases to be considered during different handling operations:

- Force $F_{(Top)}$ applied on package top side, where bending stress at the die backside could exceeds silicon fracture strength

Figure 30. Load cases for package handling



- Force $F_{(Bottom)}$ applied on package bottom side, where bending stress at the active die surface could exceeds silicon fracture strength

Bending of the devices during handling should be avoided when possible. Ideally, the device should be mechanically supported from the opposite side. The graphs in Figure 31. Maximum bending moments for 0.50 mm package height and Figure 32. Maximum bending moments for 0.35 mm package height provide a guideline for maximum allowable bending moments depending on package size and package height.

The critical load depends on package height and on die-to-package ratio. Thicker packages and larger die in the same package are more robust.

The guideline assumes a symmetrical square package with exposed pad. The strength of other package designs may vary significantly. Contact the ST sales team for data of such packages.

Figure 31. Maximum bending moments for 0.50 mm package height

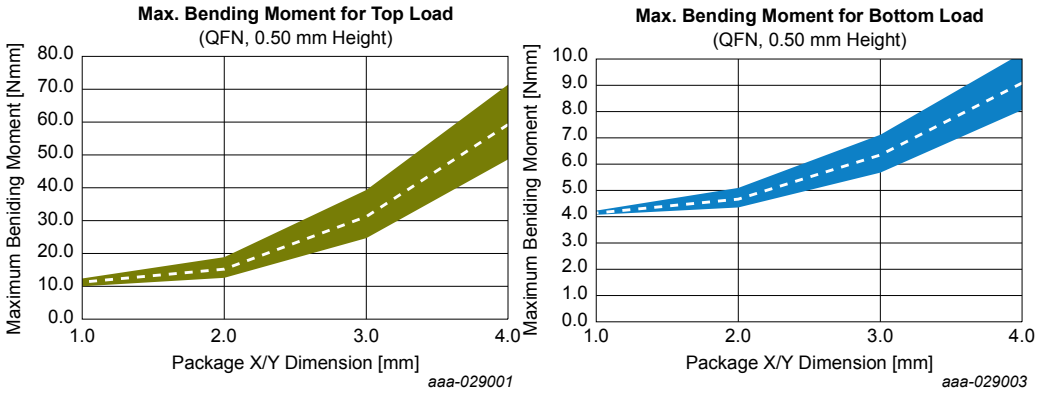
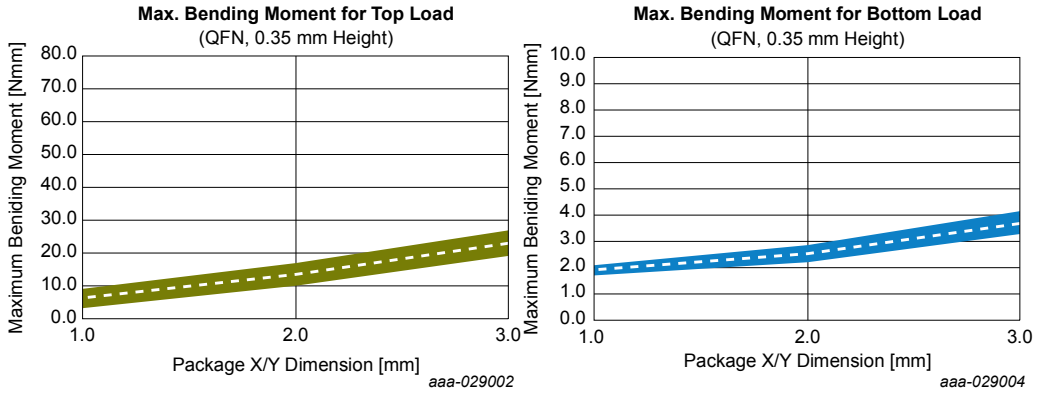


Figure 32. Maximum bending moments for 0.35 mm package height



5.4 Packing of devices

QFN/SON devices are contained in tray or tape and reel configurations. The packing media are design to protect devices from electrical, mechanical and chemical damages (as well as moisture absorption).

Devices are shipped with dry packing or non-dry packing depending on the MSL level of the device per IPC/JEDEC J-STD-033 (Table 5). Moisture sensitive devices are dry packed for transportation and storage with a vacuum sealed moisture barrier bag, including a desiccant and a moisture indicator card (refer to Section 5.2). MSL1 components do not require dry packing, but, for devices with Sulphur sensitive Au/Ag plating alloy, a Sulphur barrier pack is used to protect the device also from airborne Sulphur contamination.

Proper handling and storage of dry packs are recommended. Improper handling and storage (dropping dry packs, storage exceeding 40 °C/90 % RH environment, excessive stacking of dry packs, etc.) will increase various quality and reliability risks.

Table 5. **Dry packing requirements (IPC/JEDEC J-STD-033)**

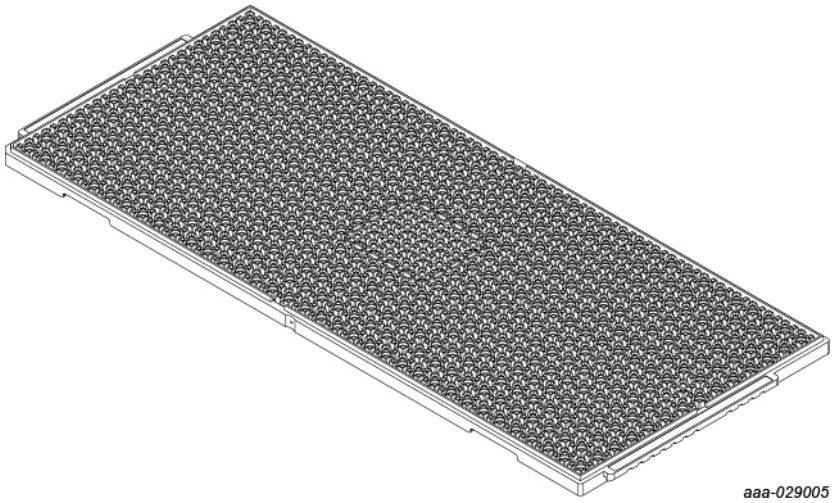
MSL level	Dry before bag	MBB with HIC	Desiccant	MSID label	Caution label
1	Optional	Optional	Optional	Not Required	Not required if classified at 220 to 225 °C Required if classified at other than 220 to 225 °C
2	Optional	Required	Required	Required	Required
2a to 5a	Required	Required	Required	Required	Required
6	Optional	Optional	Optional	Required	Required

- MBB: Moisture barrier bag
- HIC: Humidity indicator card
- MSID: Moisture sensitive identification

5.4.1 Trays

- Compliance with standard JEDEC tray design configuration (see Figure 33. JEDEC tray example).
- Devices will be oriented with pin 1 toward the chamfered corner of the tray.
- Trays are designed to be baked for moisture-sensitive SMDs, but the temperature rating of tray should NOT be exceeded when the devices are baked. The temperature rating can be found on the end-tab of the tray. The recommended baking temperature of trays is 125 °C.
- Trays are typically banded together with 5 + 1 (five fully-loaded trays and one cover tray) stacking, and dry packed in a moisture barrier bag (MBB). Partial stacking (1 + 1, 2 + 1, etc.) is also available, depending on individual requirements.

Figure 33. **JEDEC tray example**



5.4.2 Tape and reel

- Tape and reel carriers are in accordance with ANSI/EIA-481 (Figure 34. Typical reel pack for SMD: Guard band, ESD shielding bag).
- The packing information document (which can be either in PDF format or Excel table format) provides detail information on:
  - Packing method
  - Reel dimensions (Figure 37. Schematic view of reel and Table 7. Reel dimensions (in accordance with IEC 60286-3))
  - Packing quantity
  - Product pin 1 orientation
  - Carrier tape dimensions and tolerances (Figure 36. Example of carrier tape dimensions (in accordance with IEC 60286-3) and Table 6. Example of carrier tape dimensions)
- The product pin 1 orientation in the carrier tape (Figure 35. Product orientation in carrier tape) follows the orientation guide of ANSI/EIA-481 standard, but exceptions are possible depending on the product characteristics.
- Tape and reels are NOT designed to be baked at high temperatures.
- Each tape and reel is typically dry packed in a moisture barrier bag.

Figure 34. Typical reel pack for SMD: Guard band, ESD shielding bag

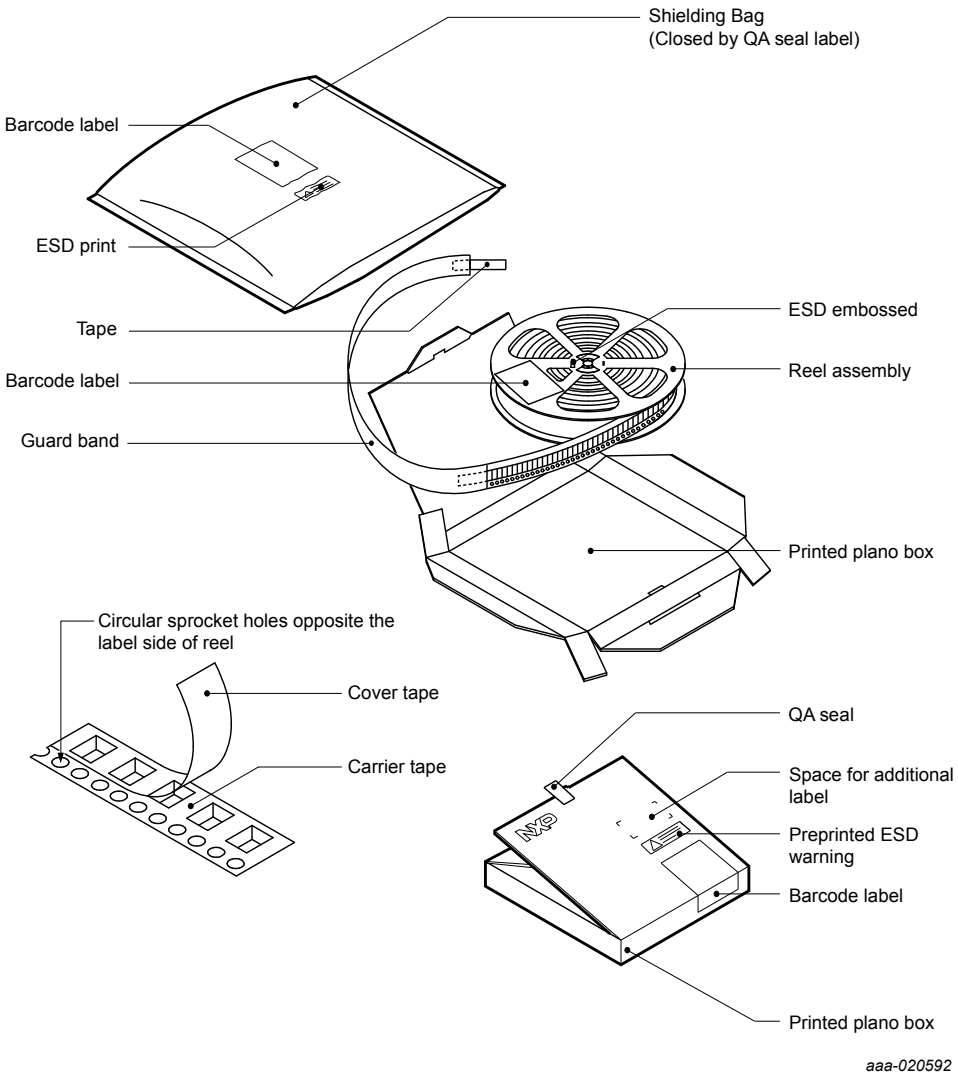


Figure 35. **Product orientation in carrier tape**

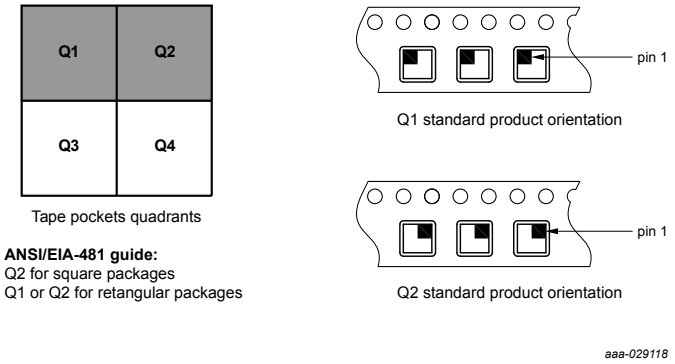


Figure 36. **Example of carrier tape dimensions (in accordance with IEC 60286-3)**

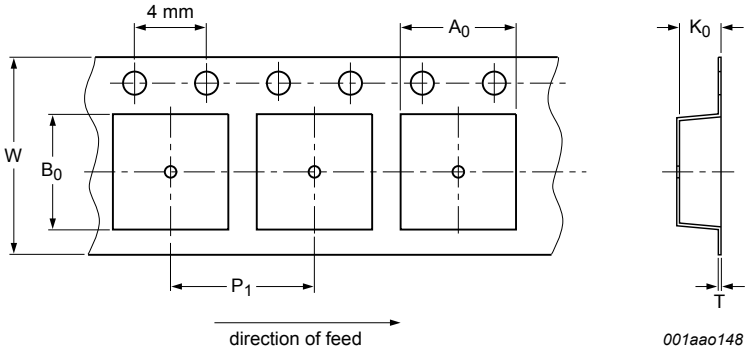


Table 6. **Example of carrier tape dimensions**

A_g (mm)	B_g (mm)	K_g (mm)	T (mm)	P_1 (mm)	W (mm)
2.30 ± 0.10	2.30 ± 0.10	0.75 ± 0.10	0.30 ± 0.05	4.0 ± 0.1	0.80 ± 0.3

Figure 37. **Schematic view of reel**

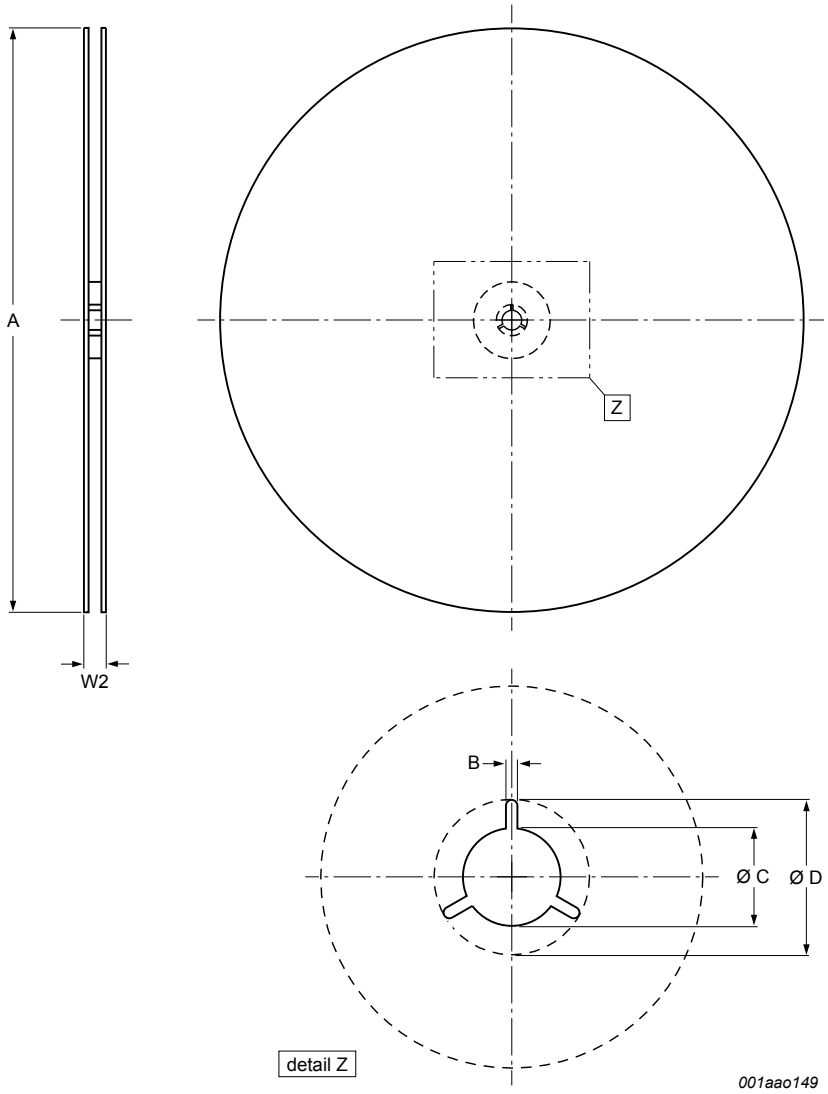


Table 7. **Reel dimensions (in accordance with IEC 60286-3)**

A [nom] (mm)	W2 (mm)	B [min] (mm)	C [min] (mm)	D [min] (mm)
180 (7”)	Depending on tape width	1.5	12.8	20.2
330 (13”)				

6 References

[1] JEDEC MO-220, Thermally Enhanced Plastic Very Thin and Very Very Thin Fine Pitch Quad Flat No Lead Package

[2] JEDEC MO-229, Thermally Enhanced Plastic Very Thin, Very Very Thin and Ultra Thin Fine Pitch Small Outline No Lead Package

[3] IEC 60286-3, Packaging of components for automatic handling. Part 3: Packaging of surface mount components on continuous tapes

[4] JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)

[5] JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

[6] JESD51-5, Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms

[7] JESD 51-6, Integrated Circuits Thermal Test Method Environment Conditions – Forced Convection (Moving Air)

[8] JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages, February 1999

[9] JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

[10] JESD51-8, Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board, October 1999

[11] IPC/JEDEC J-STD-020, Moisture/reflow sensitivity classification for nonhermetic surface mount devices

[12] IPC/JEDEC J-STD-033, Handling, packing, shipping, and use of moisture/reflow sensitive surface-mount devices

[13] MIL-STD-883, Method 1012.1 Thermal Characteristics

[14] IPC-7351B, Generic Requirements for Surface Mount Design and Land Pattern Standards

[15] IPC-7093, Design and Assembly Process Implementation for Bottom Termination SMT Components

[16] IPC, J-STD-004, Requirements for Soldering Fluxes

[17] IPC, J-STD-005, Requirements for Soldering Pastes

[18] IPC, J-STD-006, Requirements for Electronic Grade Solder Alloys

[19] ANSI/EIA-481, 8 mm Through 200 mm Embossed Carrier Taping and 8 mm & 12 mm Punched Carrier Taping of Surface Mount Components for Automatic Handling

Revision history

Table 8. **Document revision history**

Date	Version	Changes
30-Jul-2026	1	Initial release from ST, rebranded NXP document

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