Parasitic turn-on evaluation in silicon carbide MOSFETs

Introduction

This application note provides fundamental design considerations for gate bias supply circuits and presents several implementation examples that can be used as a starting point in power conversion applications. In addition, it describes the main characteristics of ST gate drivers and their influence on circuit behavior under real operating conditions. To further support the design discussion, the document includes measurement data collected with 650 V and 1200 V devices, to evaluate the effects associated with parasitic turn-on (PTO). These results help illustrate the conditions under which PTO may occur and the impact it can have on system performance. Finally, the application note outlines practical guidelines and mitigation techniques aimed at reducing the risk of parasitic turn-on and improving overall robustness and reliability in high-voltage gate-driving applications.

Silicon carbide (SiC) MOSFETs enable significantly higher switching frequency, lower switching losses, and higher temperature operation than silicon IGBTs and superjunction MOSFETs. However, these advantages come with stricter gate-drive and layout requirements. Fast voltage slew rate dv/dt, higher di/dt, low gate threshold voltage, and strong Miller coupling make gate-driver architecture one of the most critical parts of the power stage design.

1 Characteristics of SiC MOSFETs relevant to gate driving

Silicon carbide (SiC) MOSFETs are characterized by extremely fast switching capabilities, with voltage slew rates commonly exceeding 50 V/ns to 200 V/ns. Compared with conventional IGBT-based solutions, these transition rates are roughly one order of magnitude higher. While this enables substantial gains in efficiency, switching frequency, and power density, it also places significantly stricter requirements on the inverter or converter design.

The high dv/dt and di/dt associated with SiC devices can generate several undesirable parasitic effects. Fast switching transitions may lead to:

- Ringing and oscillation driven by package, PCB, and layout parasitic inductances and capacitances.
- Common-mode current injection, which can propagate through parasitic capacitances and affect system behavior.
- Electromagnetic interference (EMI), increasing the complexity of compliance and filtering design.
- Additional stress on insulation and isolation barriers, especially in high-voltage applications.
- Parasitic turn-on (PTO) in bridge topologies, caused by Miller effect coupling during fast commutation events.

To improve switching robustness and reduce susceptibility to parasitic effects, several design techniques are commonly employed. Negative gate bias is often used in the off-state to increase the noise margin against unintended turn-on. In addition, Kelvin source connections help isolate the current power from the gate return path, thereby reducing the influence of common source inductance and improving switching accuracy.

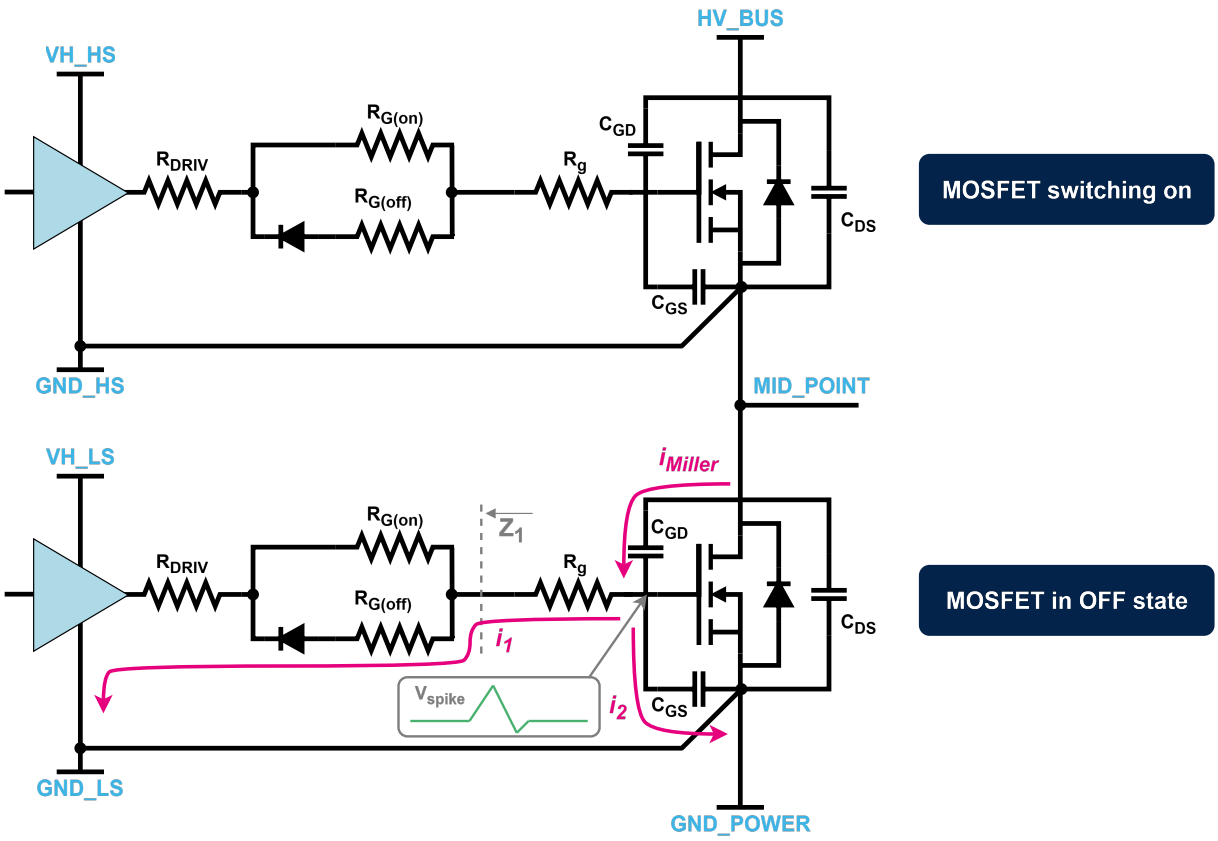
In conclusion, the use of SiC MOSFETs requires a comprehensive design approach that addresses parasitic optimization, gate-driver performance, EMI control, and insulation robustness to fully benefit from their superior switching characteristics.

2 Parasitic turn-on (PTO) phenomenon

The SiC MOSFETs are predominantly employed in bridge-based configurations across most power conversion topologies. To achieve high system performance with silicon carbide (SiC) MOSFETs, it is essential to select device characteristics that minimize switching and conduction losses.

When fast switching is introduced into a power application, careful attention must be given to the influence of switching transients on the unavoidable stray parasitic elements present in the circuit layout, packaging, and device environment. As switching edges become faster, the associated voltage and current transitions can interact with these parasitic components in ways that were previously negligible at lower switching speeds. In particular, the high dv/dt behavior of SiC MOSFETs can be coupled through the device's internal capacitances and external parasitic impedances, potentially generating unintended gate voltage glitch.

Figure 1. Gate glitch effect when the high-side MOSFET acts as an active switch



In a bridge configuration, the devices in the same leg share a common switching node (midpoint). When one MOSFET is turned on or off, the voltage transition at this node imposes a dv/dt of the same magnitude but opposite polarity across the complementary device. This induces a capacitive current that reaches the gate through the miller capacitance, as shown in the Figure 1. This Miller current can be calculated as:

$$i_{Miller} = C_{GD} \cdot \frac{dV_{DS}}{dt} \quad (1)$$

And this is what generates the gate glitch with an amplitude of:

$$V_{spike} = \left(R_g + Z_1\right) \cdot i_1 \quad (2)$$

Where $i_1 = i_{Miller} - i_2$ and R_g is the gate input resistance of SiC MOSFET.

If the amplitude of this glitch exceeds the threshold required to activate the device, it could trigger parasitic turn-on (PTO) events, which can lead to additional switching losses, increased electromagnetic interference, abnormal stress on the power stage, and reduced overall system robustness.

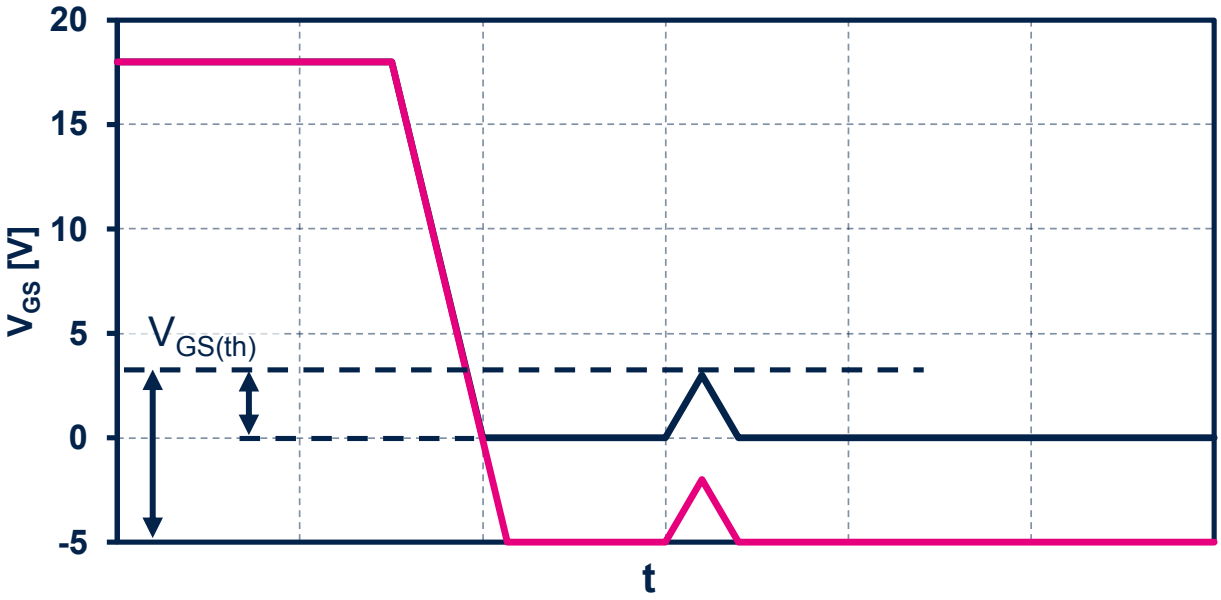
In a half-bridge circuit, the presence of severe PTO can simultaneously activate both MOSFETs to conduction, this may result in shoot-through failure. For this reason, minimizing parasitic turn-on is highly recommended.

SiC MOSFETs in the market have typical threshold voltages that range from $V_{GS(th)} \approx 2$ to 5 V. The low threshold voltage makes the devices vulnerable to unintended turn-on caused by:

- Miller current injection
- Ground bounce
- Source inductance coupling
- A transient gate spike

The Figure 2 shows how the negative turn-off voltage helps to keep the glitch away from the threshold voltage $V_{GS(th)}$.

Figure 2. Gate curves with turn-off level changing



The following figures show the different effect on the gate glitch in the positive or negative dv/dt: during a positive slew rate the glitch effect is positive too and can cause PTO (see the Figure 3), instead, during a negative slew rate the glitch will be negative (see the Figure 4).

Figure 3. Glitch phenomena during positive V_{DS} slew rate

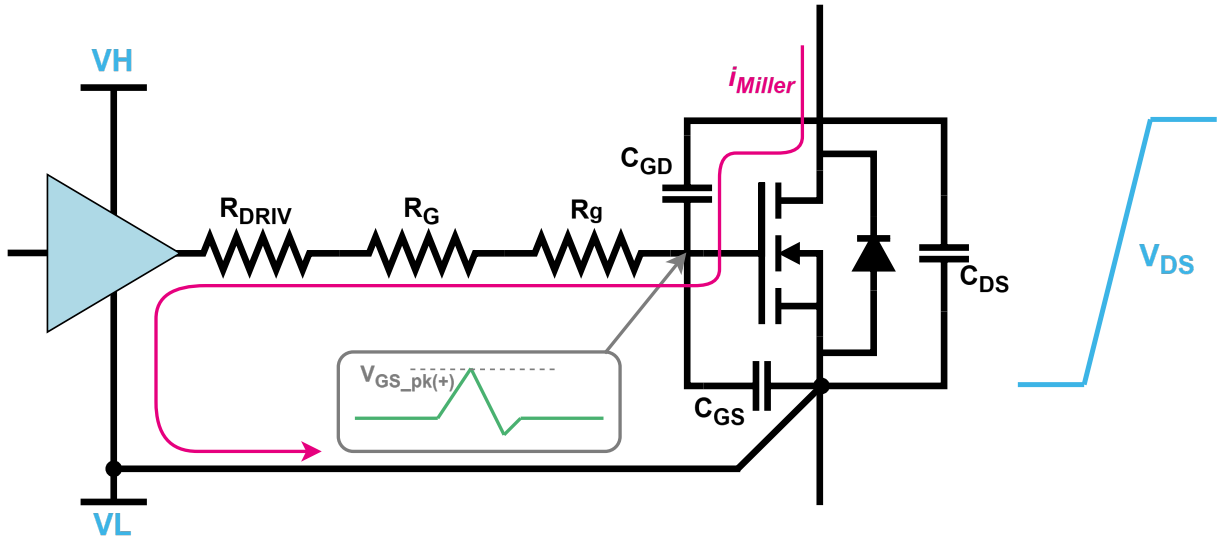
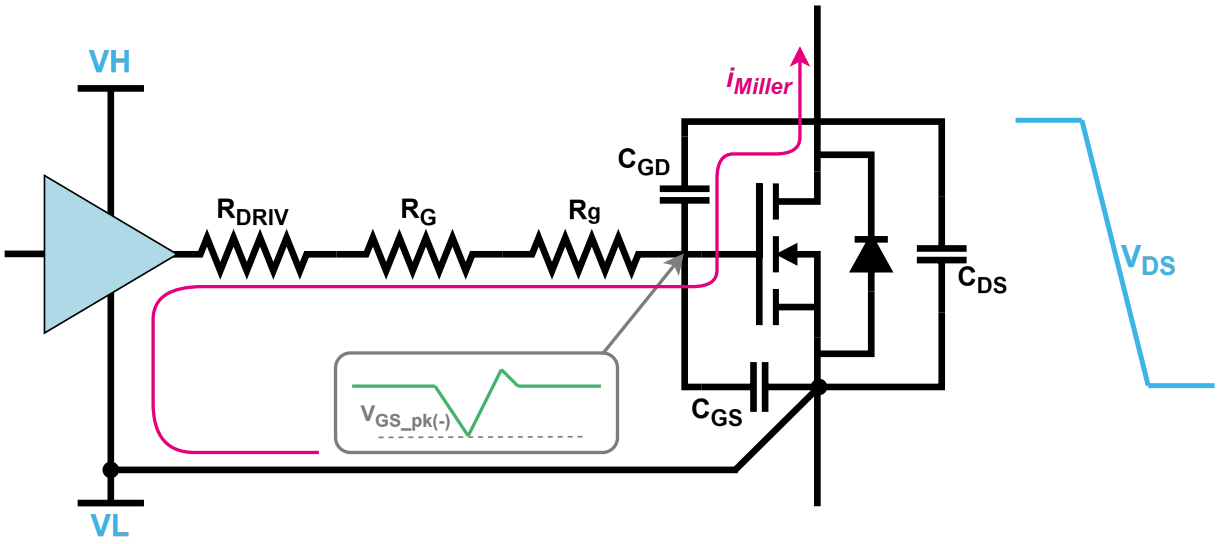


Figure 4. **Glitch phenomena during negative V_{DS} slew rate**



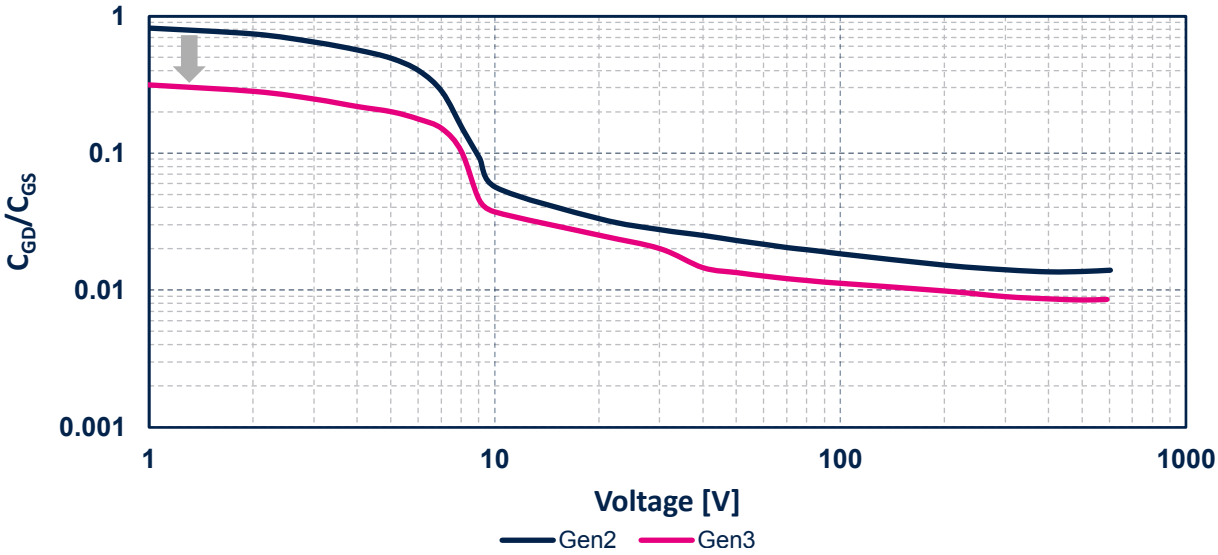
Compared to silicon MOSFETs, SiC MOSFETs' gate oxide is more sensitive having a lower maximum gate voltage rating. For this reason, also the negative glitches caused by negative dv/dt (see the Figure 4) need to be evaluated to keep the device in safe operation.

As regards Gen 3 SiC MOSFETs, ST declares $V_{GS(-)}$ = -10 V and $V_{GS(+)}$ = 22 V as absolute maximum ratings and a recommended operating voltage of $V_{GS(-)}$ = -5 V and $V_{GS(+)}$ = 18 V to have a safeguard with respect to the limits.

Considering the significant advantages offered by silicon carbide (SiC) MOSFETs in power conversion applications, designers should carefully consider a set of key recommendations during system development to fully leverage the benefits of this technology and ensure optimal performance under operating conditions:

- **Gate resistance**
  In topologies where high side and low side MOSFETs have the same couple of gate resistors (that is, in totem pole) it should be advisable to select $R_{G(on)} > R_{G(off)}$. This to contain the voltage spike on the gate of the MOSFET supposed off while the complementary device is switching on.
- **External capacitance (C_{GS-ext})**
  Add an external capacitance between the gate and source, a few nF can be enough to improve performance and reduce V_{GS} spikes.
- **Active Miller clamp**
  Use a gate driver with an active Miller clamp that keeps low the gate-source impedance of the MOSFETs in off state.
- **PCB layout**
  Optimize the PCB layout to minimize stray inductances, which can exacerbate the Miller effect.
- **Miller capacitance ratio**
  Choose MOSFETs with a gate-drain to gate-source capacitance ratio (C_{GD}/C_{GS}) as low as possible (see the Figure 5).
- **Threshold voltage ($V_{GS(th)}$)**
  Threshold voltage is a key parameter and the worst-case condition must be considered for appropriate design immunity in case of gate spikes.

Figure 5. C_{GD}/C_{GS} capacitance ratio for Gen2 and Gen3 20 mΩ, 650 V SiC MOSFETs



3 STGAP3S gate driver series for SiC MOSFETs

The STGAP product series offers gate drivers with advanced embedded features and configurable options designed to properly support the switching characteristics, fast transient behavior, and high dv/dt immunity requirements of SiC MOSFETs in high-performance power systems.

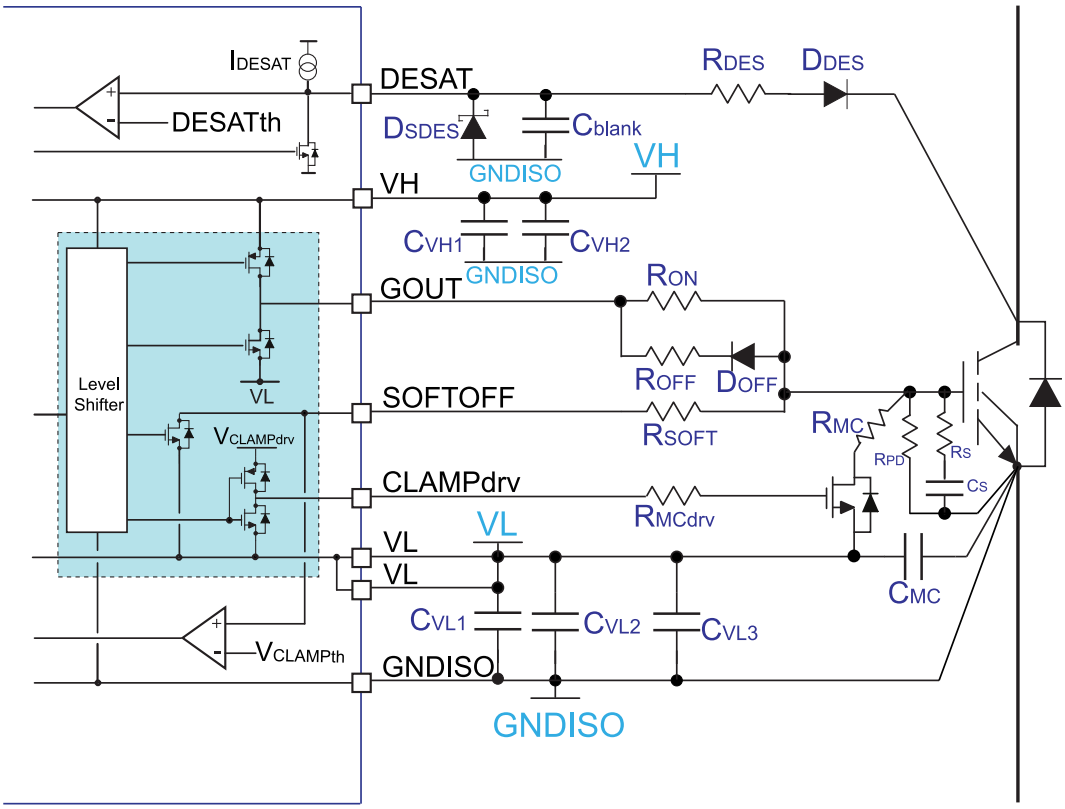
STGAP3S is a product of the STGAP family series. The embedded characteristics include fast desaturation protection and a flexible Miller clamp function, making it suitable for industrial and energy applications. With high common-mode transient immunity (CMTI), this gate driver meets the latest requirements in terms of current capability and protection functions. The STGAP3S series includes different options with 10 A and 6 A current capabilities, each available with dedicated UVLO variants for SiC MOSFETs and IGBTs.

The list of the key features of the STGAP3S includes:

- BCD9S galvanic isolation technology
- High voltage: up to 1200 V
- Driver current: 6 A and 10 A
- Drive SiC MOSFETs and IGBTs
- Desaturation protection
- Adjustable soft turn-off function
- Fast response: 75 ns delay
- Miller CLAMP function
- Optional negative driving
- ±200 V/ns CMTI

A practical implementation to drive a SiC MOSFET using all the STGAP3S features is shown in the Figure 6.

Figure 6. STGAP3S gate driving side schematic with all protection and features



Related links

STGAP3Sxx: Galvanically isolated 6/10 A single gate drivers with protection features

4 Driving circuit implementation examples

The STGAP3S allows to implement either unipolar gate driving or bipolar gate driving for the power switch. In the case of bipolar gate driving (see the Figure 7), the negative supply voltage shall be connected between the GNDISO and VL pins. The use of negative gate driving can further mitigate the risk of induced turn-on due to Miller effect in hard-switching conditions and can also help to increase the turn-off speed of the power switch.

If a unipolar gate driving is used (see the Figure 8), the GNDISO and VL pins shall be connected by means of short traces.

Figure 7. Minimal circuit for bipolar gate driving

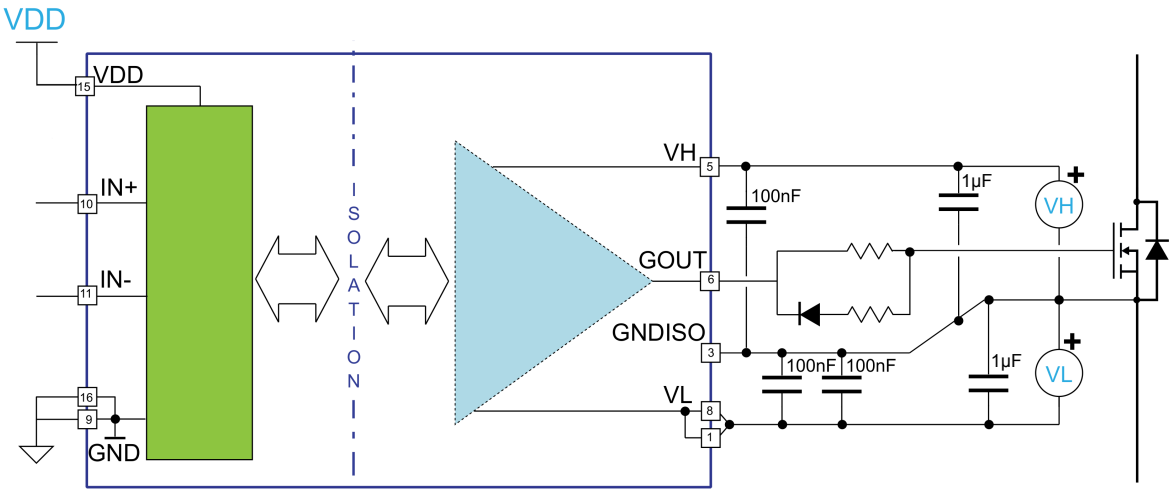
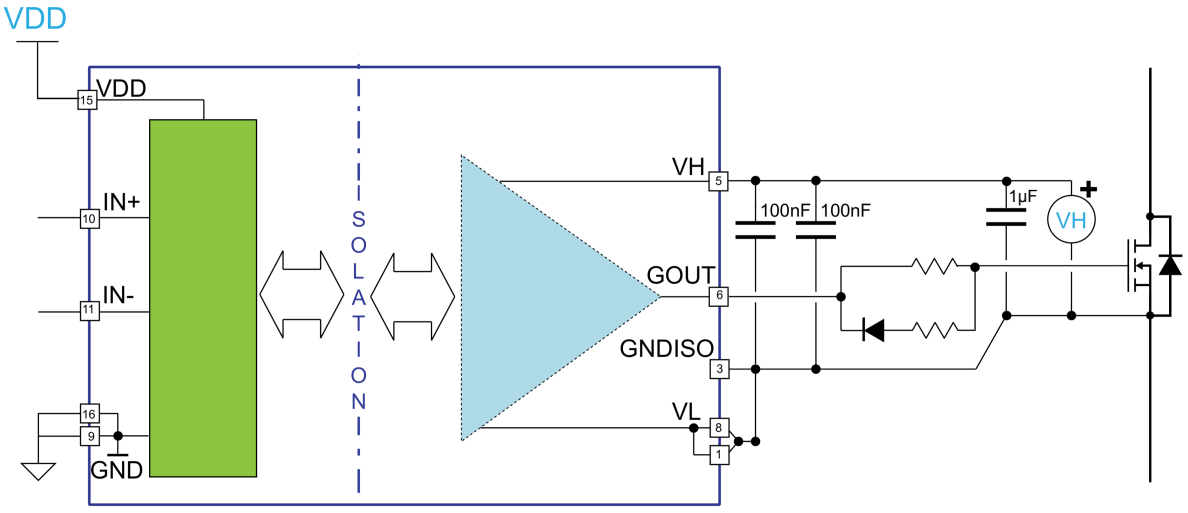


Figure 8. Minimal circuit for unipolar gate driving



Typical ways to generate gate bias power supply rails with negative turn-off voltage are shown in the Figure 9 and Figure 10.

Figure 9. Gate bias power supply for bipolar gate driving with flyback transformer

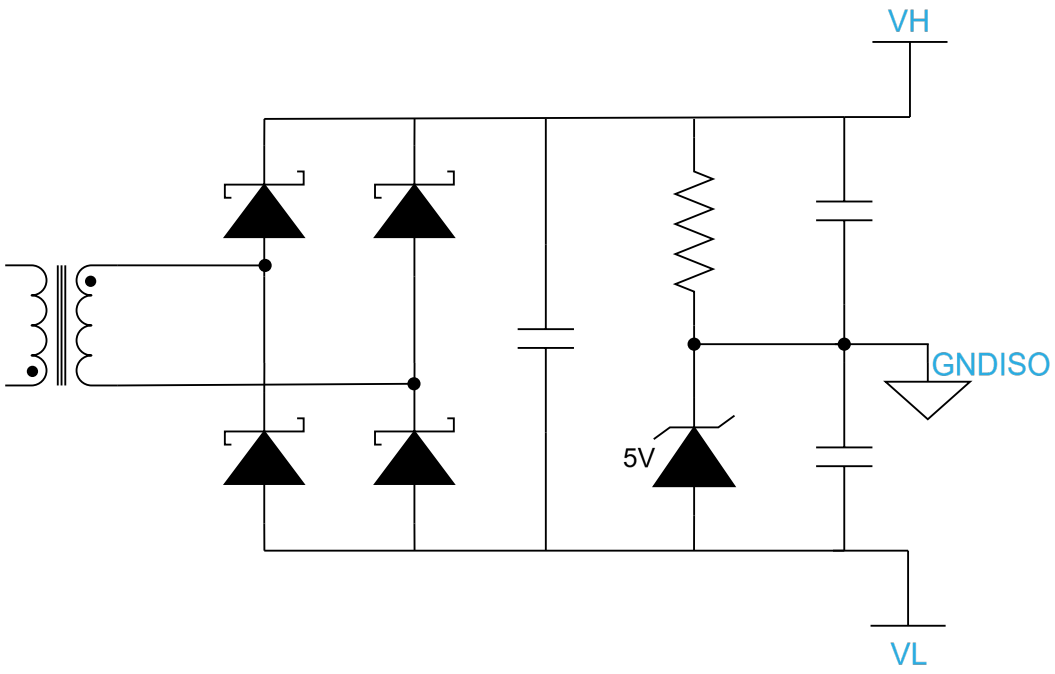
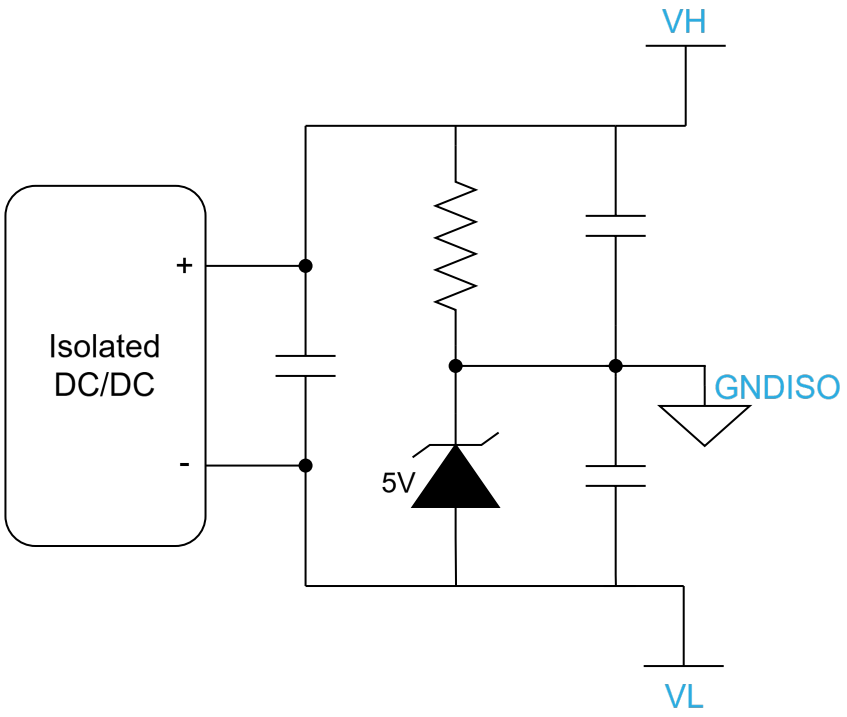


Figure 10. Gate bias power supply for bipolar gate driving with isolated DC-DC



Most of the time, a negative bias for turning off SiC MOSFETs is recommended for hard-switched operation; this helps to improve the device immunity to undesired to on.

The use of a 0 V turn-off gate voltage can simplify SiC gate-driver design by eliminating the requirement for a negative supply rail, thereby reducing circuit complexity and component count. This approach is particularly advantageous in compact power converters, where board-area, minimization and reduction of auxiliary circuitry are key design objectives. It can also ease the transition from silicon-based to SiC-based implementations by preserving a unipolar gate-drive architecture, which is generally more straightforward to integrate into existing system designs.

In addition, eliminating the negative bias rail may reduce isolation requirements, lower auxiliary power consumption, and simplify PCB routing. These benefits may improve manufacturability and enable higher power density, especially in applications such as SMPS for datacenter AI.

Nevertheless, the use of 0 V turn-off must be assessed with care, since SiC MOSFETs exhibit very fast switching transients that can induce unwanted gate voltage rise through the Miller capacitance. Ensuring reliable operation therefore requires attention to gate-loop inductance, Kelvin-source connection quality, gate resistance selection, and overall layout optimization. Under properly controlled conditions, 0 V turn-off can be an effective solution that balances implementation simplicity with switching robustness.

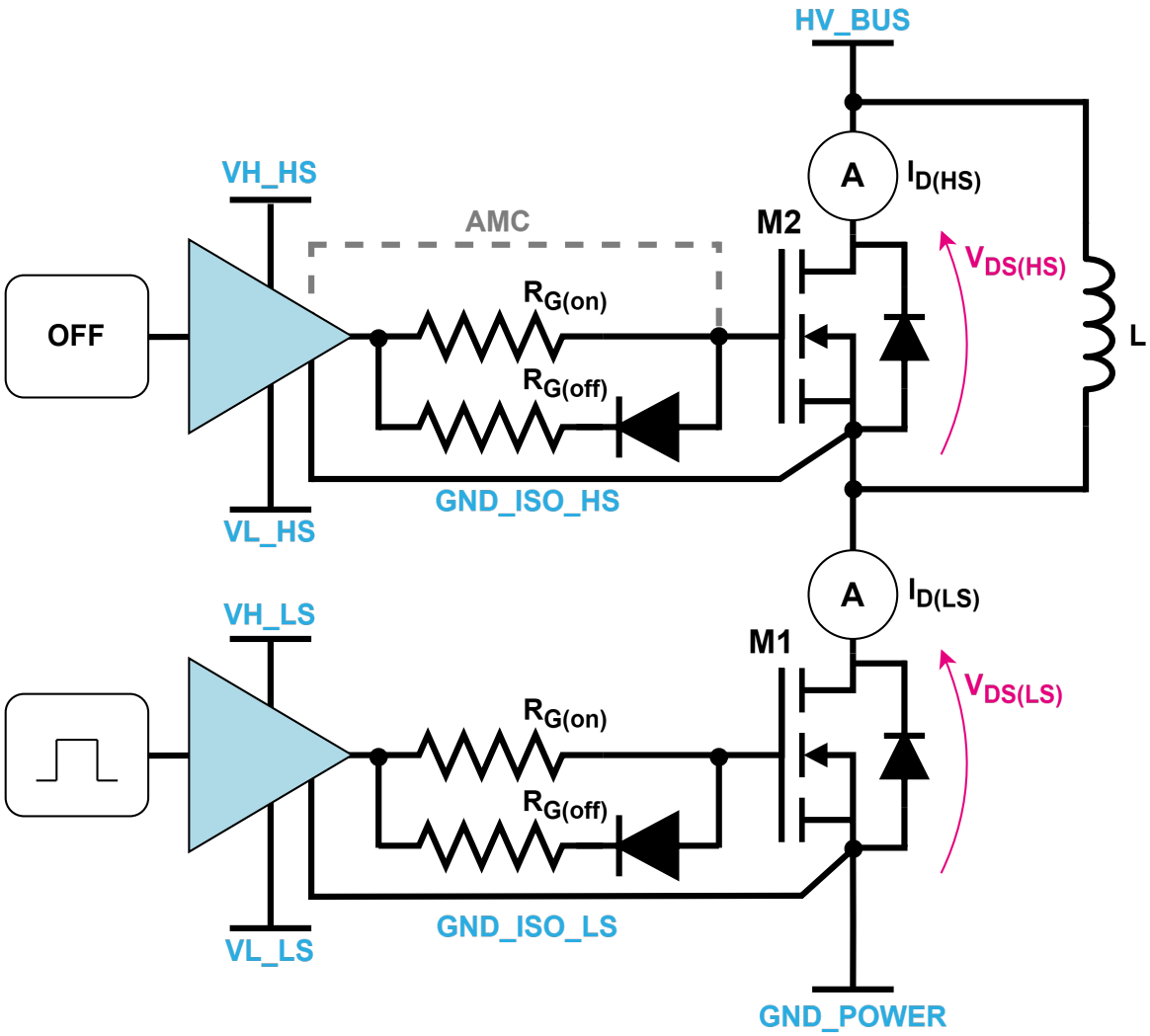
5 Case study about PTO using SiC MOSFET Gen3 technology

To evaluate the PTO susceptibility, SiC MOSFET Gen3 experimental tests were done using devices with two breakdown voltage 650 V and 1200 V.

The objective was to verify the device's behavior in a half-bridge configuration during controlled dynamics voltage and current commutations by means of double pulse test shown in the Figure 11. In half-bridge application conditions, we assume that the gate-drive resistors are the same for both MOSFETs.

The probes $I_{D(HS)}$ and $V_{DS(HS)}$ are used to measure the E_{rec} energy dissipated on the HS MOSFET due to the recovery energy of the body diode and including the contribution of the PTO if present. The $I_{D(LS)}$ and $V_{DS(LS)}$ are used to measure the switching energies of the LS MOSFET (E_{on} and E_{off}). Since we are focusing on the PTO of the HS MOSFET, the E_{off} was not reported.

Figure 11. Double pulse test schematic for PTO evaluation



For both the 650 V and 1200 V device classes, a preliminary check of the DPT board was performed to ensure that the electrical dynamics to be applied to the DUTs would not create any critical stress at the device level. Test conditions have been then considered next.

6 Case study SiC 650 V

In this section, the measurement results of a SCT027TO65G3 are presented under the following test conditions:

- T_J = 150 °C (worst case)
- Turn-on, current slew rate: di/dt_{ON} ≈ 1.5 A/ns (by setting $R_{G(on)}$ value)
- Turn-off, voltage slew rate: dv/dt_{OFF} ≈ 18 V/ns (by setting by $R_{G(off)}$ value)
- V_{BUS} = 400 V
- $I_{D(max)}$ = 40 A
- $V_{GS(off)}$ = 0V with and without active Miller clamp versus negative voltage as PoR
- $V_{GS(th)}$ = 2.8 V (measured)

The comparison of E_{sw} versus I_D was performed using a 27 mΩ typ Gen3 SiC MOSFET as the test vehicle. To ensure a consistent basis for energy comparison under the two gate-bias conditions, $V_{GS(off)}$ = -5 V and $V_{GS(off)}$ = 0 V, the same evaluation criterion was adopted for both measurement sets. Because di/dt_{ON} does not depend on the value of $V_{GS(off)}$ but on the value of $V_{GS(on)}$ (which remains unchanged at 18 V), the value of $R_{G(on)}$ for $V_{GS(off)}$ = 0 V is the same as the value used for $V_{GS(off)}$ = -5 V. The procedure was initiated at $V_{GS(off)}$ = -5 V.

The criterion used to select $R_{G(on)}$ and $R_{G(off)}$, evaluated at $I_{D(MAX)}$, is as follows:

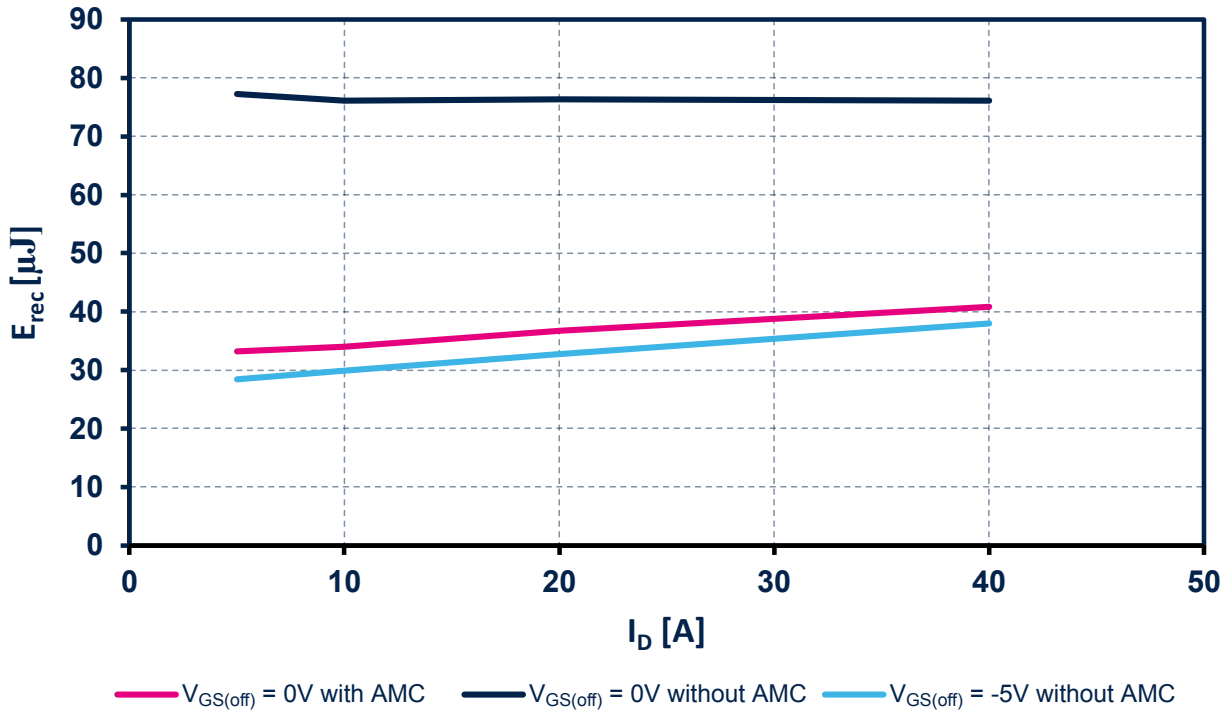
- Set the $R_{G(on)}$ value by imposing the target di/dt(on) of M1 and the overvoltage across M2 associated to its body diode recovery.
- Set the $R_{G(off)}$ value to achieve a target dv/dt, and therefore a di/dt, to keep the overvoltage on M1 below $V_{(BR)DSS}$.

The first set of switching measurements was then recorded.

A similar procedure was then repeated using $V_{GS(off)}$ = 0 V. Once the corresponding $R_{G(off)}$ value was adjusted to meet the target condition, a new set of switching energy measurements was recorded. Noted that $R_{G(off)}$ at 0 V has not the same value of the $R_{G(off)}$ at -5 V.

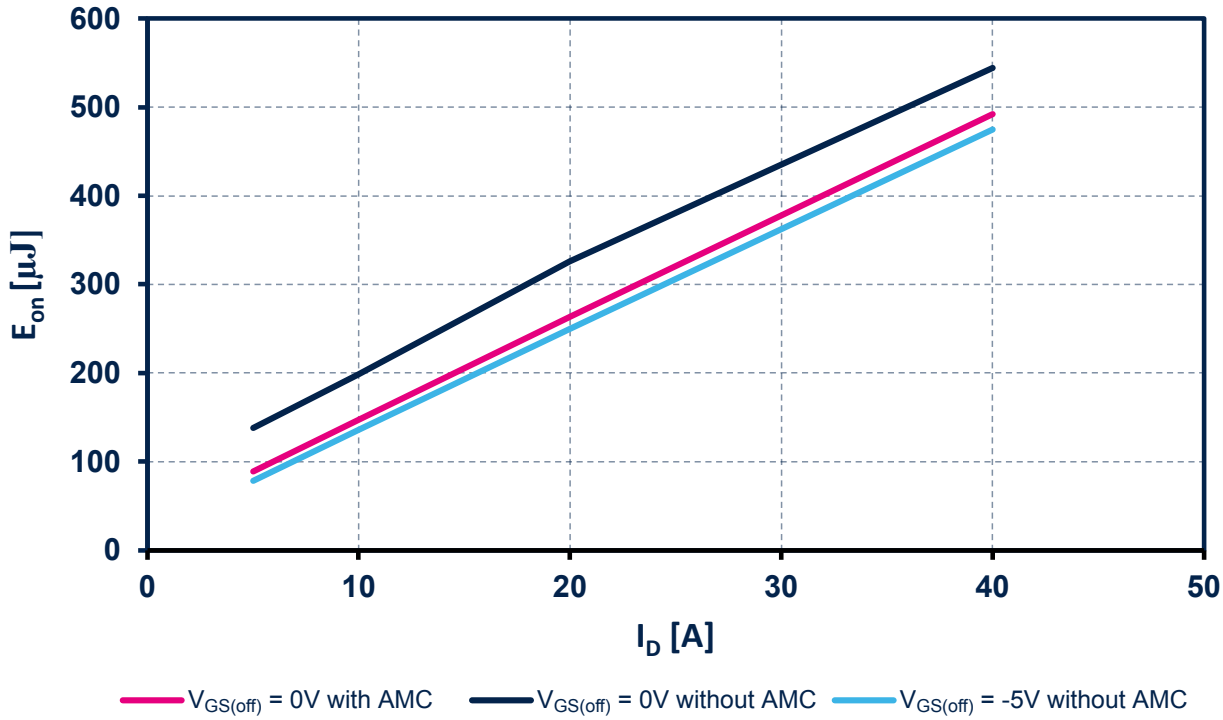
The Figure 12 shows E_{rec} at different gate driving conditions. In particular, when the $V_{GS(off)}$ is set to 0 V and no active Miller clamp (AMC) is used, the E_{rec} is significantly higher than with -5 V and no AMC. A substantial improvement is visible in the chart when 0 V is used in combination with AMC. In this case, the recovered energy almost overlaps with the curve obtained at -5 V without AMC. This result confirms that 0 V driving is feasible when used together with the AMC function.

Figure 12. **Recovery energy vs drain current with SCT027TO65G3 SiC MOSFET**



The Figure 13 shows that there is no significant difference between -5 V and 0 V when the latter is used together with AMC. In this case as well, the contribution of E_{rec} to E_{on} is practically negligible for both -5 V and 0 V with AMC. By contrast, in the 0 V without AMC condition, an increase of E_{rec} is observed.

Figure 13. **On-energy vs drain current with SCT027TO65G3 SiC MOSFET**



Related links

SCT027TO65G3: Silicon carbide Power MOSFET 650 V, 29 mΩ typ., 60 A in a TO-LL package

7 Case study SiC 1200 V

In this section, the measurement results of a SCT025W120G3-4AG are presented under the following test conditions:

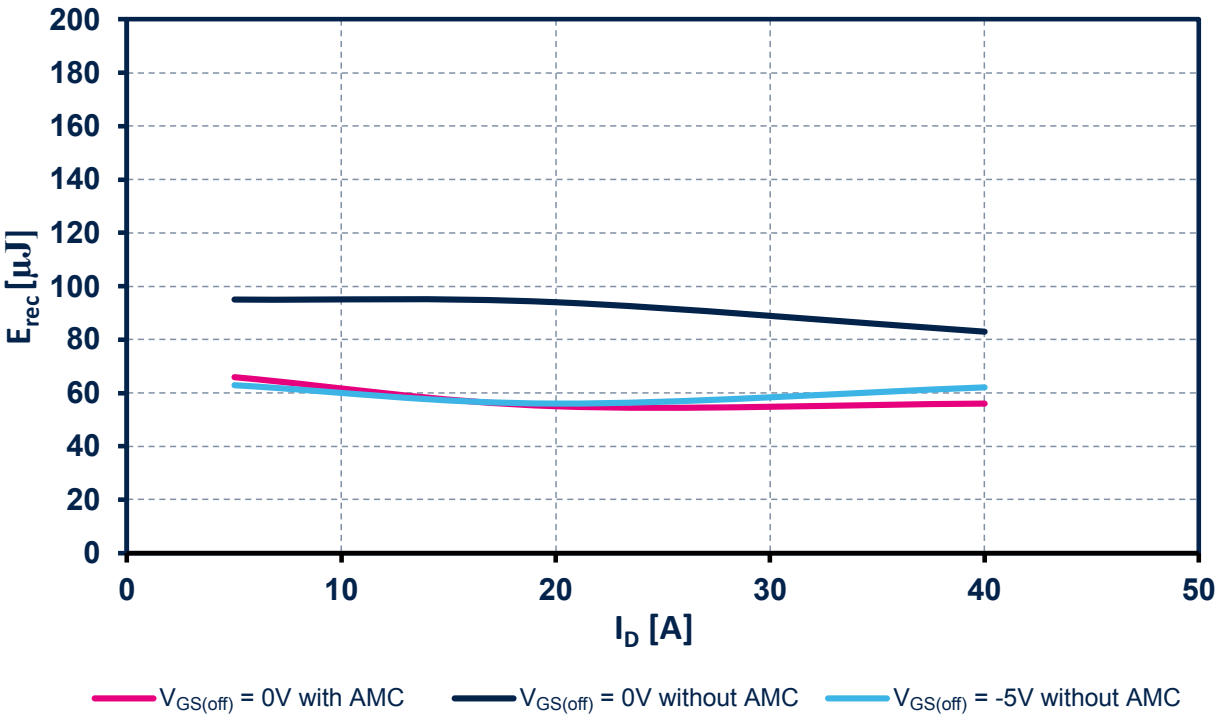
- T_J = 150 °C (worst case)
- Turn-on, current slew rate: $di/dt_{ON} \approx 2$ A/ns (by setting $R_{G(on)}$ value)
- Turn-off, voltage slew rate: $dv/dt_{OFF} \approx 35$ V/ns (by setting by $R_{G(off)}$ value)
- V_{BUS} = 800 V
- $I_{D(max)}$ = 40 A
- $V_{GS(off)}$ = 0V with and without active Miller clamp versus negative voltage as PoR
- $V_{GS(th)}$ = 2.8 V (measured)

Even with 1200 V devices the results are consistent with 650 V when AMC is used.

The same procedure used for the 650 V device was also applied to the 1200 V device in order to meet the target conditions.

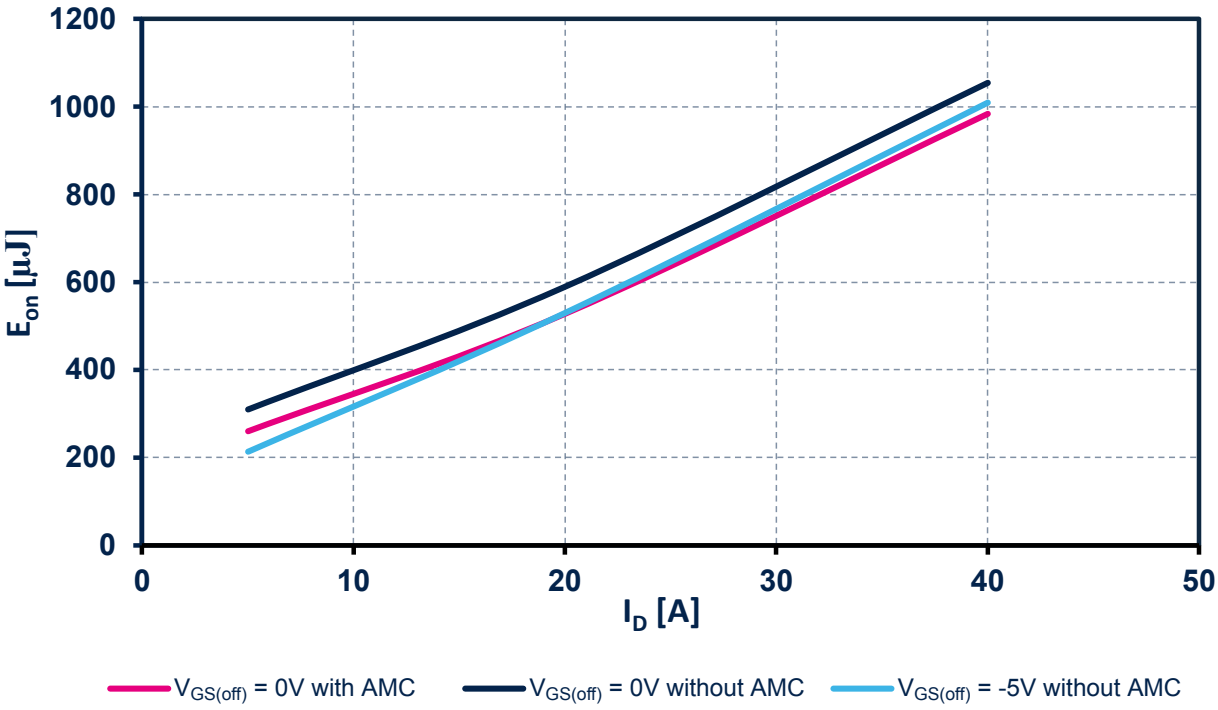
The Figure 14 shows E_{rec} at different gate driving conditions. In particular, when the $V_{GS(off)}$ is set to 0 V and no active Miller clamp (AMC) is used, the recovered energy is significantly higher than with -5 V and no AMC.
A substantial improvement is visible in the chart when 0 V is used in combination with AMC. In this case, the recovered energy almost overlaps with the curve obtained at -5 V without AMC. This result confirms that 0 V driving is feasible when used together with the AMC function.

Figure 14. Recovery energy vs drain current with SCT025W120G3-4AG SiC MOSFET



The Figure 15 shows that there is no significant difference between -5 V and 0 V when the latter is used together with AMC. In this case as well, the contribution of E_{rec} to E_{on} is practically negligible for both -5 V and 0 V with AMC. By contrast, in the 0 V without AMC condition, an increase of E_{rec} is observed.

Figure 15. On-energy vs drain current with SCT025W120G3-4AG SiC MOSFET



Related links

SCT025W120G3-4AG: Automotive-grade silicon carbide Power MOSFET 1200 V, 27 mΩ typ., 56 A in an HiP247-4 package

8 Conclusion

The results for both voltage classes, 650 V and 1200 V, are consistent and lead to the same conclusion. The observed behavior does not depend on the voltage rating within the tested range. Instead, it depends on the operating conditions associated with the $V_{GS(off)}$ = 0 V state. Under this condition, PTO has a more pronounced effect on switching performance and can significantly increase total switching losses. From a design perspective, if the goal is to reduce the switching-loss penalty associated with PTO, an AMC gate driver circuit is strongly recommended. Without an AMC gate driver circuit, increased switching losses must be considered, with possible effects on efficiency, thermal performance, and converter optimization. For efficiency-critical applications, especially under the $V_{GS(off)}$ = 0 V condition, the AMC gate driver circuit is the most effective solution to mitigate PTO effects and ensure robust system performances.

Appendix A Other information

A.1 Reference documents

[1] Application note *Mitigation technique of the SiC MOSFET gate voltage glitches with Miller clamp* (AN5355)

[2] Datasheet *Automotive-grade silicon carbide Power MOSFET 1200 V, 27 mΩ typ., 56 A in an HiP247-4 package* (DS14279)

[3] Datasheet *Galvanically isolated 6/10 A single gate drivers with protection features* (DS14758)

[4] Datasheet *Silicon carbide Power MOSFET 650 V, 29 mΩ typ., 60 A in a TO-LL package* (DS14846)

Revision history

Table 1. **Document revision history**

Date	Revision	Changes
05-Aug-2026	1	First release.

Contents

List of figures