How to design a 10BASE-T1S application using STM32

Introduction

This application note explains how to design an application using Single-Pair Ethernet 10BASE-T1S connectivity. It focuses on microcontrollers, especially STM32 devices, integrating an Ethernet MAC that complies with IEEE 802.3.

The document provides hardware guidelines for the STM32 NUCLEO-H563ZI board to support the X-CUBE-T1S reference firmware package. It is intended to help users understand the required system architecture and key design considerations for developing 10BASE-T1S-enabled embedded applications.

1 Single-Pair Ethernet 10BASE-T1S overview

Single-Pair Ethernet (SPE) is an Ethernet physical layer defined by the IEEE 802.3-2022 standard that transmits data over a single pair of copper wires instead of two-pair or four-pair cables.

SPE maintains compatibility with Ethernet-based communication stacks and extends Ethernet communication to field-level devices.

SPE includes different variants based on data rate, connection topology, cable features, and distance coverage. Among these variants, 10BASE-T1S provides a 10 Mbit/s data rate over a single unshielded twisted pair.

10BASE-T1S supports both full-duplex and half-duplex point-to-point communication over distances up to 15 m, and half-duplex multidrop network topology over distances up to 25 m. In multidrop mode, multiple devices can share the same physical medium, typically up to at least eight nodes.

To avoid collisions in shared-medium communication, 10BASE-T1S supports PLCA (Physical Layer Collision Avoidance). This feature improves network efficiency, ensures fair access to the medium, and provides bounded maximum latency compared to traditional CSMA/CD behavior.

These features make 10BASE-T1S particularly suitable for short-reach, cost-effective, IP-based communication in automotive, industrial automation, building automation, robotics, and sensor or actuator networks.

2 Embedded system hardware design guidelines

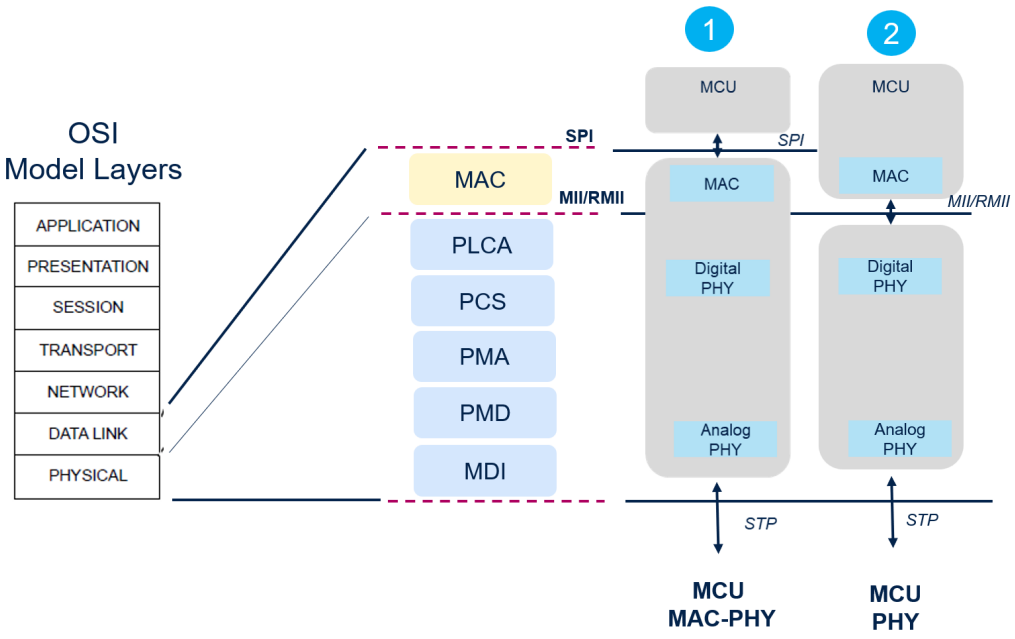
This section describes the physical and data link layers of the OSI model. It focuses on standard Ethernet and 10BASE-T1S. The section also presents possible architecture options. These options are for implementing 10BASE-T1S in systems that use microcontrollers as hosts.

2.1 MCU-based 10BASE-T1S architecture

In a microcontroller-based design, a 10BASE-T1S network requires two main functional blocks: a standard Ethernet MAC (media access controller) and the suitable PHY (physical layer transceiver) made of digital and analog sub blocks. Depending on microcontroller integrated features, the system can be implemented in two different ways. Figure 1 represents the options in relation to the OSI layers, device features and proper interface peripherals. 10BASE-T1S has a specific physical layer integrating PCS (physical coding sublayer), PMA (physical medium attachment), PMD (physical medium dependent), and PLCA (physical layer collision avoidance) components, while the data link layer is the standard Ethernet layer based on MAC (media access control).

The upper layers support a multitude of protocols used in the standard Ethernet applications.

Figure 1. 10BASE-T1S MCU and PHY architecture options



2.1.1 Architecture 1: General purpose MCU without integrated Ethernet MAC

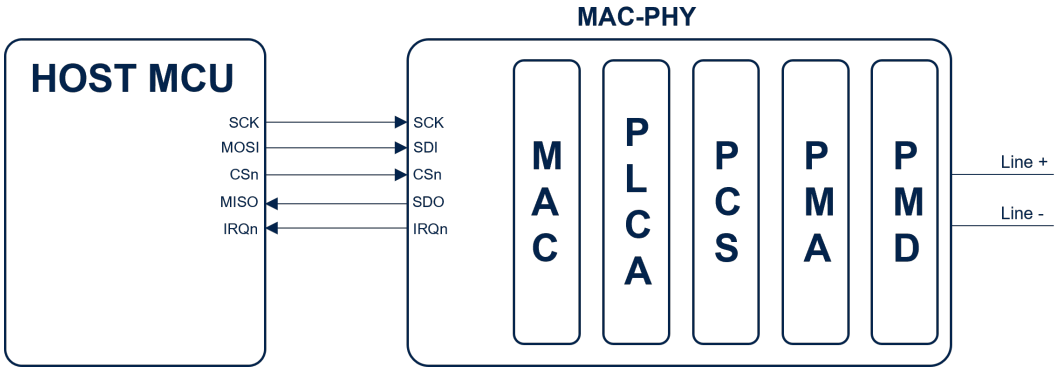
For general purpose MCUs not integrating a standard Ethernet MAC, it is possible to interface them with a 10BASE-T1S MAC-PHY using a standard high-speed SPI (Serial Peripheral Interface) plus an interrupt pin (see Figure 2).

In this case, the standard Ethernet MAC sublayers and the 10BASE-T1S PHY are integrated into the same device.

In this scenario, the host MCU includes the MAC client layer, and it has to build Ethernet packets and parse incoming ones according to the OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification.

Operations such as padding and frame check sequence (FCS) computation are delegated to the MAC sublayers integrated in the MAC-PHY devices, as well as the implementation of PLCA and physical layers (PCS, PMA, and PMD).

Figure 2. **10BASE-T1x serial interface pins (OPEN Alliance specification)**



This architecture is suitable for applications based on MCUs without an integrated standard Ethernet MAC.

However, since SPI is not an Ethernet-native data path, it has certain limitations, including increased latency and additional firmware overhead required to manage the OPEN Alliance specification.

2.1.2 Architecture 2: MCU with integrated Ethernet MAC

The most common hardware architecture used in Ethernet applications involves a microcontroller equipped with a standard Ethernet MAC and a PHY device, with the two interconnected via MII (media independent interface) or RMII (reduced media independent interface).

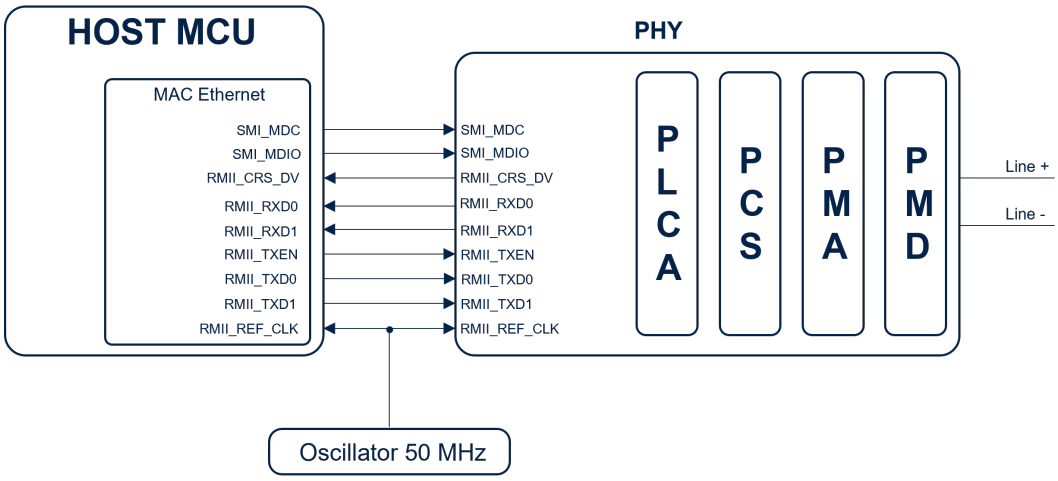
The same interfaces can also be used in Single-Pair Ethernet 10BASE-T1S applications, connecting the MCU to a 10BASE-T1S PHY via MII or RMII.

This solution is the easiest to manage, since it requires very limited additional hardware and firmware adaptations compared with a standard Ethernet scenario.

From the microcontroller perspective, there are no additional operations required, apart from configuring the PLCA parameters, compared to a standard Ethernet PHY implementation.

Thanks to these advantages, the reuse of IP-based application protocols is more effective and quicker to implement.

Figure 3. **10BASE-T1S PHY interface**



3 Reference hardware design

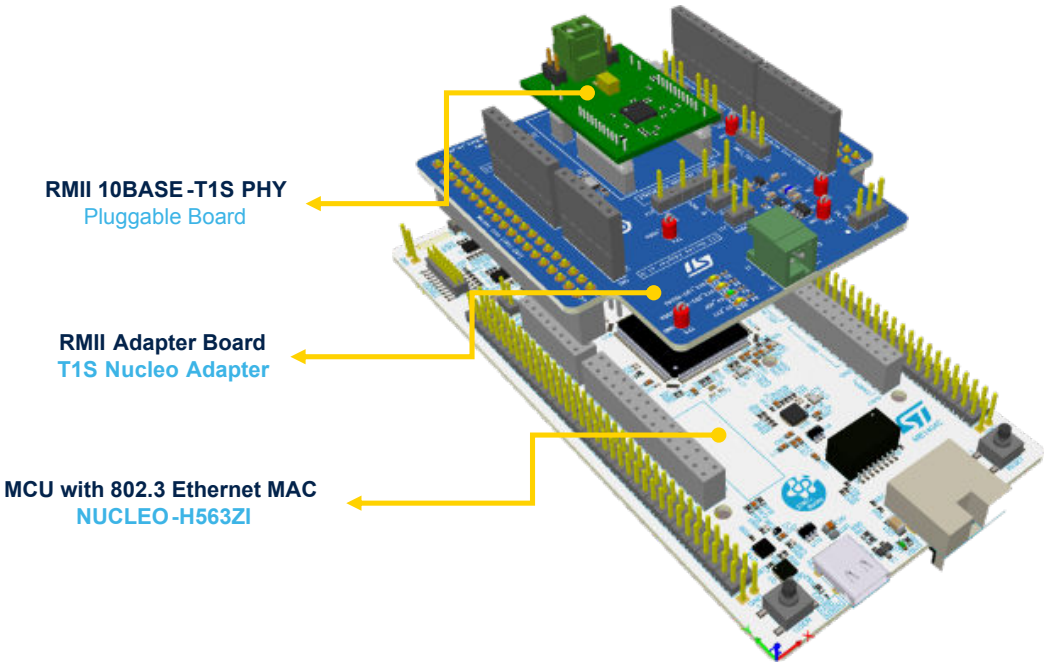
This section describes a possible hardware implementation that is suitable for evaluating a 10BASE-T1S application in combination with the available X-CUBE-T1S firmware package that runs on an STM32 microcontroller.

It is based on architecture 2 described in Section 2.1.2 and on an STM32 microcontroller integrating a media access control (MAC) interface connected to a 10BASE-T1S PHY through RMII.

The proposed system is based on the STM32 NUCLEO-H563ZI, a development board with the STM32H563ZI microcontroller (MCU) that features an 802.3 Ethernet MAC, an RMII 10BASE-T1S PHY, and a dedicated adapter board that bridges the STM32 to the external PHY.

The adapter board, hereinafter referred to as the T1S Nucleo Adapter, includes the minimum external components that are required for proper operation, such as the RMII 10BASE-T1S PHY board, a 50 MHz RMII clock, and related signal connections that ensure the link between the MAC and the PHY.

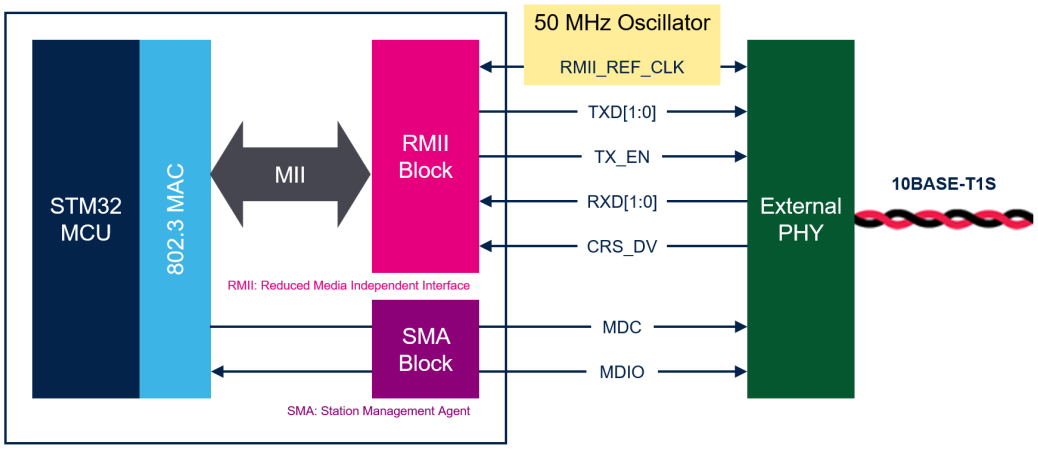
Figure 4. 10BASE-T1S node based on STM32



3.1 How to interface STM32NUCLEO board to PHY

The STM32 NUCLEO-H563ZI board is based on the STM32H563ZI microcontroller, which comes with an 802.3 Ethernet MAC that can be connected to a 10BASE-T1S PHY through the MII (Media Independent Interface) or RMII (Reduced Media Independent Interface). In this example, we address the RMII connection as reported in Figure 5. RMII-SMA block diagram.

Figure 5. RMII-SMA block diagram



A 50 MHz stable and accurate oscillator (RMII_REF_CLK) must be provided for both MAC and PHY as reference clock, to ensure correct operation.

On the NUCLEO-H563ZI, the MCU RMII is wired with the on-board Ethernet transceiver PHY. To use the RMII with an external PHY, the on-board one must be disconnected by acting on specific solder bridges. This makes the RMII path routed only between the MCU and the Morpho connectors. Please note that the NUCLEO-H563ZI board, as well as all STM32 Nucleo-144 development boards in general, does not come with the Morpho connectors (CN11 and CN12) soldered. Therefore, two 0.100” pitch and 70 position (35 x2) PCB header strips (e.g., Samtec TSW-135-07-F-D or equivalent) must be soldered as CN11 and CN12 of NUCLEO-H563ZI to allow RMII Adapter Board to be plugged on top of it.

The fixes to be made are shown in the table below.

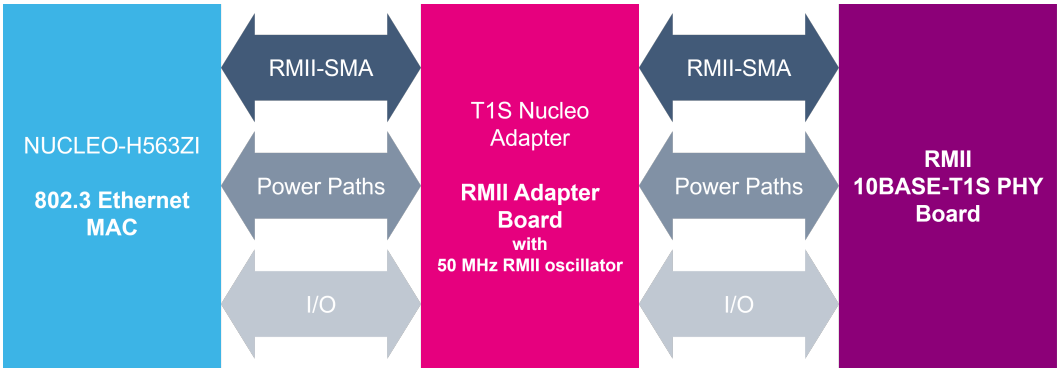
Table 1. NUCLEO-H563ZI Fixes

Pin	Signal	SB/JP to remove/open
PA1	RMII_REF_CLK	SB58
PG13	RMII_TXD0	SB37
PB15	RMII_TXD1	JP6
PG11	RMII_TX_EN	SB34
PC4	RMII_RXD0	SB42
PC5	RMII_RXD1	SB36
PA7	RMII_CRS_DV	SB38
PC1	RMII_MDC	SB62
PA2	RMII_MDIO	SB69

After that, the STM32 Nucleo board can be interfaced to an RMII 10BASE-T1S PHY using the signals reported in Figure 5. RMII-SMA block diagram, and Table 1 by following the scheme as in Figure 6.

This can be done by connecting the T1S Nucleo Adapter board on top of the NUCLEO-H563ZI, but the user can design and evaluate his own adapter.

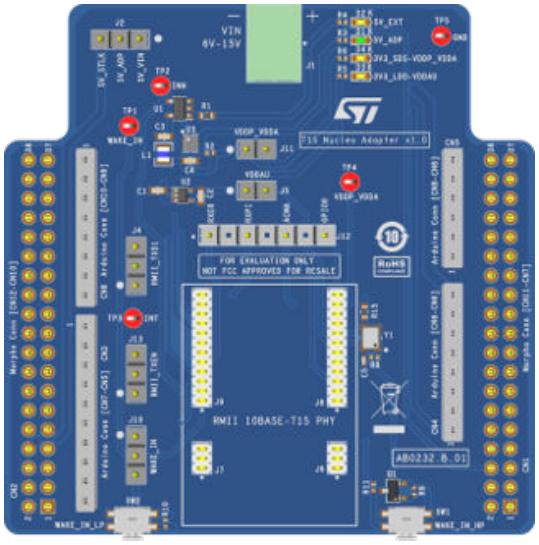
Figure 6. **Hardware block diagram**



3.2 T1S Nucleo Adapter board

The T1S Nucleo Adapter board (see Figure 7) is an example of the RMII adapter board, hosting the required components, and has a suitable form factor to be plugged on the NUCLEO-H563ZI board and interface with the 10BASE-T1S PHY.

Figure 7. **T1S Nucleo Adapter board**



The hardware is also compatible with NUCLEO-H723ZG and NUCLEO-H755ZI-Q, in addition to NUCLEO-H563ZI.

Note: The hardware reference shown in this application note is an example implementation proposed to support the accompanying X-CUBE-T1S firmware package. It is not an officially released board and is not optimized for industrial or production deployment.

The reference schematic is provided in Section 5.

4 Firmware package example

The hardware described in Section 3: Reference hardware design, can be used as an example to run the X-CUBE-T1S firmware package. The package provides a comprehensive set of 10BASE-T1S examples based on TCP/IP (transmission control protocol / internet protocol), such as UDP (user datagram protocol) client-server echo messaging and data exchange. The examples support both point-to-point and multidrop topologies with PLCA enabled. The package is developed to run on an STM32H5 Nucleo board, which acts as the media access control (MAC), and is connected to an RMII 10BASE-T1S PHY board, which acts as the physical layer (PHY). For more information, see the X-CUBE-T1S page.

5 Schematic diagrams

Figure 8. **T1S Nucleo Adapter Board (1 of 4)**

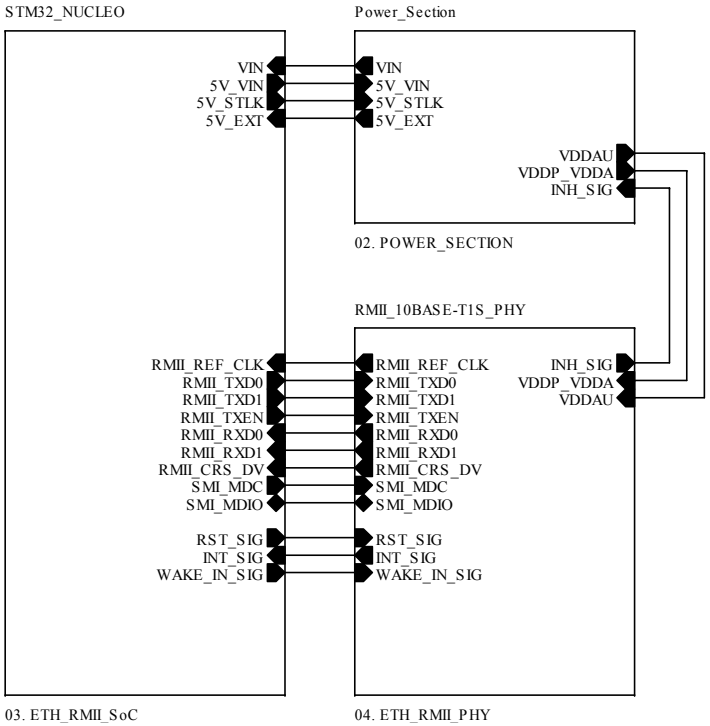


Figure 9. T1S Nucleo Adapter Board (2 of 4)

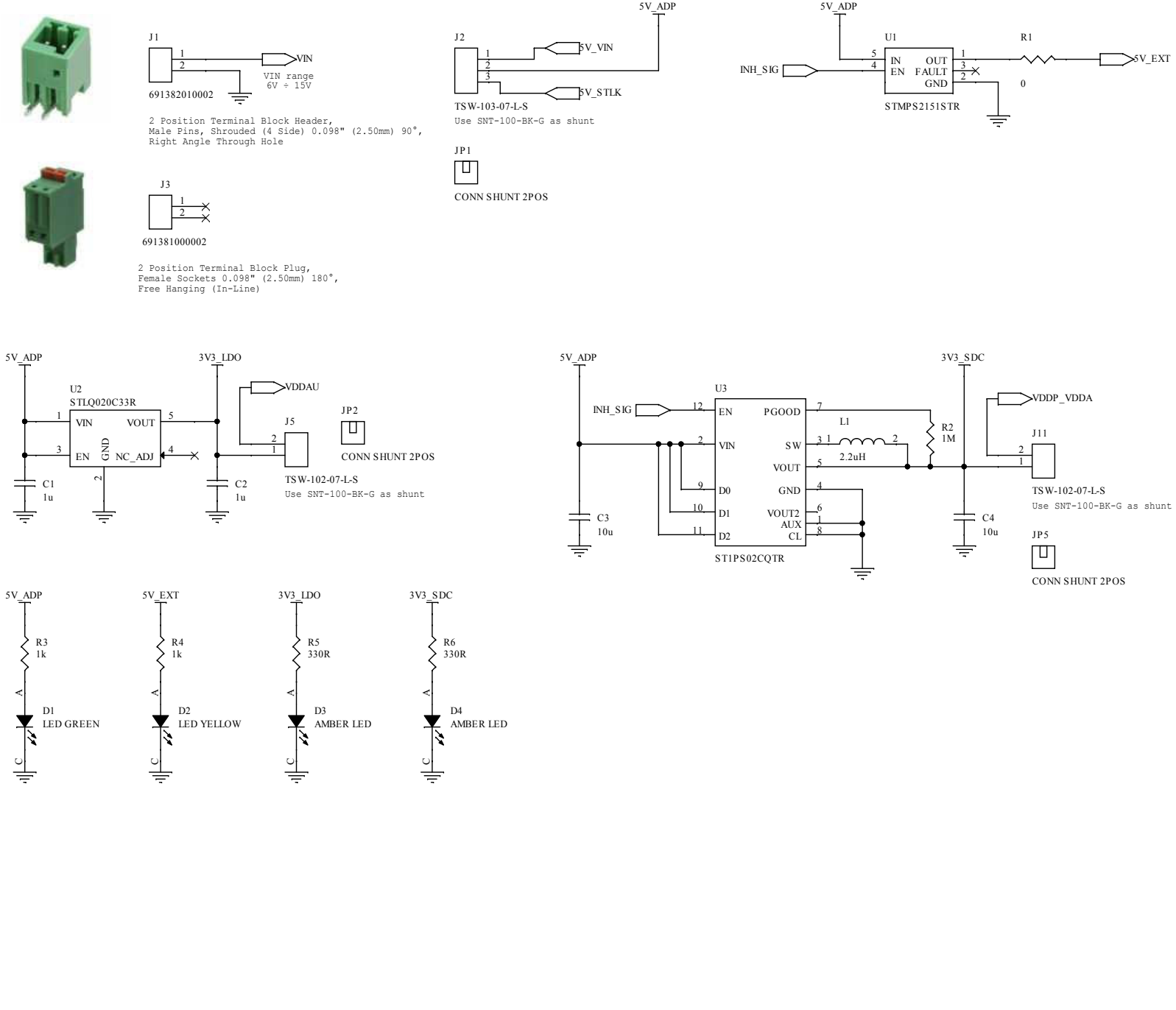


Figure 10. T1S Nucleo Adapter Board (3 of 4)

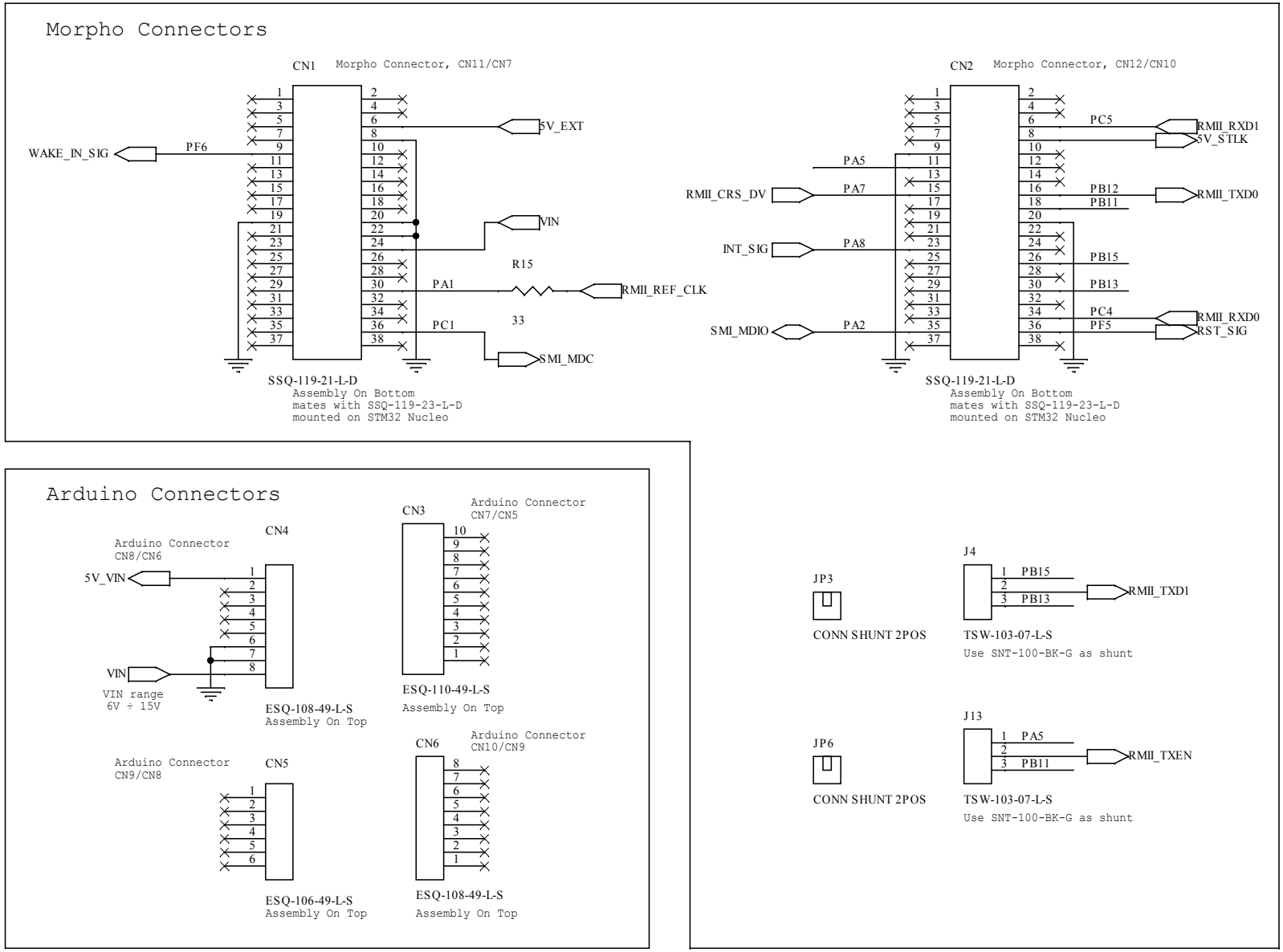
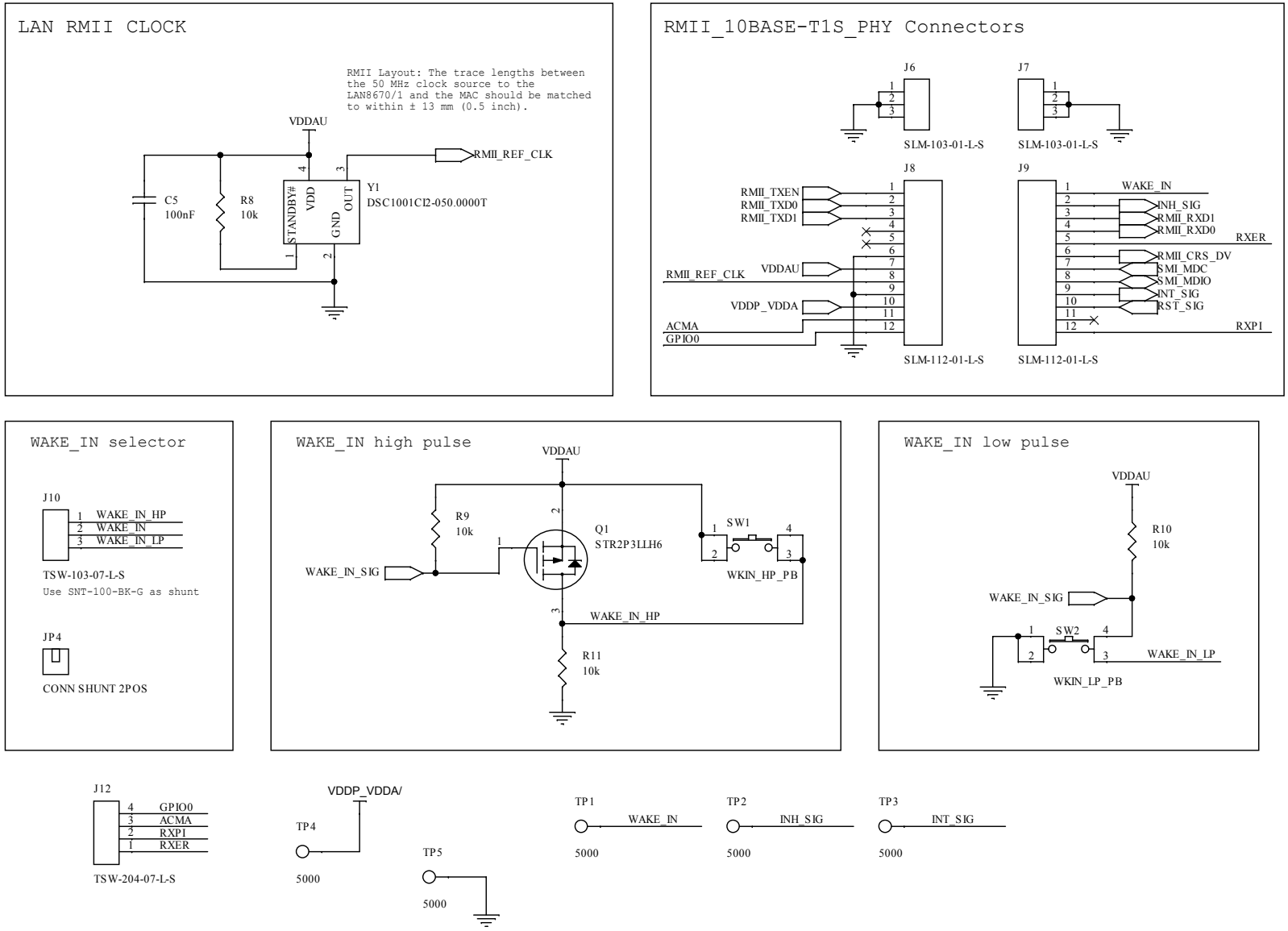


Figure 11. T1S Nucleo Adapter Board (4 of 4)



6 Bill of materials

Table 2. **T1S Nucleo Adapter Board Bill of Material**

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order Code
1	2	C1, C2	1u	CAP CER 1UF 50V X7R 0603	Wurth Electronics Inc.	885012206126
2	2	C3, C4	10u	CAP CER 10UF 25V X5R 0603	Wurth Electronics Inc.	885012106031
3	1	C5	100nF	CAP CER 0.1UF 50V X7R 0402	Wurth Electronics Inc.	885012205092
4	2	CN1, CN2	SSQ-119-21-L-D	CONN RCPT 38POS 0.1 TIN PCB	Samtec Inc.	SSQ-119-21-L-D
5	1	CN3	ESQ-110-49-L-S	CONN SOCKET 10POS 0.1 TIN PCB	Samtec Inc.	ESQ-110-49-L-S
6	2	CN4 CN6	ESQ-108-49-L-S	CONN SOCKET 8POS 0.1 TIN PCB	Samtec Inc.	ESQ-108-49-L-S
7	1	CN5	ESQ-106-49-L-S	CONN SOCKET 6POS 0.1 TIN PCB	Samtec Inc.	ESQ-106-49-L-S
8	1	D1	LED GREEN	LED GREEN CLEAR 0603 SMD	Wurth Electronics Inc.	150060VS75000
9	1	D2	LED YELLOW	LED YELLOW CLEAR 0603 SMD	Wurth Electronics Inc.	150060YS75000
10	2	D3, D4	AMBER LED	LED AMBER CLEAR 0603 SMD	Wurth Electronics Inc.	150060AS75000
11	1	J1	691382010002	TERM BLOCK HDR 2POS 2.50MM	Wurth Electronics Inc.	691382010002
12	4	J2, J4, J10, J13	TSW-103-07-L-S	CONN HEADER VERT 3POS 2.54MM	Samtec Inc.	TSW-103-07-L-S
13	1	J3	691381000002	TERM BLOCK PLUG 2POS 2.50MM	Wurth Electronics Inc.	691381000002
14	2	J5, J11	TSW-102-07-L-S	CONN HEADER VERT 2POS 2.54MM	Samtec Inc.	TSW-102-07-L-S
15	2	J6, J7	SLM-103-01-L-S	.050 MICRO STRIPS	Samtec Inc.	SLM-103-01-L-S
16	2	J8, J9	SLM-112-01-L-S	CONN RCPT 12POS 0.05 GOLD PCB	Samtec Inc.	SLM-112-01-L-S

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order Code
17	1	J12	TSW-204-07-L-S	SAMTEC - TSW-204-07-T-S - Pin Header, Vertical, Board-to-Board, 5.08 mm, 1 Rows, 4 Contacts, Through Hole, TSW	Samtec Inc.	TSW-204-07-L-S
18	6	JP1, JP2, JP3, JP4, JP5, JP6	CONN SHUNT 2POS	CONN JUMPER SHORTING 2.54MM GOLD	Samtec Inc.	SNT-100-BK-G
19	1	L1	2.2uH	FIXED IND 2.2UH 1.1A 270 MOHM	Wurth Electronics Inc.	74438343022
20	1	Q1	STR2P3LLH6	MOSFET P-CH 30V 2A SOT-23	ST	STR2P3LLH6
21	1	R1	0	CHIP RESISTOR SMD 1% 1/10W 0603	Any Manufacturer	/
22	1	R2	1M	CHIP RESISTOR SMD 5% 1/16W 0402	Any Manufacturer	/
23	2	R3, R4	1k	CHIP RESISTOR SMD 5% 1/16W 0402	Any Manufacturer	/
24	2	R5, R6	330R	CHIP RESISTOR SMD 5% 1/16W 0402	Any Manufacturer	/
25	1	R8	10k	RES 10K OHM 1% 1/16W 0402	Vishay Dale	CRCW040210K0FKED
26	3	R9, R10, R11	10k	CHIP RESISTOR SMD 5% 1/16W 0402	Any Manufacturer	/
27	1	R15	33	CHIP RESISTOR SMD 1% 1/10W 0603	Any Manufacturer	/
28	1	SW1	WKIN_HP_PB	SWITCH TACTILE SPST-NO 0.05A 12V Actuator Color Black	Wurth Electronics Inc.	434331045822
29	1	SW2	WKIN_LP_PB	SWITCH TACTILE SPST-NO 0.05A 12V	Wurth Electronics Inc.	434351045816
30	5	TP1, TP2, TP3, TP4, TP5	5000	TEST POINT PC MINI .040"D RED	Keystone Electronics	5000
31	1	U1	STMPS2151STR	IC PWR SWITCH 1CH 500MA SOT23-5	ST	STMPS2151STR

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order Code
32	1	U2	STLQ020C33R	IC REG LIN 3.3V 200MA SOT323-5	ST	STLQ020C33R
33	1	U3	ST1PS02CQTR	400MA NANO-QUIESCENT SYNC VOUT 2.6-3.3V	ST	ST1PS02CQTR
34	1	Y1	DSC1001CI2-050.0000T	MEMS OSC XO 50.0000MHZ CMOS SMD	Microchip Technology	DSC1001CI2-050.0000T

Revision history

Table 3. **Document revision history**

Date	Revision	Changes
05-Aug-2026	1	Initial release.

Contents