AN6561

Application note

SiC gen.3 performance evaluation on bidirectional three-phase, three-level PFC Vienna T-type converter

Introduction

This application note provides a complete analysis of the power losses of STMicroelectronics gen.3 SiC MOSFETs in a high-power bidirectional Vienna power factor correction (PFC) converter. The analysis is based on a 15 kW three-phase active front end (AFE) converter application that supports PFC and inverter modes. The application uses a three-phase, three-level T-type topology for direct current (DC) fast-charging stations [1] to [3]. However, this topology is not limited to industrial DC fast-charging station applications. It is versatile and can be used in renewable energy systems (RES), electric vehicles (EVs), energy storage systems (ESS), and other applications.

The *STM32G474RET3* microcontroller is an affordable, high-performance Arm 32-bit Cortex®-M0+ CPU that operates at up to 48 MHz. It provides full control of the power factor (PF), DC voltage, and load-to-grid (L2G) ancillary services. It also manages grid connection, soft startup, and grid-to-load (G2L) charging. The converter operates in high-bandwidth continuous conduction mode (CCM). This mode allows maximum power quality in terms of total harmonic distortion (THD) and PF of the Vienna PFC converter, especially in high-power applications [2].

Silicon carbide (SiC) MOSFET technology offers several benefits. It provides low current ripple and low electromagnetic interference (EMI). It also reduces conduction and switching losses.

This technology is effective in a three-phase, three-level T-type converter. The switching frequency is 70 kHz. This configuration can reach an efficiency of nearly 99%. High-frequency operation of the T-type converter helps optimize the size and cost of passive power components [4] to [5].

1 Overview of the DC charging station

DC charging stations are a cornerstone of modern electric vehicle (EV) infrastructure. They deliver high-speed charging by supplying direct current (DC) power directly to an EV battery. Unlike alternating current (AC) chargers, which rely on the vehicle onboard charger (OBC) to process power, DC chargers perform AC-to-DC conversion within the charging station, as shown in Figure 1. It shows the block diagram of the power conversion stages and the digital control unit that the microcontroller unit (MCU) performs.

This design bypasses the limitations of the OBC and provides significantly faster charging. It is ideal for EVs with larger battery capacities and for scenarios in which time is critical. Power output typically categorize DC charging stations from standard fast chargers at 50 kW to ultrafast chargers at 350 kW or more. These chargers can replenish hundreds of kilometers of range in minutes.

Figure 1. DC charging station [2]

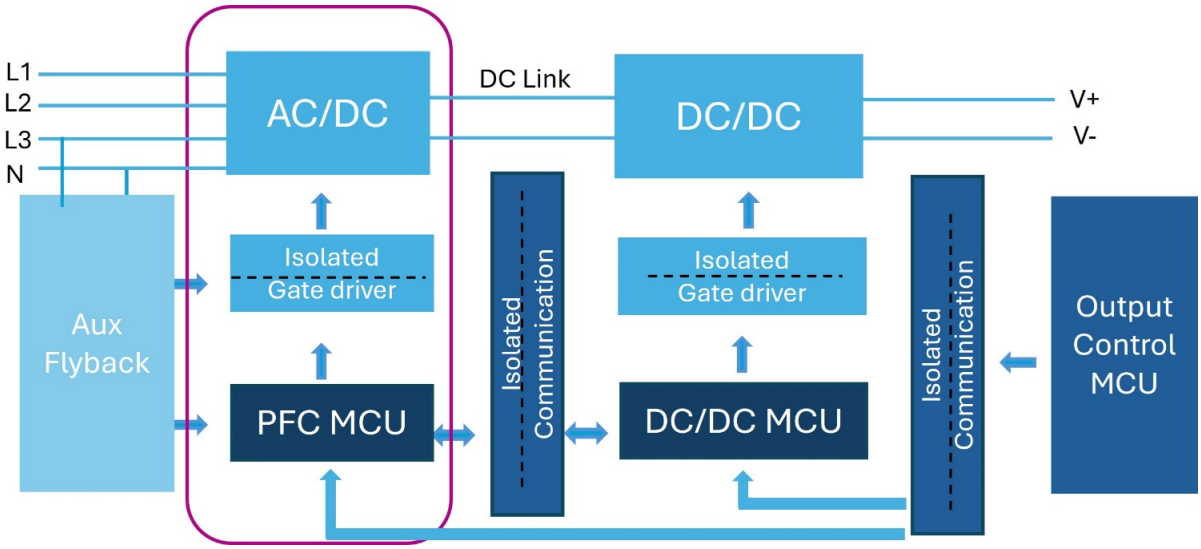


Table 1. Classification of charging station

Power level	Type	Voltage supply	Power rate	Charging time (from 20% to 80%)
Level 1 (USA only)	Onboard	120 V 1-Ph AC	1.4 to 1.9 kW	4-11 hours
Level 2 (EU and USA)	Onboard	208 or 240 V (1-Ph AC) 400 V (3-Ph AC)	4-44 kW	1-4 hours
Level 3 (DC Fast charging)	Off-board DC charger	400 or 800 V (DC supply)	50-240 kW	30 minutes

Table 1 provides brief details of the charging station used for EV battery charging. It includes classification of different power levels, types of chargers, charging times, and other relevant information.

2 STMicroelectronics DC charging station solution

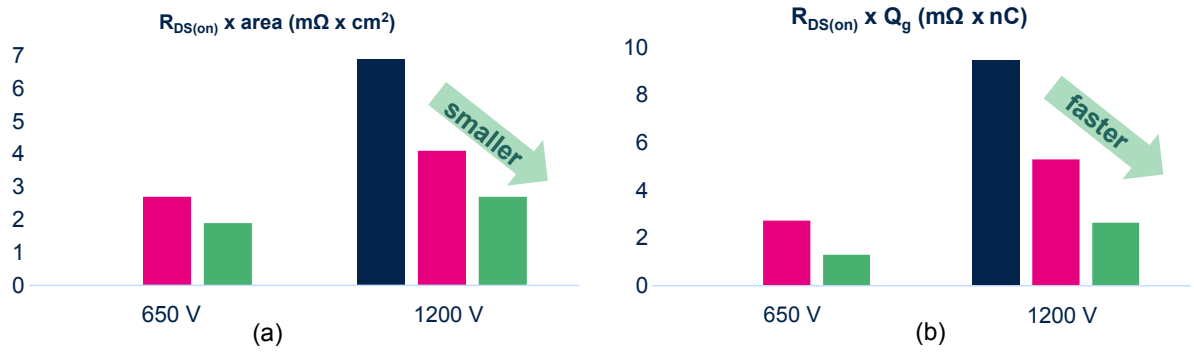
STMicroelectronics plays a key role in the electric vehicle (EV) charging market by delivering smart semiconductor solutions that make charging systems faster and more reliable. Its SiC MOSFETs and diodes help create compact power converters with high efficiency and low energy loss. These devices also support higher switching frequencies and better thermal performance, which are important for fast DC chargers.

In addition, STMicroelectronics enables intelligent energy management (IEM) through microcontrollers and digital signal processors (DSPs). These technologies allow better power control, smooth communication with EVs, and easier integration of renewable energy sources such as solar and wind. As a result, charging stations can deliver rapid and dependable charging while supporting sustainability goals. As the EV market grows quickly, STMicroelectronics continues to help build a strong and scalable charging infrastructure for the future of electric mobility.

STMicroelectronics introduced its gen.1 SiC devices based on wide-bandgap (WBG) materials, opening the way to a new generation of power technology. Through continuous optimization, this technology evolved into later SiC families, including STPOWER gen.3, which ST launched in 2023. The second-generation planar technology reached high-volume production and helped ST build market leadership. With further innovation, the gen.3 SiC Power MOSFET achieved a lower specific on-resistance, smaller cell size, and improved performance.

ST optimized both the horizontal layout and the vertical structure to deliver higher efficiency without making the devices harder to use. As a result, gen.3 offers very low switching losses and helps designers meet certification targets more easily. This technology makes it possible to build smaller, lighter, and more efficient switching systems.

Figure 2. Technological enhancement from gen.1 to gen.3: (a) $R_{DS(on)}$ * area, (b) $R_{DS(on)}$ x Q_g



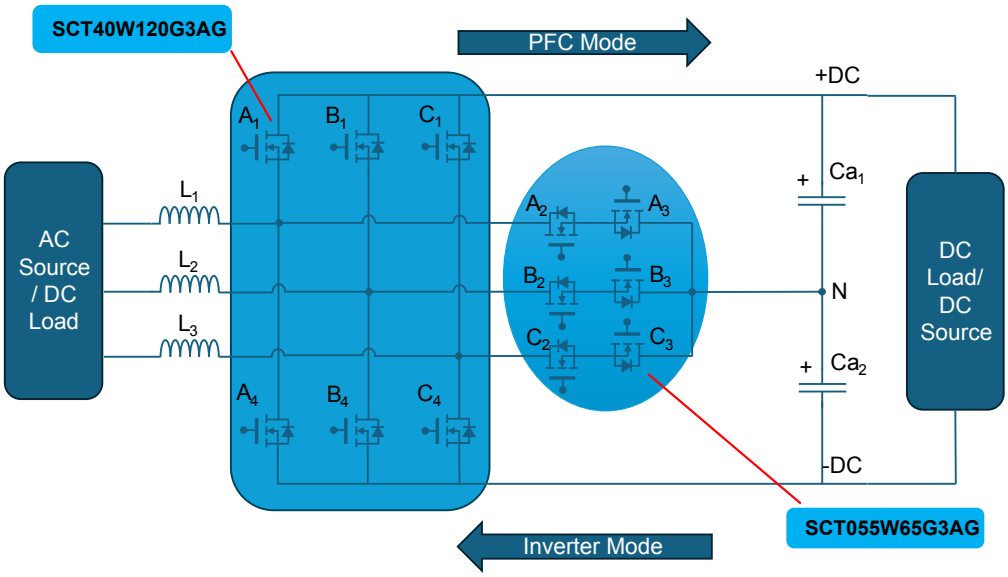
The automotive and industrial semiconductor market is moving toward lower $R_{DS(on)}$ × area, faster switching, and package options that support higher power density. STMicroelectronics addresses these needs through its gen.1 to gen.3 SiC MOSFET evolution, as shown in Figure 2 (a), by reducing die size while meeting the target $R_{DS(on)}$. This evolution allowed much lower $R_{DS(on)}$ values in the same package. It achieved a nearly 72% reduction in $R_{DS(on)}$ multiplied by area in the 1200 V class. For example, in the TO-247 package, $R_{DS(on)}$ improved from 50 mΩ in gen.1 to 14 mΩ in gen.3. In addition, the figure of merit (FOM), $R_{DS(on)}$ × Q_g, which reflects switching capability, also improved significantly. This improvement enables faster switching and lower switching losses from gen.1 to gen.3, as shown in Figure 2 (b) [5].

Figure 3. Technological enhancement from gen.1 to gen.3 for power density of the same package

3 Three-phase, three-level T-type high performance converter general concepts

Figure 4 illustrates the core topology of the three-phase, three-level T-type converter. The conventional two-level converter topology is upgraded by incorporating an active anti-series common-source configuration between the midpoint of the DC link and the grid.

Figure 4. Schematic of three-phase, three-level T-type converter



In this application, the DC bus voltage is fixed at 800 V. This requirement means that the SiC MOSFETs in the vertical legs must have a 1200 V blocking capability. They handle the constant DC bus voltage. They also sustain the voltage spikes that switching effects cause.

Additionally, the switches in the horizontal legs are configured in an antiseries common-source arrangement. This configuration reduces the voltage stress on the switches because they must block only half of the DC bus voltage. Consequently, 650 V SiC MOSFETs can be selected for each horizontal leg [6].

3.1 Current flow in single leg of T-type converter

This application note analyzes only the devices in the first vertical leg. These devices are A1 and A4. It also looks at the first horizontal leg, which includes A2 and A3. The same concepts apply to the other two legs. The T-type configuration provides three DC potential points: +DC, -DC, and N (neutral). The converter operating mode and MOSFET switching determine the current flow, as shown in Figure 5*(a), (b), (c)*. Figure 5*(a), (b), (c)* explain the reverse-mode current flow, that is, line to grid (L2G). To establish the connection from +DC to neutral and from neutral to +DC, switch A1 and A2 sequentially in a complementary manner. A1 is the control switch, also called the main switch. When A1 is on, the +DC point is connected to the AC grid, and current flows in the first quadrant of A1 (Figure 5*(a)*). During the transition from +DC to N, A1 opens, and A2 has a turn-on delay (Figure 5*(b)*). During this delay, the antiparallel diode of A2 conducts before the channel conducts in the third quadrant (Figure 5*(c)*). This conduction allows the recirculating current to flow from N to the AC grid. Before A1 switches on again, the channel of A2 switches off to avoid cross-conduction and starts to conduct through its body diode (Figure 5*(b)*). Then, A1 switches on, and the antiparallel diode of A2 blocks the voltage (Figure 5*(a)*).

Figure 5. Current flow

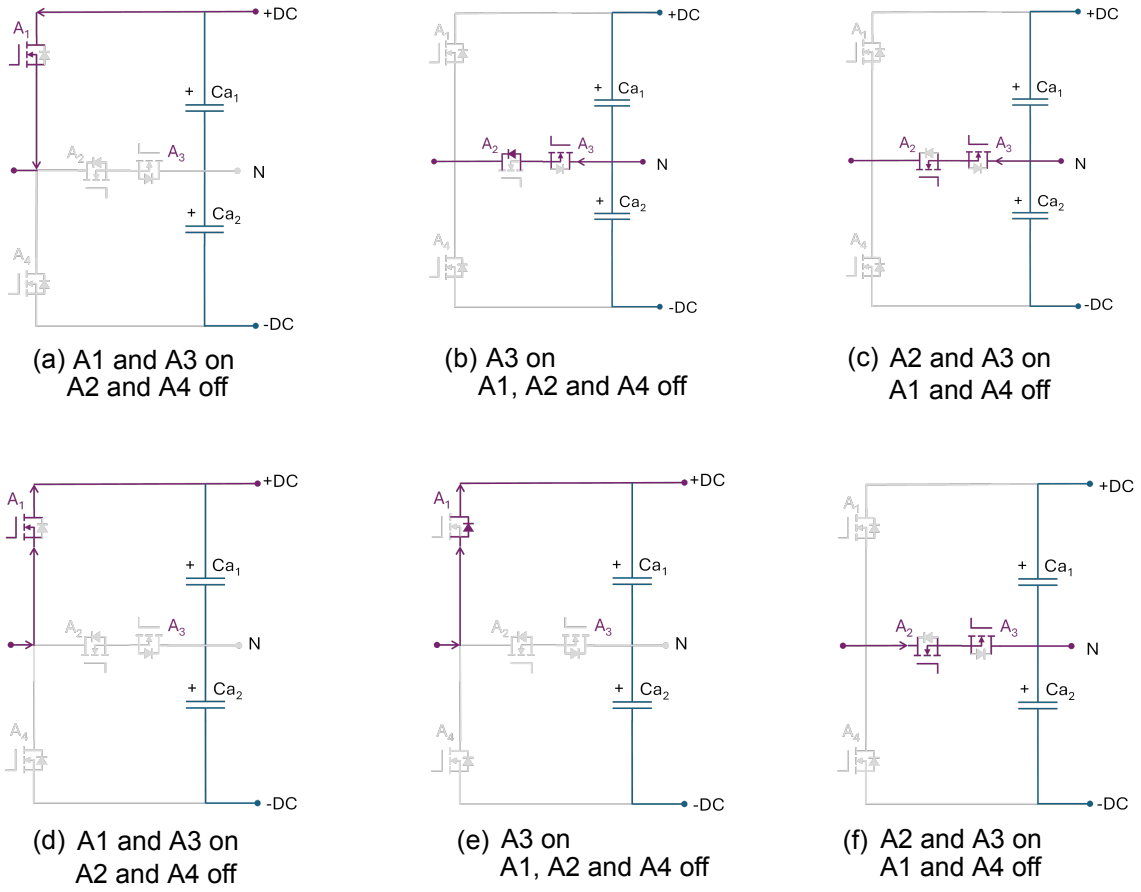


Figure 5*(d)* to Figure 5*(f)* explain the current flow in forward mode, that is, G2L. In this case, A2 is the main control switch. When A1 is on, the +DC point connects to the AC grid, and current flows in the third quadrant, as Figure 5*(d)* shows. Before A2 switches on, the A1 channel switches off to avoid cross conduction and then conducts through the body diode, as Figure 5*(e)* shows. During the transition from +DC to N, A2 closes, and the antiparallel diode of A1 is reverse biased, as Figure 5*(f)* shows. Then A2 switches off, and the antiparallel diode of A1 starts to conduct during the turn-on delay of A1, as Figure 5*(e)* shows. After the turn-on delay, the A1 channel closes and conducts in the third quadrant, as Figure 5*(d)* shows. During both operating modes, A3 remains on to maintain current flow because the parasitic diode is reverse biased [3]. Figure 5 shows the transition states from +DC to N and from N to +DC in power factor correction (PFC) mode and inverter mode. In the positive half-cycle, A1 and A2 are the control switches, while A3 remains on. The same approach applies to the negative half-cycle with the -DC node through A4 and A3 as the control switches, while A2 remains on in PFC mode and inverter mode.

4 STDES-PFCBIDIR board and specification

Figure 6 shows the sections of the STDES-PFCBIDIR power board for converter operation. The board regulates bidirectional power by using ST gen.3 SiC MOSFETs in the HiP247 package. The board can support output power of up to 15 kW. It features a 3-phase, 3-level active front end (AFE) in a T-type configuration for industrial applications and EV DC fast chargers.

The devices under test (DUTs) use two configurations:

1. *SCT040W120G3AG* for the vertical leg
2. *SCT040W65G3AG* for the horizontal leg.

Figure 6. *STDES-PFCBIDIR* board

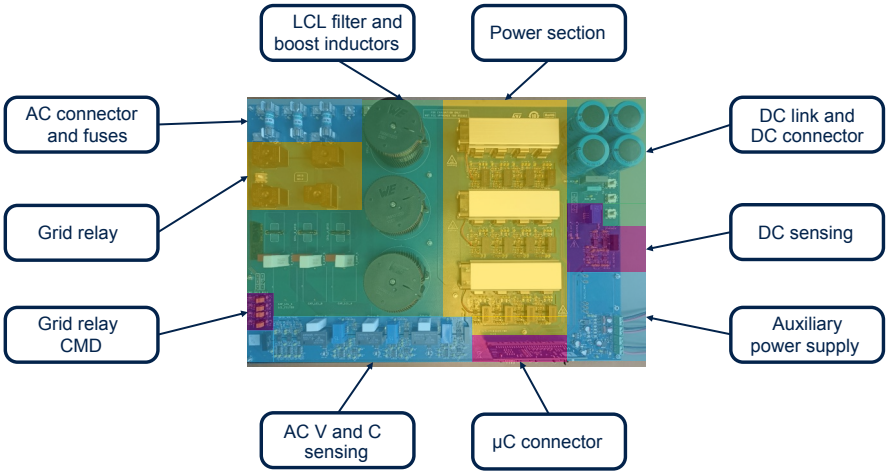


Figure 7. (a) PFC mode setup and (b) Inverter mode setup

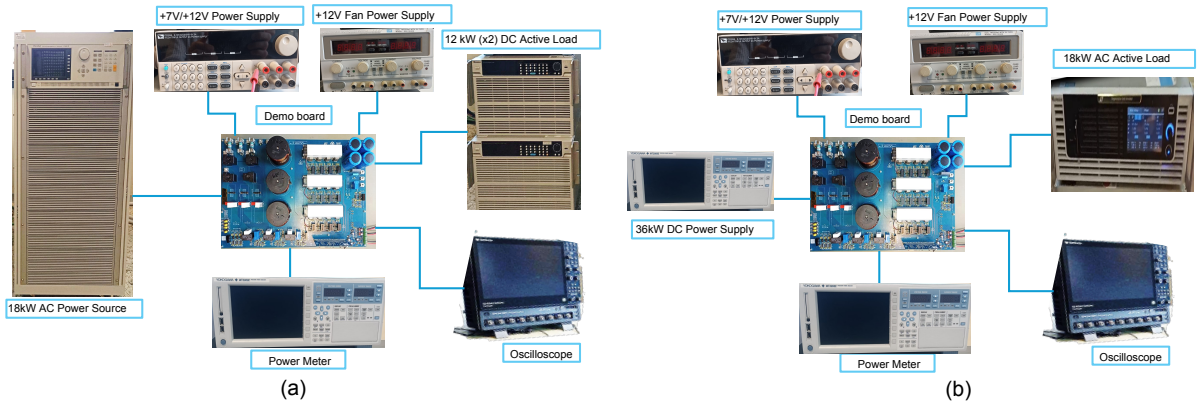


Figure 7 show the converter test setup in power factor correction (PFC) mode and inverter mode, respectively. During PFC mode testing of the STDES-PFCBIDIR board, the Chroma 61612 AC power supply provides input power. The *YOKOGAWA WT300E* power meter measures input power, output power, and overall system efficiency. The GW Instek GPE-2323 supplies 12 V to the DC-DC driver circuit and 7 V to the *STM32G474RET3* microcontroller. The GW GPC-3030P supplies power to the fan that cools the MOSFETs. The *Teledyne LeCroy WaveRunner 8058* oscilloscope captures all current and voltage waveforms. Two *Chroma 63212A-1200-480* DC active loads, rated at 12 kW each, are connected in parallel to reach the maximum load of 15 kW [2].

The inverter mode test setup is similar to the PFC mode setup, with some modifications. Additional equipment includes the *Itech IT6036C-1500-40* 36 kW DC power supply for the system input power and the *Chroma 61815* 18 kW AC active load. Equipment removed from the PFC mode setup includes the *Chroma 61612* AC power supply and the two *Chroma 63212A-1200-480* DC active loads. Table 2 lists the specifications of the T-type converter in PFC mode and inverter mode.

Table 2. Specification

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Three-phase input voltage	V_{AC}	208	-	400	V	-
AC line frequency	Hz	47	-	63	Hz	-
Maximum output power	P_{OUTmax}	-	15	-	kW	I_{AC_RMS} = 18.76 A
Output voltage	V_{DC}	-	800	-	V	-
Power factor	PF	-	>0.99	-	-	From 20% of load
Total harmonic distortion	THD	-	< 5	-	%	From 20% of load
Switching frequency	f_{SW}	-	70	-	kHz	-
Boost inductor	L	-	470	-	µH	-
Max. ripple current	$\Delta_{I_{Lppmax}}$	-	10	-	%	-
Gate source voltage	V_{GS}	-	+18/-5	-	V	-

4.1 SiC MOSFETs selection

The selection of SiC MOSFETs depends on several factors, such as voltage, current, and switching speed. However, the topology plays an important role in the blocking capability of SiC MOSFETs. Figure 4 shows the schematic of the T-type converter. The T-type converter topology allows the selection of two SiC MOSFETs with different blocking capabilities for the DC bus in the vertical and horizontal legs, as explained in Section 3.

In addition to voltage, the choice of the SiC MOSFET depends on other factors listed in Table 3 for STMicroelectronics Power MOSFET. These factors include switching characteristics, power rating, and other specifications that suit this application. Switching losses depend on voltage, current amplitude, and switching frequency. These parameters are critical for determining the slew rate. Figure 8 show the switching energies, E_{ON} and E_{OFF}, of SiC MOSFETs in both leg configurations at different ID currents. Conduction losses depend on $R_{DS(on)}$. According to Table 3, for SiC MOSFETs rated at 1200 V and 650 V, the $R_{DS(on)}$ values at the nominal junction temperature are 40 mΩ (16 A), and 45 mΩ (20 A), respectively. However, at a junction temperature of 200 °C, the $R_{DS(on)}$ values increase to 77 mΩ (16 A), and 69 mΩ (20 A), respectively. Therefore, the variations in $R_{DS(on)}$ with temperature are not excessively high.

Table 3. Specification of SIC MOSFETs

Parameters	*SCT40W120G3AG* (Vertical leg)	*SCT040W65G3AG* (Horizontal leg)
B_{Vdss} [V]	1200	650
I_{D_max} [A] at 25 °C	40	30
I_{D_max} [A] at 100 °C	40	30
$V_{GS(th)\_typ}$ [V]	3.1 (5 mA)	3 (1 mA)
$R_{DS(on)\_typ}$ [mΩ] at 25 °C, V_{GS} = 18 V	40 (16 A)	45 (20 A)
$R_{DS(on)\_typ}$ [mΩ] at 200 °C, V_{GS} = 18 V	77 (16 A)	69 (20 A)
V_{SD} [V]	2.6 (16 A)	2.9 (20 A)
R_{thJC} [°C/W]	0.56	0.73
Q_G	56 nC at V_{DD} = 800 V, I_D = 20 A, V_{GD} = -5 to 18 V	38.5 nC V_{DD} = 400 V, I_D= 20 A, V_{GD}= -5 to 18 V
Q_{GS}	17 nC at V_{DD} = 800 V, I_D= 20 A, V_{GD}= -5 to 18 V	10.8 nC V_{DD}= 400 V, I_D= 20 A, V_{GD}= -5 to 18 V
Q_{GD}	19 nC at V_{DD}= 800 V, I_D= 20 A, V_{GD}= -5 to 18 V	13.7 nC V_{DD}= 400 V, I_D= 20 A, V_{GD}= -5 to 18 V
C_{iss}	1329 pF at V_{DD}= 800 V, f = 1 MHZ, V_{GD}= -5 to 18 V	897 pC V_{DD}= 400 V, f = 1 MHZ, V_{GD}= -5 to 18 V
C_{oss}	78 pF at V_{DD} = 800 V, f = 1 MHZ, V_{GD}= -5 to 18 V	84 V_{DD}= 400 V, f = 1 MHZ, V_{GD}= -5 to 18 V
C_{rss}	10 pF at V_{DD} = 800 V, f = 1 MHZ, V_{GD}= -5 to 18 V	12 pC V_{DD}= 400 V, f = 1 MHZ, V_{GD}= -5 to 18 V
Q_{rr}	91 nC at I_{SD} = 16 A, di/dt = 1000 A/µs, V_{DD} = 800 V	91 nC at I_{SD} = 20 A, di/dt = 1000 A/µs, V_{DD} = 400 V

Related links

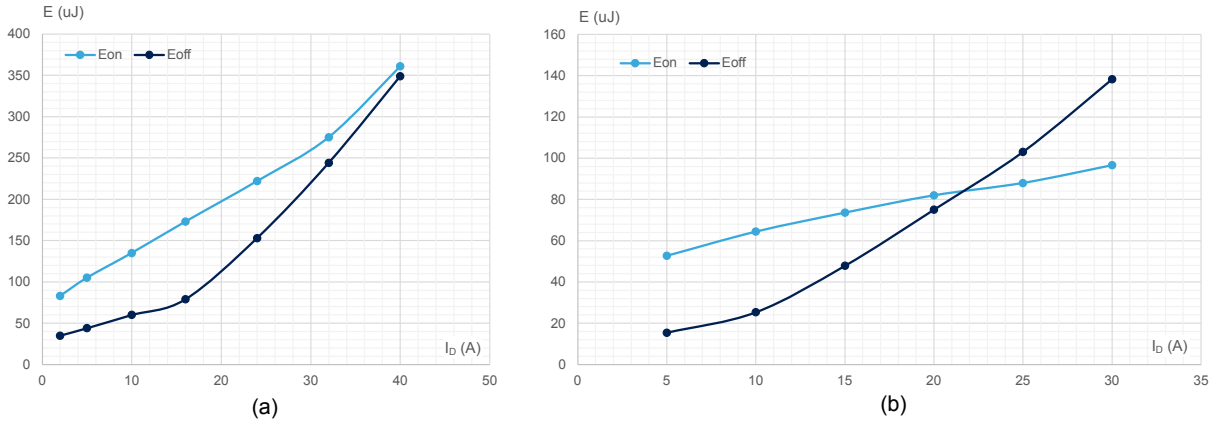
SCT040W120G3AG: Automotive-grade silicon carbide Power MOSFET 1200 V, 40 mΩ typ., 40 A in an HiP247 package

SCT040W65G3AG: Automotive-grade silicon carbide Power MOSFET 650 V, 45 mOhm typ., 30 A in an HiP247 package

4.2 Loss evaluation of SiC MOSFETs

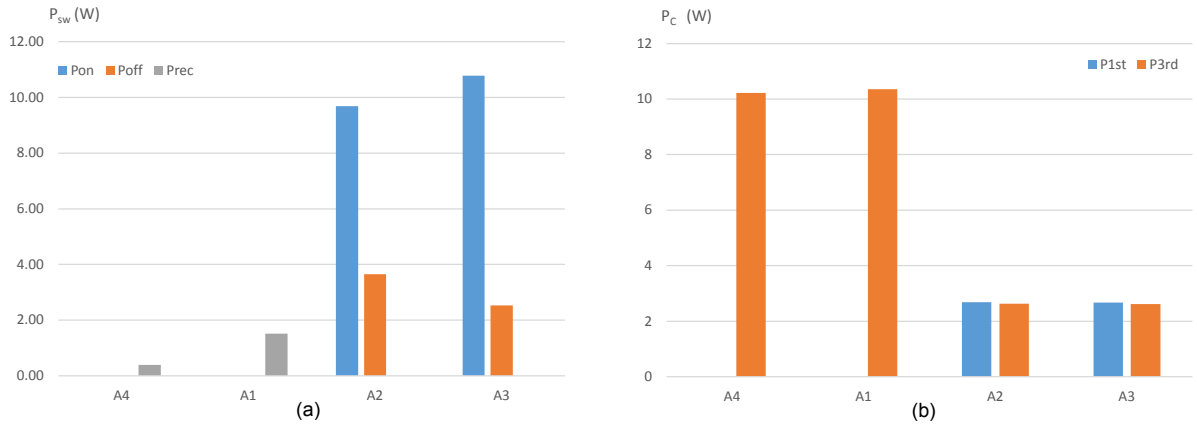
To estimate the loss in any application, several factors must be considered, such as power, load, topology, the performance of the switching devices, and other components used in topology. In this section, we address the SiC MOSFET loss profiles, which depend on the conduction and switching loss characteristics in the context of the T-type converter by using the STDES-PFCBIDIR board with the set of MOSFETs as mentioned in Section 4.

Figure 8. E_{ON} and E_{OFF} vs I_D *SCT040W120G3AG* (a), *SCT040W65G3AG* (b)



Switching losses evaluation by STDES-PFCBIDIR board are measured though the waveforms analysis and they are influenced by several factors, such as gate drive circuits, gate resistance, and free-wheeling diodes, which affect the switching energy under varying operating conditions.

Figure 9. PFC: (a), switching loss (b), conduction loss



According to Figure 4, the T-type converter is split into horizontal and vertical legs to complete the path for the flow of current from the G2L and vice versa. The operation mode of the converter also affects the losses that occur in the SiC MOSFETs. For example, when it operates in PFC mode (power flow in G2L), the vertical leg SiC MOSFET conduction starts with the diode in the 3rd quadrant. This causes soft switching at the turn-on of the device, while the horizontal SiC MOSFET, which is the complementary switch of the vertical SiC MOSFET, experiences hard switching. This results in low switching losses on the vertical leg and high switching losses in the horizontal leg. Conversely, when the T-type converter operates in inverter mode (power flow in L2G) the horizontal leg SiC MOSFET conduction starts with the diode in the 3rd quadrant. This causes soft switching at the turn-on of the device, while the vertical SiC MOSFET, which is the complementary switch of the horizontal SiC MOSFET, experiences hard switching. This results in low switching loss in the horizontal leg and high switching loss in the vertical leg.

Regarding conduction losses estimation, it is possible to use the SiC MOSFET datasheet. The initial specification of $R_{DS(on)}$ was mentioned in Section 4.1. However, the datasheet also provides information on the temperature dependency $R_{DS(on)}$ parameters, which increases with rising in die temperature. The STPOWER Studio is a valuable tool that helps identify the conduction losses in different topologies under various load conditions. It is an online electro-thermal simulation software tool dedicated to a growing number of STPOWER devices, providing comprehensive power and thermal analysis. With the help of STPOWER Studio we estimate the conduction loss for T-type converter in each mode of operation.

4.2.1 G2L operation

During the positive half wave in G2L operation, A2 is the control switch and A3 is always on, so A2 experiences both switching and conduction losses due to hard switching, whereas A3 incurs only conduction losses. When A1 starts conducting through its parasitic diode, it undergoes soft switching during turn-on.

Therefore, A1 has only parasitic diode recovery losses and conduction losses. A4 is off state for all the positive half cycle. The whole concepts regarding the positive half cycle can be applicated in the negative half cycle by swapping the operation of A1 with A4 and A2 with A3.

Based on the above discussion, mathematical models for estimating losses, including conduction, switching, and recovery of the body diode of the SiC MOSFETs, are provided below in equations (1-3) for G2L operation mode during the positive half wave [7].

$$P_{\text{Con\_Pfc}} = P_{\text{Con\_A1}} + P_{\text{Con\_A1\_d}} + P_{\text{Con\_A2}} + P_{\text{Con\_A3}} \quad (1)$$

$$\boldsymbol{P_{A_{1\_d\_rec\_Pfc}} = f_{sw} V_o Q_{rr\_A1}} \quad (2)$$

$$\boldsymbol{P_{Sw\_Pfc} = P_{Sw\_A_2}} \quad (3)$$

Where:

P_{Con_Pfc} : Total conduction loss in one switching state of MOSFETs in PFC Mode

$P_{Con\_A_1}$: Conduction loss of MOSFET A_1

$P_{Con\_A_{1\_d}}$: Conduction loss of MOSFET A_1 body diode

$P_{Con\_A_2}$: Conduction loss of MOSFET A_2

$P_{Con\_A_3}$: Conduction loss of MOSFET A_3

$P_{A_{1\_d\_rec\_Pfc}}$: MOSFET A_1 body diode recovery loss

f_{sw} : Switching frequency

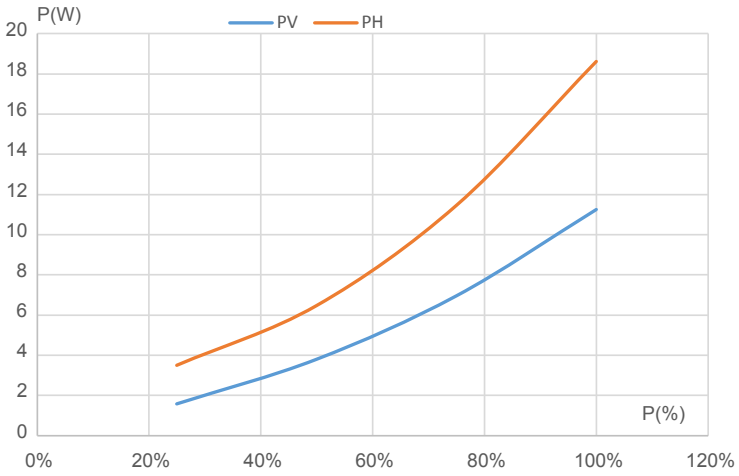
V_o : Output Voltage

Q_{rr_A1} : Recovery charge of A1 body diode

P_{Sw_Pfc} : Total switching loss in one switching state of MOSFETs in PFC Mode

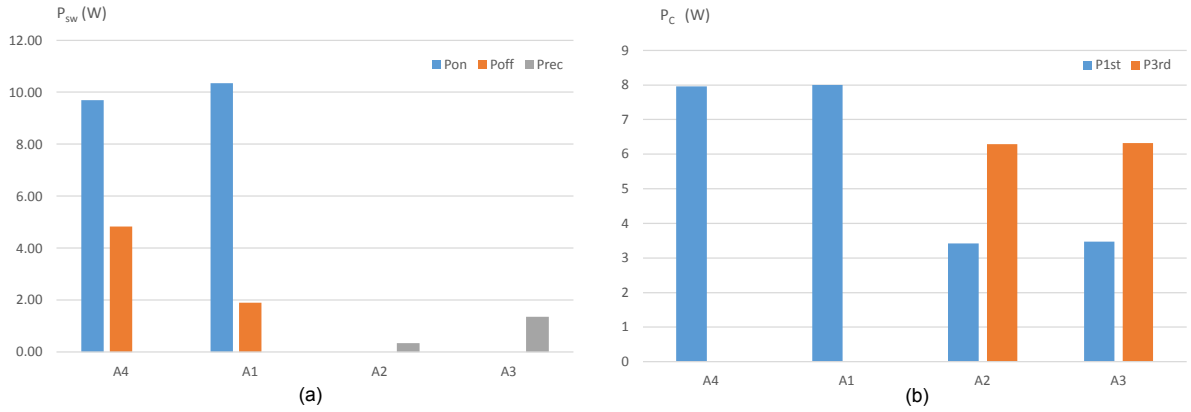
$P_{Sw\_A_2}$: Switching loss of MOSFET A_2

Figure 10. Power losses per device in PFC mode



Turn-on, turn-off, recovery of the body diode, and conduction losses of first and second configuration of each SiC MOSFETs in a single-leg operation are shown in Figure 8, respectively, at the 100% loading condition. The cumulative loss estimation for both vertical and horizontal MOSFET is shown in Figure 10 under different loading conditions.

Figure 11. Inverter: (a), switching loss (b), conduction loss



4.2.2 L2G operation

During the positive half wave in L2G operation, A1 acts as the control switch. A3 remains always on. A1 faces both switching losses and conduction losses due to hard switching. In contrast, A3 incurs only conduction loss. When A2 starts conducting through its parasitic diode, it undergoes soft switching during turn-on.

Therefore, A2 has only parasitic diode recovery losses and conduction losses. A4 is in an off-state for all the positive half cycle. You can replicate the whole concepts of the positive half cycle in the negative half cycle. Just swap the operations of A1 with A4, and A2 with A3.

Based on the discussion above, we provide mathematical models for estimating losses. These models include conduction, switching, and recovery of the body diode of the SiC MOSFETs. The equations for the L2G operation mode during the positive half wave are shown in Eq. (4), Eq. (5) and Eq. (6).

$$P_{\text{Con\_Inv}} = P_{\text{Con\_A1}} + P_{\text{Con\_A2\_d}} + P_{\text{Con\_A2}} + P_{\text{Con\_A3}} \quad (4)$$

$$\boldsymbol{P_{d\_A_2\_rec\_Inv} = f_{sw} V_o Q_{rr\_A2}} \quad (5)$$

$$\boldsymbol{P_{Sw\_Inv} = P_{Sw\_A_1}} \quad (6)$$

Where:

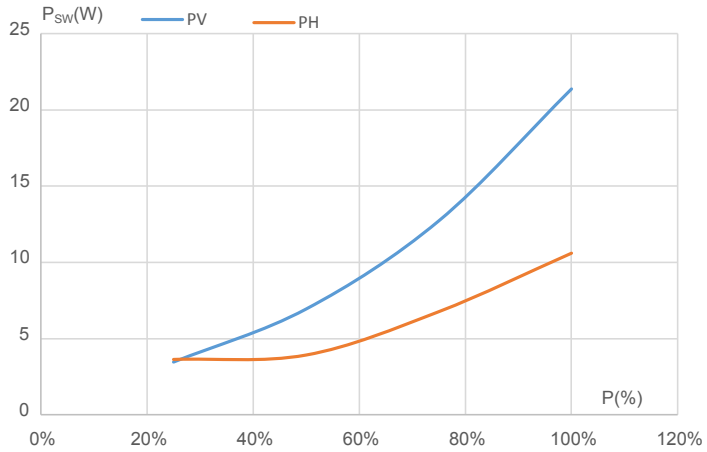
P_{Con_Inv} : Total conduction loss in one switching state of MOSFETs in inverter mode

$P_{Con\_A_{2\_d}}$: MOSFET A_2 body diode recovery loss

$Q_{rr\_A_2}$: Recovery charge of A2 body diode

Turn-on, turn-off, recovery of the body diode and conduction losses of each SiC MOSFETs in a single-leg operation are shown in Figure 11 (a) and (b), respectively, at the 100% loading condition. The cumulative loss estimation for both vertical and horizontal MOSFET is shown in Figure 12 under different loading conditions.

Figure 12. Power losses per device in inverter mode



The switching loss expressions for T_{ON} and T_{OFF} are provided in Eq. (7)) and Eq. (8). These expressions apply to both modes of operation of the T-type converter for estimating the switching loss.

$$P_{\mathrm{Sw}} = \frac{E_{\mathrm{sw}} f_{\mathrm{sw}}}{\pi} \tag{7}$$

$$\boldsymbol{E_{sw} = E_{on} + E_{off}} \tag{8}$$

Where:

P_{Sw} : Switching loss

E_{sw} : switching energy

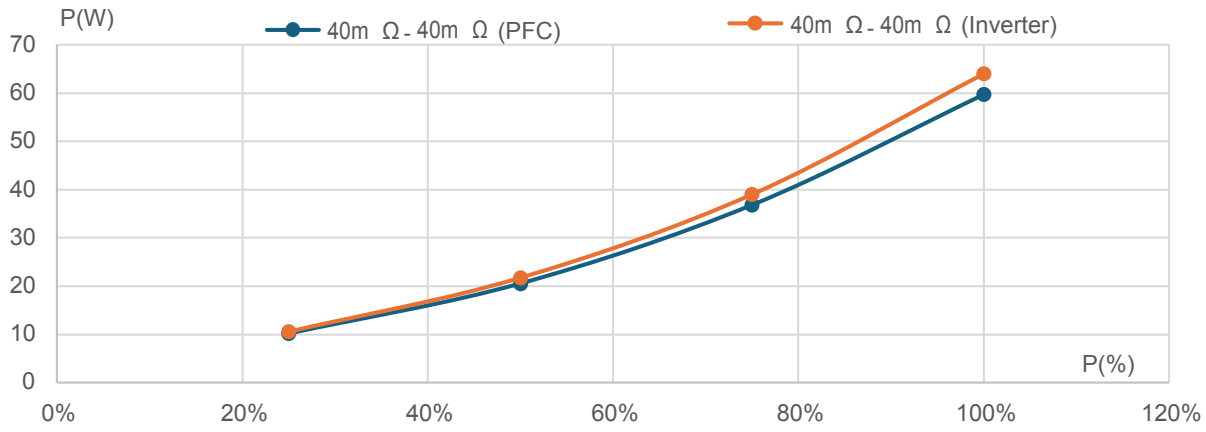
E_{on} : Turn on energy

E_{off} : Turn off energy

Table 4. Efficiency at 100% loading

Mode	Power (%)	Leg power losses (W)	Efficiency (%)
PFC	100%	59.72	97.97
Inverter	100%	63.93	97.51

Figure 13. Total power loss plot of single leg of 3ph-3L-T-type convertor in PFC and inverter mode



5 Result and discussion

Figure 13 illustrates the first-leg power loss of a 3-phase, 3-level T-type converter. It operates in power factor correction (PFC) and inverter modes. The loss varies under different load conditions in both configurations.

In the first configuration at 100% load, the losses are 64.82 W in PFC mode. In inverter mode, the losses are 59.72 W.

In the second configuration at 100% load, the losses are 58.86 W in PFC mode. In inverter mode, the losses are 63.93 W.

Table 4 shows the efficiency of the T-type converter in PFC and inverter modes at 100% load, and Figure 14 shows the efficiency curves.

In power factor correction (PFC) mode, the efficiencies configurations have a bell shape. The peak efficiencies is 98.31% (blue) at 50% load, and at 100% load, the efficiencies is 97.65% (blue).

In inverter mode, the efficiency decreases monotonically. The maximum efficiencies is 99.59% (orange) at 25% load. At 100% load, the efficiencies is 97.51% (orange). Further the total losses caused by all switches in one complete cycle at 100% of load condition are approximately 179 W and 192 W, respectively for PFC and inverter mode.

Figure 14. Efficiency plot for PFC and inverter mode of T-type converter

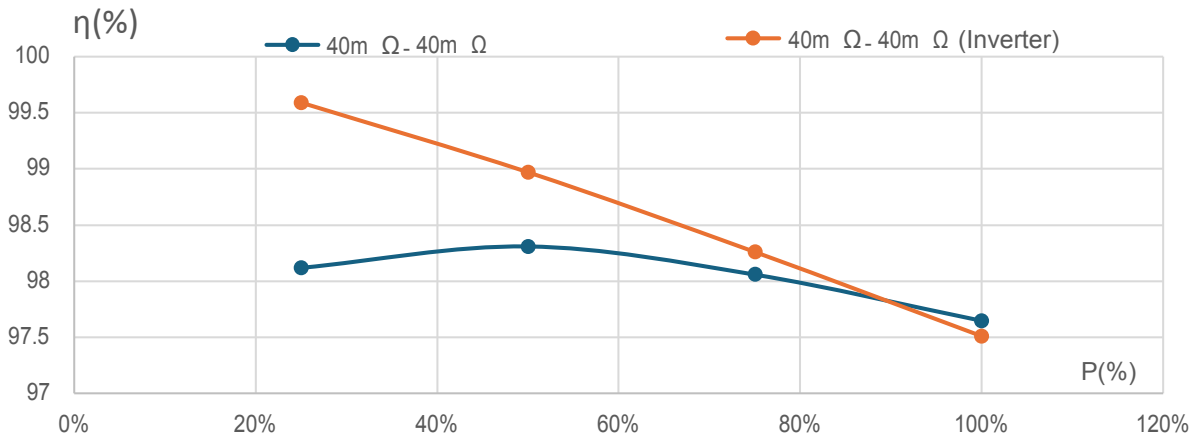


Table 5 shows the switching energy and recovery energy data that the experiment acquired for MOSFETs A1 and A2, and the parasitic diode in power factor correction (PFC) mode and inverter mode. It covers the first and second configurations at 100% load.

Table 5. Experimentally acquire switching energy source rms current at 100% loading

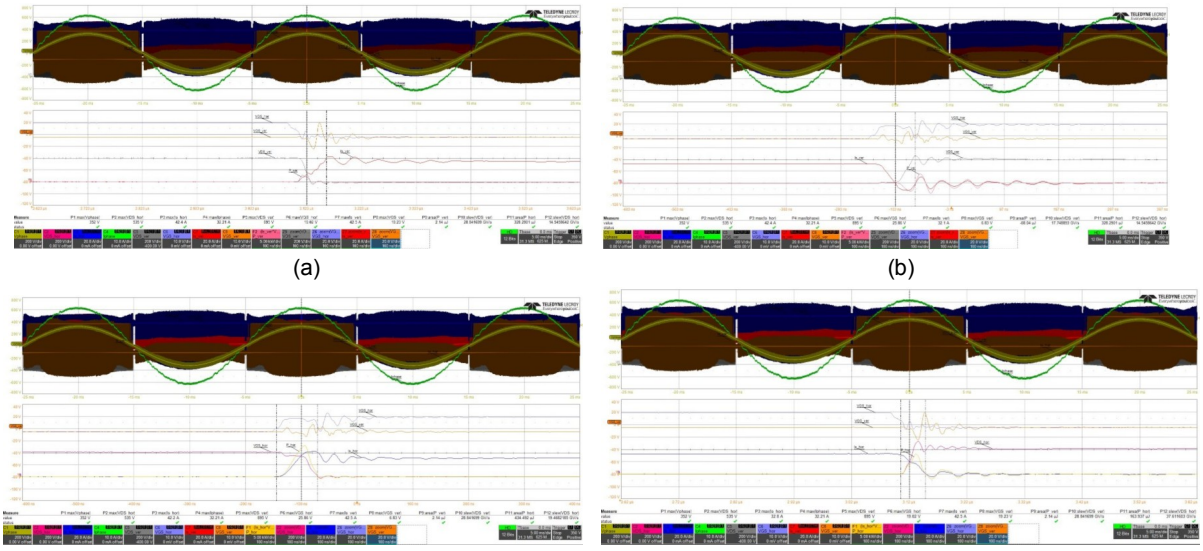
Mode	Switch	I_{SRMS}[A]	E_{ON} [µJ]	E_{OFF} [µJ]	E_{REC}[µJ]
PFC	A1	22.337	0	0	105.21
	A2		434.49	163.94	0
Inverter	A1	21.195	464.21	85.17	0
	A2		0	0	15.27

The waveforms were acquired and measured for all devices connected to the first leg of the ph-3l-T-type converter. The waveforms in Figure 15 and Figure 16 show the A1 and A2 devices. They highlight the switching performance of the tested SiC MOSFETs at the maximum power of 15 kW. The performance is measured in power factor correction (PFC) mode and inverter mode.

These color codes are used in the following Figure 15 and Figure 16:

- A1 source (or drain) current: "I_{S_A1}" signal in purple
- A2 source (or drain) current: "$IS_{\_A2}$" signal in dark blue
- A1 drain-source voltage: "V_{DS_A1}" signal in orange
- A2 drain-source voltage: " I_{S_A2}" signal in pink
- P_A1 instantaneous power (I_{S_A1} x V_{DS_A1}): "Power" signal in light pink
- P_A2 instantaneous power (I_{S_A2} x I_{S_A2}): "Power" signal in yellow.

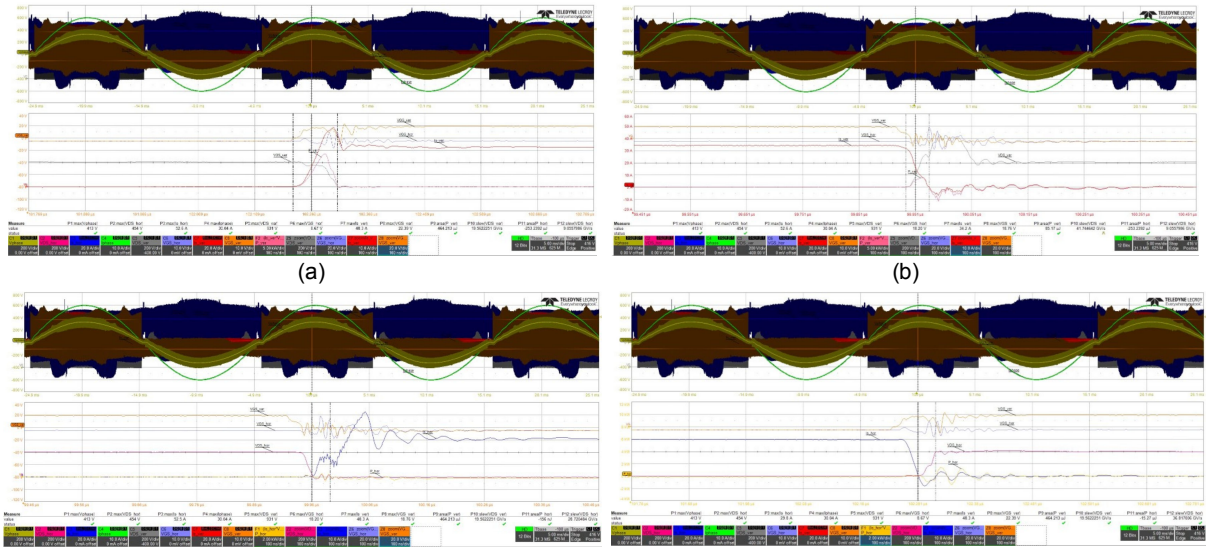
Figure 15. PFC mode A1: (a) turn on, (b) turn off and A2: (c) turn on, (d) turn off at maximum power



(a) (b)

(c) (d)

Figure 16. Inverter mode A1: (a) turn on, (b) turn off and A2: (c) turn on, (d) turn off at maximum power



(a) (b)

(c) (d)

6 Conclusion

The gen.3 SiC MOSFET device configurations show high performance. They perform well in the vertical and horizontal legs of the T-type converter under full-load conditions of 15 kW. The performance is notable in power factor correction (PFC) and inverter mode operation. These devices help achieve nearly 99% efficiency in this application.

Consequently, ST is already planning to expand the product portfolio to cover a broader power range by using the diverse package solutions that STMicroelectronics offers.

The 650 V and 1200 V G3 SiC MOSFET series sets a benchmark in the growing SiC market. It finds extensive use in various applications. These applications include power factor correction, onboard chargers (OBC), uninterruptible power supplies, solar inverters, and welding machines. This development further strengthens STMicroelectronics' leadership in these important market segments.

Appendix A Other information

A.1 Reference documents

[1] User manual, “*How to use the 15 kW three-level three-phase Vienna rectifier with digital control for power factor correction*”, (UM2975).

[2] Data brief, “*15 kW, three-phase, three-level active front end (AFE) bidirectional converter for industrial and electric vehicle DC fast charging applications*”, (DB4071).

[3] *M. Schweizer and J. W. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications," in IEEE Transactions on Power Electronics, vol. 28, no. 2, pp. 899-907*, Feb. 2013.

[4] *A. Anthon, Z. Zhang, M. A. E. Andersen, D. G. Holmes, B. McGrath and C. A. Teixeira, "The Benefits of SiC mosfets in a T-Type Inverter for Grid-Tie Applications," in IEEE Transactions on Power Electronics, vol. 32, no. 4, pp. 2808-2821*, April 2017.

[5] Flyer, “*STPOWER Gen3 SiC MOSFETs ideal for EV*”.

[6] *E. Gurpinar and A. Castellazzi, "Single-Phase T-Type Inverter Performance Benchmark Using Si IGBTs, SiC MOSFETs, and GaN HEMTs," in IEEE Transactions on Power Electronics, vol. 31, no. 10, pp. 7148-7160*, Oct. 2016.

[7] *Kumar, A.; Bertoluzzo, M.; Jha, R.K.; Sagar, A. “Analysis of Losses in Two Different Control Approaches for S-S Wireless Power Transfer Systems for Electric Vehicle”, Energies, 16*, 1795, 2023.

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
17-Aug-2026	1	First release.

Contents

List of figures